AK5394A

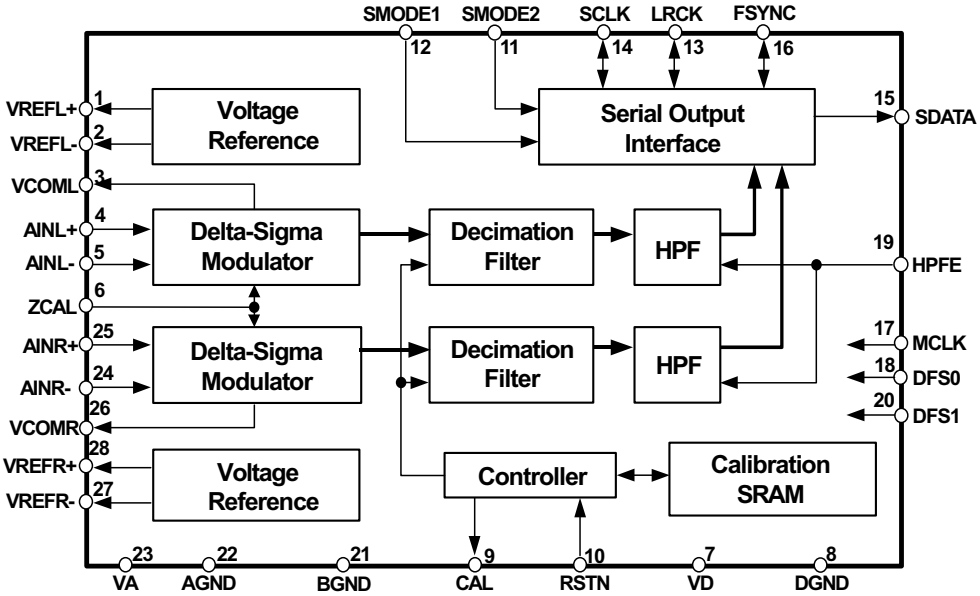
Super High Performance 192kHz 24-Bit ΔΣ ADC

GENERAL DESCRIPTION

The AK5394A is a 24bit, 192kHz sampling 2ch A/D Converter for professional digital audio systems. The modulator in the AK5394A uses the new developed advanced multi bit architecture. This new architecture achieves the wide dynamic range and wide bandwidth, while keeping superior distortion characteristics. The AK5394A performs 123dB dynamic range, so the device is suitable for professional studio equipment such as digital mixer, digital VTR etc. The operating voltages support analog 5V and digital 3.3V, so it is easy to I/F with 3.3V logic IC.

FEATURES

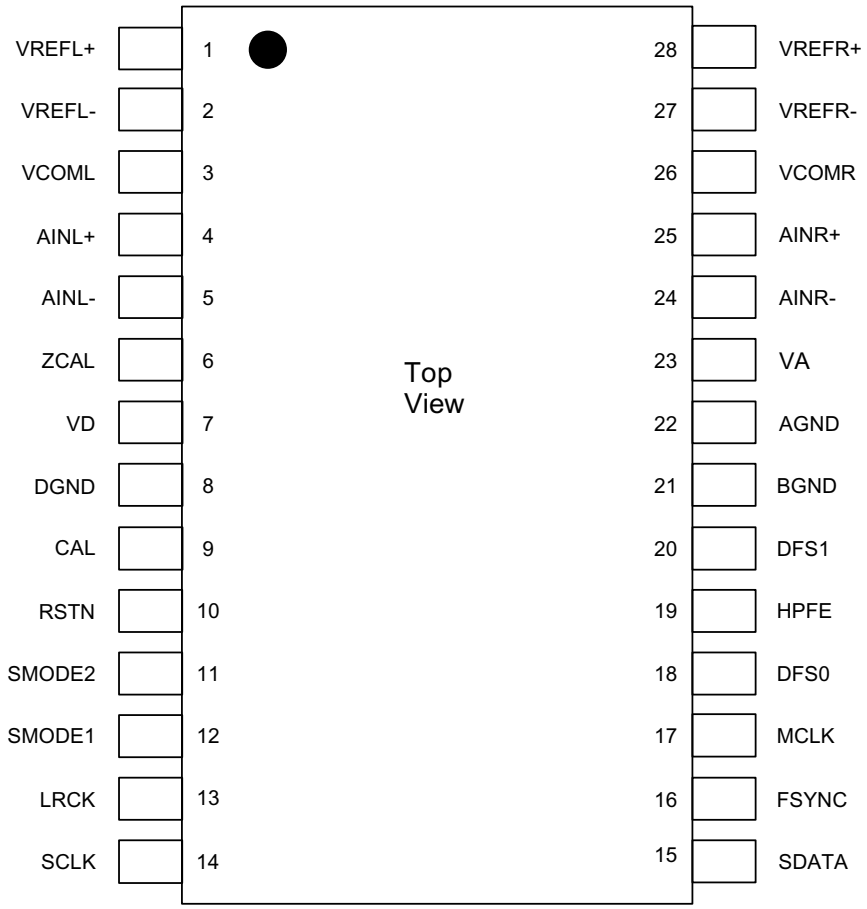
- 128x Oversampling
- New advanced multi bit Architecture ADC
- Sampling Rate: 1kHz ~ 216kHz
- Full Differential Inputs
- S/(N+D): 110dB
- DR: 123dB
- S/N: 123dB
- High Performance Linear Phase Digital Anti-Alias filter
  - Passband: 0 ~ 21.768kHz(@fs=48kHz)
  - Ripple: 0.001dB
  - Stopband: 120dB
- Digital HPF & Offset Calibration for Offset Cancel
- Power Supply: 5V±5%(Analog), 3 ~ 5.25V(Digital)
- Power Dissipation: 665mW
- Package: 28pin SOP
- AK5392/3 Semi-Pin Compatible



■ Ordering Guide

AK5394AVS	–10 ~ +70°C	28pin SOP
AKD5394A	AK5394A Evaluation Board	

■ Pin Layout

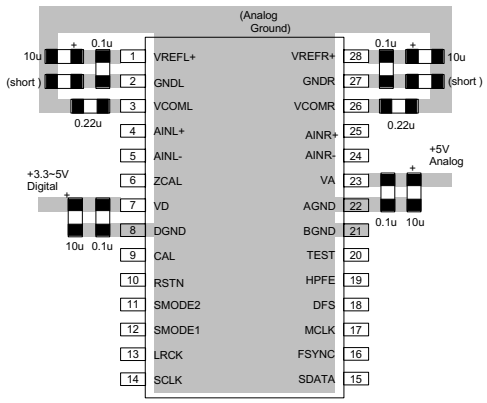


■ Compatibility with AK5392/3

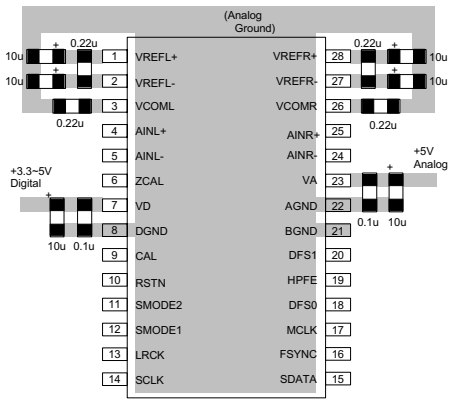
	AK5394A	AK5393	AK5392
Pin 2	VREFL–	GNDL	GNDL
Pin 18	DFS0	DFS	CMODE
Pin 20	DFS1	TEST	TEST
Pin 27	VREFR–	GNDR	GNDR
fs (max)	216kHz	108kHz	54kHz
MCLK at 48kHz	256fs	256fs	256fs or 384fs
MCLK at 96kHz	128fs	128fs	N/A
MCLK at 192kHz	64fs	N/A	N/A
DR	123dB	117dB	116dB
S/N	123dB	117dB	116dB

■ Common PCB layout example between AK5393 and AK5394A

AK5393



AK5394A



Pin#	AK5393	AK5394A
2	GNDL	VREFL–
	Connected to AGND	Connected to AGND with a 10uF electrolytic capacitor, and connected to VREFL+ with a 0.22uF ceramic capacitor.
18	DFS	DFS0
20	TEST	DFS1
27	GNDR	VREFR–
	Connected to AGND	Connected to AGND with a 10uF electrolytic capacitor, and connected to VREFR+ with a 0.22uF ceramic capacitor.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFL+	O	Lch Positive Reference Voltage, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL– with a 0.22μF ceramic capacitor.
2	VREFL–	O	Lch Negative Reference Voltage, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL+ with a 0.22μF ceramic capacitor.
3	VCOML	O	Lch Common Voltage Pin, 2.75V
4	AINL+	I	Lch Analog positive input Pin
5	AINL-	I	Lch Analog negative input Pin
6	ZCAL	I	Zero Calibration Control Pin This pin controls the calibration reference signal. "L" :VCOML and VCOMR "H" : Analog Input Pins (AINL±, AINR±)
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin, 0V
9	CAL	O	Calibration Active Signal Pin "H" means the offset calibration cycle is in progress. Offset calibration starts when RSTN pin goes "H". CAL goes "L" after 8704 LRCK cycles for DFS pin = "L", 17408 LRCK cycles for DFS pin = "H".
10	RSTN	I	Reset Pin When "L", the digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.
11 12	SMODE2 SMODE1	I I	Serial Interface Mode Select Pin MSB first, 2's compliment. SMODE2 SMODE1 MODE LRCK L L Slave mode : MSB justified : H/L L H Master mode : Similar to I^2S : H/L H L Slave mode : I^2S : L/H H H Master mode : I^2S : L/H
13	LRCK	I/O	Left/Right Channel Select Clock Pin When RSTN pin = "L" in master mode, LRCK outputs "L".

14	SCLK	I/O	Serial Data Clock Pin SDATA is clocked out on the falling edge of SCLK. Slave mode: SCLK requires more than 48fs clock. Master mode: AK5394A outputs following clocks as SCLK. Normal Speed Mode: 128fs Double Speed Mode: 64fs Quad Speed Mode: 64fs When RSTN pin = "L", SCLK outputs "L"(normal/double speed mode) or outputs the inverted MCLK (quad speed mode).
15	SDATA	O	Serial Data Output Pin MSB first, 2's complement.
16	FSYNC	I/O	Frame Synchronization Signal Pin Slave mode: When "H", the data bits are clocked out on SDATA. In I^2S mode, FSYNC is don't care. Master mode: FSYNC outputs 2fs clock. FSYNC stays "L" during reset.
17	MCLK	I	Master Clock Input Pin DFS1 DFS0 MCLK fs(typ) L L 256fs 48kHz L H 128fs 96kHz H L 64fs 192kHz H H (N/A) (N/A)
18	DFS0	I	Sampling Speed Select Pin 0 DFS1 DFS0 fs(typ) L L 48kHz L H 96kHz H L 192kHz H H (N/A)
19	HPFE	I	High Pass Filter Enable Pin "L": Disable "H": Enable
20	DFS1	I	Sampling Speed Select Pin 1 (see #18 DFS0)
21	BGND	-	Substrate Ground Pin, 0V
22	AGND	-	Analog Ground Pin, 0V
23	VA	-	Analog Supply Pin, 5V
24	AINR−	I	Rch Analog negative input Pin
25	AINR+	I	Rch Analog positive input Pin
26	VCOMR	O	Rch Common Voltage Pin, 2.75V
27	VREFR−	O	Rch Negative Reference Voltage, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR+ with a 0.22µF ceramic capacitor.
28	VREFR+	O	Rch Positive Reference Voltage, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR- with a 0.22µF ceramic capacitor.

Note: All digital inputs should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND, BGND, DGND = 0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	−0.3	6.0	V
Digital	VD	−0.3	6.0	V
|BGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage	VINA	−0.3	VA+0.3	V
Digital Input Voltage	VIND	−0.3	VD+0.3	V
Ambient Temperature (power applied)	Ta	−10	70	°C
Storage Temperature	Tstg	−65	150	°C

Notes: 1. All voltages with respect to ground.
2. AGND, BGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, BGND, DGND = 0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA	4.75	5.0	5.25	V
(Note 3) Digital	VD	3.0	3.3	5.25	V

Notes: 1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VA=5.0V; VD=3.3V; AGND=BGND=DGND=0V; fs=48kHz; Signal Frequency=1kHz; 24bit Output; Measurement frequency=10Hz ~ 20kHz; DFS0="L", DFS1="L"; External circuit: Figure 9 Inputted through XLR; unless otherwise specified)

Parameter			min	Typ	Max	Units
Resolution					24	Bits
Analog Input Characteristics:						
S/(N+D)	fs=48kHz	−1dBFS (Note4)	-	110		dB
		−1dBFS	87	94		dB
		−20dBFS	-	100		dB
		−60dBFS	-	60		dB
	fs=96kHz BW=40kHz	−1dBFS (Note4)	-	110		dB
		−1dBFS	87	94		dB
		−20dBFS		97		dB
		−60dBFS	-	57		dB
	fs=192kHz BW=80kHz	−1dBFS	-	94		dB
		−20dBFS	-	92		dB
		−60dBFS	-	52		dB
Dynamic Range (-60dBFS with A-weighted)			117	123		dB
		(Note4)	-	120		dB
S/N (A-weighted)			117	123		dB
		(Note4)	-	120		dB
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				150		ppm/°C
Offset Error	After calibration, HPF=OFF			±1000	-	LSB_{24}
	After calibration, HPF=ON			±1	-	LSB_{24}
Offset Drift	(HPF=OFF)		-	±10	-	LSB_{24}/°C
Offset Calibration Range	(HPF=OFF) (Note5)			±50		mV
Input Voltage (AIN+) − (AIN−)			±2.25	±2.4	±2.55	V
Power Supplies:						
Power Supply Current						
VA				127	165	mA
VD (fs=48kHz; DFS0="L", DFS1="L")				9	13.5	mA
(fs=96kHz; DFS0="H", DFS1="L")				13	20	mA
(fs=192kHz; DFS0="L", DFS1="H")				21	32	mA
Power Dissipation				665	870	mW
Power Supply Rejection	(Note 6)			70		dB

Notes: 4. Using the circuit as shown in Figure9 (Analog input buffer circuit example 1). 1000µF capacitors connected between VREF+/− pin and GND.
5. The output level reduces equivalent to DC offset after calibration.
6. PSRR is applied to VA and VD with 1kHz, 20mVpp.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; fs=48kHz, DFS0="L", DFS1="L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband	(Note 7)	PB	0		21.768	kHz
Stopband	(Note 7)	SB	26.232			kHz
Passband Ripple		PR			±0.001	dB
Stopband Attenuation	(Note 8)	SA	120			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay	(Note 9)	GD		63		1/fs
ADC Digital Filter(HPF):						
Frequency response	(Note 7) –3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; fs=96kHz, DFS0="H", DFS1="L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband	(Note 7)	PB	0		43.536	kHz
Stopband	(Note 7)	SB	52.464			kHz
Passband Ripple		PR			±0.003	dB
Stopband Attenuation	(Note 10)	SA	120			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay	(Note 9)	GD		63		1/fs
ADC Digital Filter(HPF):						
Frequency response	(Note 7) –3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; fs=192kHz, DFS0="L", DFS1="H")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband	(Note 7)	PB	0		87.072	kHz
Stopband	(Note 8)	SB	104.928			kHz
Passband Ripple		PR			±0.007	dB
Stopband Attenuation	(Note 11)	SA	120			dB
Group Delay Distortion		ΔGD		0		μs
Group Delay	(Note 9)	GD		63		1/fs
ADC Digital Filter(HPF):						
Frequency response	(Note 7) –3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

Notes: 7. The passband and stopband frequencies are proportional to fs.

8. The analog modulator samples the input at 6.144MHz for an output word rate of 48kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 21.768kHz, where n=1,2,3···).
9. The calculating delay time which takes place due to the digital filtering process. This time is taken from when the analog signal ia input, to the time of setting the 24-bit data (from both channels) to the output register. 65/fs typ. (normal/double/quad speed mode) at HPF=ON.
10. The analog modulator samples the input at 6.144MHz for an output word rate of 96kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 43.536kHz, where n=1,2,3···)
11. The analog modulator samples the input at 6.144MHz for an output word rate of 192kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 6.144MHz ± 87.072kHz, where n=1,2,3···).

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD = 3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-100μA	VOH	VD−0.5	-	-	V
Low-Level Output Voltage Iout= 100μA	VOL	-		0.5	V
Input Leakage Current	Iin	-	-	±10	μA

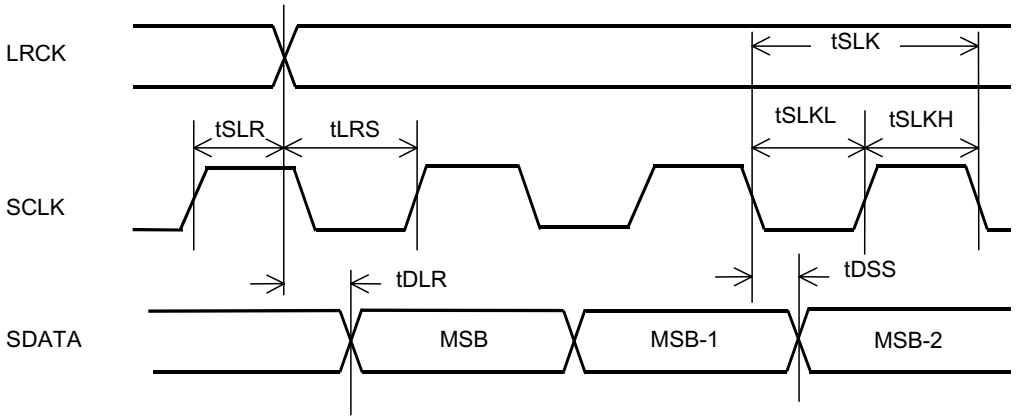
SWITCHING CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; C_L=20pF)

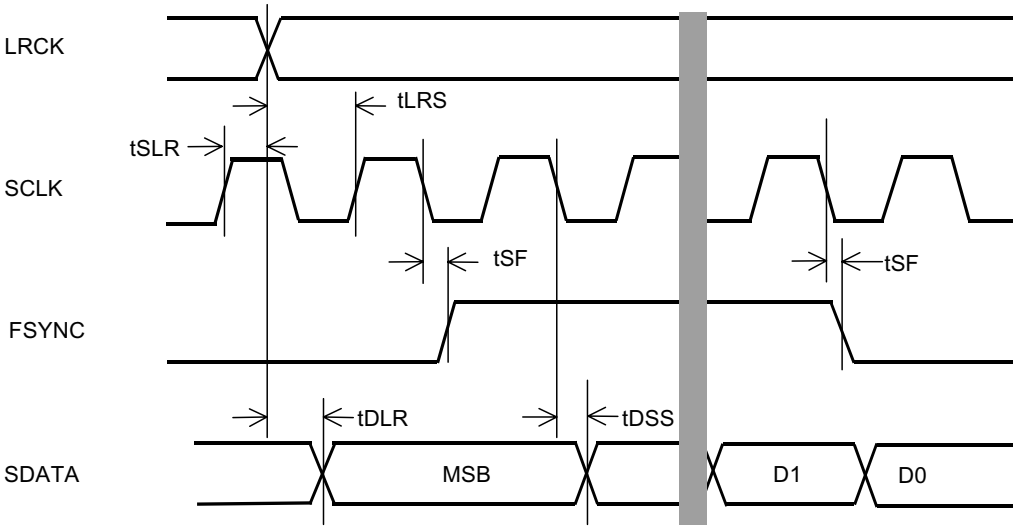
Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock	fCLK	0.256	12.288	13.824	MHz
Pulse width Low	tCLKL	29			ns
Pulse width High	tCLKH	29			ns
Serial Data Output Clock (SCLK)	fSLK		6.144	13.824	MHz
Channel Select Clock (LRCK)	fs	1	48	216	kHz
duty cycle		25		75	%
Serial Interface Timing (Note 12)					
Slave Mode (SMODE1 = "L")					
SCLK Period (Note 13)					
Normal Speed Mode	tSLK	1/128fs			ns
Double Speed Mode	tSLK	1/64fs			ns
Quad Speed Mode	tSLK	1/64fs			ns
SCLK Pulse width Low	tSLKL	33			ns
Pulse width High	tSLKH	33			ns
SCLK rising to LRCK Edge (Note 14)	tSLR	20			ns
LRCK Edge to SCLK rising (Note 14)	tLRS	20			ns
LRCK Edge to SDATA MSB Valid	tDLR			20	ns
SCLK falling to SDATA Valid	tDSS			20	ns
SCLK falling to FSYNC Edge	tSF	–20		20	ns
Master Mode (SMODE1 = "H")					
SCLK Frequency					
Normal Speed Mode	fSLK		128fs		Hz
Double Speed Mode	fSLK		64fs		Hz
Quad Speed Mode	fSLK		64fs		Hz
SCLK duty cycle	dSLK		50		%
FSYNC Frequency	fFSYNC		2fs		Hz
FSYNC duty cycle	dFSYNC		50		%
SCLK falling to LRCK Edge	tMSLR	–20		20	ns
LRCK Edge to FSYNC rising	tLRF		1		tSLK
SCLK falling to SDATA Valid	tDSS			20	ns
SCLK falling to FSYNC Edge	tSF	–20		20	ns
Reset / Calibration timing					
RSTN Pulse width	tRTW	150			ns
RSTN falling to CAL rising	tRCR			50	ns
RSTN rising to CAL falling (Note 15)					
Normal Speed Mode	tRCF		8704		1/fs
Double Speed Mode	tRCF		17408		1/fs
Quad Speed Mode	tRCF		34816		1/fs
RSTN rising to SDATA Valid (Note 15)					
Normal Speed Mode	tRTV		8719		1/fs
Double Speed Mode	tRTV		17423		1/fs
Quad Speed Mode	tRTV		34831		1/fs

Notes: 12. Refer to Serial Data Interface Section.
13. At Slave Mode, SCLK must be continuously provided more than 16fs at LRCK="H" and "L".
14. Specified LRCK edges not to coincide with the rising edges of SCLK.
15. The number of the LRCK rising edges after RSTN pin brought high.

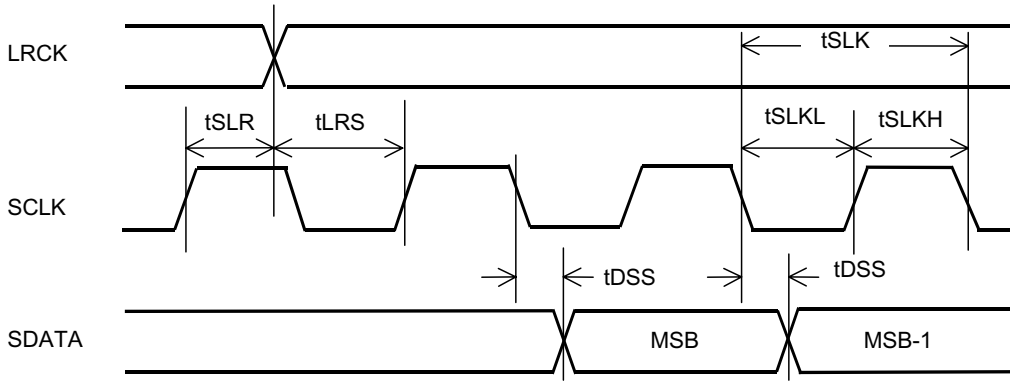
■ Timing Diagram



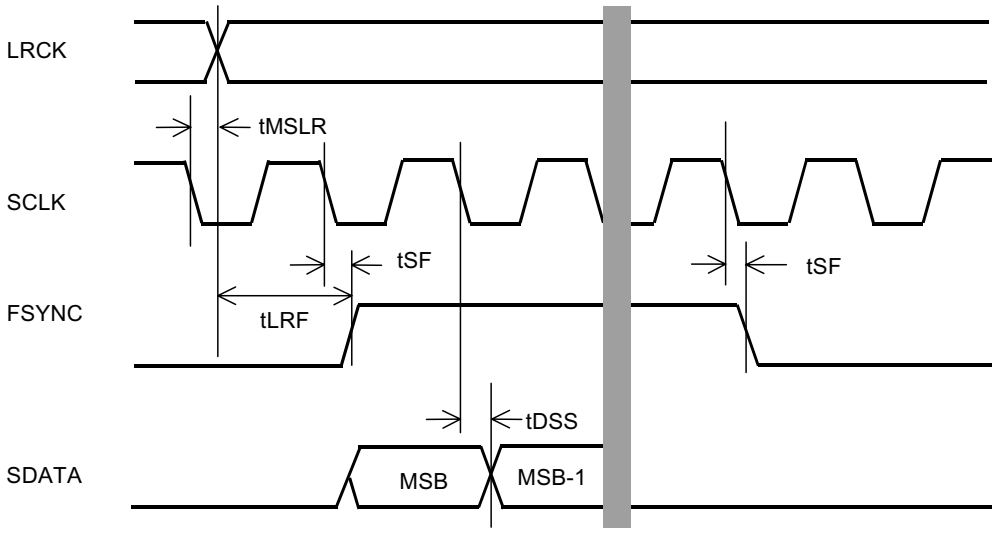
Serial Data Timing (Slave Mode, FSYNC = "H")



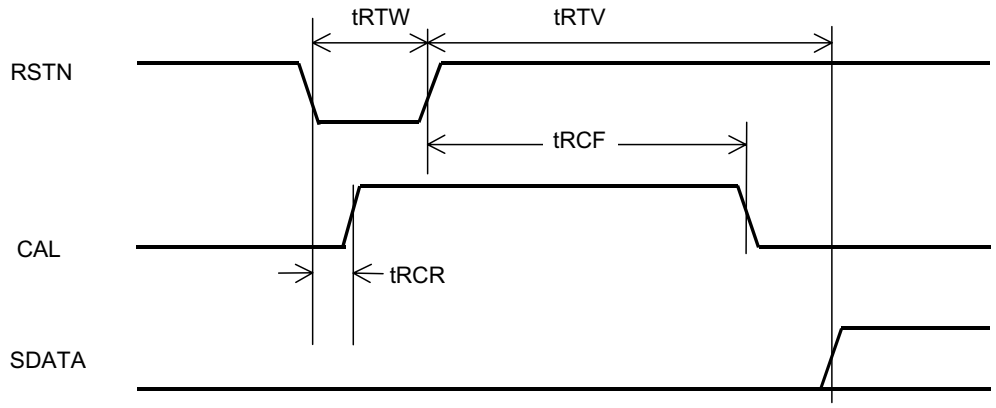
Serial Data Timing (Slave Mode)



Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)



Serial Data Timing (Master Mode & I^2S Master Mode, Normal Speed Mode)



Reset & Calibration Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks that are required to operate the AK5394A are MCLK, LRCK(fs) and SCLK. MCLK should be synchronized with LRCK but the phase is free of care. Table 1 and 2 show the relationship between the sampling rate and the frequencies of MCLK and SCLK.

As the AK5394A includes the phase detect circuit for LRCK, the AK5394A is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

All external clocks must be present unless RSTN pin = "L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

Sampling Speed		Normal	Double	Quad
	DFS0	L	H	L
	DFS1	L	L	H
LRCK (fs)		~ 54kHz	~ 108kHz	~ 216kHz
SCLK (Slave Mode)		~ 128fs	~ 64fs	~ 64fs
SCLK (Master Mode)		128fs	64fs	64fs
MCLK		256fs	128fs	64fs

Table 1. System Clocks

LRCK (fs)	MCLK	SCLK
32kHz	8.1920MHz	~ 4.0960MHz
44.1kHz	11.2896MHz	~ 5.6448MHz
48kHz	12.2880MHz	~ 6.1440MHz
96kHz	12.2880MHz	~ 6.1440MHz
192kHz	12.2880MHz	~ 12.288MHz

Table 2. Examples of System Clock Frequency

■ Serial Data Interface

The AK5394A supports four serial data formats that can be selected via SMODE1 and SMODE2 pins (Table 3). The data format is MSB-first, 2's complement.

Figure	SMODE2	SMODE1	Mode	LRCK
Figure 1	L	L	Slave Mode	Lch = H, Rch = L
Figure 2	L	H	Master Mode	Lch = H, Rch = L
Figure 3	H	L	I^2S Slave Mode	Lch = L, Rch = H
Figure 4	H	H	I^2S Master Mode	Lch = L, Rch = H

Table 3. Serial I/F Formats

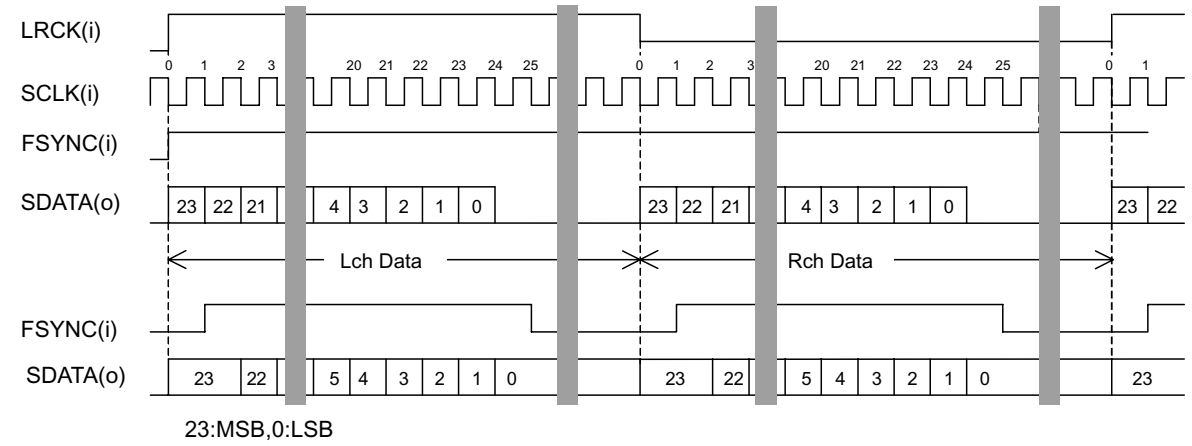


Figure 1. Serial Data Timing (Slave Mode)

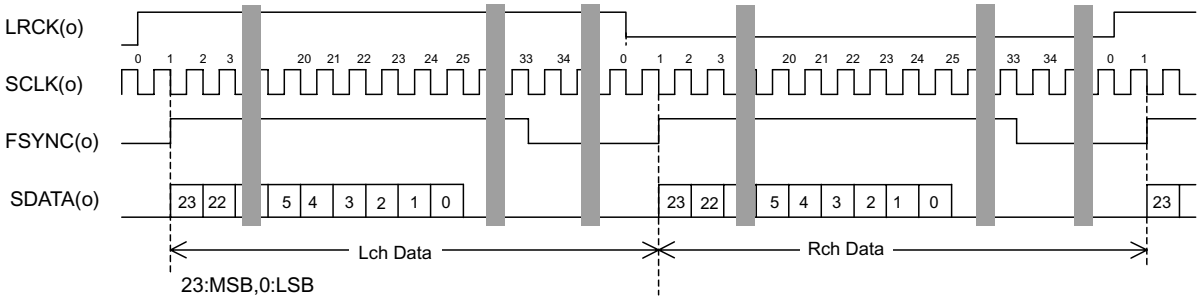


Figure 2. Serial Data Timing (Master mode, Normal Speed Mode)

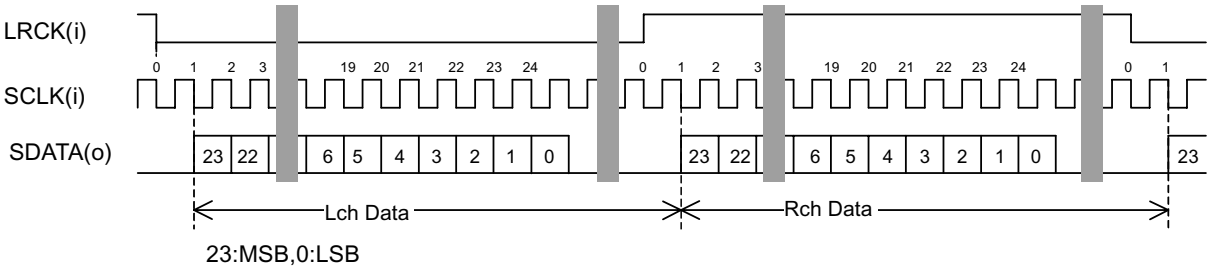


Figure 3. Serial Data Timing (I^2S Slave mode, FSYNC: Don't care)

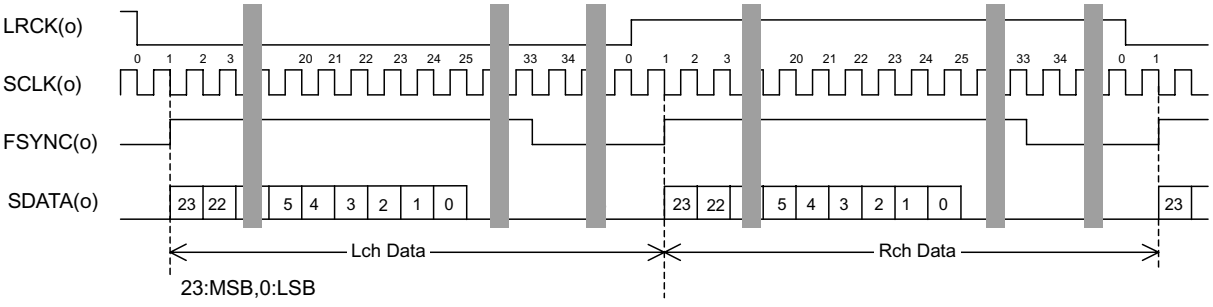


Figure 4. Serial Data Timing (I^2S Master mode, Normal Speed Mode)

■ Offset Calibration

1. When the capacitors of 10µF or less are connected between VREF pin and GND:

When RSTN pin goes to "L", the digital section is powered-down. Upon returning "H", the offset calibration cycle is started. The offset calibration cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the part measures and stores the values of calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AIN+/–) or the VCOM pins depending on the state of the ZCAL pin. With ZCAL "H", the analog input pin voltages are measured, and with ZCAL "L", the VCOM pin voltages are measured. The CAL output is "H" during calibration.

2. When capacitors more than 10µF are connected between VREF pin and GND:

The distortion at low frequency can be improved by connecting large capacitors (C in Figure 5) to VREF pins. (Refer to Figure 12) However, when the capacitors of VREF pins are larger than 10µF, it is possibility that the offset calibration does not performed correctly if the offset calibration cycle is started right after power-up. Because the internal VREF can not settle to the appropriate voltage when the calibration cycle is completed. In this case, the offset calibration cycle should be started again after the VREF voltage settled. The timing is shown in Figure 6. Table 4 shows the relationship between the capacitance and the VREF settling time.

Capacitor C[µF]	Settling Time T[s]=5000 x C
1000	5
470	2.4
220	1.1
100	0.5

Table 4. Settling Time and capacitors connected between VREF and GND

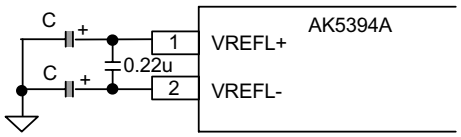


Figure 5. VREF circuit example

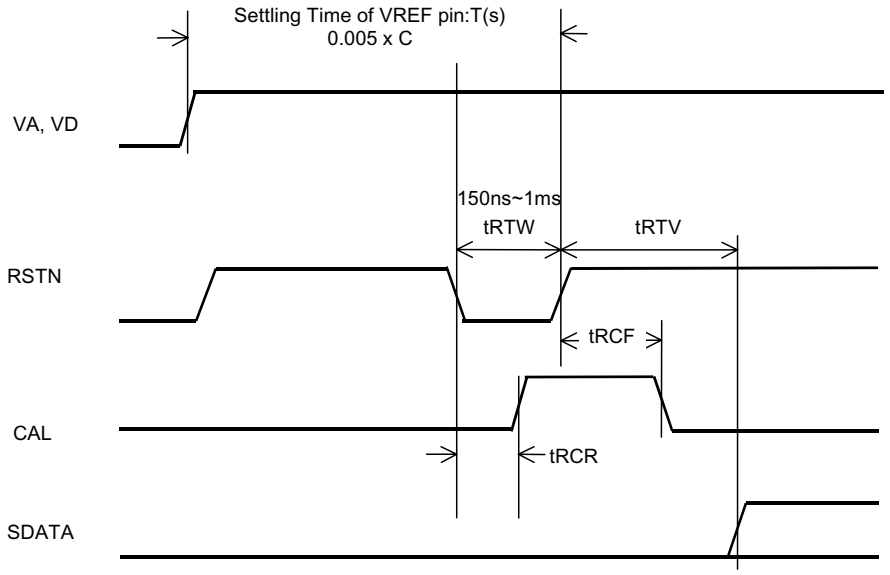


Figure 6. Reset & Calibration Timing

■ Digital High Pass Filter

The AK5394A includes a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1Hz at fs=48kHz (Normal Speed Mode), at fs=96kHz (Double Speed Mode), at fs=192kHz (Quad Speed Mode) and also scales with sampling rate (fs) respectively.

Sampling Speed	DFS1	DFS0	fc (Cut-off frequency)
Normal	L	L	fs/48kHz
Double	L	H	fs/96kHz
Quad	H	L	fs/192kHz

Table 5. Cut-off frequency

SYSTEM DESIGN

Figure 7 and 8 show the system connection diagram. An evaluation board [AKD5394A] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

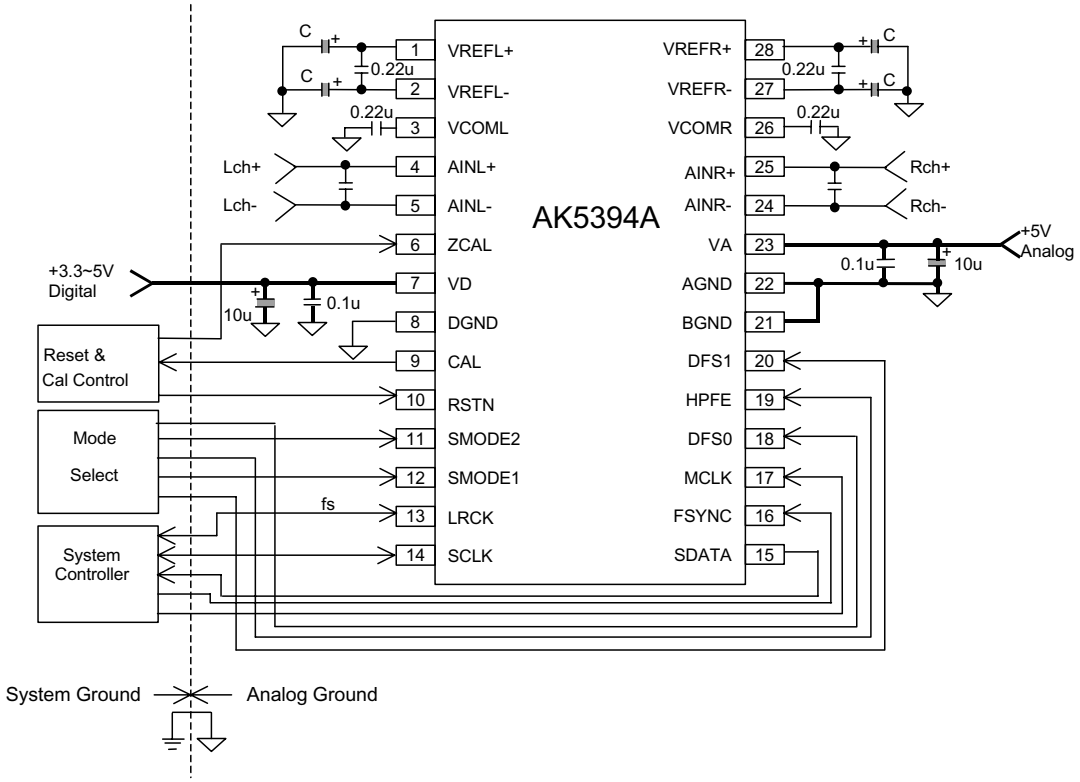


Figure 7. Typical Connection Diagram

Notes:
- LRCK = fs, SCLK = 64fs.
- Power lines of VA and VD should be distributed separately from the point with low impedance of regulator etc.
- AGND, BGND and DGND must be connected to the same analog ground plane.
- All digital input pins should not be left floating.
- Refer Table 4 and Figure 12 about C.

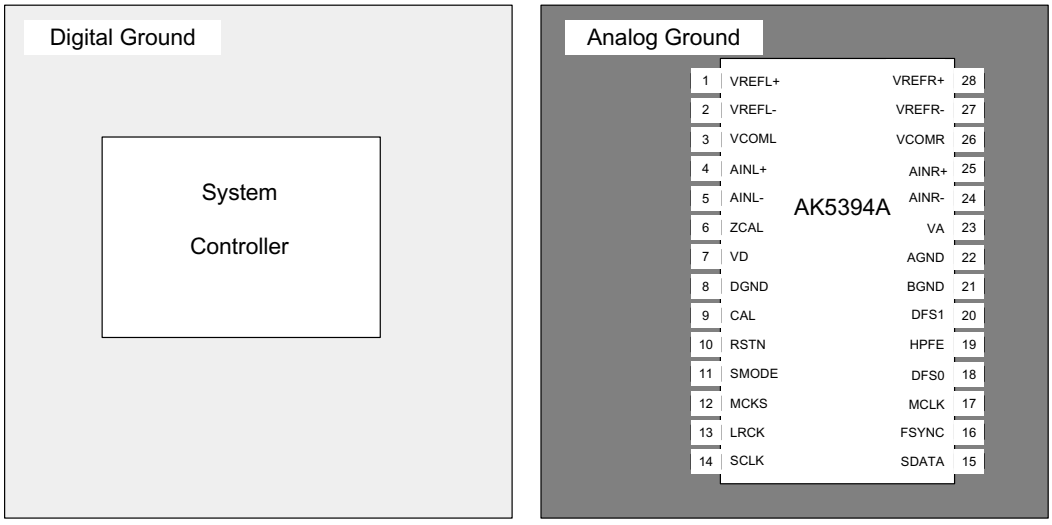


Figure 8 Ground layout

1. Grounding and Power Supply Decoupling

The AK5394A requires careful attention to power supply and grounding arrangements. Analog ground and digital ground of the system should be separate and connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5394A as possible, with the small value ceramic capacitor being the nearest.

2. On-chip Voltage Reference and VCOM

The reference voltage for A/D converter is supplied from VREF+/– pin at AGND reference. A 0.22µF ceramic capacitor should be attached between VREF+ and VREF–. An electrolytic capacitor (<1000µF) should be connected between AGND and VREF+/– respectively to eliminate the effects of low frequency noise. Especially a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREF+/– pins in order to avoid unwanted coupling into the AK5394A. No load current may be taken from the VREF+/– pins.

VCOM is a common voltage of the analog signal. In order to eliminate the effects of high frequency noise, a 0.22µF ceramic capacitor should be connected as near to the VCOM pin as possible. And all signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5394A. No load current may be drawn from the VCOM pin.

3. Analog Inputs

Analog signal is differentially input into the modulator via the AIN+ and the AIN– pins. The input voltage is the difference between AIN+ and AIN– pins. The full-scale of each pin is nominally ±2.4Vpp (typ). The AK5394A can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFH (@24bit) for input above a positive full scale and 800000H (@24bit) for input below a negative full scale. The ideal code is 000000H (@24bit) with no input signal. The DC offset is removed by the offset calibration.

The AK5394A samples the analog inputs at 128fs (6.144MHz@fs=48kHz, Normal Speed Mode). The digital filter rejects noise above the stop band except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs and most audio signals do not have significant energy at 128fs.

The AK5394A accepts +5V supply voltage. Any voltage which exceeds the upper limit of VA+0.3V and lower limit of AGND–0.3V and any current beyond 10mA for the analog input pins (AIN+/–) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

4. External analog circuit

Figure 9 shows an input buffer circuit example 1. (1st order HPF; fc=0.70Hz, 2nd order LPF; fc=320kHz, gain=−14.5dB). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/−12.7Vpp (AK5394A: +/−2.4Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=120dB, S/(N+D)=105dB.

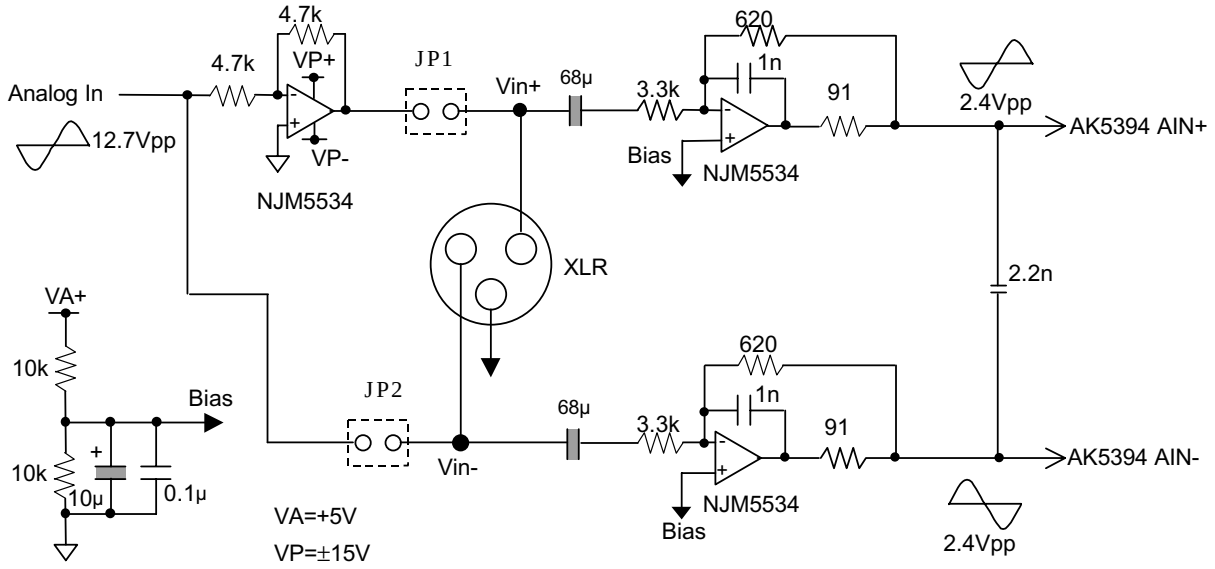


Figure 9. Analog input buffer circuit example 1

Fin	1Hz	10Hz
Frequency Response	−1.77dB	−0.02dB

Table 6. Frequency Response of HPF

Fin	20kHz	40kHz	80kHz	6.144MHz
Frequency Response	0.00dB	0.00dB	0.00dB	−51.36dB

Table 7. Frequency Response of LPF

Figure 10 shows an input buffer circuit example 2. (1st order HPF; fc=0.66Hz, 1st order LPF; fc=590kHz, gain=−14dB). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/−12.1Vpp (AK5394A: +/−2.4Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=123dB, S/(N+D)=94dB.

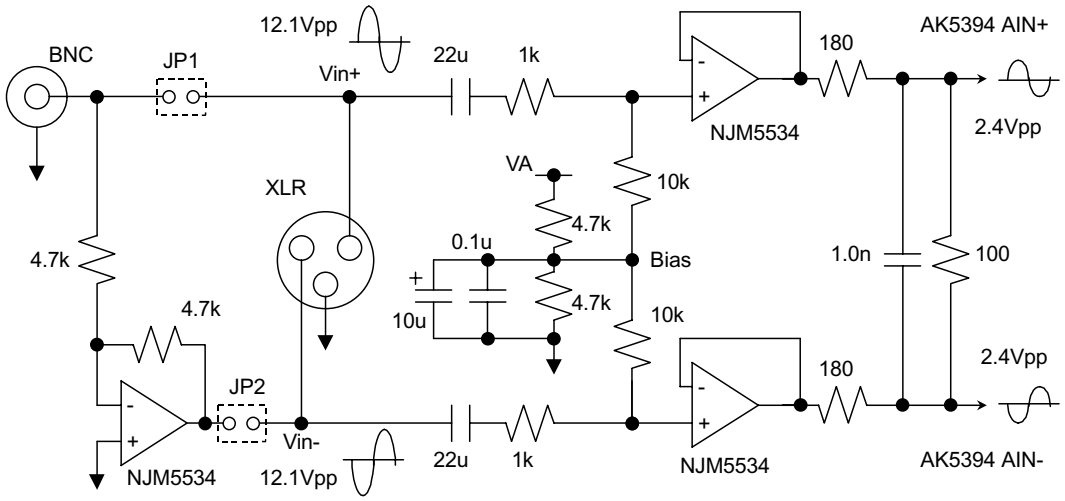


Figure 10. Analog input buffer circuit example 2

Fin	1Hz	10Hz
Frequency Response	−1.56dB	−0.02dB

Table 8. Frequency Response of HPF

Fin	20kHz	40kHz	80kHz	6.144MHz
Frequency Response	−0.005dB	−0.02dB	−0.08dB	−20.4dB

Table 9. Frequency

5. Measurement example

Figure 11 plot is the THD+N vs Input Level with circuit Figure 9 and circuit Figure 10. X-AXIS is input level, Y-AXIS is THD+N (ratio).

Measurement condition
Ta=25°C; VA=5.0V; VD=3.3V; AGND, BGND, DGND=0V; fs=48kHz; Input frequency=1kHz; 24 bit Output;
Measurement frequency =10Hz ~ 20kHz; DFS0="L", DFS1="L", VREF capacitors=1000µF
Measured by Audio Precision System Two.

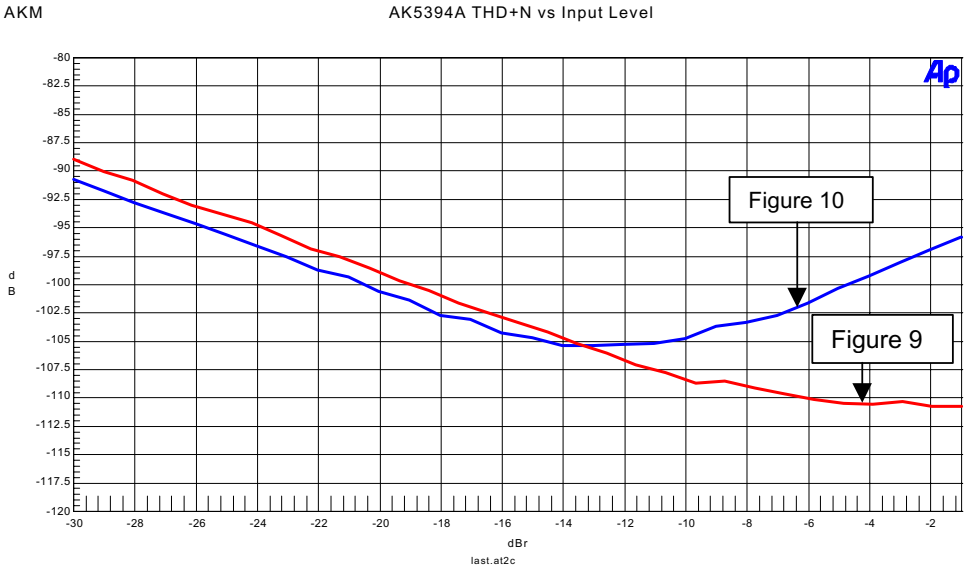


Figure 11. THD+N(ratio) vs. Input Level

Figure 12 shows the relationship between THD+N and Frequency with capacitors on Table 4. Input circuit uses Figure 9.

Measurement condition
Ta=25°C; VA=5.0V; VD=3.3V; AGND, BGND, DGND=0V; fs=48kHz; 24 bit Output; BW=10Hz ~ 20kHz; DFS0="L", DFS1="L", Measured by Audio Precision System Two.

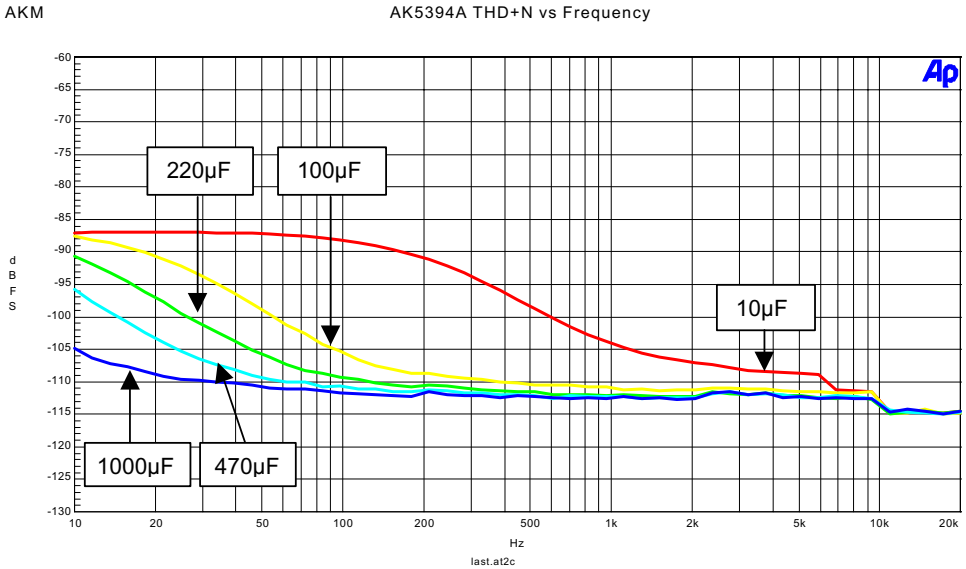


Figure 12. THD+N vs. Frequency

6. Noise floor of AK5394A

The AK5394A has a sprious noise of about −135dBFS on the noise floor of Lch output at no signal input. When this noise causes a trouble in system, it can be removed by adding a minute offset to the analog inputs of both channels externally using a circuit as Figure 13. The relationship between the frequency range (f_T) of the sprious noise to be removed and the adding offset voltage (V_{of}) is f_T [kHz] = 20 x V_{of} [mV] − 20. The example is shown in Table 10.

Sprious noise Frequency	Offset Voltage
0 ~ 20kHz	+2mV
0 ~ 40kHz	+3mV
0 ~ 80kHz	+5mV

Table 10. Sprious noise Frequency vs. Offset voltage

A resistor, R in Figure 13 should be 8Ω to add an offset of 2mV to the analog inputs. The relationship between R and V_{of} is shown by the following equation.

$$V_{of} = \frac{R}{20k + R} \times 5[V]$$

An offset voltage of the op-amps should be considered in the actual circuit. For example, when removing the sprious noise of 20kHz or less, the adding offset voltage should be 2+2=4mV if the op-amp has an offset of +/−2mV. In this case, the dynamic range of the ADC output decreases 4mV.

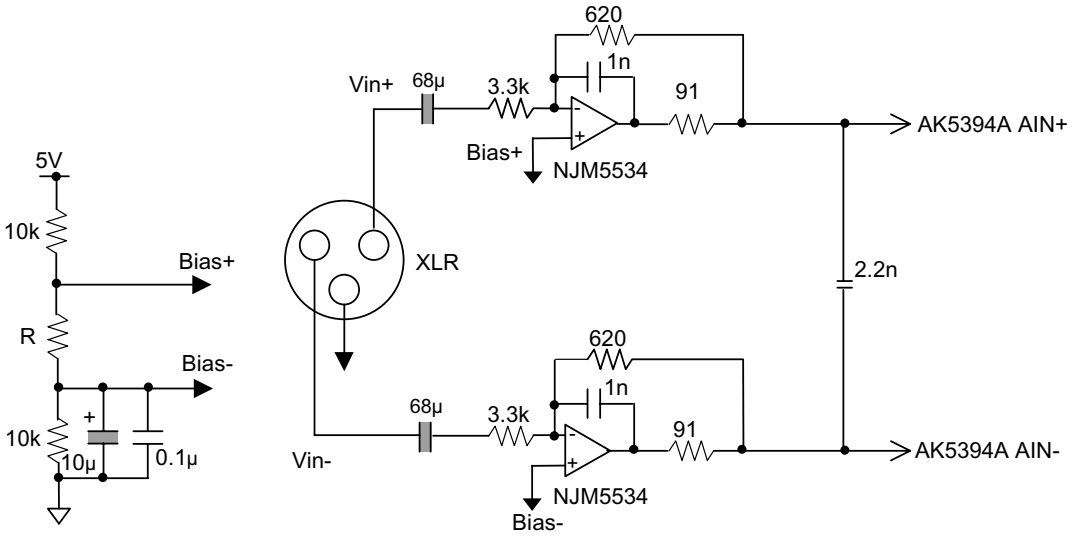
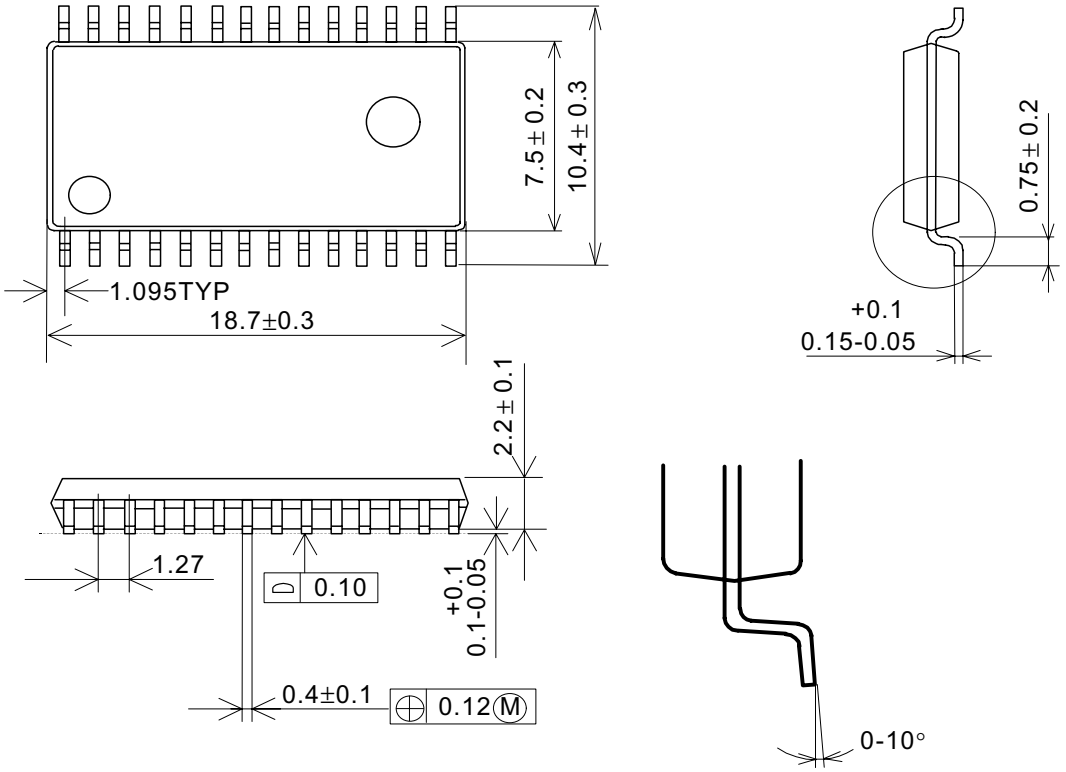


Figure 13. Removing the sprious noise circuit

PACKAGE

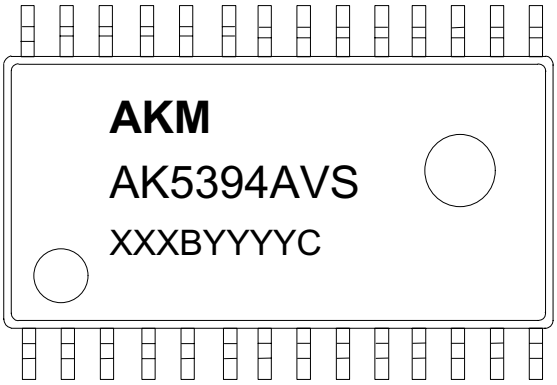
28pin SOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



Contents of XXXBYYYYC

XXXB:	Lot # (X : numbers, B : alphabet)
YYYYC:	Data Code (Y : numbers, C : alphabet)