

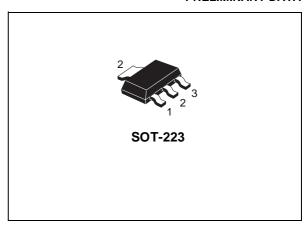
STN1NK60Z

N-CHANNEL 600V - 13Ω - 0.25A - SOT-223 Zener-Protected SuperMESH™ Power MOSFET

PRELIMINARY DATA

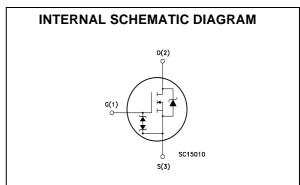
TYPE	V _{DSS}	R _{DS(on)}	I _D	Pw
STN1NK60Z	600 V	< 15 Ω	0.25 A	2 W

- TYPICAL $R_{DS}(on) = 13\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.



APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITH MODE POWER SUPPLIES (SMPS)

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STN1NK60Z	1NK60Z	SOT-223	TAPE & REEL

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STN1NK60Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	0.25	A
ID	Drain Current (continuous) at T _C = 100°C	0.16	A
I _{DM} (•)	Drain Current (pulsed)	1	A
P _{TOT}	Total Dissipation at T _C = 25°C	2	W
	Derating Factor	0.016	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150	ဗင

^(•) Pulse width limited by safe operating area

THERMAL DATA

Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W	ĺ
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GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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⁽¹⁾ $I_{SD} \le 0.3A$, di/dt $\le 200A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_i \le T_{JMAX}$.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50 \mu A$	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 0.4 A		13	15	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = V _, I _D = 0.4 A		0.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		94 17.6 2.8		pF pF pF
Coss eq. (3)	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$		11		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$V_{DD} = 300$ V, $I_D = 0.4$ A $R_G = 4.7\Omega$ $V_{GS} = 10$ V (Resistive Load see, Figure 3)		5.5 5		ns ns
$egin{array}{c} Q_{g} \ Q_{gs} \ Q_{gd} \end{array}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V, I_D = 0.8 A,$ $V_{GS} = 10V$		4.9 1 2.7	6.9	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	$V_{DD} = 300 \text{V}, I_D = 0.4 \text{A}$ $R_G = 4.7 \Omega \text{ V}_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		13 28		ns ns
t _{r(Voff)} t _f t _C	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} =480V, I_D = 0.8A, R_G = 4.7 Ω , V_{GS} = 10V (Inductive Load see, Figure 5)		28 12.5 48		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				0.25 1	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 0.25A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 0.8 A, di/dt = 100A/µs V_{DD} = 20V, T_j = 150°C (see test circuit, Figure 5)		140 224 3.2		ns nC A

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Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.
 3. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Fig. 1: Unclamped Inductive Load Test Circuit

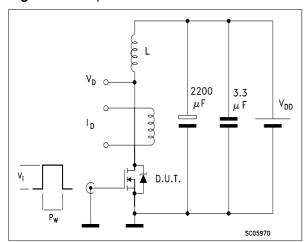


Fig. 3: Switching Times Test Circuit For Resistive Load

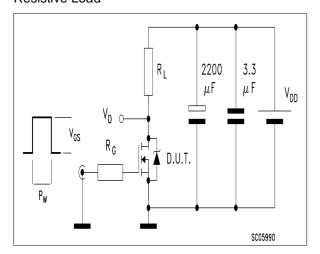


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

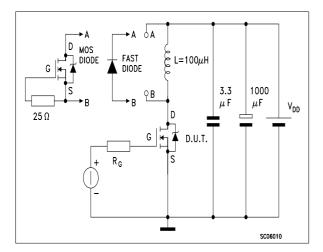


Fig. 2: Unclamped Inductive Waveform

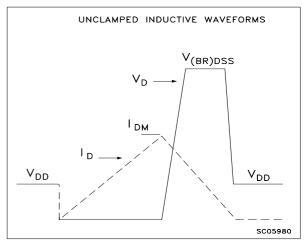
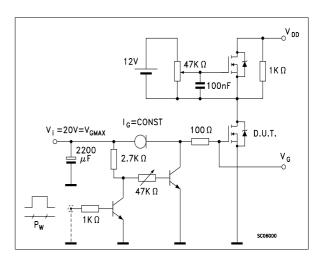


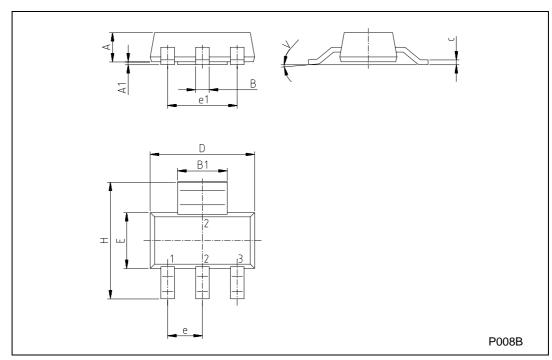
Fig. 4: Gate Charge test Circuit



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SOT-223 MECHANICAL DATA

DIM.		mm			inch		
Diiii.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			1.80			0.071	
В	0.60	0.70	0.80	0.024	0.027	0.031	
B1	2.90	3.00	3.10	0.114	0.118	0.122	
С	0.24	0.26	0.32	0.009	0.010	0.013	
D	6.30	6.50	6.70	0.248	0.256	0.264	
е		2.30			0.090		
e1		4.60			0.181		
Е	3.30	3.50	3.70	0.130	0.138	0.146	
Н	6.70	7.00	7.30	0.264	0.276	0.287	
V			10°			10°	
A1		0.02					



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