NB4L52

2.5V/3.3V/5V Differential Data/Clock D Flip-Flop with Reset

Multi−Level Inputs to LVPECL Translator w/ Internal Termination

The NB4L52 is a differential Data and Clock D flip−flop with a differential asynchronous Reset. The differential inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, LVCMOS, LVTTL, CML, or LVDS logic levels. When Clock transitions from Low to High, Data will be transferred to the differential LVPECL outputs. The differential Clock inputs allow the NB4L52 to also be used as a negative edge triggered device. The device is housed in a small 3x3 mm 16 pin QFN package.

Features

- Maximum Input Clock Frequency > 4 GHz Typical
- 330 ps Typical Propagation Delay
- 145 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 750 mV Peak−to−Peak, Typical
- Operating Range: V_{CC} = 2.375 V to 5.5 V with V_{EE} = 0 V
- Internal Input Termination Resistors, 50 Ω
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- −40°C to +85°C Ambient Operating Temperature

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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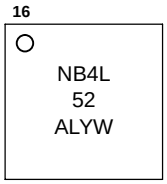
QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week

*For additional marking information, refer to Application Note AND8002/D.

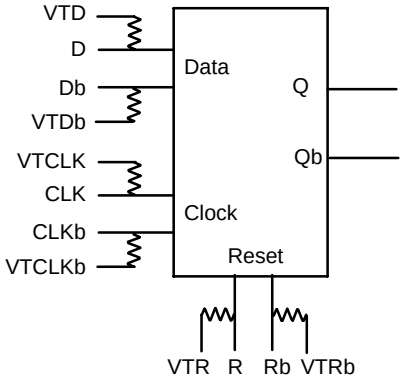


Figure 1. Logic Diagram

Table 1. TRUTH TABLE

R	D	CLK	Q
H	x	x	L
L	L	Z	L
L	H	Z	H

Z = LOW to HIGH Transition
x = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

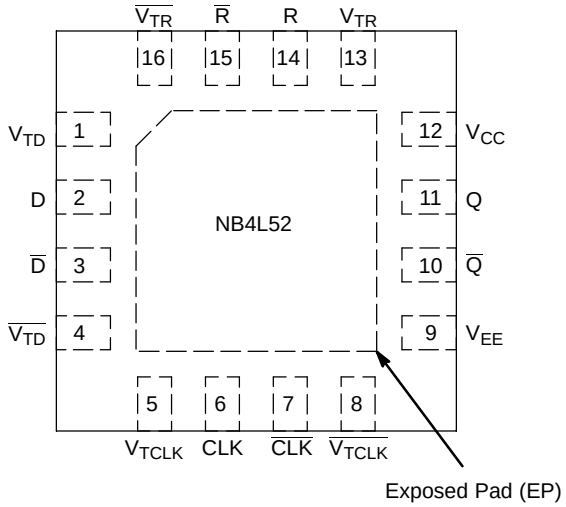


Figure 2. Pinout: QFN−16 (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	V_{TD}	−	Internal 50 Ω Termination Pin. (See Table 4)
2	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. (Note 1)
3	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. (Note 1)
4	$\overline{V_{TD}}$	−	Internal 50 Ω Termination Pin. (See Table 4)
5	V_{TCLK}	−	Internal 50 Ω Termination Pin. (See Table 4)
6	CLK	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. (Note 1)
7	$\overline{CLK}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. (Note 1)
8	$\overline{V_{TCLK}}$	−	Internal 50 Ω Termination Pin. (See Table 4)
9	V_{EE}	−	Negative Supply Voltage
10	$\overline{Q}$	ECL Output	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} − 2.0 V.
11	Q	ECL Output	Noninverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} − 2.0 V.
12	V_{CC}	−	Positive Supply Voltage
13	V_{TR}	−	Internal 50 Ω Termination Pin. (See Table 4)
14	R	LVECL, LVCMOS, LVTTL Input	Noninverted Differential Reset Input. (Note 1)
15	$\overline{R}$	LVECL, LVCMOS, LVTTL Input	Inverted Differential Reset Input. (Note 1)
16	$\overline{V_{TR}}$	−	Internal 50 Ω Termination Pin. (See Table 4)
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pin (VTD, VTDB, VTR, VTRB, VTCLK, VTCLKB) are connected to a common termination voltage or left open, and if no signal is applied on D/DB,CLK/CLKB,R/RB input then the device will be susceptible to self−oscillation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection Machine Model Charged Device Model	Human Body Model	> 2 kV > 200 V > 1 kV
Moisture Sensitivity (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		164
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		6.0	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−6.0	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6.0 −6.0	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$			2.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 LFPM 500 LFPM	16 QFN 16 QFN	41.6 35.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 4)	16 QFN	4.0	°C/W
T_{sol}	Wave Solder Pb−Free	< 3 sec @ 260°C		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

3. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, CLOCK INPUTS, LVPECL OUTPUTS
(V_{CC} = 2.375 V to 5.5 V, V_{EE} = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Inputs and Outputs Open)		16	25	mA
V_{OH}	Output HIGH Voltage (Note 5, 6)	V_{CC} − 1145	V_{CC} − 1020	V_{CC} − 895	mV
	V_{CC} = 5.0 V	3855	3980	4105	
	V_{CC} = 3.3 V	2155	2280	2405	
	V_{CC} = 2.5 V	1355	1480	1605	
V_{OL}	Output LOW Voltage (Note 5, 6)	V_{CC} − 1945	V_{CC} − 1770	V_{CC} − 1600	mV
	V_{CC} = 5.0V	3055	3230	3400	
	V_{CC} = 3.3V	1355	1530	1700	
	V_{CC} = 2.5V	555	730	900	
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 6 & 8)					
Vth	Input Threshold Reference Voltage Range (Note 7)	1050		V_{CC} − 150	mV
V_{IH}	Single−ended Input HIGH Voltage	Vth + 150		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		Vth − 150	mV
DIFFERENTIAL INPUT DRIVEN DIFFERENTIALLY (Figures 7 & 9)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 150	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 8)	1125		V_{CC} – 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})	150		2800	mV
I_{IH}	Input HIGH Current D / Db, CLK / CLKb, R /Rb (VTx/VTxb Open)	−150		150	μA
I_{IL}	Input LOW Current D / Db, CLK / CLKb, R /Rb (VTx/VTxb Open)	−150		150	μA
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. LVPECL outputs loaded with 50 Ω to V_{CC} – 2.0 V for proper operation.
6. Input and output parameters vary 1:1 with V_{CC}.
7. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{CMRMIN} varies 1:1 with V_{EE}, V_{CMRMAX} varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 5.5 V; V_{EE} = 0 V (Note 9)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 11) (See Figure 4) $f_{in} \le 2.0$ GHz $f_{in} \le 3.0$ GHz $f_{in} \le 4.0$ GHz	530 490 380	770 720 580		530 490 380	780 730 580		530 490 380	760 680 530		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK to Q R to Q					330	400 500				ps
t_s	Setup Time	100			100			100			ps
t_h	Hold Time	50			50			50			ps
t_{RR}	Reset Recovery	400			400			400			ps
t_{PW}	Minimum Pulse Width R/$\overline{R}$	250			250			250			ps
t_{JITTER}	RMS Random Clock Jitter (Note 10) $f_{in} \le 2.0$ GHz $f_{in} \le 3.0$ GHz $f_{in} \le 4.0$ GHz Peak−to−Peak Data Dependent Jitter $f_{in} \le 2.0$ GHz $f_{in} \le 3.0$ GHz $f_{in} \le 4.0$ GHz						1 1 1 20 20 20				ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 11)	150		2800	150		2800	150		2800	mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz (20% − 80%)	80	135	190	80	145	190	80	155	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Measured by forcing V_{INPPt} (MIN) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC} – 2.0 V. Input edge rates 40 ps (20% − 80%).
10. Additive RMS jitter with 50% duty cycle clock signal at 2 GHz & 3 GHz.
11. Input and output voltage swing is a single−ended measurement operating in differential mode.

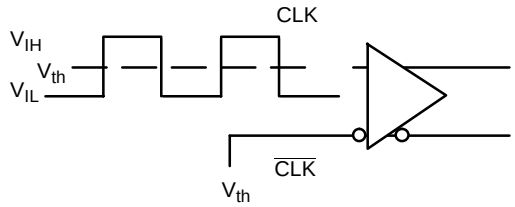


Figure 3. Differential Input Driven Single−Ended

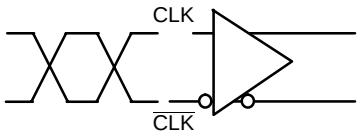


Figure 4. Differential Inputs Driven Differentially

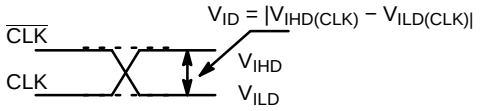


Figure 5. Differential Inputs Driven Differentially

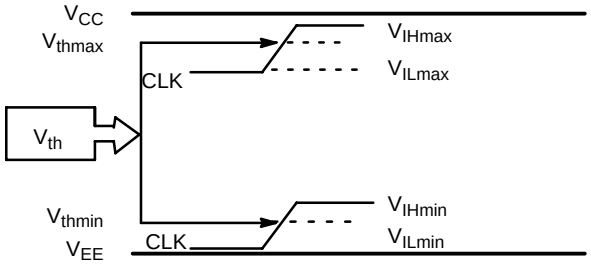


Figure 6. V_{th} Diagram

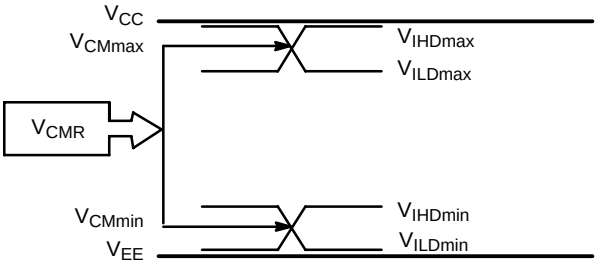


Figure 7. V_{CMR} Diagram

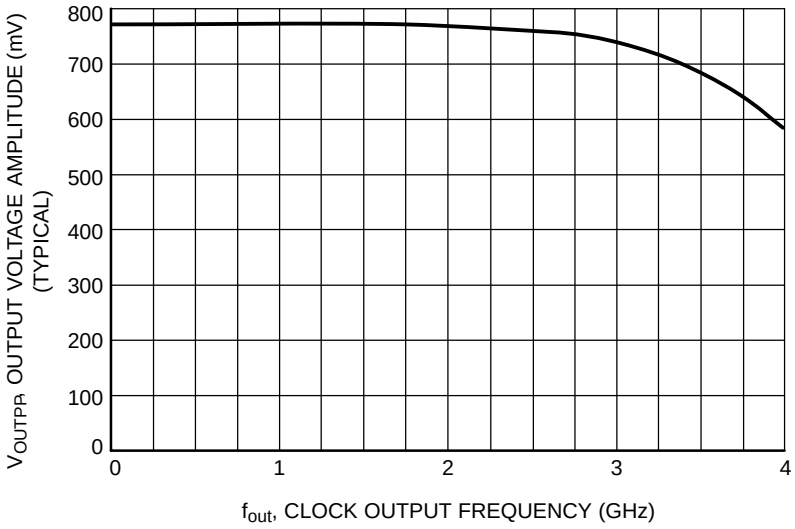


Figure 8. Output Voltage Amplitude (V_{OUTPP}) versus Clock Output Frequency at Ambient Temperature (Typical) (f_{out} QA/QB) = f_{in} ÷ n; f_{in} ≤ 3.0 GHz).

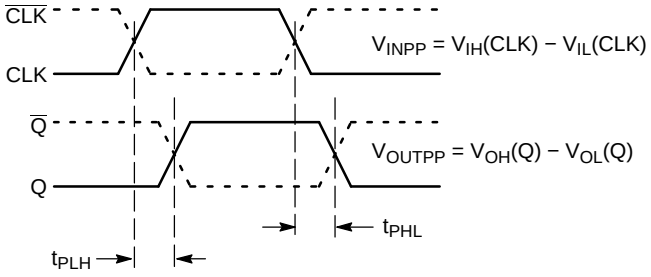


Figure 9. AC Reference Measurement

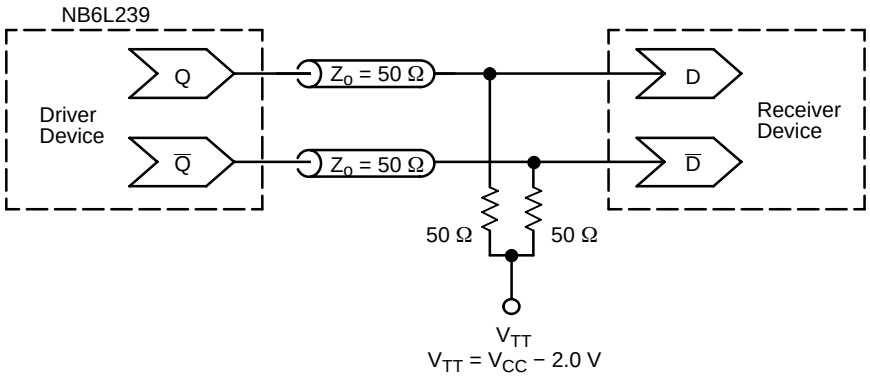


Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NB4L52MNG	QFN−16, 3 x 3 mm (Pb−Free)	123 Units / Rail
NB4L52MNR2G	QFN−16, 3 x 3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1642/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

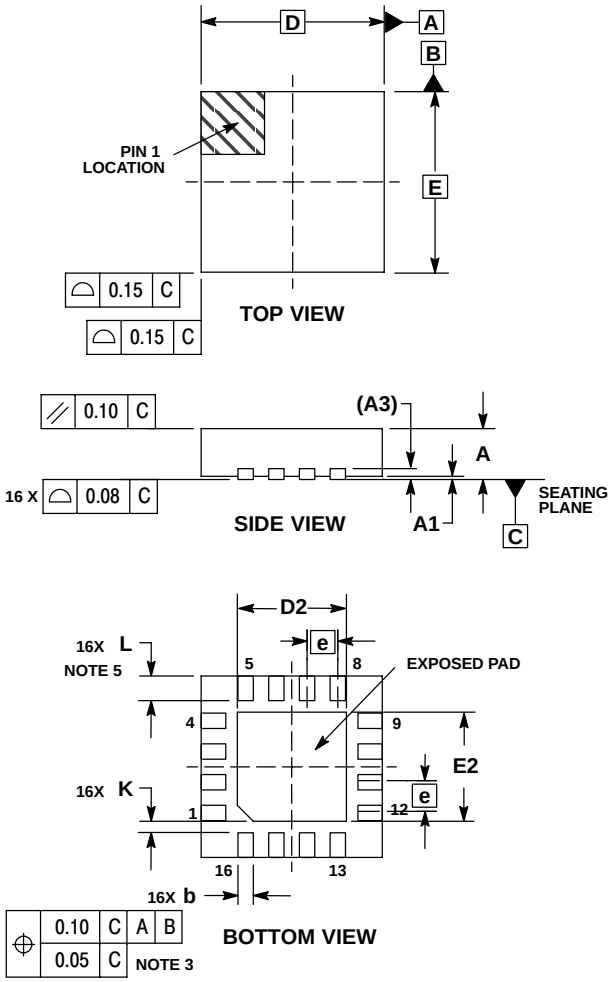
AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

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