MR27V3266D

2M x16 / 1M x32 Synchronous OTP ROM

DESCRIPTION

The MR27V3266D is a 32Mbit One Time Programmable Synchronous Read Only Memory whose configuration can be electrically switched between 2,097,152 x16bit(word mode) and 1,048,576 x32bit(double word mode) by the state of the /WORD pin. The MR27V3266D supports high speed synchronous read operations using a single 3.3V power supply.

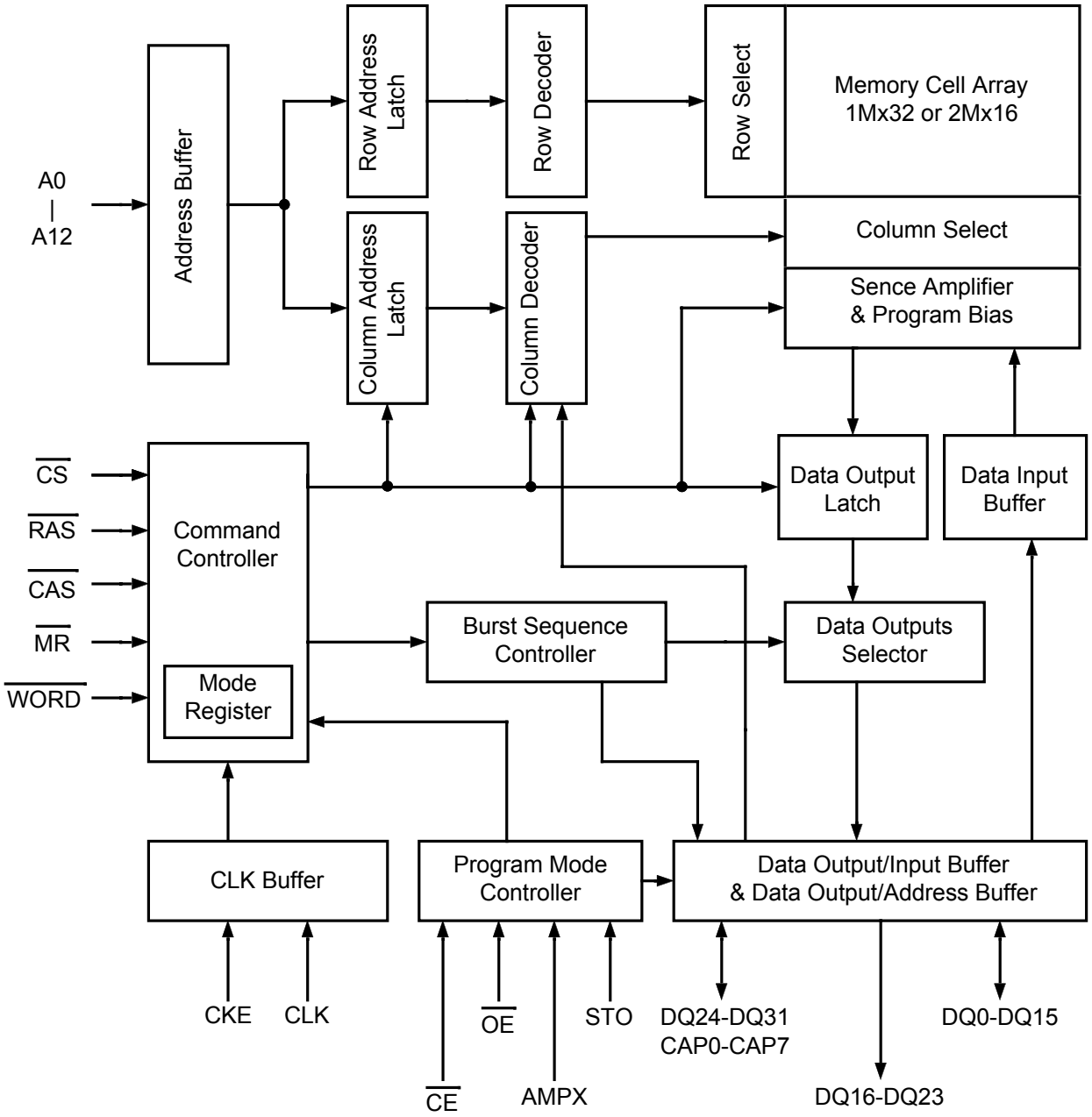
FEATURES ON READ

- 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual, electrically switchable configurations
  2M x16(word mode) / 1M x32(double word mode)
- All inputs are sampled at the rising edge of the system clock
- High speed read operation
  - 66MHz (CAS Latency=5) / 50MHz (CAS Latency=4, 5)
    - tRCDmin : 2 Clock cycle
    - Burst Length (4, 8)
    - Data scramble (sequential, interleave)
- DQM for data out masking
- No Precharge operation is required. No Refresh operation is required.
- No power on sequence is required.
  - Mode register is automatically initialized to the default state after power on.
  - "Row Active" command to read data is applicable as the first command just after power on.
- Single Bank operation
- Package : TSOP II 86-P-400-0.50-K

FEATURES ON PROGRAMMING

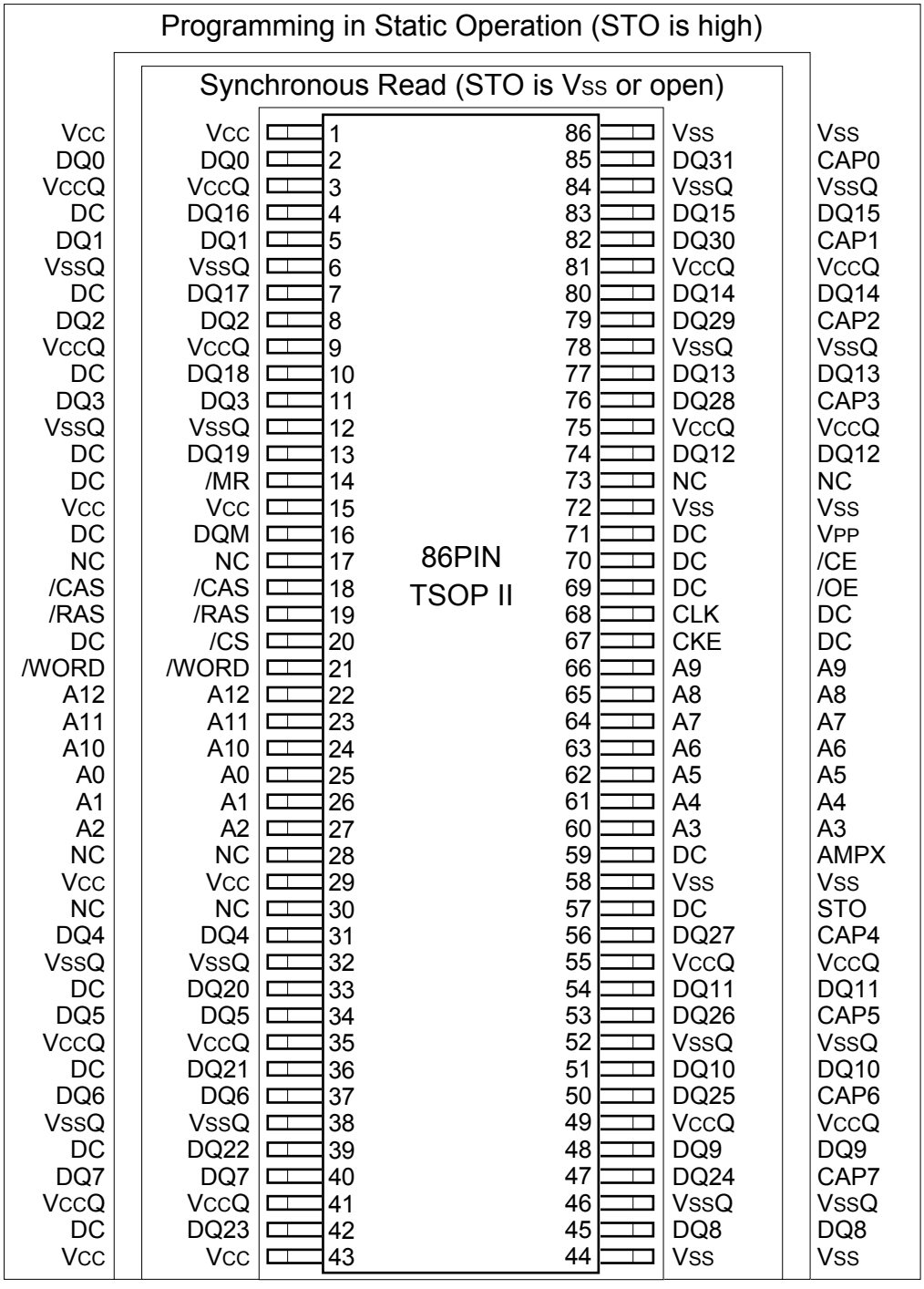
- 9.75V programming Power supply
- Programming algorithm is compatible with conventional asynchronous 32M OTP.
  MR27V3266D can be programmed with conventional EPROM programmers.
  - Synchronous Burst read or Static Programming Operation are selected by the state of STO pin.
    - High STO level enables full static programming. (Program, Program Verify, asynchronous Read)
    - Low STO level enables synchronous burst read.
  - Exclusive 86pin socket adapters are available from OKI to support programming requirements.
    - The socket adapter is used on a 48DIP socket on the programmer.
    - The socket adapter is designed with the STO pin connected to V_{CC} in order to program MR27V3266D as conventional 32M OTP.
  - EPROM programmer must have the proper algorithm for 32M OTP.
    - *Device damage can occur if improper algorithm is used.
- High speed programming
  - 10μs programming pulse per word allows high speed programming.

FUNCTION BLOCK DIAGRAM



PIN CONFIGURATION

TOP VIEW



DC(Don't Care) : Logical input level is ignored, however the pin is connected to input buffer of OTP

PIN FUNCTION FOR SYNCHRONOUS READ OPERATION (STO pin is low level or open)

PIN NAME	FUNCTION	DESCRIPTION
STO	Static Operation	Must be low for synchronous operation. Internal resistance (around 10k ohms) pulls the input level down to VSS when this pin is open. High level STO enables programming operation compatible with standard OTPs.
CLK	System Clock	All inputs are sampled at the rising edge.
/CS	Chip Select	Enables command sampling by the CLK signal with a low level on the /CS input.
CKE	Clock Enable	Masks internal system clock to freeze the CLK operation of subsequent CLK cycle. CKE must be enabled for command sampling cycles. CLK is disabled for two types of operations. 1)Clock Suspend 2)Power down.
A0-A12	Address	Row and column addresses are multiplexed on the same pins. Row address:RA0-RA12 Column address:CA0-CA6(x32) / CA0-CA7(x16)
/RAS	Row Address Strobe	Functionality depends on the combination. See the function table.
/CAS	Column Address Strobe	
/MR	Mode Register Set	
DQ0-DQ31	Data Output	Data outputs are valid at the rising edge of CLK for read cycles. Except for read cycles DQn is high-Z state.
DQM	Data Output Masking	Data outputs are masked after two cycles from when high level DQM is applied.
/WORD	x32/x16 Organization Selection	The /WORD pin defines the organization of each read command to be x16 (word mode) or x32 (double word mode). High=x32 Low=x16
VCC	Power Supply	3.3V Power supply
VSS	Ground	
VCCQ	Data Output Power Supply	3.3V Power supply to DQ0-DQ31
VSSQ	Data Output Ground	
NC	No Connection	
DC	Don't Care	Logical input level is ignored.

PIN FUNCTION FOR PROGRAMMING OPERATION (STO pin is high level)

PIN NAME	FUNCTION	DESCRIPTION
STO	Static Operation	Must be set high for programming operation. Internal resistance (around 10k ohms) pulls the input level down to V_{SS} for open state condition to be low level for synchronous read operation.
AMPX	Address Multiplex	When AMPX is high, multiplexed address inputs are enabled on A0-A12. When AMPX is low, the addresses are not multiplexed and all address bits must be supplied to A0-A12(Row Address) and CAP0-CAP7(Column Address) simultaneously. This pin should be set low for loose device programming operation.
A0-A12	Address	When AMPX is low, A0-A12 is row address input. When AMPX is high, row and column addresses are multiplexed on the same pins.
/RAS	Row address strobe	When AMPX is high, row address is latched at the falling edge of /RAS. When AMPX is low, input is not used.
/CAS	Column address strobe	When AMPX is high, column address is latched at the falling edge of /CAS. When AMPX is low, input is not used.
DQ0-DQ15	Data Input/Output	Input of data for programming and output for program verify and read data.
/WORD	x32/x16 organization Selection	The /WORD pin defines the organization to be x16(word mode) or x32(double word mode). High= x32 Low = x16 This pin is pulled down to V_{SS} for programming operation only when STO is high level.
CAP0-CAP7	Address Input	When /WORD is low, High-Z state on CAP0-CAP7 is held to be input pins. When AMPX is low, CAP0 - CAP7 is column address input. When AMPX is high, input is not used.
/OE	Output Enable	Control signal input for programming. /OE of conventional OTP.
/CE	Chip Enable	Control signal input for programming. Function for programming is associated with conventional OTP.
V_{CC}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V_{CC}Q/V_{SS}Q	Data Output Power/Ground	Power and ground for output.
V_{PP}	Program Power Supply	High voltage program power is supplied through V_{PP} pin. When V_{PP} is higher than a predetermined voltage level between V_{CC}+0.5V and V_{CC}+2V, pin function alters to high V_{PP} mode. To keep stable static read operation V_{PP} pin must be kept lower than V_{CC}+0.5V.

The functionality of loose device programming must be studied with the specification of socket adapter that will be supplied by OKI. MR27V3266D on the socket adapter is the same programming functionality as conventional OTP.

FUNCTION TABLE FOR SYNCHRONOUS READ

COMMAND NAME	FUNCTION	CKEn-1	CKEn	/CS	/RAS	/CAS	/MR	DQM	Add.	/WORD	STO	Notes
Mode Register Set	Mode Register Set	H	X	L	L	L	L	X	Code	X	L	1
Row Active	Row Address Latch	H	X	L	L	H	H	X	RA	X	L	2
Read Word (x16)	Column Address Latch Trigger Burst Read	H	X	L	H	L	H	X	CA	L	L	3
Read Double Word (x32)	Column Address Latch Trigger Burst Read	H	X	L	H	L	H	X	CA	H	L	3
Burst Stop	Burst Stop	H	X	L	H	H	L	X	X	X	L	4
Precharge	Burst Stop	H	X	L	L	H	L	X	X	X	L	4
Clock Suspend (on Read)	Entry	H	L	X	X	X	X	X	X	X	L	5
	Exit	L	H	X	X	X	X	X	X	X	L	5
Power Down (on Active Standby)	Entry	H	L	H	X	X	X	X	X	X	L	6
	Exit	L	H	X	X	X	X	X	X	X	L	6
Read Output	Output Enable	H	X	X	X	X	X	L	X	X	L	
Mask Output	High-Z Output	H	X	X	X	X	X	H	X	X	L	
No Operation	Write on SDRAM	H	X	L	H	L	L	X	X	X	L	
	Self Refresh on SDRAM	H	L	L	L	L	H	X	X	X	L	
	Illegal on SDRAM	H	H	L	L	L	H	X	X	X	L	
		H	X	H	X	X	X	X	X	X	L	
		H	X	L	H	H	H	X	X	X	L	

(H=Logical high, L=Logical low, X=Don't Care, L of STO includes pin open due to internal pull down resistor)

(CKEn expresses the logical level at the simultaneous cycle with a command.)

Note

1. Refer to "Mode register Field Table" for Address Codes, and Mode Transition Chart for operational state.
   After power on any command can be sampled at any cycle in Active Standby state.
   After "Mode register Set" command is sampled, no new command can be accepted for 3 CLK cycles.
   The /CS input must be kept high for the 3 CLK cycles to prevent unexpected sampling of a command.
2. The "Row Active" command is effective till new "Row Active" command is implemented.
3. The /WORD input is sampled simultaneously with "Read" command to select data width.
   A Double Word Burst(x32) or a Word Burst(x16) is selected by the /WORD input for each "Read" command.
   On condition of constant voltage level on /Word pin, organization is fixed to either x16 or x32.
   "Read" command ends it's implementation by itself at the finishing cycle of the burst read.
4. Since OTP technology uses static sense amplifiers, the "Precharge" command is not required however, due to customer request for the similarity of logical input code with SDRAM command, the name of "Precharge" is adopted. Function of "Precharge" command and "Burst Stop" command is only to stop the burst read cycles delayed by CAS Latency.
5. Sampled low level CKE disables CLK buffer to suspend internal clock signals at the next rising edge of CLK.
   Sampled high level CKE enables internal clock at the next rising edge of CLK.
   Low level CKE sampled in the period from the simultaneous cycle with a "Read" command till the end of the burst read cycle is distinguished with internal command controller from the low level CKE sampled in Active Standby state not to stop data sensing and burst read operation those consume power.
6. Low level CKE sampled in Active Standby state cuts power dissipation to be in Power Down state.
   High level CKE sampled in Power Down state enables internal CKE to be in Active Standby state with preserved row address.

MODE REGISTER FIELD TABLE

Address	A5	A4	A3	A2	A1	A0
Function	CAS Latency			Burst Type	Burst Length	

A5	A4	A3	Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	4
1	0	0	5
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	Type
0	Sequential
1	Interleave

A1	A0	Length
0	0	Reserved
0	1	4
1	0	8
1	1	Reserved

Note
A7 and A8 must be low during Mode Register Set cycle.
During power on, mode register is initialized to the default state when V_{CC} reaches a specific voltage. (less than 3.0V)
The default state of Mode Register is below.
CAS Latency=5
Burst Type=Sequential
Burst length=4

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

ADDRESSING MAP

(1) /WORD = "H" : x32 Organization

Pin Name	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Row Address	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Column Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	X	X	X	X	X	X

(X = Don't Care)

(2) /WORD = "L" : x16 Organization

Pin Name	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Row Address	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Column Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	X

(X = Don't Care)

(3) Programming

Address displayed on programmer : x16	Ad0	Ad1	Ad2	Ad3	Ad4	Ad5	Ad6	Ad7	Ad8	Ad9	Ad10	Ad11	Ad12
Device Address : x16 STO = "H", AMPX = "L"	CAP0	CAP1	CAP2	CAP3	CAP4	CAP5	CAP6	CAP7	A0	A1	A2	A3	A4
Device Address : x16 STO = "H", AMPX = "H"	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	RA0	RA1	RA2	RA3	RA4
Address (STO = "L") /WORD = "L" : x16	CA0	Note2 CA1	Note3 CA2	CA3	CA4	CA5	CA6	CA7	RA0	RA1	RA2	RA3	RA4
Address (STO = "L") /WORD = "H" : x32	Note1	CA0	Note4 CA1	Note5 CA2	CA3	CA4	CA5	CA6	RA0	RA1	RA2	RA3	RA4

Address displayed on programmer : x16	Ad13	Ad14	Ad15	Ad16	Ad17	Ad18	Ad19	Ad20
Device Address : x16 STO = "H", AMPX = "L"	A5	A6	A7	A8	A9	A10	A11	A12
Device Address : x16 STO = "H", AMPX = "H"	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Address (STO = "L") /WORD = "L" : x16	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Address (STO = "L") /WORD = "H" : x32	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12

User of MR27V3266D is recommended to study the relation between "Address displayed on programmer" and "Address(STO="L")" ignoring "Device Address:x16, STO="H"".
Order of data on Synchronous Read operation(STO="L") is checked on this table.
"Device Address:x16, STO="H"" will be utilized to design socket adapter on programmer or to check boards designed to mount blank OTP and program OTP on board.
OKI will supply socket adapter to program MR27V3266D as conventional x16 standard OTP. The users and the venders of programmer who use the socket adapter can ignore "Device Address:x16, STO="H"".

Note
1. A0 in programmer distinguishes upper word(x16) or lower word(x16) of Double word(x32).
   On word(x16) organization the address of device corresponds to the address of programmer.
   On double word(x32) organization the address numeral code of device is half of that in programmer, and output on DQ0-DQ15 is lower word(A0="0") and output on DQ16-DQ31 is upper word(A0="1").
2. CA1 is MSB of burst read on condition of /WORD="L" and BL=4
3. CA2 is MSB of burst read on condition of /WORD="L" and BL=8
4. CA1 is MSB of burst read on condition of /WORD="H" and BL=4
5. CA2 is MSB of burst read on condition of /WORD="H" and BL=8

READ OPERATIONS

CLOCK (CLK)

The clock input enables MR27V3266D to sample all the inputs, control internal circuitry, and turn on output drivers. All timings are referred to the rising edge of the clock. All inputs with high level CKE and low level /CS should be valid at the rising edge of CLK for proper functionality.

CLOCK ENABLE (CKE)

The clock enable(CKE) turns on or switches off the admission of the clock input into the internal clock signal lines. All internal circuits are controlled by the internal clock signal to implement every command. High level CKE sampled at CKEn-1 clock cycle enables the admission of the rising edge of clock input into internal clock line at CKEn cycle. Low level CKE sampled at CKEn-1 cycle suspends the rising edge of CLK at CKEn cycle. The suspension of internal clock signal in all state ignores new input except CKE, and holds internal state and output state. Low level CKE in Active Standby state, defined as Power Down state, cuts power dissipation. In Power Down state the contents of mode register and Row Address are preserved. After recovering high level CKE to exit from Power Down state, MR27V3266D is in Active Standby state. Low level CKE just after the sampling of "Read" command till the completion of burst read, defined as Clock Suspend, makes read operation go on with power dissipation. Any command operation does not interrupted by arbitrary low level CKE. Sampling command with low level CKE preceded with high level CKE is illegal.

POWER ON

Apply power and start clock considering following issues.

1. During power on Mode Register is initialized into default state.
   (default state: CAS latency=5, Burst Type=Sequential, Burst length=4)
2. After power on MR27V3266D is in Active Standby state and ready for "Mode Register set" command or "Row Active" command. MR27V3266D requires neither command nor waiting time as power on sequence after starting CLK input in order to start "Row Active" command to read data.
3. It is recommended in order to utilize default state of Mode Register that /MR and CKE inputs are maintained to be pulled up during power on till the implementation of the first "Row Active" command.
   After above power on "Row Active" command and "Read" command can be started immediately on default Mode Register state.
4. It is recommended that DQM input is maintained to be pulled up to prevent unexpected operation of output buffers.

ORGANIZATION CONTROL

Organization of data output(DQ0-DQ31) depends on the logical level on /WORD at the input timing of every "Read" command. High level sampling of /WORD derives double word mode(x32) output and low level sampling of /WORD derives word mode(x16) output. Constant /WORD level input brings consistent organization.

MODE REGISTER

Mode register stores the operating mode of MR27V3266D. Operating modes are consisted with CAS latency, Burst Type, and Burst Length. Registration of RAS latency is not required, because RAS to CAS delay(tRCD) is requested independently of system clock. When the contents of Mode register are required to be changed for the next operation, "Mode Register Set" command can be sampled at any cycle in Active Standby state. After "Mode Register Set" command is sampled, /CS must be fixed to logical high level to prevent sampling of new command input during succeeding three clock cycles.
Refer to Mode Register Field Table for the relation between Operation modes and input pin assignment.

READ OPERATIONS

CAS LATENCY

After sampling "Read" command MR27V3266D starts actual data read operation with sense amplifiers, and transmits the data from sense amplifiers to data out buffers to start burst read. This flow of sequential functionality takes time as clock cycles defined as CAS latency(CL). CAS latency is set in Mode Register as either four cycles or five cycles. In this sequence(from sampling "Read" command to start of driving data bus) sense amplifiers consume maximum current flow. The detailed sequence is below.

1. Fix column address of memory matrix driver. Row address is already fixed with "Row Active" command. (at 1st cycle)
2. Read data of selected memory cells with sense amplifiers.
3. Deliver data detected with sense amplifiers to the register for data output latch.
4. Couple selectively the section of the register storing each (double)word to output buffers.
5. Turn off sense amplifiers to save power. (at CL-1 cycle)
6. Enable output buffers to drive data bus. (at CL-1 cycle)
7. Data output on data bus can be sampled at the rising edge of system clock at CL cycle.

New "Row Active" command or new "Read" command can be sampled to perform gapless burst read at CL-1 clock cycle of the last "Read" command. New command preceding CL-1 cycle interrupts sense amplifiers to read the data at the selected memory cells of the last "Read" command. Interrupted "Read" command perishes or outputs invalid data before the starting of the data burst of new "Read" command. Refer to the timing chart of "Burst Read/Interrupt I" and "Burst Read/Interrupt II".

BURST READ

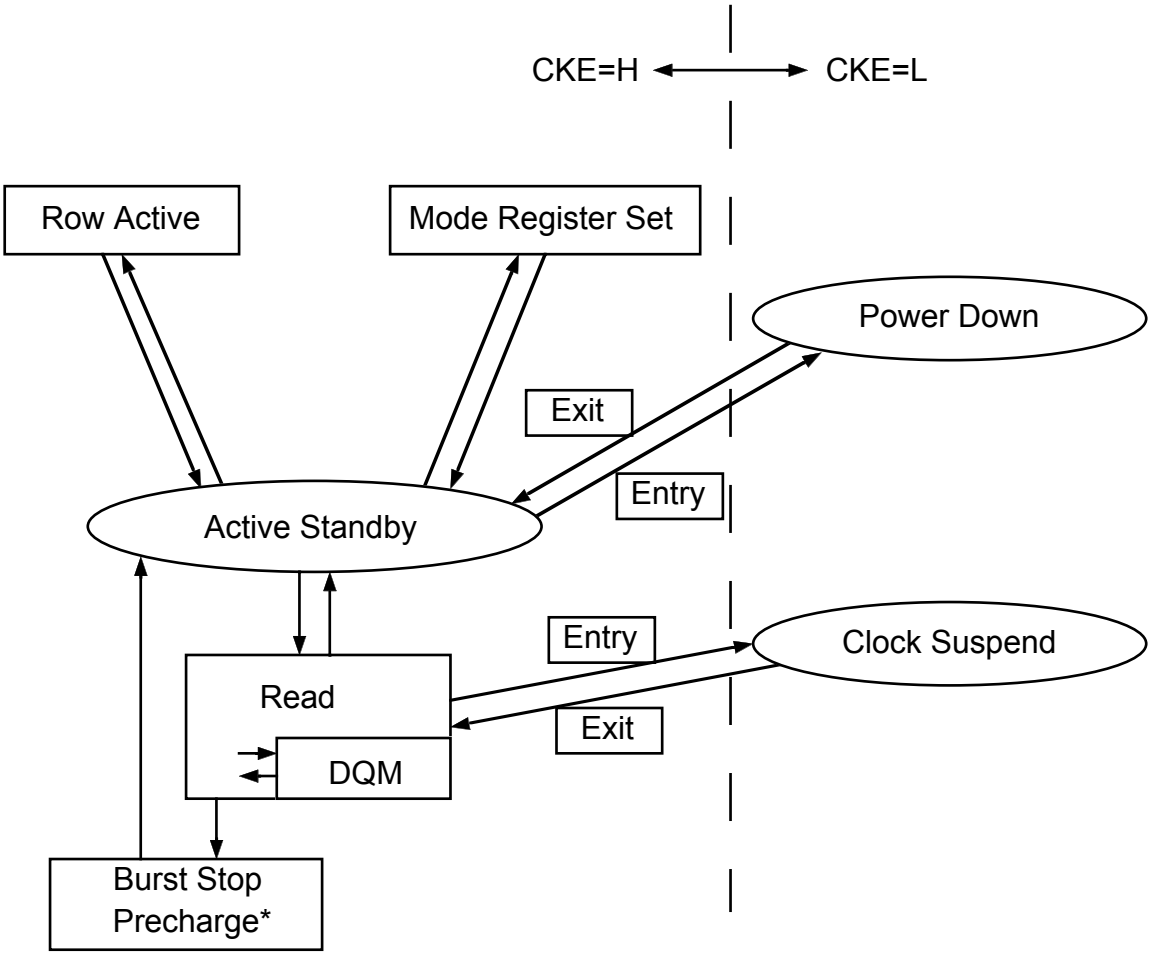
Data outputs are consecutive during the cycle number defined as Burst Length(BL). The latest burst read is completed unless any interruption such as "Precharge" command stops the sequential data output. Burst Length is set in Mode Register as either four or eight. After sampling of "Read" command the first output can be read at the cycle delayed by CAS latency. Burst Type is also stored in Mode register as either sequential or interleave. The output buffers go into high impedance state after burst read sequence is finished, unless a new "Read" command has been sampled to perform gapless read or preemptive read. Burst read can be interrupted by "Burst Stop" command or "Precharge" command at the cycle delayed by CAS latency from the command. On condition that reading data with sense amplifiers of preceding "Read" command is not interrupted by new "Read" command or "Row active" command, burst read of preceding "Read" command is continued regularly until the burst data sequence of the new "Read" command starts. The new(latest) burst data sequence always starts regularly.

DQM

Input level on DQM is sampled at rising edge of system clock to mask data at two cycles later. Output of masked data is high-Z state.

READ OPERATIONS

MODE TRANSITION CHART



*All operation of "Precharge" command is to stop burst read.

Note

: passing command

: state can be kept for any duration

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} Relative to V_{SS}	V_{CC},$V_{CC}Q$	-0.5	5	V
Voltage on Any pin Relative to V_{SS}	V_{IN}, V_{OUT}, DC	-0.5	V_{CC} + 0.5	V
Voltage on V_{PP} Relative to V_{SS}	V_{PP}	-0.5	10	V
Operating Temperature	Ta	0	70	degree C
Storage Temperature	Tstg	-55	125	degree C
Short Circuit Current	I_{OS}	-	50	mA
Power Dissipation	P_D	-	1	W

RECOMMENDED OPERATING CONDITIONS for SYNCHRONOUS READ

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC},$V_{CC}Q$	3.0	3.3	3.6	V
Voltage Level on DC pin	-	-0.5	-	V_{CC} + 0.3	V
Input High Voltage	V_{IH}	2.0	-	5	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	Ta	0	-	70	degree C

CAPACITANCE

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C_{IN}	-	5	pF
Output Capacitance	C_{OUT}	-	7	pF

DC CHARACTERISTICS FOR SYNCHRONOUS READ

Parameter	Symbol	Min	Max	Unit	Test condition	
Power Down Current	I_{CCS1}	-	1	mA	CKE = 0.8V	tCC = 15ns
	I_{CCS2}	-	100	µA	CKE = 0V	
Active Standby Current	I_{CC1}	-	100	mA	CKE = 2.0V	/CS = V_{CC} tCC = 15ns
Gapless Burst Read Current	I_{CC2}	-	150	mA	CKE = V_{CC}	tCC = 15ns, DQM = H, CL = 4, BL = 4
Input Leak Current	I_{IL}	-10	10	µA	0V > V_{IN} > V_{CC} + 0.3V	
Output Leak Current	I_{OL}	-10	10	µA	0V > V_{IN} > V_{CC}	
Input High Voltage	V_{IH}	2.0	5	V		
Input Low Voltage	V_{IL}	-0.3	0.8	V	Note1	
Voltage Level on DC pin		-0.5	V_{CC} + 0.3	V		
Output High Voltage Level	V_{OH}	2.4	-	V	I_{OH} = -2mA	
Output Low Voltage Level	V_{OL}	-	0.4	V	I_{OL} = 2mA	

(Voltage levels are referred to V_{SS})

Note
1. V_{IL} min can be -1.5V for the pulse width shorter than 10ns.
   Pulse width is measured at 50% of pulse peak level.

AC CHARACTERISTICS FOR SYNCHRONOUS READ (1/2)

Parameter			Symbol	Min	Max	Unit	Notes
CLK Cycle time			tCC	15	-	ns	
Data to Valid Output Delay			tAC	-	10	ns	
Data Output Hold Time			tOH	4	-	ns	
CLK High Pulse Width			tCH	4	-	ns	
CLK Low Pulse Width			tCL	4	-	ns	
Input Setup Time			tSI	4	-	ns	
Input Hold Time			tHI	2	-	ns	
CLK to Output in Low-Z			tOLZ	0	-	ns	
CLK to Output in High-Z			tOHZ	-	10	ns	
Input Level Transition Time			tT	0.1	10	ns	
"Row Active" to "Read" Delay Time			tRCD	2CLK	-	Cycle	
"Read" to "Row Active" delay (Words of preceding "Read" command can be read) < Random Access >	BL = 4	CL = 4	tCRD	3CLK	-	Cycle	1,2
		CL = 5	tCRD	4CLK	-	Cycle	1
	BL = 8	CL = 4	tCRD	3CLK	-	Cycle	1,2
		CL = 5	tCRD	4CLK	-	Cycle	1
"Read" to "Read" delay (Words of preceding "Read" command can be read) < Sequential Access >	BL = 4	CL = 4	tCCD	3CLK	-	Cycle	1,2
		CL = 5	tCCD	4CLK	-	Cycle	1
	BL = 8	CL = 4	tCCD	3CLK	-	Cycle	1,2
		CL = 5	tCCD	4CLK	-	Cycle	1
"Row Active" Cycle Time (Words of preceding "Read" command can be read) < Random Access >	BL = 4	CL = 4	tRC	3CLK + tRCD	-	Cycle	1,2
		CL = 5	tRC	4CLK + tRCD	-	Cycle	1
	BL = 8	CL = 4	tRC	3CLK + tRCD	-	Cycle	1,2
		CL = 5	tRC	4CLK + tRCD	-	Cycle	1
"Read" to "Read" delay (Gapless burst read) < Sequential Access >	BL = 4	CL = 4	tCCD	4CLK	-	Cycle	2
		CL = 5	tCCD	4CLK	-	Cycle	1
	BL = 8	CL = 4	tCCD	8CLK	-	Cycle	2
		CL = 5	tCCD	8CLK	-	Cycle	
"Read" to "Burst Stop" Delay				1CLK	-	Cycle	
"Read" to "Precharge" Delay				1CLK	-	Cycle	
Power Down Exit Setup Time			tPDE	tSI + 1CLK	-	Cycle	

Note

1. Shortage of clock cycles interrupt the data sensing of preceding "Read" command.
   The shortage of cycle time for preceding command is detected by internal command controller to cease the preceding command operation.
   The latest "Row Active" or "Read" command is completed.
   When legal tCCD is shorter than BL, burst read is terminated with another burst read.
2. 50MHz only

AC CHARACTERISTICS FOR SYNCHRONOUS READ (2/2)

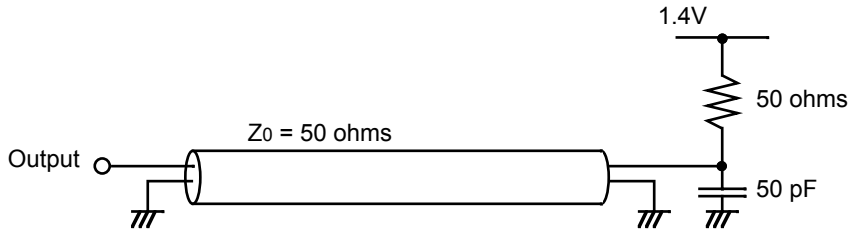
Parameter	Symbol	Value	Unit	Notes
Clock Disable time from CKE	tCKE	1CLK	Cycle	
Clock Enable time from CKE	tCKE	1CLK	Cycle	
Output High impedance from DQM	tDQM	2CLK	Cycle	
Recovery from DQM	tDQM	2CLK	Cycle	
Output High impedance from "Burst Stop"	tBOH	CL	Cycle	
Output High impedance from "Precharge"	tPOH	CL	Cycle	
"Row Active" input from "Mode Register Set"	tMRD	3	Cycle	

AC TEST CONDITIONS

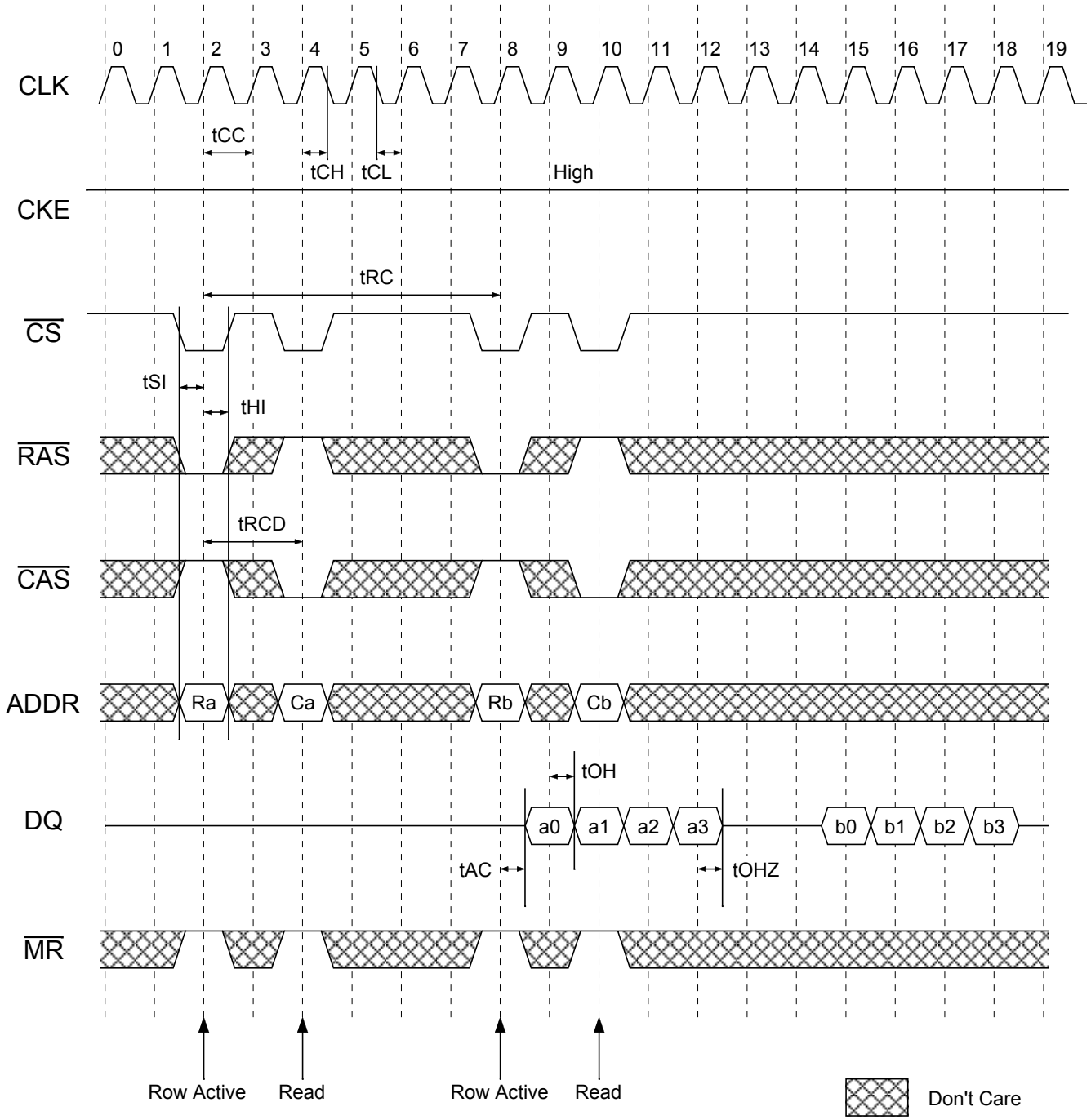
Parameter	Values	Notes
Input Signal Levels	V_{IH} / V_{IL} = 2.4V / 0.4V	
Timing Reference Level of Input/Output Signals	1.4V	
Transition Time of Input Signals	tr / tf = 1ns / 1ns	1
Output Load	LVTTL	2

Note1
Transition time of input signals is measured between 0.8V and 2.0V .
If tr or tf is longer than 1ns, "Timing Reference Level of Input/Output Signals" is changed to V_{IL} or V_{IH} / 0.8V or 2.0V respectively.

Note2
Output Load



Read Cycle I : Random Access @ CAS Latency = 5, Burst Length = 4



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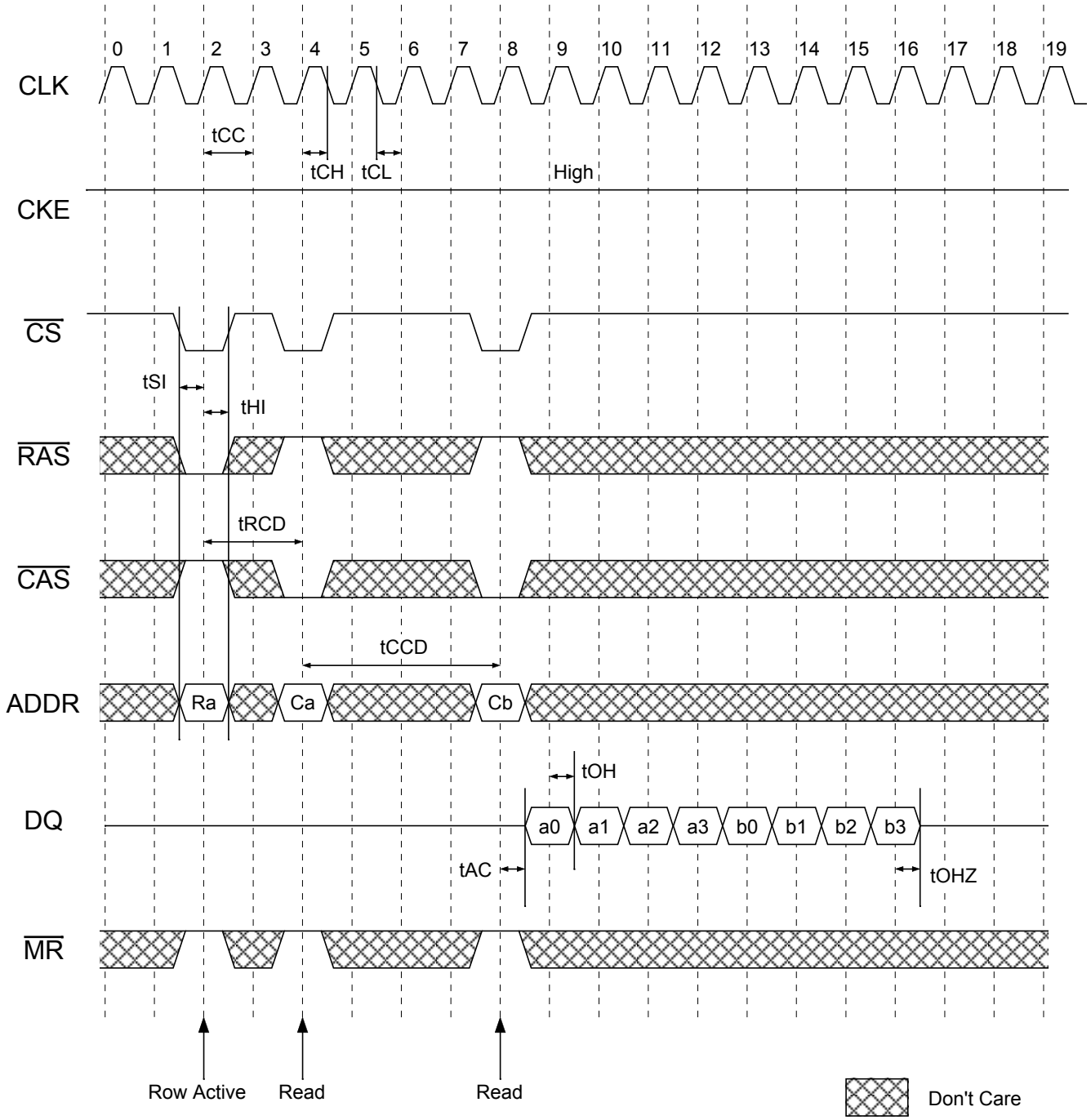
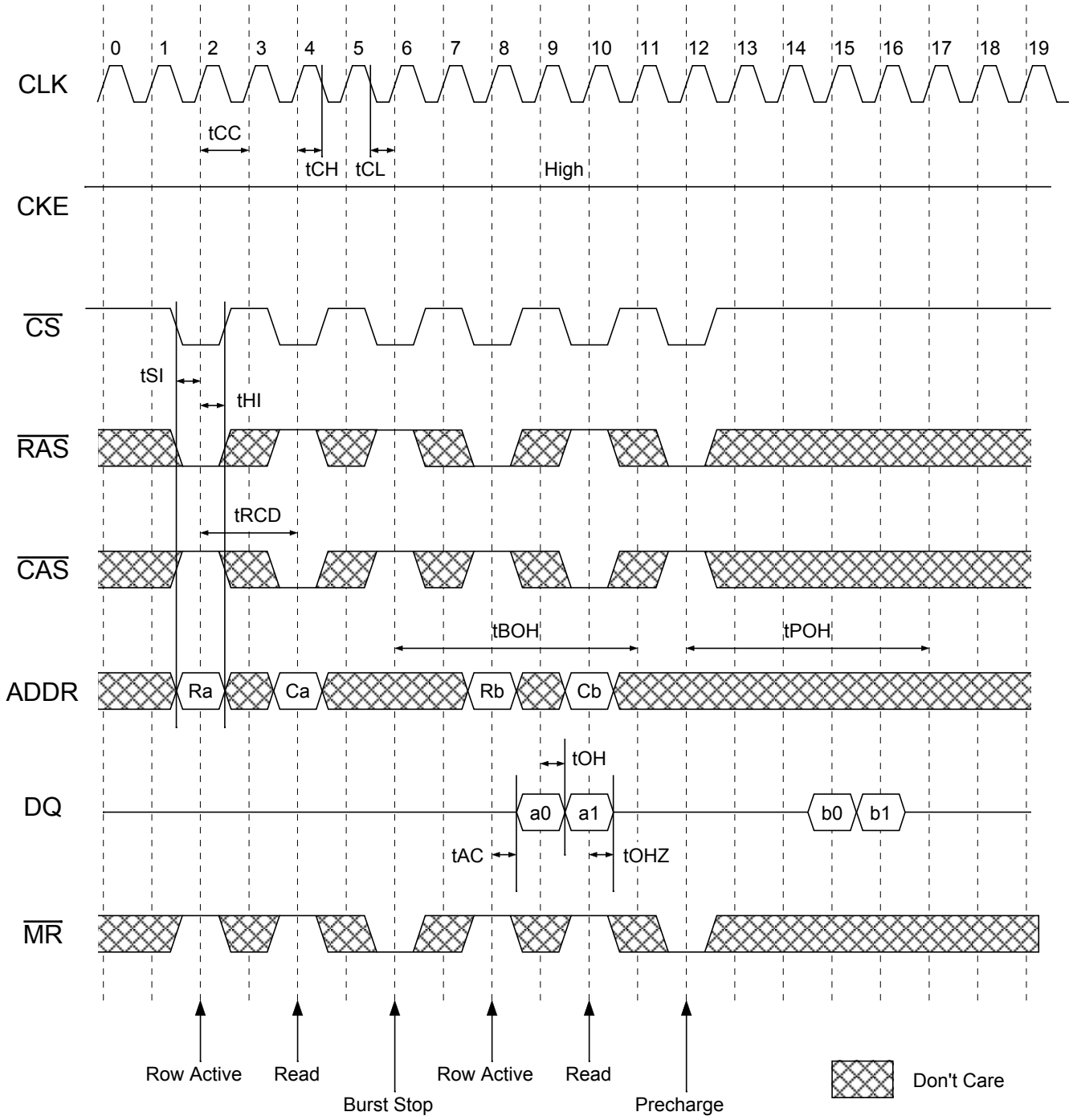
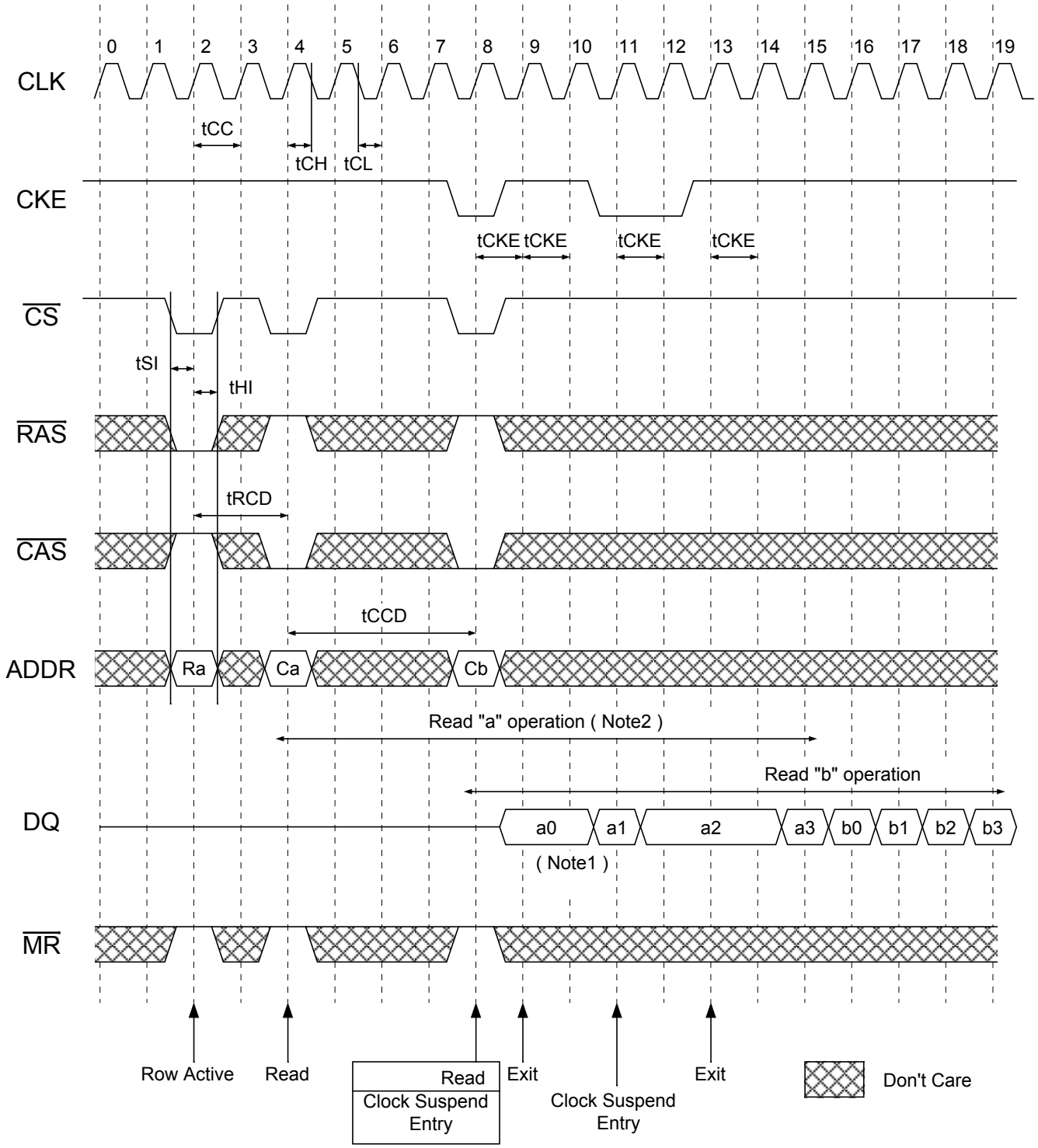
Read Cycle III : Consecutive Column Read @ CAS Latency = 5, Burst Length = 4



"Burst Stop" command & "Precharge" command @ CAS Latency = 5

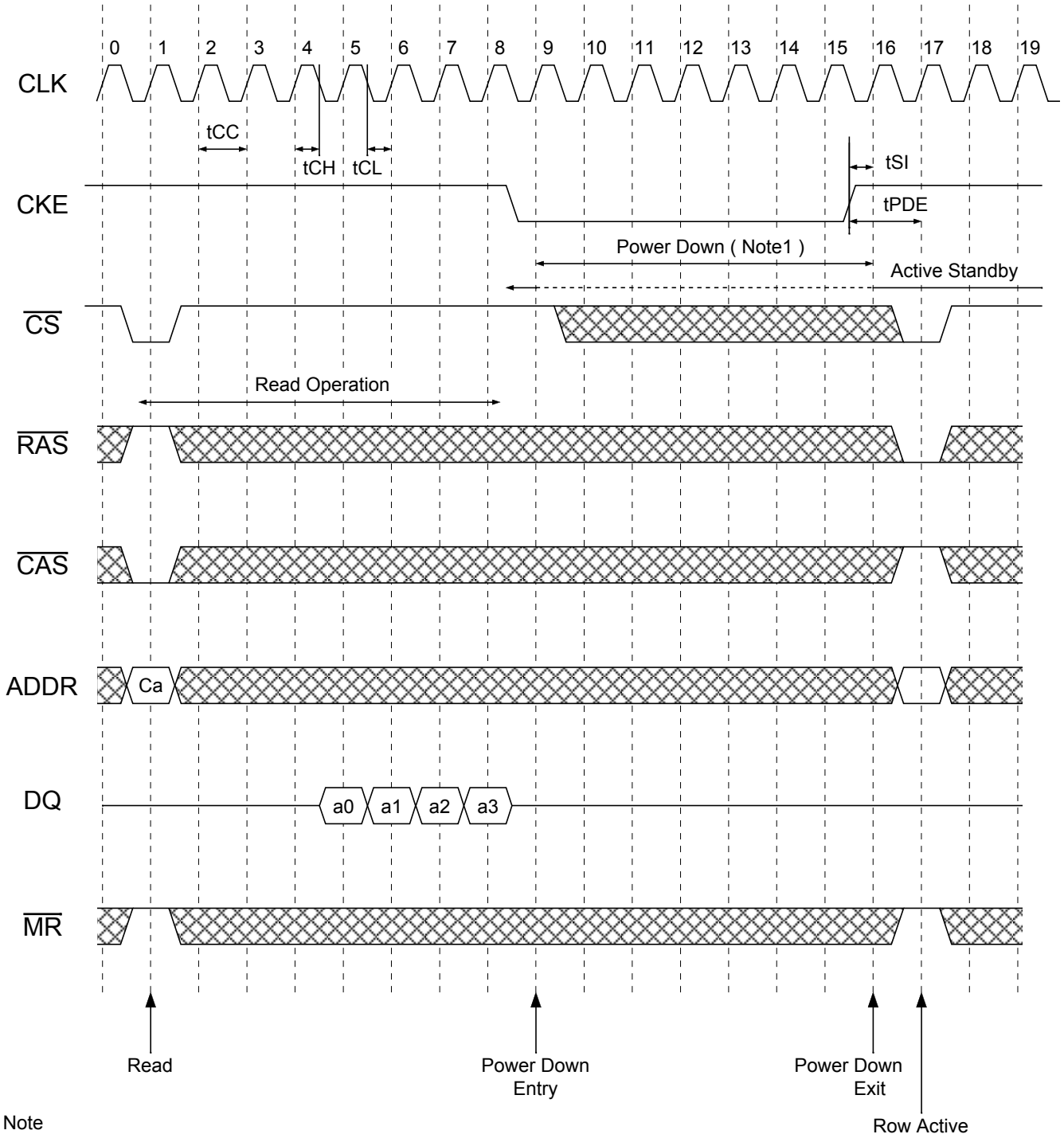


Clock Suspend @ CAS Latency = 5, Burst Length = 4



Note
1. At cycle number 9, 12, 13, rising edge of internal clock is omitted because of low level CKE at cycle 8, 11,12.
2. Clock suspend is defined with the low level CKE sampled in the period of Read operation.

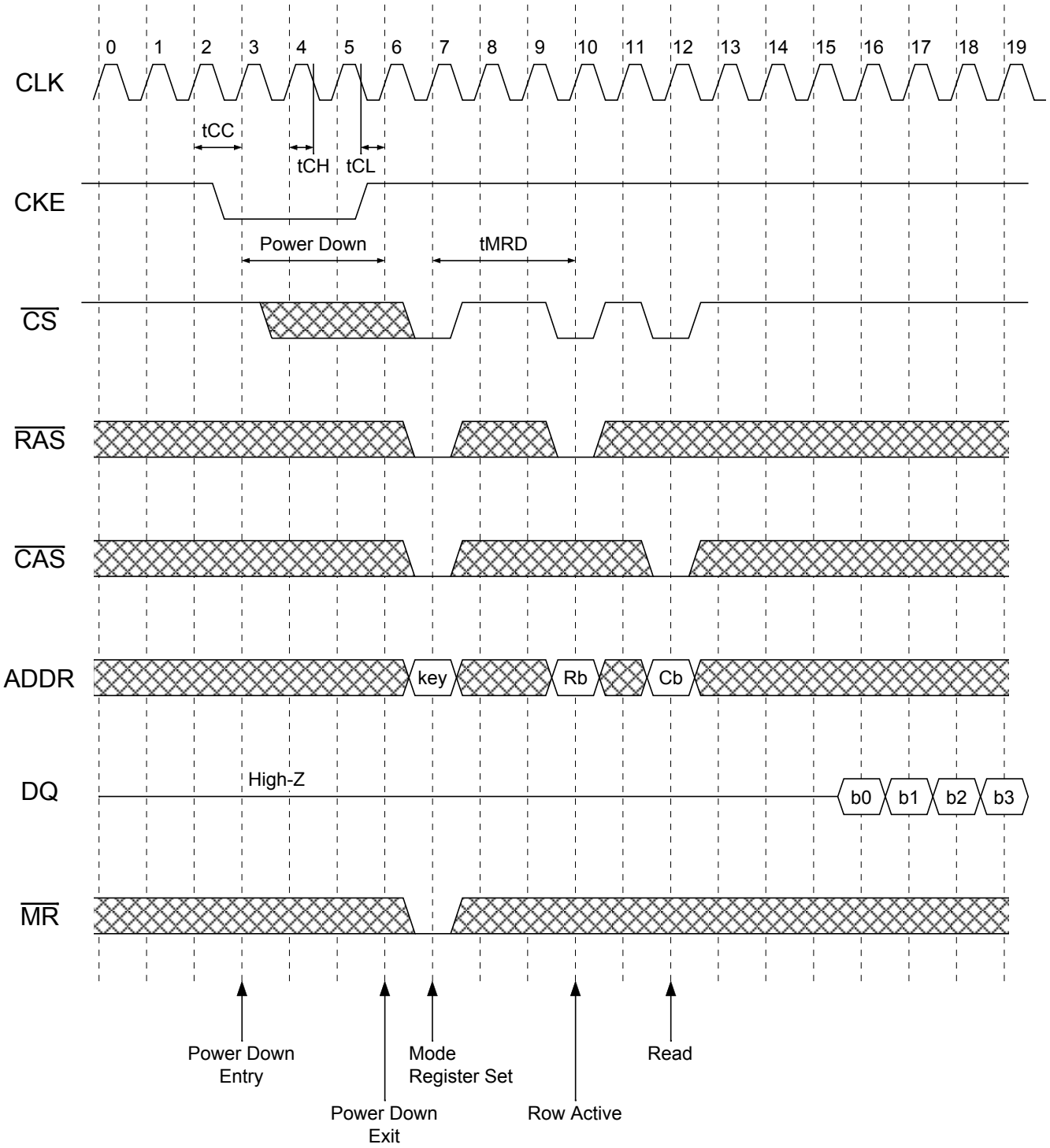
Power Down @ CAS Latency = 4, Burst Length = 4



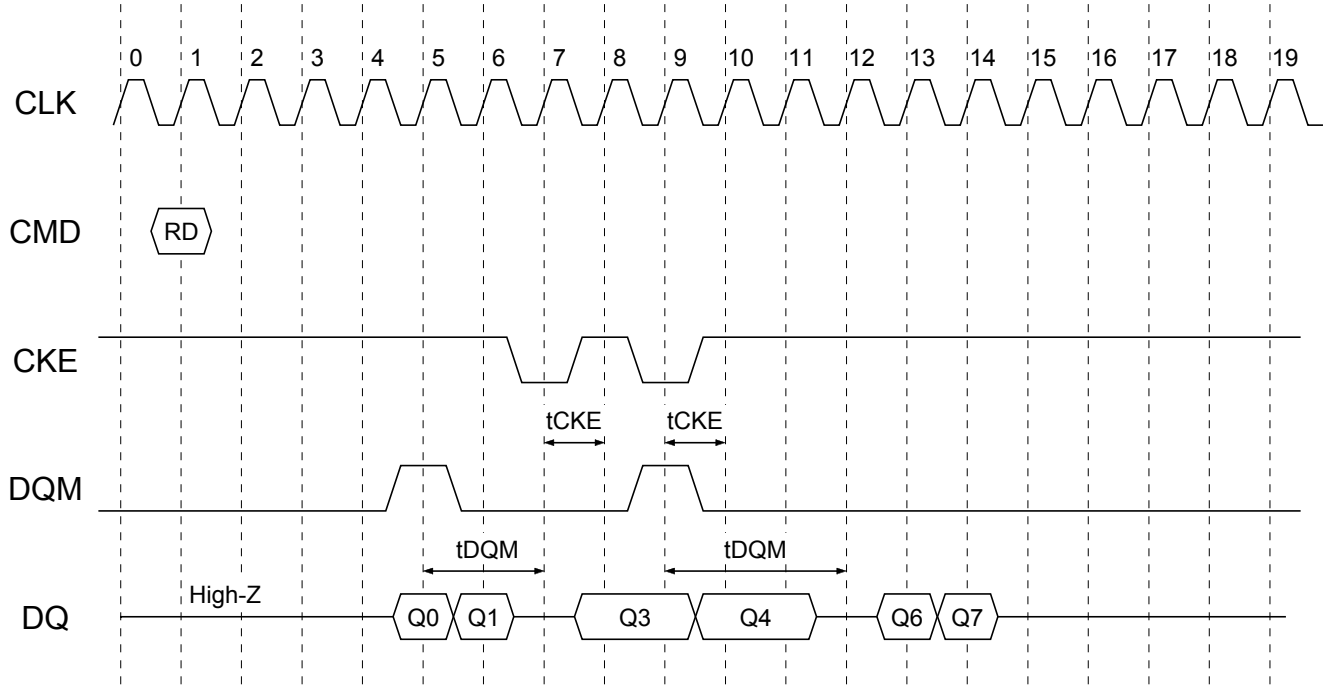
Note

1. Minimum current consumption is expected in Power Down state.
   Low level CKE sampled only in Active Standby state is defined as Power Down "Entry" command and it cuts current consumption into minimum level.
   After Power Down "Exit" the contents of Mode Register and row address is preserved.
   During Power Down state no command can be sampled.

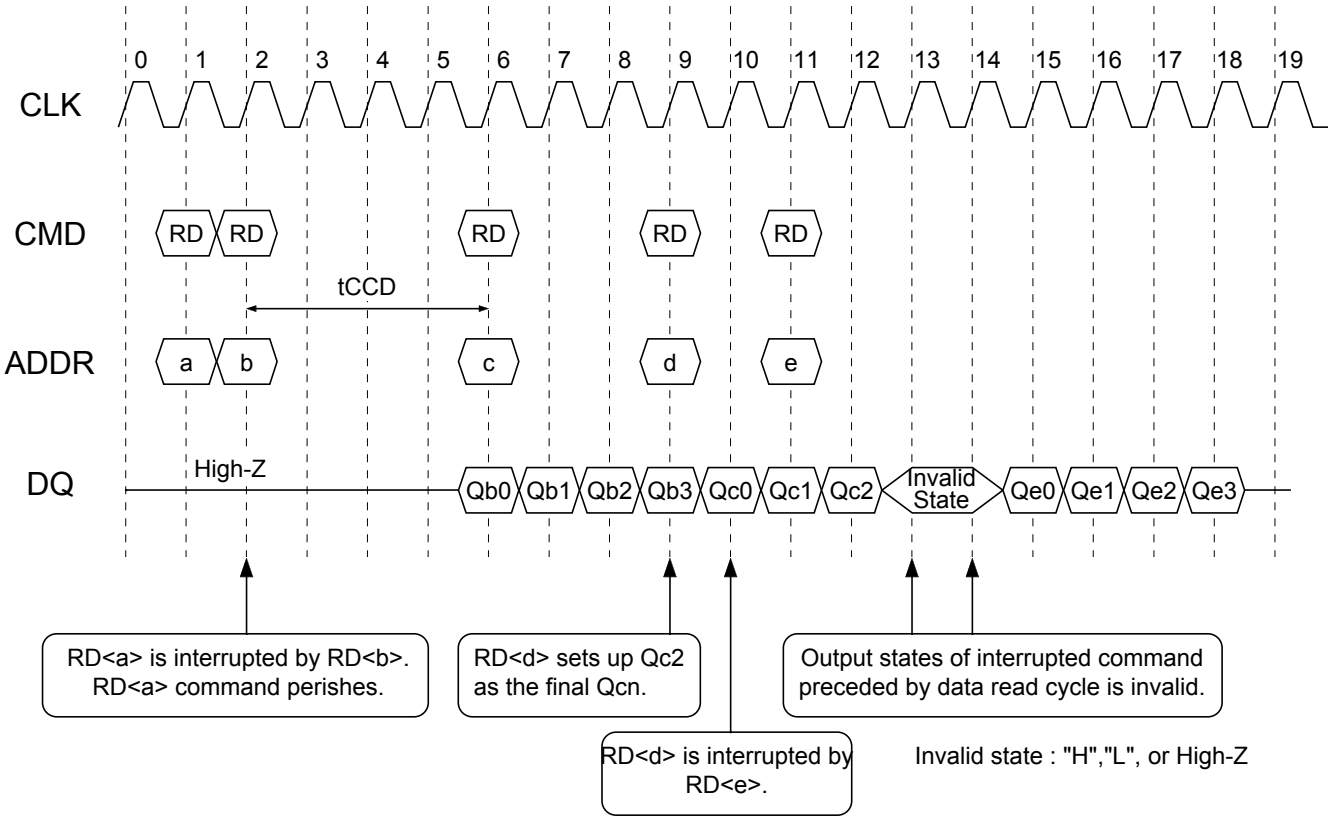
Mode Register Set @ CAS Latency = 4, Burst Length = 4



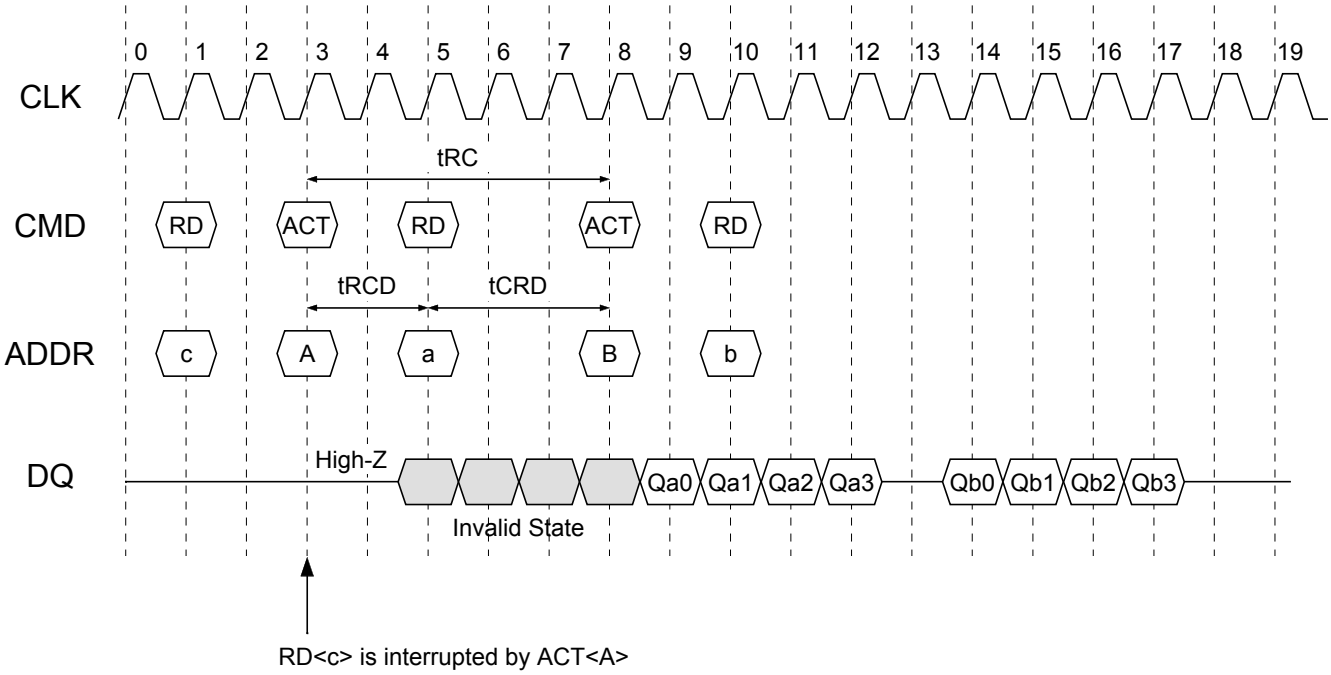
DQM Operation @ CAS Latency = 4, Burst Length = 8



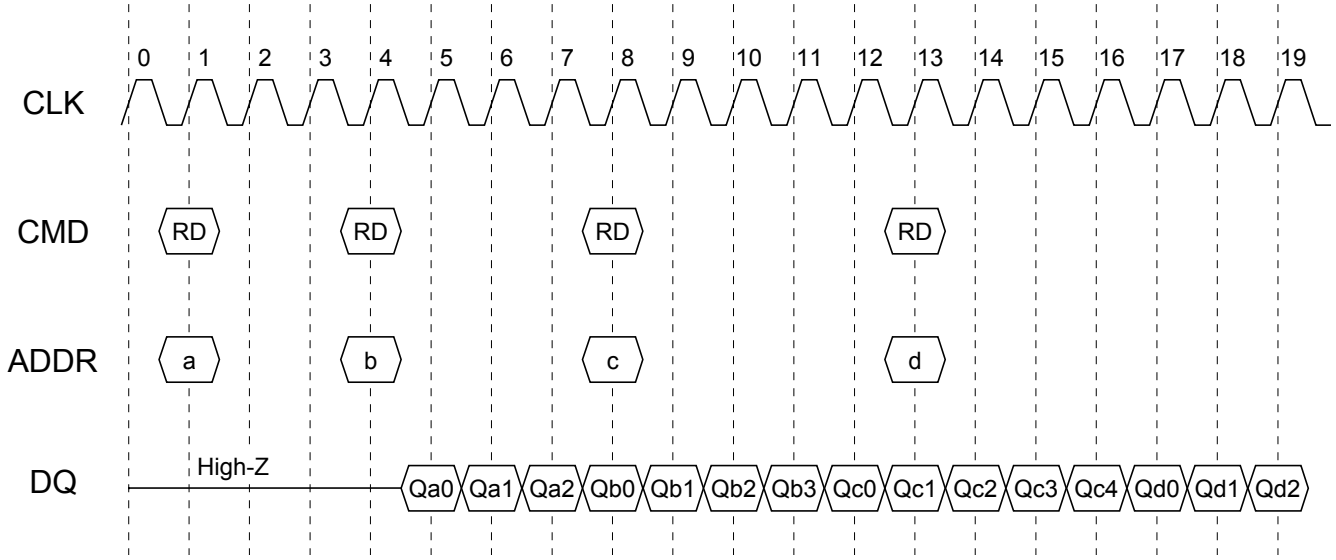
Burst Read / Interrupt I @ CAS Latency = 4, Burst Length = 4



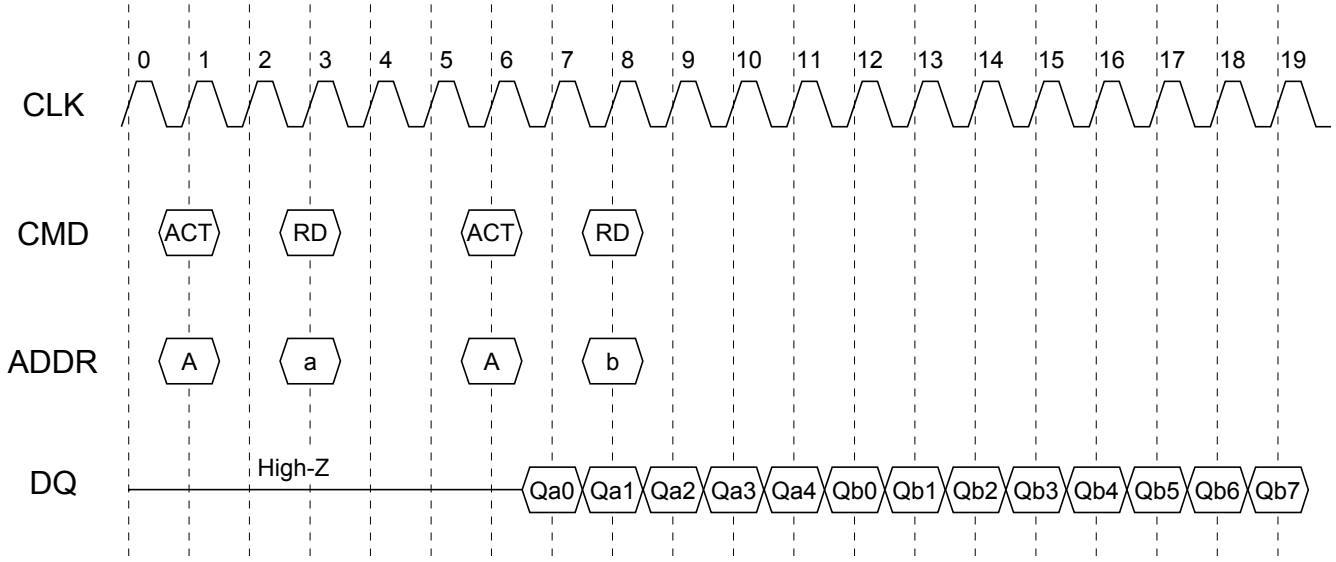
Burst Read / Interrupt II @ CAS Latency = 4, Burst Length = 4



Preemptive Burst Read I @ CAS Latency = 4, Burst Length = 8



Preemptive Burst Read II @ CAS Latency = 4, Burst Length = 8



RECOMMENDED OPERATING CONDITIONS AND DC CHARACTERISTICS FOR PROGRAMMING (STO is High Level)

Parameter	Symbol	Min	Typ	Max	Unit	Condition	Notes
V_{PP} Supply Voltage	V_{PP1}	9.5	9.75	10	V	Program Mode	1
	V_{PP2}	-0.3	V_{CC}	V_{CC} + 0.5	V	Read Mode	2
V_{CC} Supply Voltage	V_{CC1}	3.9	4.0	4.1	V	Program Mode	1
	V_{CC2}	2.9	3.0	3.1	V	Read Mode	2
	V_{CC3}	2.9	-	3.4	V	Optional Read Mode	2
V_{PP} Current	I_{PP1}	-	-	50	mA	V_{PP} = 10V, V_{CC} = 4.1V	
	I_{PP2}	-	-	100	μA	V_{PP} = V_{CC} = 4.1V	
V_{CC} Current	I_{CCP1}	-	-	150	mA	V_{PP} = 10V, V_{CC} = 4.1V	
	I_{CCP2}	-	-	150	mA	V_{PP} = V_{CC} = 4.1V	
	I_{CCP3}	-	-	10	mA	V_{PP} = V_{CC} = 4.1V, tC = 1μS, /CE = H	
Input Leak Current	I_{IL}	-10	-	10	μA		
Output Leak Current	I_{OL}	-10	-	10	μA		
Output High Voltage Level	V_{OH}	2.4	-	-	V	I_{OH} = -400μA	
Output Low Voltage Level	V_{OL}	-	-	0.45	V	I_{OL} = 2.1mA	
Input High Voltage	V_{IH}	2.9	-	V_{CC} + 0.5	V	V_{CC} = 4.1V	
Input Low Voltage	V_{IL}	-0.3	-	0.45	V	V_{CC} = 2.9V	
Voltage Level on DC pin		-0.3	-	V_{CC} + 0.5	V		
/OE Input Distinctive High Voltage	V_H	7.75	8	8.25	V		
Operating Temperature	T_a	20	25	30	degree C		

(Voltage levels are referred to V_{SS})

Notes
1. Program represents the modes below.
   Program, Program Verify, Program Inhibit
2. Read represents the modes below.
   Read, Output Disable, Standby

FUNCTION TABLE FOR PROGRAMMING

	Function	Vcc	Vpp	/CE	/OE	/WORD	DQ0-DQ15	CAP0-CAP7	Add.	/RAS /CAS	AMPX	STO	Notes
Full Static	Program	4.0V	9.75V	L	H	L	DIN	A0 - A7	A8 - A20	X	L	H	
	Program Inhibit	4.0V	9.75V	H	H	L	HZ	A0 - A7	A8 - A20	X	L	H	
	Program Verify	4.0V	9.75V	L	L	L	DOUT	A0 - A7	A8 - A20	X	L	H	
	Read	3.0V	3.0V	L	L	L	DOUT	A0 - A7	A8 - A20	X	L	H	
	Output Disable	3.0V	3.0V	L	H	L	HZ	A0 - A7	A8 - A20	X	L	H	
	Standby	3.0V	3.0V	H	X	L	HZ	A0 - A7	A8 - A20	X	L	H	
	Contact Check	4.0V	4.0V	L	8V	L	AAAA	AA	16AA	X	X	H	1
	Contact Check	4.0V	4.0V	L	8V	L	5555	55	0955	X	X	H	1
Address Multiplexed	Program	4.0V	9.75V	L	H	L	DIN	X	X	Fixed	H	H	2
	Program Inhibit	4.0V	9.75V	H	H	L	HZ	X	RA / CA	↘	H	H	2
	Program Verify	4.0V	9.75V	L	L	L	DOUT	X	X	Fixed	H	H	2
	Read	3.0V	3.0V	L	L	L	DOUT	X	RA / CA	↘	H	H	3
	Output Disable	3.0V	3.0V	L	H	L	HZ	X	RA / CA	↘	H	H	3
	Standby	3.0V	3.0V	H	X	L	HZ	X	RA / CA	↘	H	H	3
	Contact Check	4.0V	4.0V	L	8V	L	AAAA	X	16AA	X	X	H	4
	Contact Check	4.0V	4.0V	L	8V	L	5555	X	0955	X	X	H	4

(H = Logical High, L = Logical Low, X = Don't Care in the range of logical level)

Note

1. Dual procedures to check complementary output codes on the indicated complementary address inputs assure every address, DQ, and /OE pin connection.
   When address input code is incorrect, output code is "FFFF".

Exclusive Notes for address multiplexed programming

2. Row address is sampled at falling edge of /RAS. Column address is sampled at falling edge of /CAS. Each internal address can be changed at any time with arbitrary order of /RAS and /CAS.
   The function of /RAS and /CAS is only to sample and latch addresses.
   When Vpp is 9.75V, internal address must be changed only in "Program Inhibit" mode and /RAS and /CAS must be fixed during "Program"(real programming operation) and "Program Verify" mode.

3. DQ0-DQ15 in "Read" mode change output instantly depending on latched address.

4. In "Contact Check" mode of "Address Multiplexed" form all inputs must be kept during reading output, because all inputs are monitored as static levels and falling edge of /RAS or /CAS is not required.

PROGRAMMING OPERATION

STO

Synchronous read is far different from anyone of conventional nonvolatile memories. STO input level switches operation mode either synchronous read or conventional EPROM/OTP type programming. The word "Programming" contains actual programming(inject electrons into floating gates of memory cells), program verify(verify data on actual programming bias), and read on programmer. High level STO assures full compatible programming operation with conventional EPROM/OTP. Low level STO assures high speed synchronous read.
"Full static programming" is recommended for loose devices.

PROGRAM

MR27V3266D is programmed with 10 microsecond pulse width on 4.0V V_{CC} and 9.75V V_{PP}. OKI recommends consecutive programming, because of the similarity of device sorting process. Almost all words can be programmed sufficiently with one pulse. Programmers are recommended to be equipped with large current capacity of V_{PP} and V_{CC} supplying source and responsive capacitance(around 0.1μF) on each socket to stabilize V_{PP} and V_{CC} voltage level, since switching speed of transistors produced with advanced wafer process technology is very fast and high voltage immunity of those is decreasing. Excessive overshooting of V_{PP} voltage may destroy device permanently. Excessive overshooting of V_{CC} voltage may cause misprogramming or disturbance. Excessive undershooting of V_{PP} or V_{CC} level may cause insufficient electron injection into floating gate. Additional programming increases programming time.

PROGRAM INHIBIT

When V_{PP} is 9.75V, address must be changed only in "Program Inhibit" mode.

PROGRAM VERIFY

This operation mode is utilized to check that each word is programmed sufficiently. It is recommended to take time more than some seconds between actual programming and "Program Verify" ("Read") for each word, because just after the actual programming(injection of electron into floating gate) of each word, pretended excessive electrons are attached around floating gate to show false sufficiency of programming. Programing flow is selected to separate "Program" and "Program Verify" to take enough time.

CONTACT CHECK

When programmed OTP lot contains failed devices by the rate of more than 0.1%, some of or almost all failed devices are caused by misconnection with the sockets on the programmer. The possibility of misconnection is increased with surface mount devices such as SOP or TSOP.
OKI will supply socket adapters exclusively applicable to MR27V3266D, but connections of all pins can not be assured with these socket adapters.
Following contact check sequence before actual programming is recommended.

1. Supply V_{CC} with 4.0V power source.
2. Bias logical low level on /CE.
3. Supply 8V on /OE to enable contact check mode.
4. Apply two address codes and check each output respectively.
   If irregular address code is applied, then output is FFFF.
   <Connection of Address, D_{OUT}, V_{CC}, /OE,and STO pins are checked>
5. /CE must be checked with a method suitable for the programmer.
6. V_{PP} can be checked with current flow(more than 100 μA) in Program Inhibit mode.
7. AMPX and /WORD pins is open in the socket adapter, since these pins are pulled down to V_{SS} when STO is high.

AC CHARACTERISTICS FOR PROGRAMMING (STO is High Level)

Parameter	Symbol	Min	Typ	Max	Unit	Condition	Notes
VPP Setup Time	tVS	2	-	-	µs	VPP = 9.75V, VCC = 4.0V	
Address Setup Time	tAS	100	-	-	ns	VPP = 9.75V, VCC = 4.0V	
Data Setup Time	tDS	100	-	-	ns	VPP = 9.75V, VCC = 4.0V	
Address Hold Time	tAH	2	-	-	µs	VPP = 9.75V, VCC = 4.0V	
Data Hold Time	tDH	100	-	-	ns	VPP = 9.75V, VCC = 4.0V	
Program Pulse Width	tPW	9	10	11	µs	VPP = 9.75V, VCC = 4.0V	
/OE Setup Time	tOES	2	-	-	µs	VPP = 9.75V, VCC = 4.0V	
Data Valid from /OE	tOE	-	-	100	ns	VPP = 9.75V, VCC = 4.0V	
/OE High to Output Float Delay	tDFP	0	-	100	ns	VPP = 9.75V, VCC = 4.0V	
Row Address Setup Time	tASR	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
Row Address Hold Time	tRAH	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
Column Address Setup Time	tASC	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
Column Address Hold Time	tCAH	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
/RAS Pulse Width	tRAS	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
/RAS Precharge Time	tRP	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	2
/CAS Pulse Width	tCAS	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	1
/CAS Precharge Time	tCP	50	-	-	ns	VPP = 9.75V, VCC = 4.0V	2

Note

1. Row address is sampled at any falling edge of /RAS and column address is sampled at any falling edge of /CAS.
   /RAS or /CAS signal starts no other operation associated with DRAM.
   The order of falling edges of /RAS or /CAS is not regulated.
   Successive row address sampling or column address sampling is acceptable.
2. "Precharge" is the name associated with DRAM. No precharge operation is required.

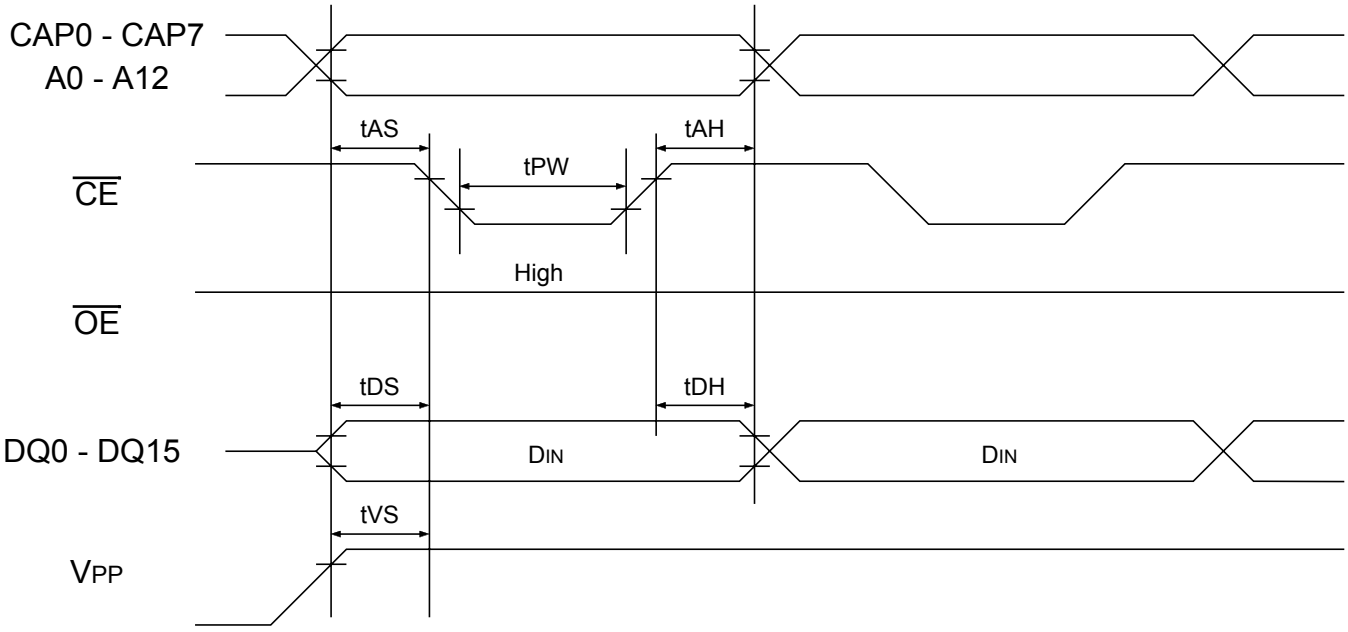
AC CHARACTERISTICS FOR VERIFY AND READ (STO is High Level)

Parameter	Symbol	Min	Typ	Max	Unit	Condition	Notes
Address Access Time	tACC	-	-	80	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/RAS Access Time	tACC	-	-	80	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/CAS Access Time	tACC	-	-	80	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/CE Access Time	tCE	-	-	80	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/OE Access Time	tOE	-	-	30	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/CE High to Output Float Delay	tCHZ	-	-	25	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
/OE High to Output Float Delay	tOHZ	-	-	20	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
Address Hold from /OE high	tAHO	0	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	
Row Address Setup Time	tASR	0	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
Row Address Hold Time	tRAH	15	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
Column Address Setup Time	tASC	0	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
Column Address Hold Time	tCAH	15	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
/RAS Pulse Width	tRAS	7	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
/RAS Precharge Time	tRP	7	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	2
/CAS Pulse Width	tCAS	7	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	1
/CAS Precharge Time	tCP	7	-	-	ns	V_{PP} = V_{CC} = 2.9 - 4.1V	2

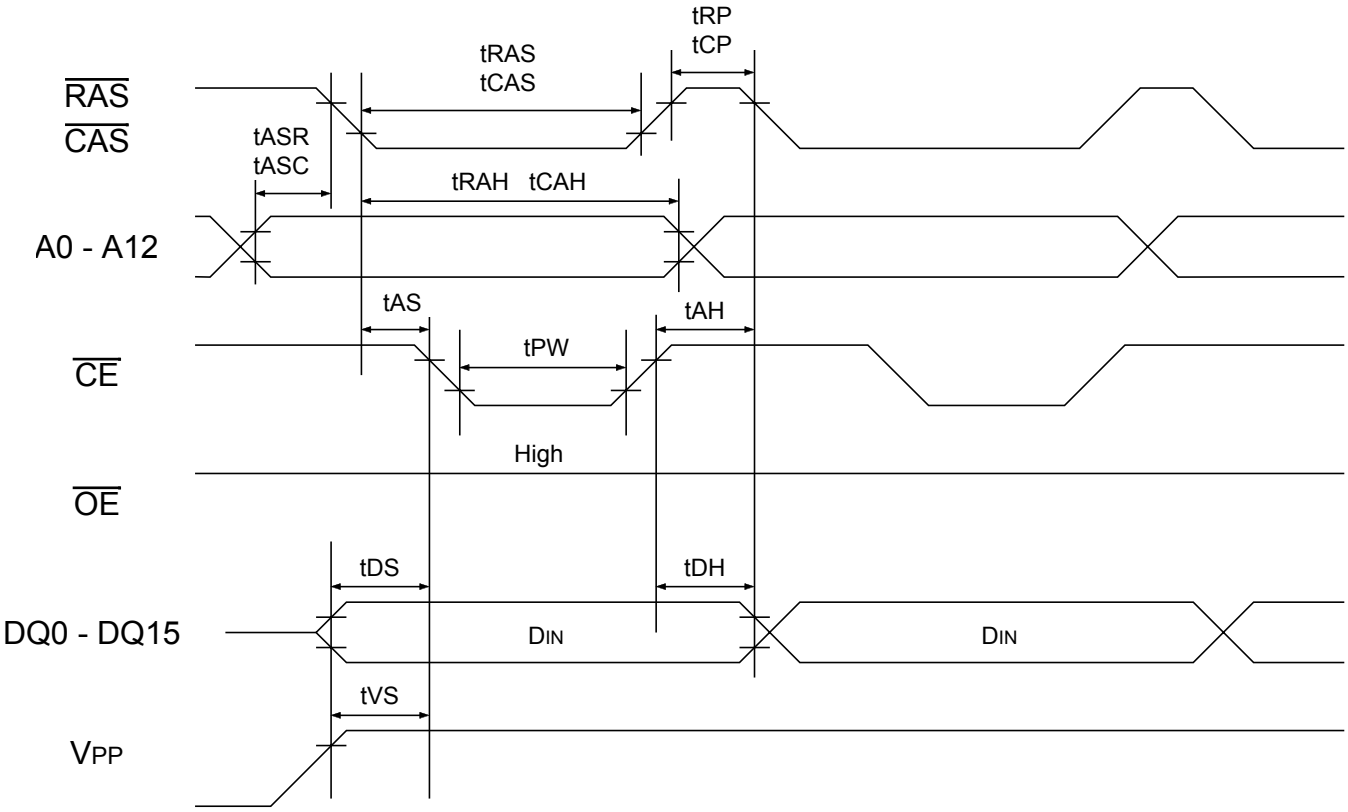
Note

1. Row address is sampled at any falling edge of /RAS and column address is sampled at any falling edge of /CAS.
   /RAS or /CAS signal starts no other operation associated with DRAM.
   The order of falling edges is not regulated.
   Successive row address sampling or column address sampling is acceptable.
2. "Precharge" is the name associated with DRAM. No precharge operation is required.

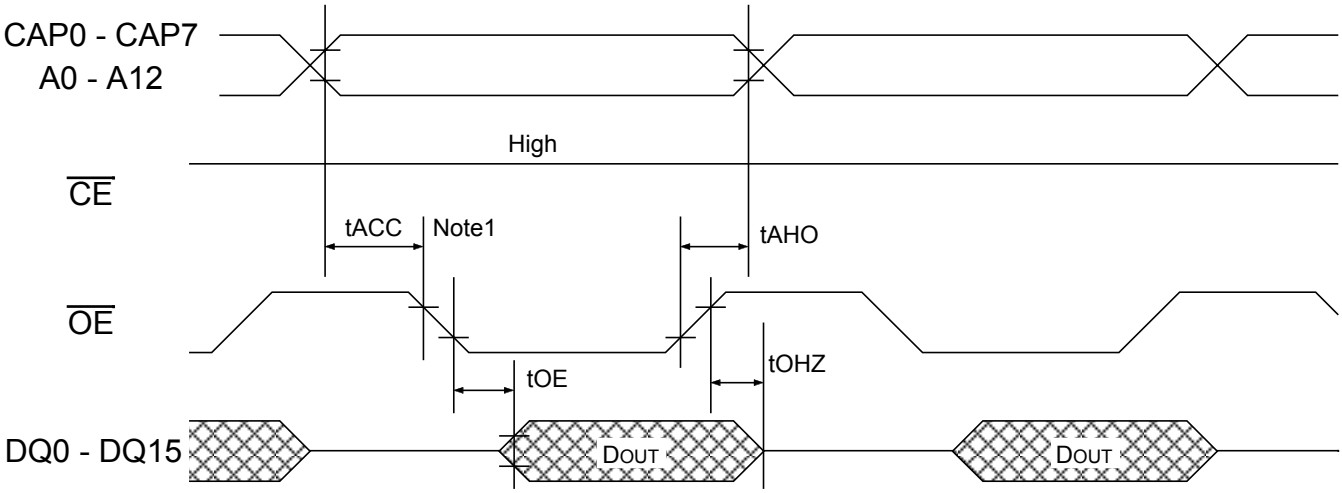
CONSECUTIVE PROGRAMMING WAVEFORMS (AMPX = L)



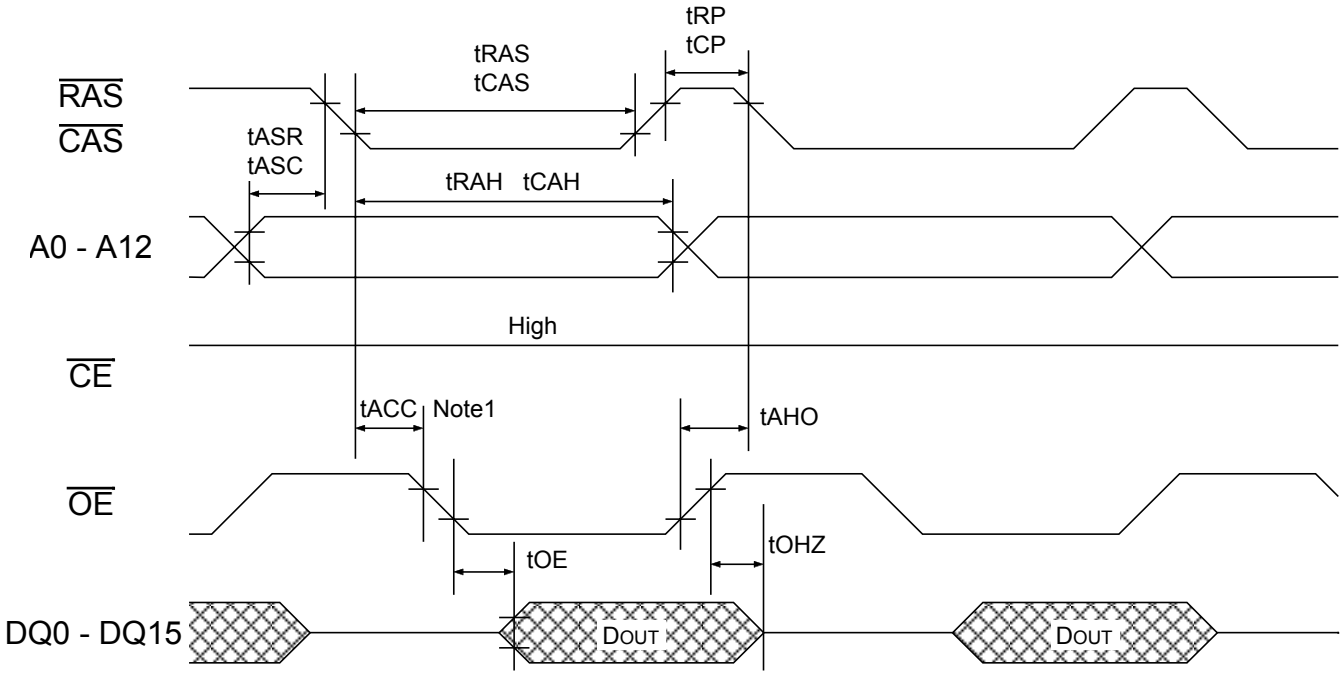
CONSECUTIVE PROGRAMMING WAVEFORMS (AMPX = H)



CONSECUTIVE PROGRAM VERIFY CYCLE (V_{PP} = 9.75V, AMPX = L)



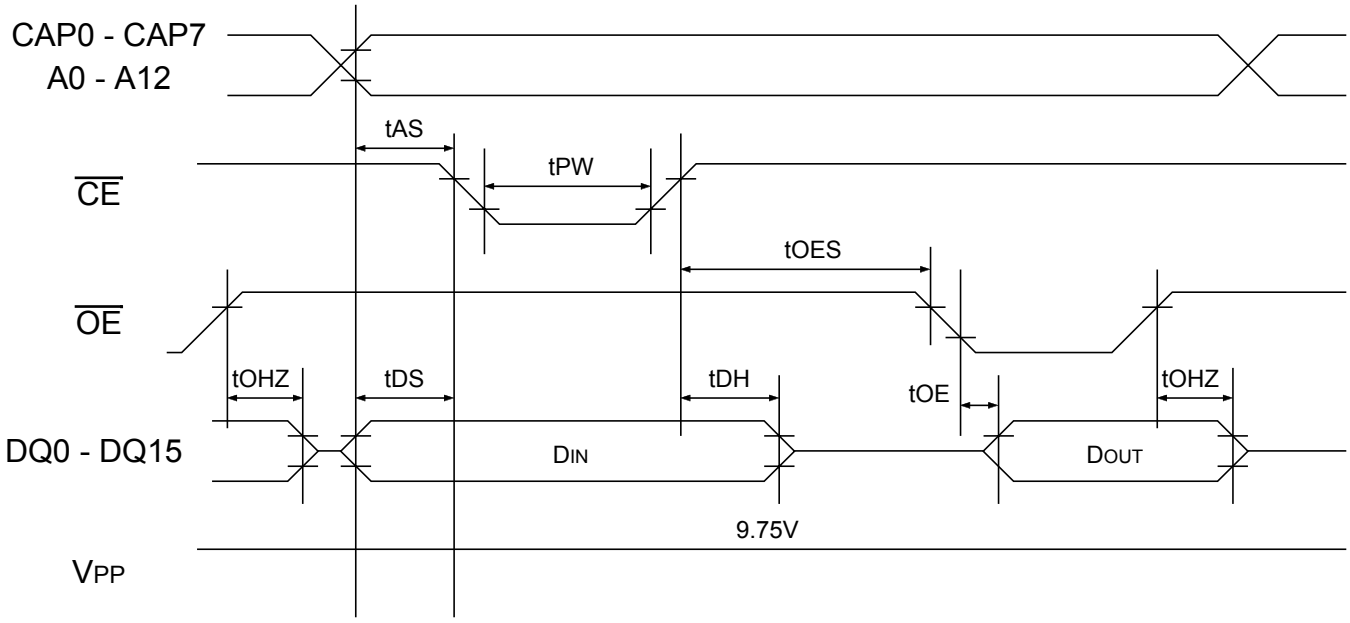
CONSECUTIVE PROGRAM VERIFY CYCLE (V_{PP} = 9.75V, AMPX = H)



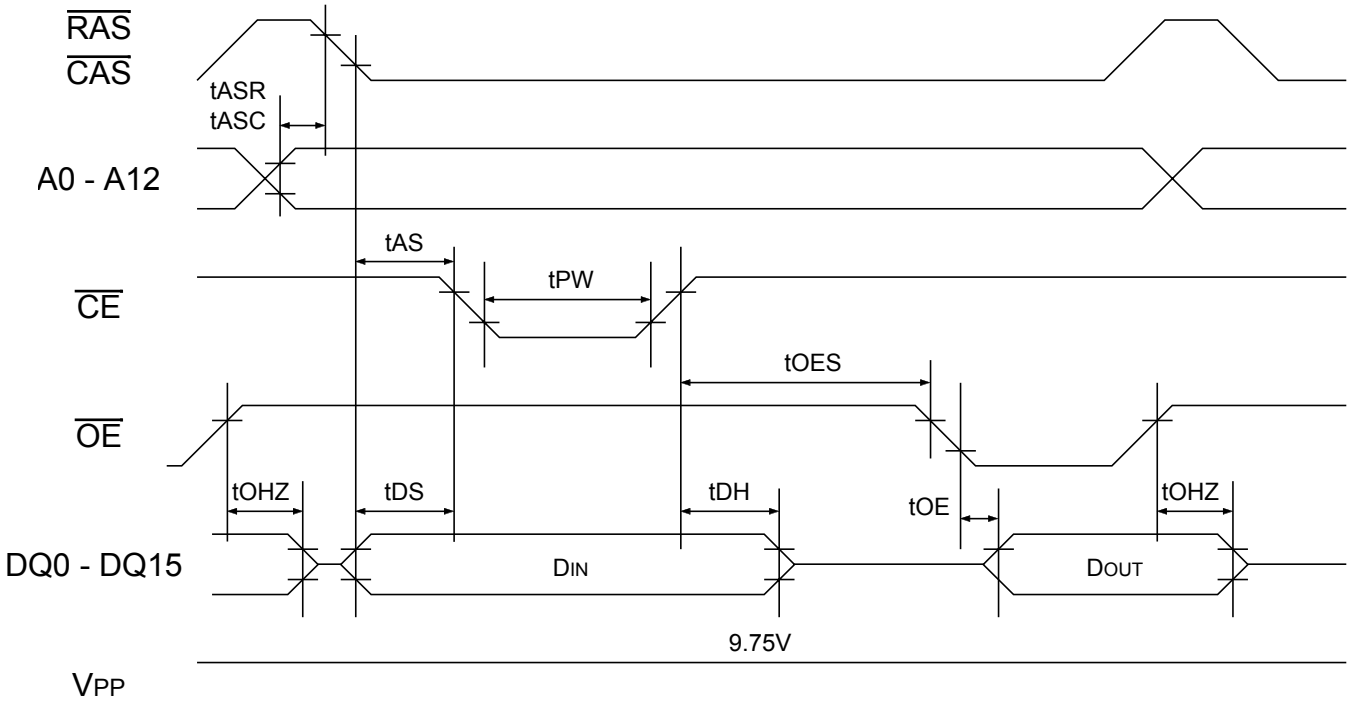
Note

1. Falling edge of /OE must be preceded with data stabilizing time of more than tACC max., because output of invalid state can cause unstable system operation.
   Output buffer of MR27V3266D is designed to drive 100pF load in 5ns.

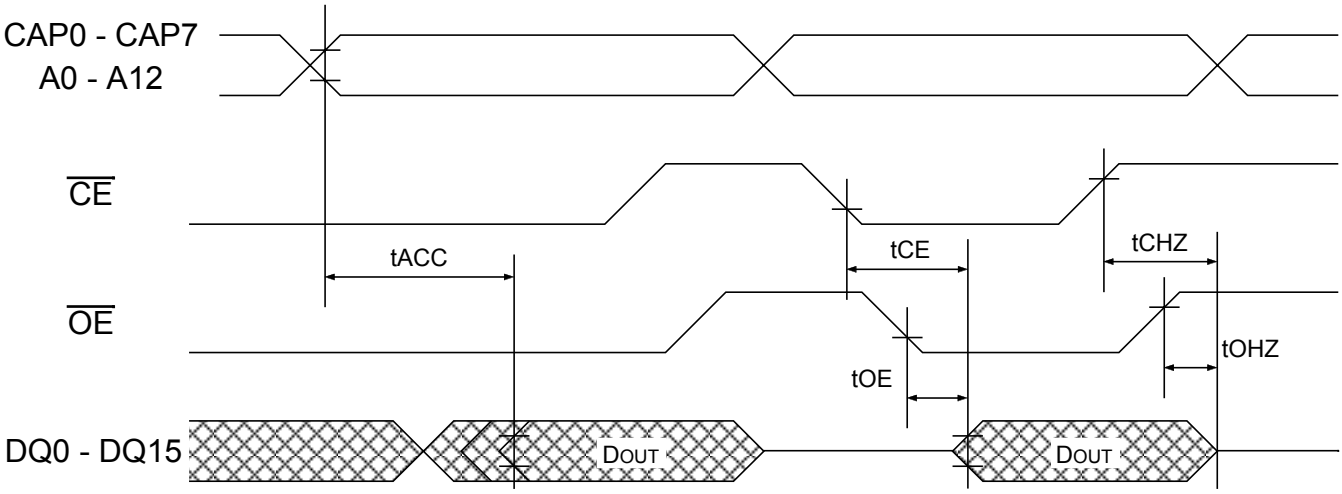
PROGRAM AND PROGRAM VERIFY CYCLE WAVEFORMS (AMPX = L)



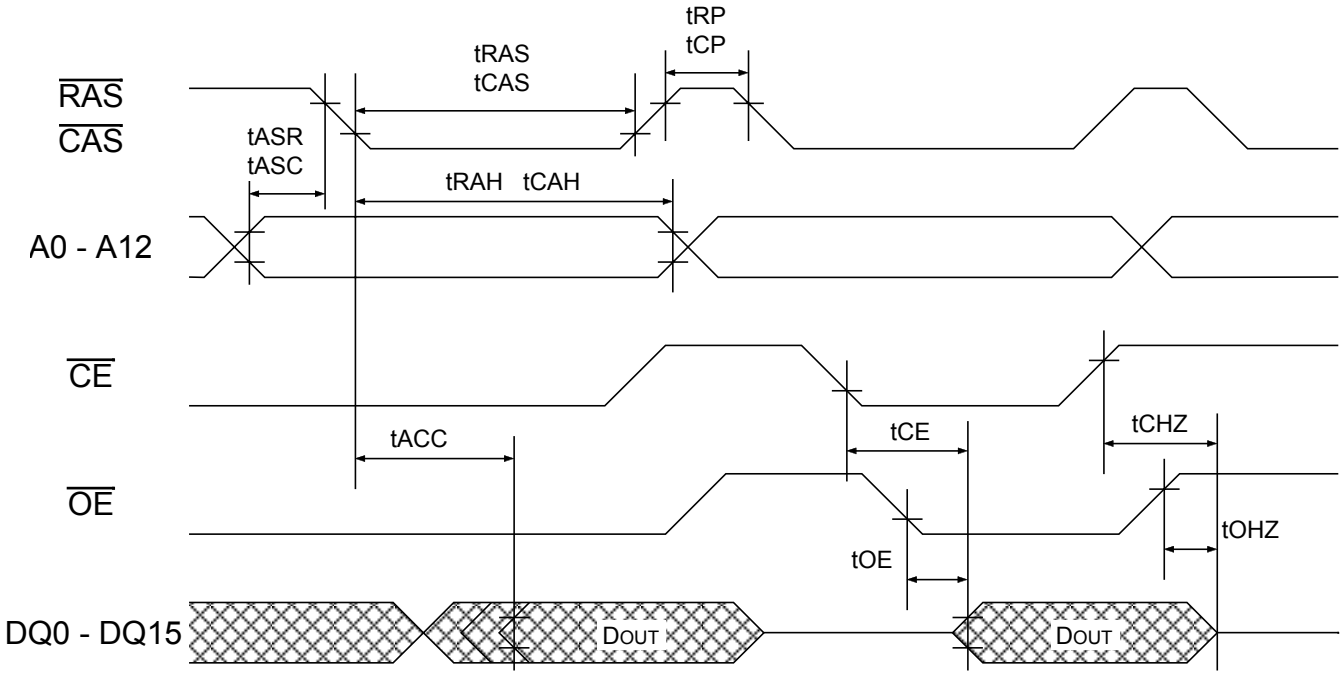
PROGRAM AND PROGRAM VERIFY CYCLE WAVEFORMS (AMPX = H)



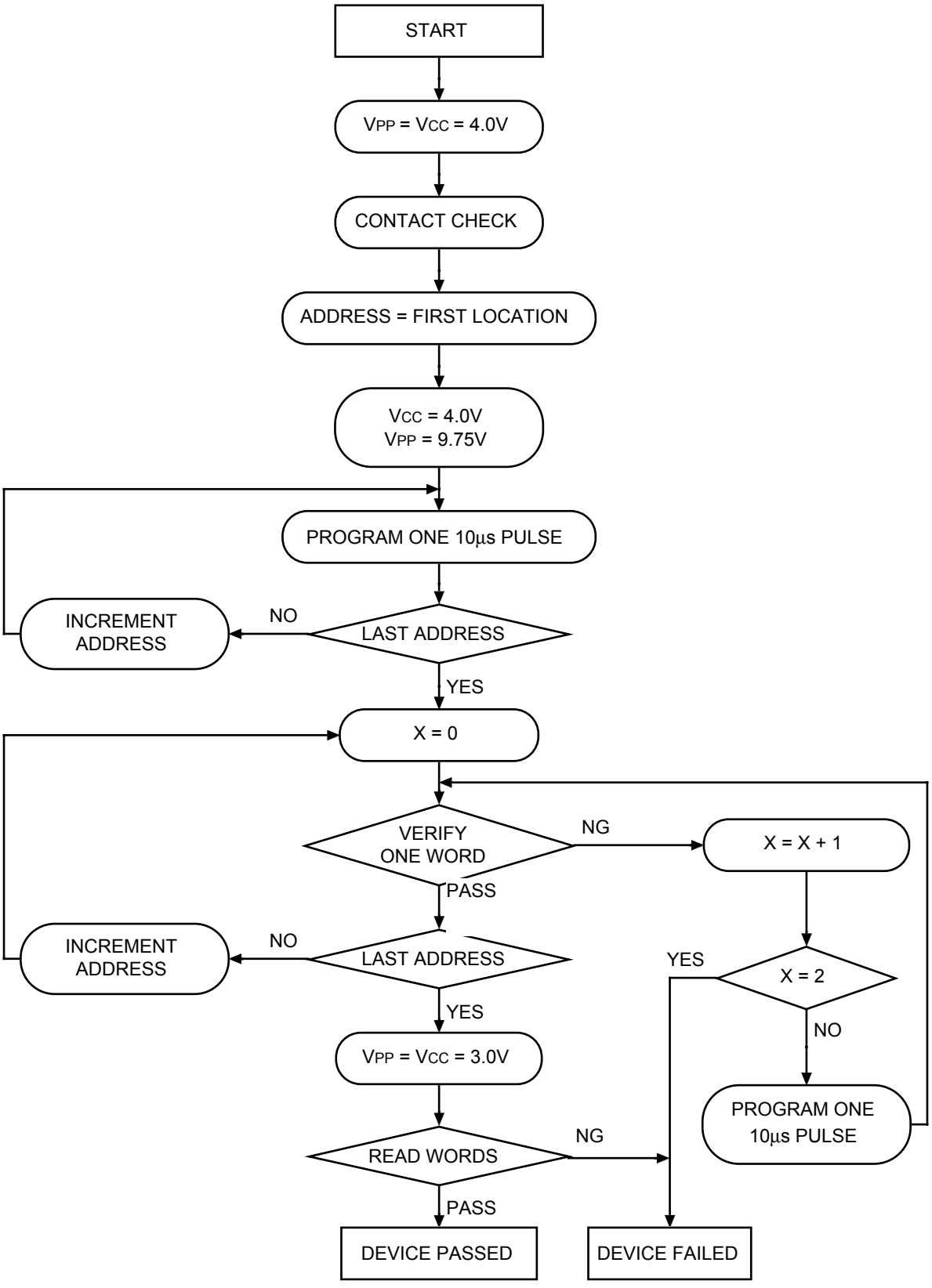
READ CYCLE (AMPX = L)



READ CYCLE (AMPX = H)



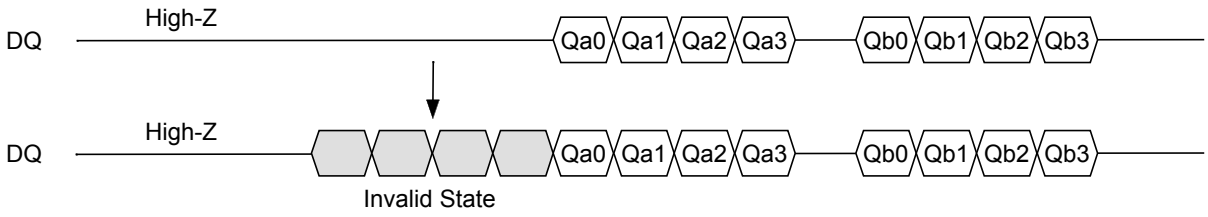
PROGRAMMING FLOW CHART



REVISION HISTORY

Revision 2.0 ⟶ Revision 2.1

1. Page 13
   Active Standby Current (ICC1) was revised from 50mA to 100mA.
2. Page 14
   Regarding Note 1, it was revised from " .... internal command controller to cease the preceding command operation to keep output buffer high-Z state instead of the null output " to " .... internal command controller to cease the preceding command operation " (underlined portion was eliminated.).
3. Page 24
   Regarding the timing diagram of " Burst Read / Interrupt II , DQ timing diagram was revised as bellow :



Revision 2.1 ⟶ Revision 2.2

1. Page 14
   tRCD (" Row Active " to " Read " Delay Time) was revised from 1CLK to 2CLK.
2. Page 17
   Contents of this page (timing diagram of " Random Access with Gapless Burst ") was eliminated.

NOTICE

The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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People To People Technology

ADDRESSES & SEMICONDUCTOR WEB SITES

OKI Electric Industry Co., Ltd.,
Device Business Group,
10-3, Shibaura, 4-chome,
Minato-ku, Tokyo 108, Japan,
Tel.: +81-(0)3-5445-6327,
Fax.: +81-(0)3-5445-6328,
http://www.oki.co.jp/semi/

OKI Semiconductor Group,
785 North Mary Avenue,
Sunnyvale, CA 94086, U.S.A.,
Tel.: +1-408-720-1900,
Fax.: +1-408-720-1918,
http://www.okisemi.com/

OKI Electric Europe GmbH,
Head Office Europe,
Hellersbergstrasse 2,
D-41460 Neuss, Germany,
Tel: +49-2131-15960,
Fax: +49-2131-103539,
http://www.oki-europe.de/

OKI Electronics (Hong Kong) Ltd.,
Suite 1901-1&19, Tower 3,
China Hong Kong City,
33 Canton Road, Tsimshatsui,
Kowloon, Hong Kong,
Tel.: +852-2-736-2336,
Fax.: +852-2-736-2395

OKI Semiconductor (Asia) Pte. Ltd.,
78 Shenton Way 09-01,
Singapore 0207,
Tel.: +65-221-3722,
Fax.: +65-323-5376

OKI Semiconductor (Asia) Pte. Ltd.,
Taipei Branch,
7th Fl. No.260, Tun Hwa North Road,
Taipei, Taiwan, R.O.C.,
Sumitomo-Flysun Building,
Tel.: +886-2-2719-2561,
Fax.: +886-2-2715-2892
http://www.oki.net.tw/

For further information, please contact: