

NPN SILICON RF POWER TRANSISTOR

DESCRIPTION:

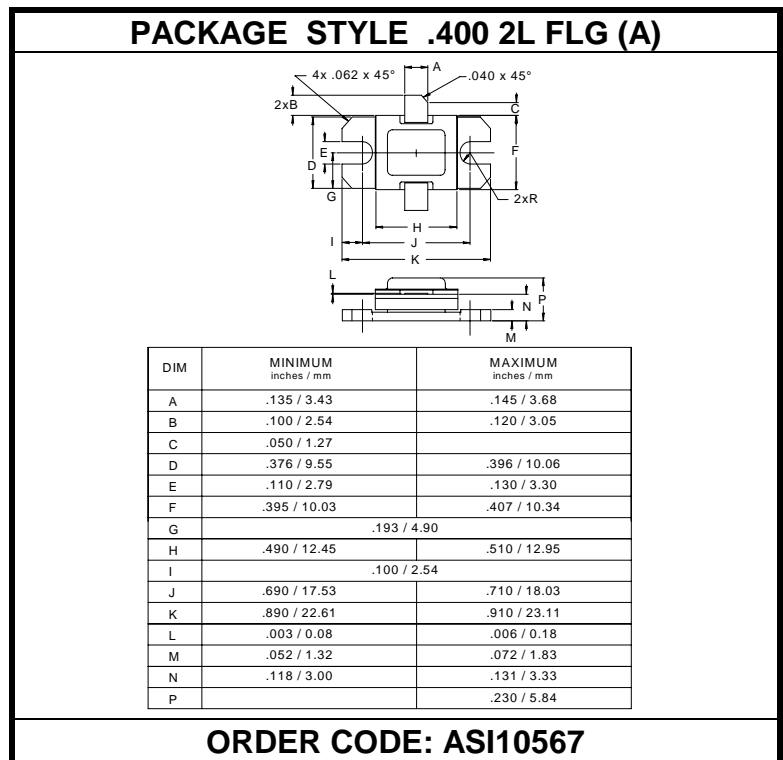
The **ASI AVD400** is a silicon NPN power transistor, designed for high power and low duty cycle DME and IFF applications.

FEATURES:

- Internal Input/Output Matching Networks
- $P_G = 6.5$ dB at 400 W/1150 MHz
- **Omnigold™** Metalization System

MAXIMUM RATINGS

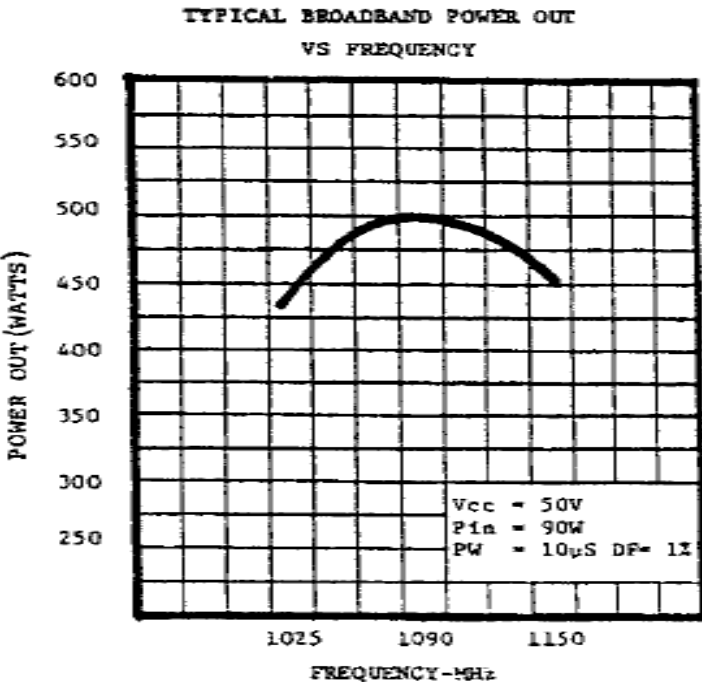
I_C	22 A
V_{CC}	55 V
P_{DISS}	1458 W @ $T_C = 25^\circ C$
T_J	-65 °C to +200 °C
T_{STG}	-65 °C to +200 °C
θ_{JC}	0.12 °C/W


CHARACTERISTICS $T_C = 25^\circ C$

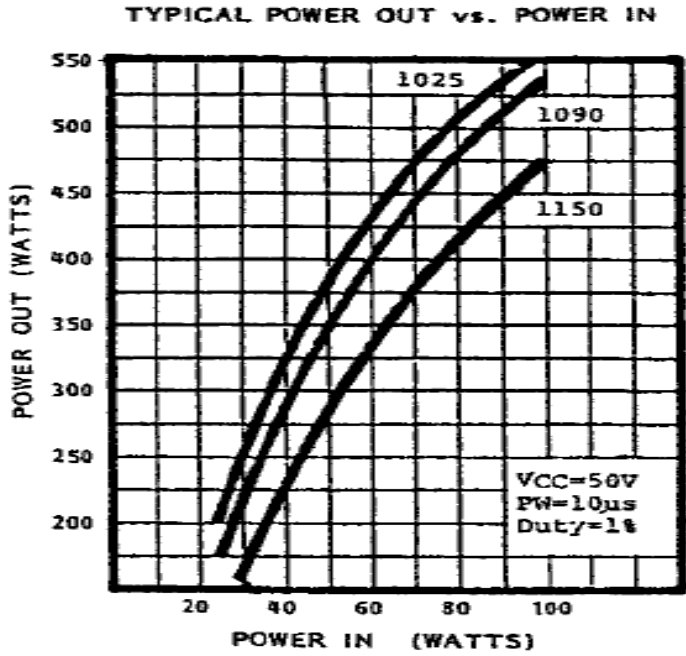
SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
BV_{CBO}	$I_C = 25$ mA	65			V
BV_{CES}	$I_C = 50$ mA	65			V
BV_{EBO}	$I_E = 10$ mA	3.5			V
I_{CES}	$V_{CE} = 50$ V			25	mA
h_{FE}	$V_{CE} = 5.0$ V $I_C = 0.25$ A	10		200	---
P_G	$V_{CC} = 50$ V $P_{OUT} = 400$ W $f = 1025 - 1150$ MHz	6.5			dB
η_C	$P_{IN} = 90$ W	40			%

Pulse Width = 10 μ sec, Duty Cycle = 1 %

POWER OUTPUT vs FREQUENCY



POWER OUTPUT vs POWER INPUT



IMPEDANCE DATA:

FREQ	$Z_{IN}(\Omega)$	$Z_{CL}(\Omega)$
1020 MHz	$2.89 + j4.1$	$1.38 - j3.2$
1090 MHz	$2.32 + j3.4$	$1.33 - j2.8$
1150 MHz	$1.99 + j2.8$	$1.26 - j2.5$

 $P_{IN} = 90 \text{ W}$
 $V_{CE} = 50 \text{ V}$