7531 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7531 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7531 Group has a serial I/O, 8-bit timers, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

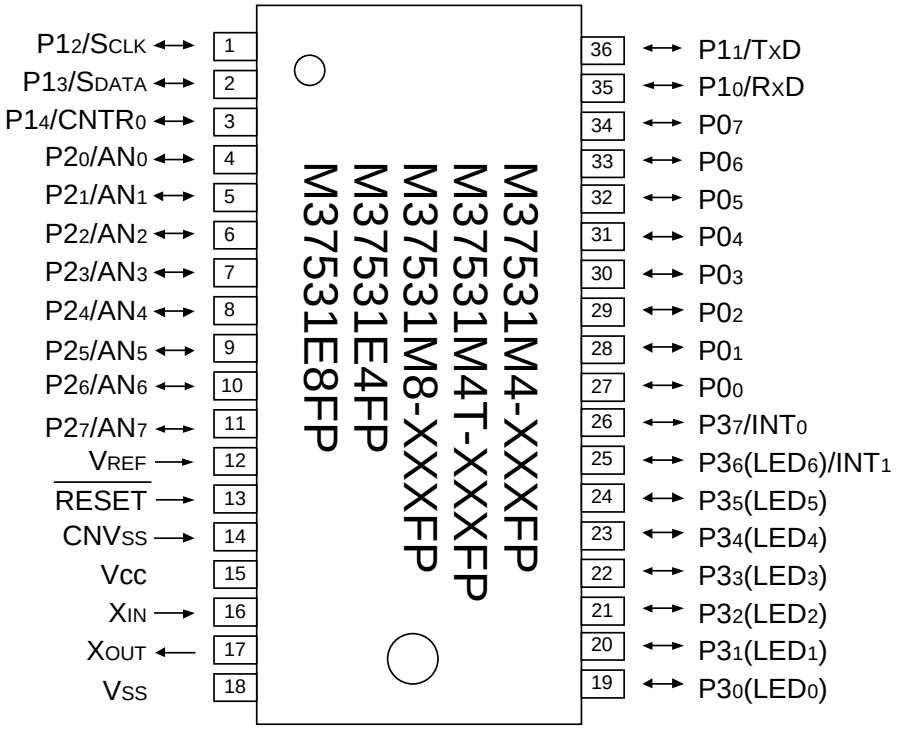
FEATURES

- Basic machine-language instructions 69
- The minimum instruction execution time ..... 0.50 µs
  (at 8 MHz oscillation frequency for the shortest instruction, in high-speed mode)
- Memory size ROM ..... 8K to 16K bytes
  RAM ..... 256 to 384 bytes
- Programmable I/O ports 29
  (25 in 32-pin version)
- Interrupts ..... 12 sources, 8 vectors
  (11 sources, 8 vectors for 32-pin version)
- Timers ..... 8-bit × 3
- Serial I/O1 ..... 8-bit × 1
  (UART)
- Serial I/O2 ..... 8-bit × 1
  (Clock-synchronized)
- A-D converter ..... 10-bit × 8 channels
  (6 channels for 32-pin version)
- Clock generating circuit ..... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  At 8 MHz XIN oscillation frequency at ceramic oscillation ..... 4.0 to 5.5 V
  At 4 MHz XIN oscillation frequency at ceramic oscillation ..... 2.4 to 5.5 V
  At 2 MHz XIN oscillation frequency at ceramic oscillation ..... 2.2 to 5.5 V
  At 4 MHz XIN oscillation frequency at RC oscillation ..... 4.0 to 5.5 V
  At 2 MHz XIN oscillation frequency at RC oscillation ..... 2.4 to 5.5 V
  At 1 MHz XIN oscillation frequency at RC oscillation ..... 2.2 to 5.5 V
- Power dissipation ..... 25 mW (standard)
- Operating temperature range ..... –20 to 85 °C
  (–40 to 85 °C or –40 to 125 °C for extended operating temperature version)

APPLICATION

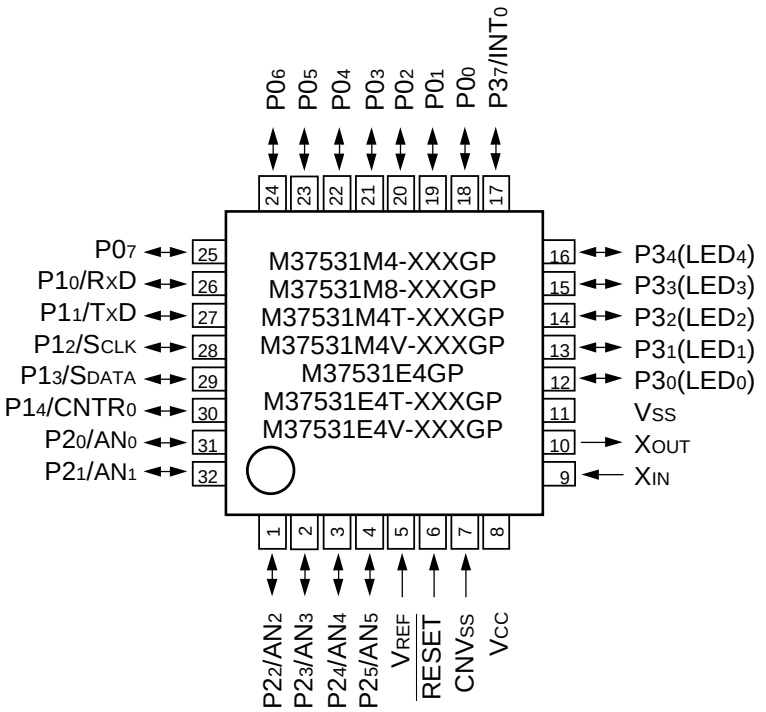
Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

PIN CONFIGURATION (TOP VIEW)



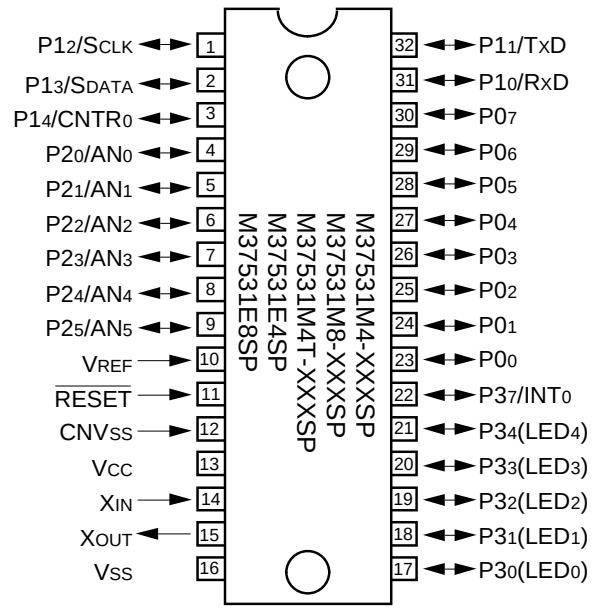
Package type: 36P2R-A

Fig. 1 Pin configuration (36P2R package type)



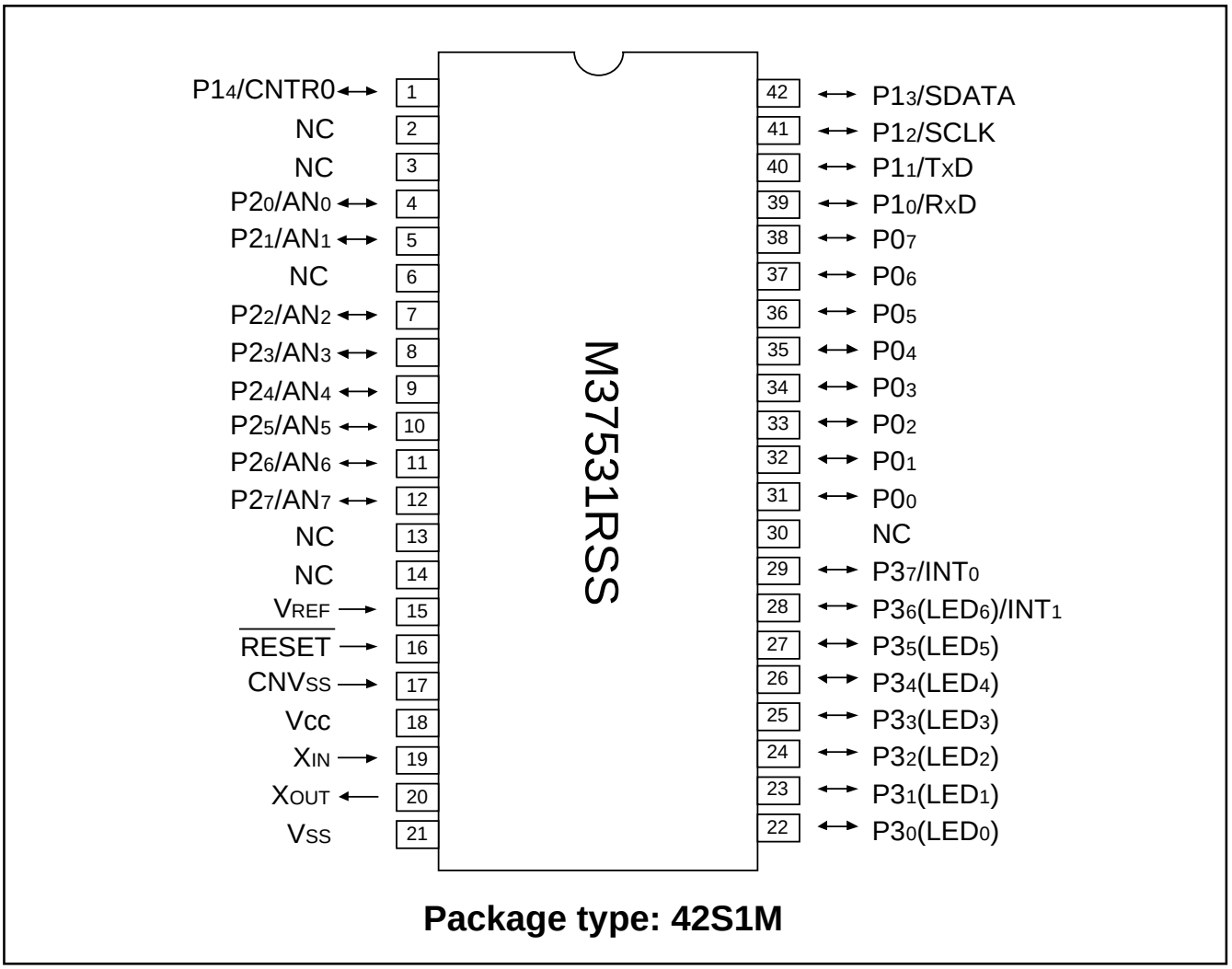
Package type: 32P6B-A

Fig. 2 Pin configuration (32P6B package type)



Package type: 32P4B

Fig. 3 Pin configuration (32P4B package type)



Package type: 42S1M

Fig. 4 Pin configuration (42S1M package type)

FUNCTIONAL BLOCK

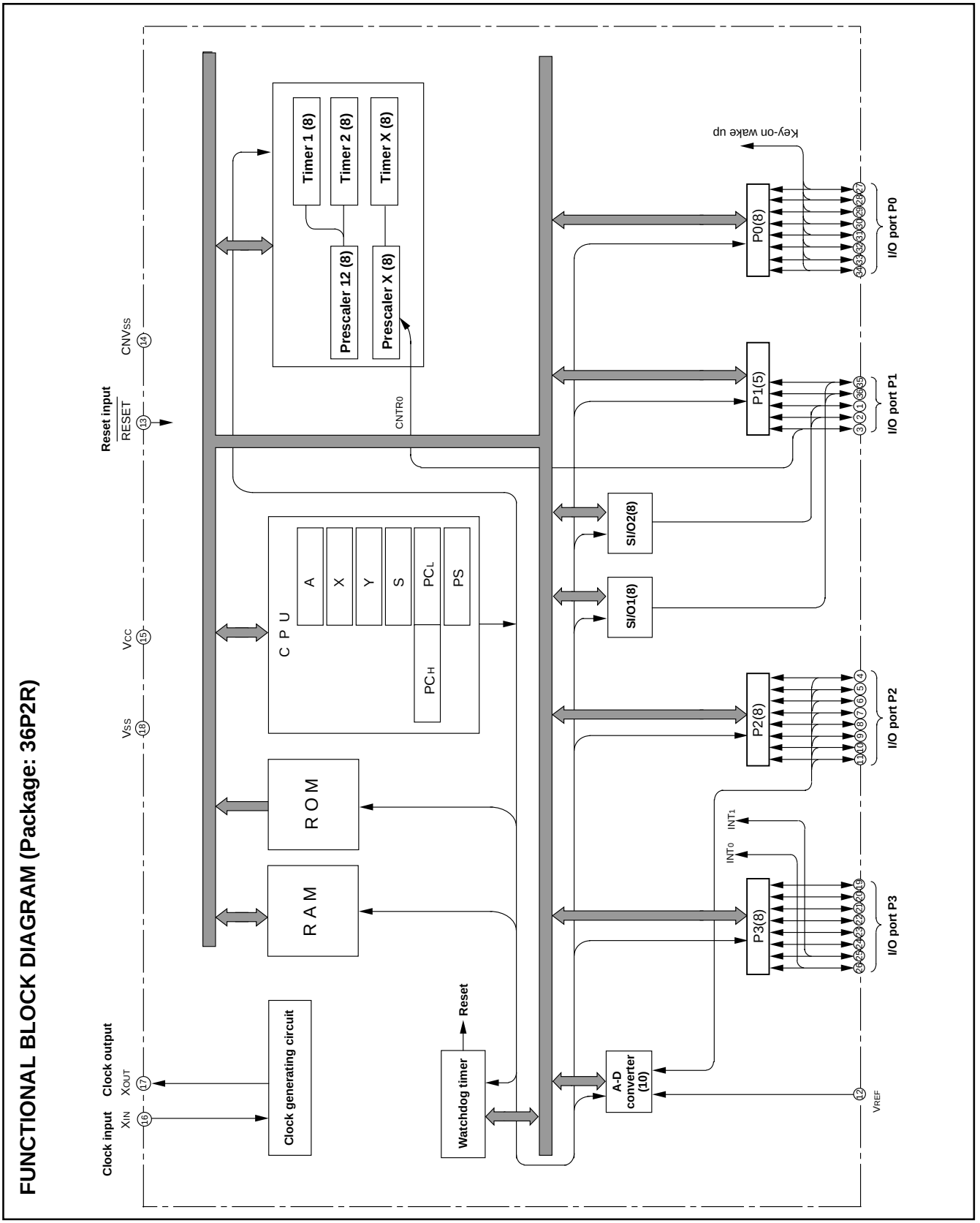


Fig. 5 Functional block diagram (36P2R package)

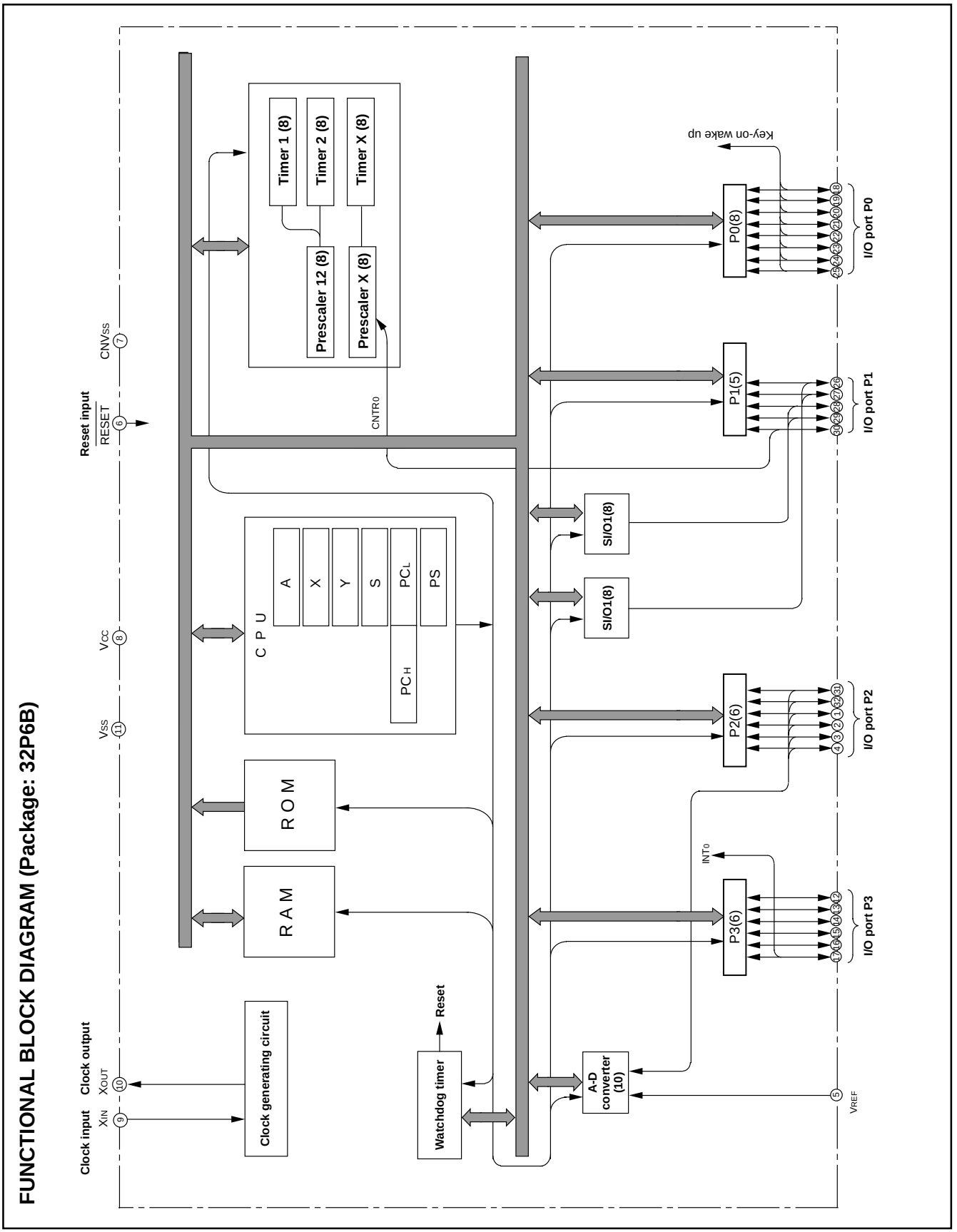


Fig. 6 Functional block diagram (32P6B package)

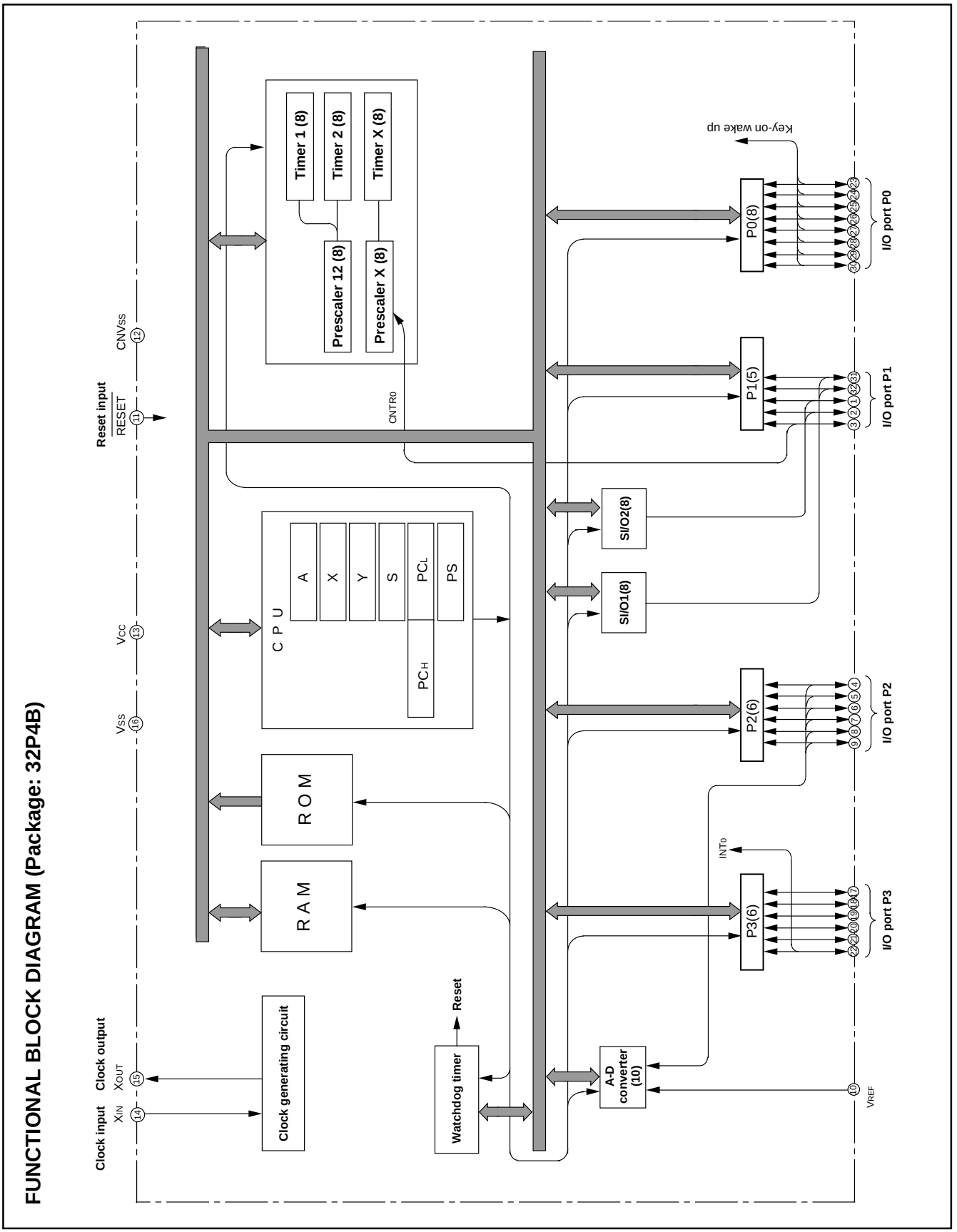


Fig. 7 Functional block diagram (32P4B package)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source (Note 1)	•Apply voltage of 2.2–5.5 V to Vcc, and 0 V to Vss.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L"	
X_{IN}	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the X_{IN} and X_{OUT} pins. •For using RC oscillator, short between the X_{IN} and X_{OUT} pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Key-input (key-on wake up interrupt input) pins
$P1_0$/RxD $P1_1$/TxD	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$, $P1_2$ and $P1_3$	•Serial I/O1 function pin
$P1_2$/S_{CLK} $P1_3$/S_{DATA}			•Serial I/O2 function pin
$P1_4$/$CNTR_0$			•Timer X function pin
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2 (Note 2)	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A-D converter
$P3_0$–$P3_5$	I/O port P3 (Note 3)	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_6$ and $P3_7$). •CMOS 3-state output structure •$P3_0$ to $P3_6$ can output a large current for driving LED.	
$P3_6$/INT_1 $P3_7$/INT_0		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Interrupt input pins

Notes 1: V_{CC} = 2.4 to 5.5 V for the extended operating temperature version (–40 to 85 °C) and the extended operating temperature 125 °C version (–40 to 125 °C).

2: 6-bit I/O port ($P2_0$–$P2_5$) for the 32-pin version.

3: 6-bit I/O port ($P3_0$–$P3_4$, $P3_7$/INT_0) for the 32-pin version.

GROUP EXPANSION

Mitsubishi plans to expand the 7531 group as follow:

Memory type

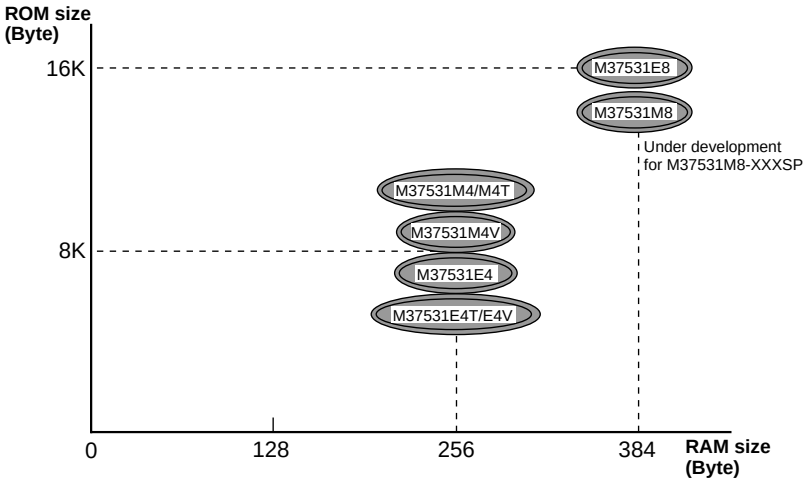
Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size ..... 8 K to 16 K bytes
RAM size ..... 256 to 384 bytes

Package

32P4B ..... 32 pin plastic molded SDIP
32P6B-A ..... 0.8 mm-pitch plastic molded LQFP
36P2R-A ..... 0.8 mm-pitch plastic molded SSOP
42S1M ..... 42 pin shrink ceramic PIGGY BACK



Note. Products under development: the development schedule and specification may be revised without notice.

Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37531M4-XXXSP	8192 (8062)	256	32P4B	Mask ROM version
M37531M4T-XXXSP				Mask ROM version (extended operating temperature version)
M37531E4SP				One Time PROM version (blank)
M37531M4-XXXFP			36P2R-A	Mask ROM version
M37531M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37531E4FP				One Time PROM version (blank)
M37531M4-XXXGP			32P6B-A	Mask ROM version
M37531M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37531M4V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37531E4GP				One Time PROM version (blank)
M37531E4T-XXXGP				One Time PROM version (shipped after programming, extended operating temperature version)
M37531E4V-XXXGP				One Time PROM version (shipped after programming, extended operating temperature 125 °C version)
M37531M8-XXXSP	16384 (16254)	384	32P4B	Mask ROM version
M37531E8SP				One Time PROM version (blank)
M37531M8-XXXFP			36P2R-A	Mask ROM version
M37531E8FP				One Time PROM version (blank)
M37531M8-XXXGP			32P6B-A	Mask ROM version
M37531RSS	————		42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

CPU

[CPU Mode Register] CPUM

The CPU mode register contains the stack page selection bit.
This register is allocated at address 003B16.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

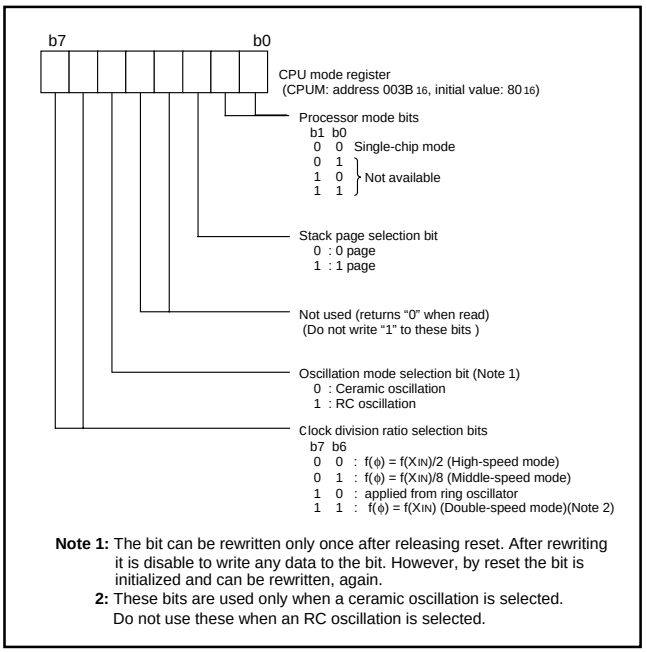


Fig. 9 Structure of CPU mode register

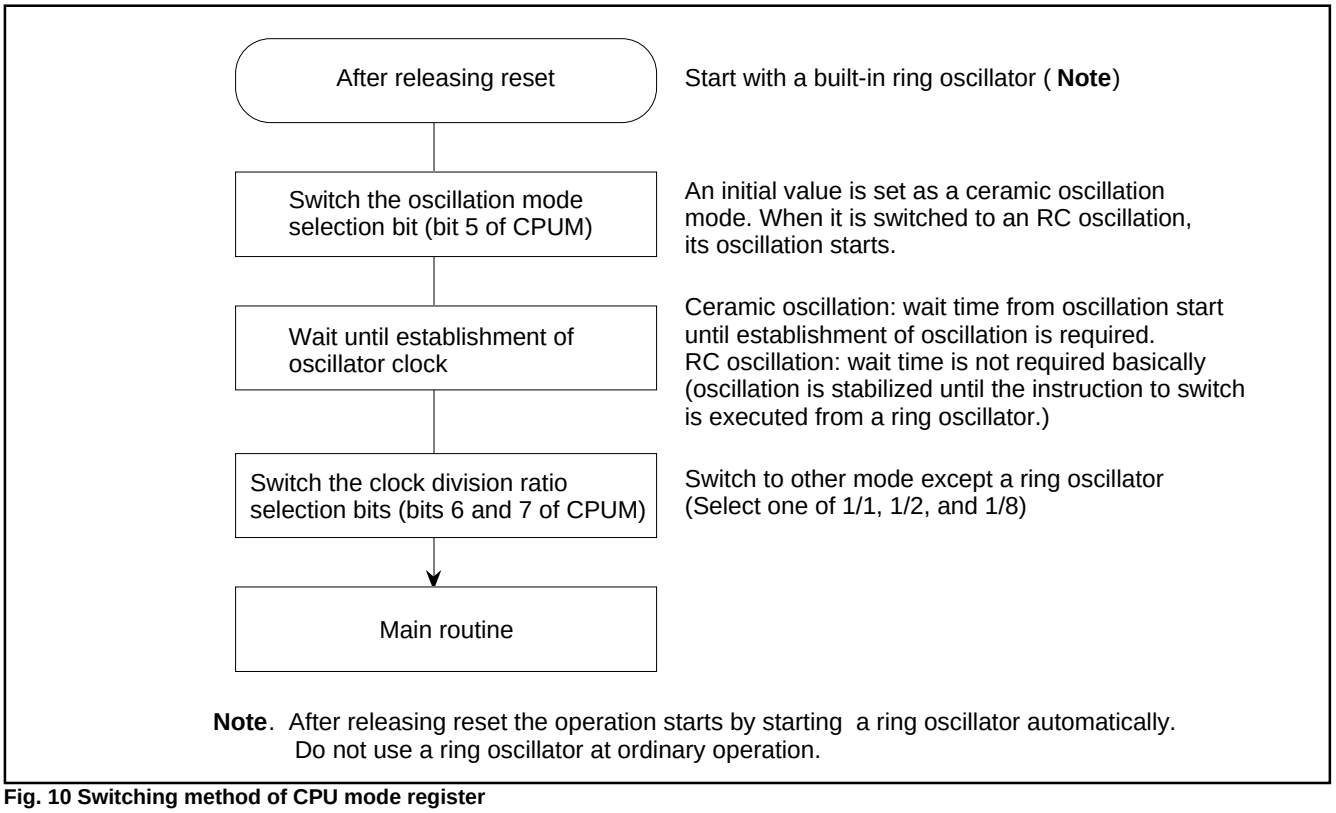


Fig. 10 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

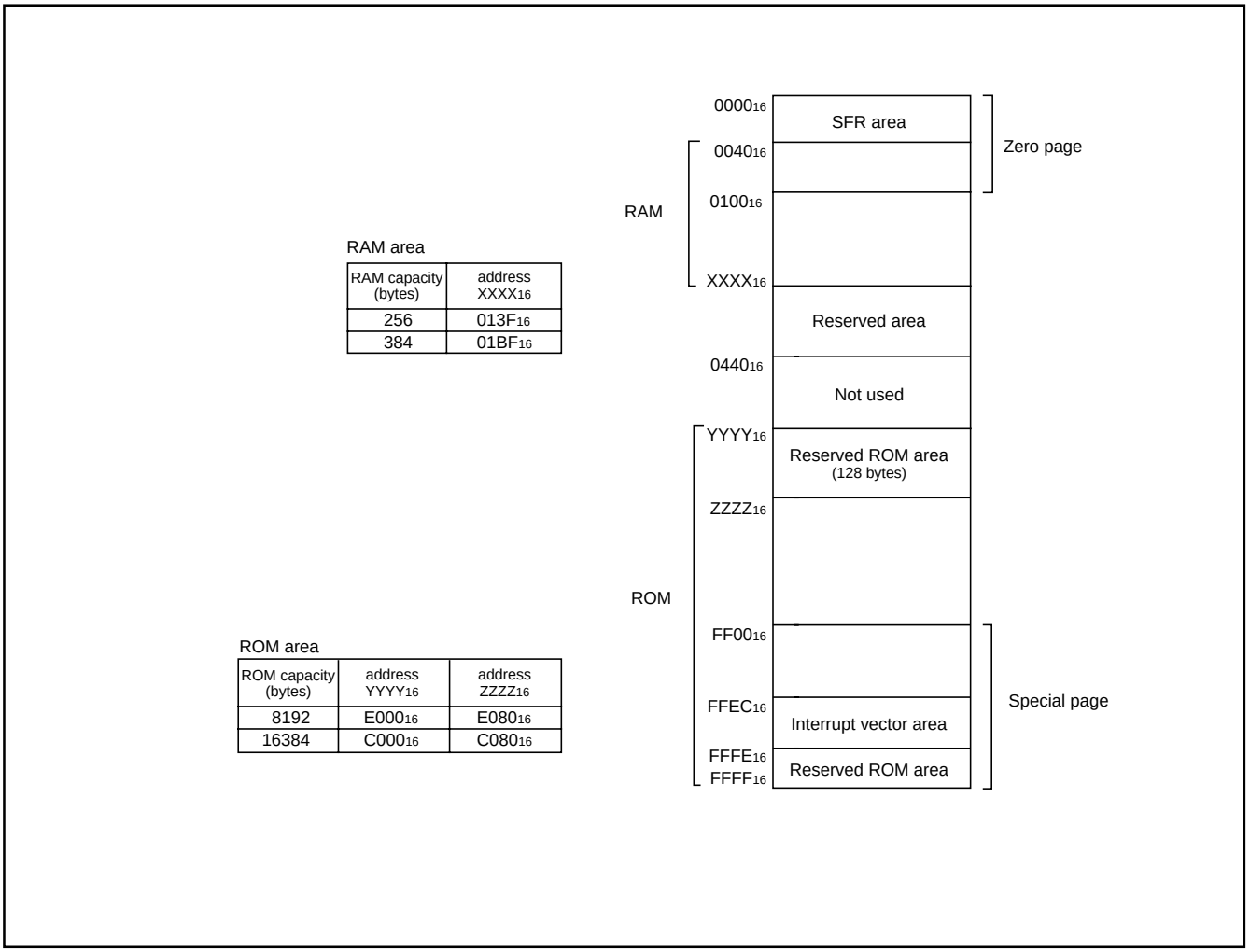


Fig. 11 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	
0001_{16}	Port P0 direction register (P0D)	0021_{16}	
0002_{16}	Port P1 (P1)	0022_{16}	
0003_{16}	Port P1 direction register (P1D)	0023_{16}	
0004_{16}	Port P2 (P2)	0024_{16}	
0005_{16}	Port P2 direction register (P2D)	0025_{16}	
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}	Port P3 direction register (P3D)	0027_{16}	
0008_{16}		0028_{16}	Prescaler 12 (PRE12)
0009_{16}		0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	Timer 2 (T2)
$000B_{16}$		$002B_{16}$	Timer X mode register (TM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source set register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$		$003D_{16}$	
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$		$003F_{16}$	

Note : Do not access to the SFR area including nothing.

Fig. 12 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port. When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

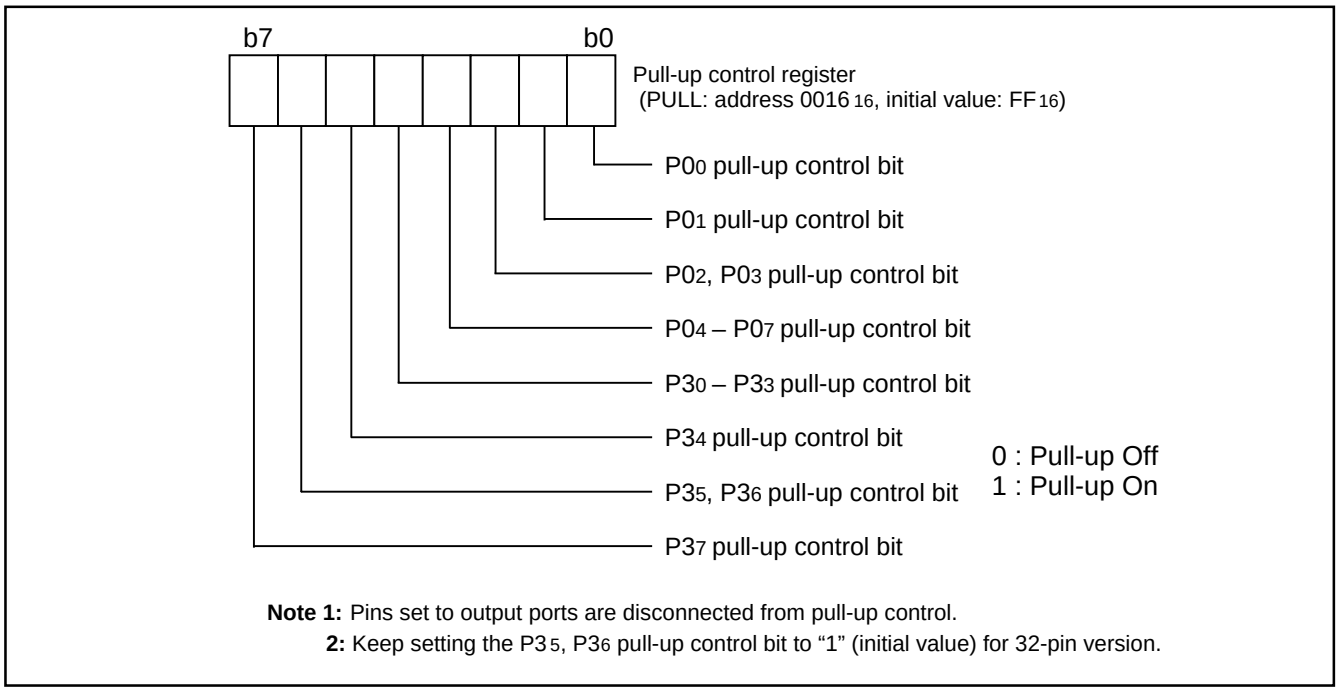
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

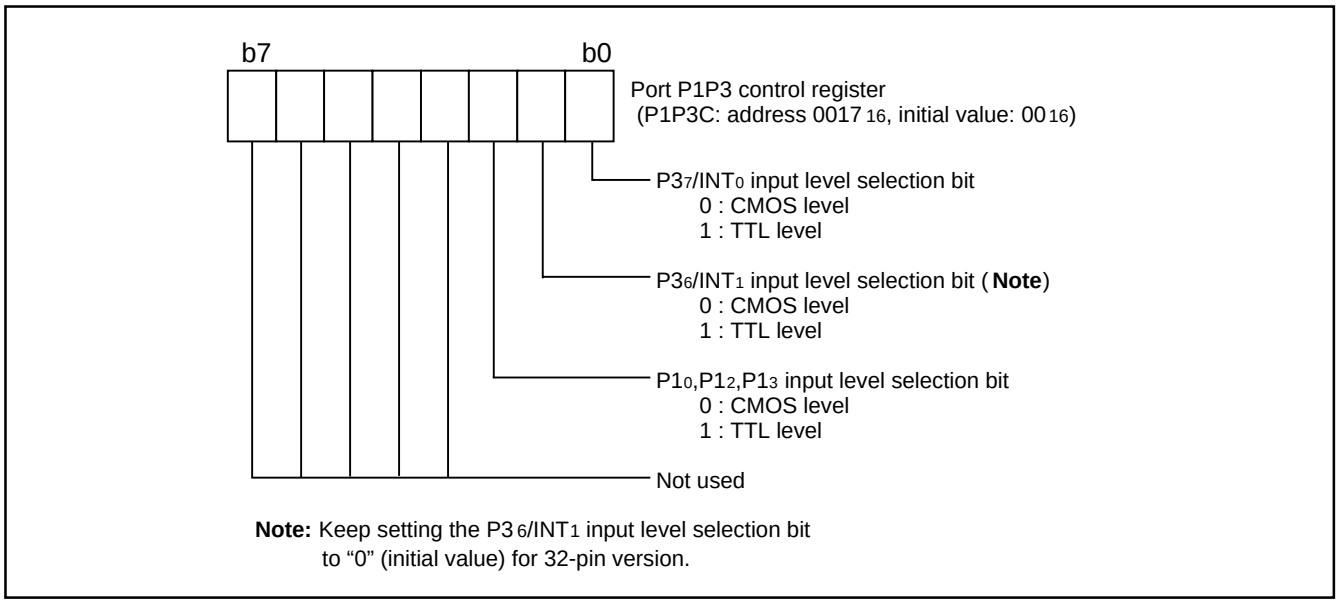
[Port P1P3 control] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ by program.



Note 1: Pins set to output ports are disconnected from pull-up control.
2: Keep setting the P35, P36 pull-up control bit to "1" (initial value) for 32-pin version.

Fig. 13 Structure of pull-up control register



Note: Keep setting the P36/INT1 input level selection bit to "0" (initial value) for 32-pin version.

Fig. 14 Structure of port P1P3 control register

Table 5 I/O port function table

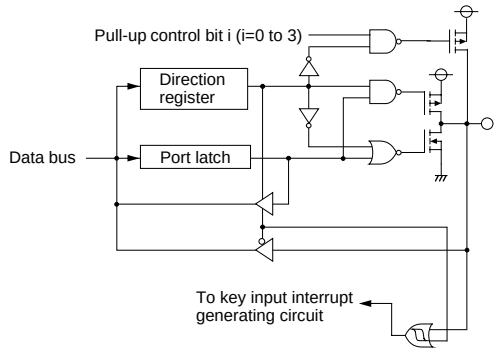
Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (Note 1)	Key input interrupt	Pull-up control register	(1)
$P1_0$/RxD	I/O port P1			Serial I/O1 function input/output	Serial I/O1 control register	(2)
$P1_1$/TxD						(3)
$P1_2$/S_{CLK}				Serial I/O2 function input/output	Serial I/O2 control register	(4)
$P1_3$/S_{DATA}						(5)
$P1_4$/$CNTR_0$				Timer X function input/output	Timer X mode register	(6)
$P2_0$/AN_0–$P2_7$/AN_7	I/O port P2 (Note 2)			A-D conversion input	A-D control register	(7)
$P3_0$–$P3_5$	I/O port P3 (Note 3)					(8)
$P3_6$/INT_1				External interrupt input	Interrupt edge selection register	(9)
$P3_7$/INT_0						

Notes 1: Ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ are CMOS/TTL level.

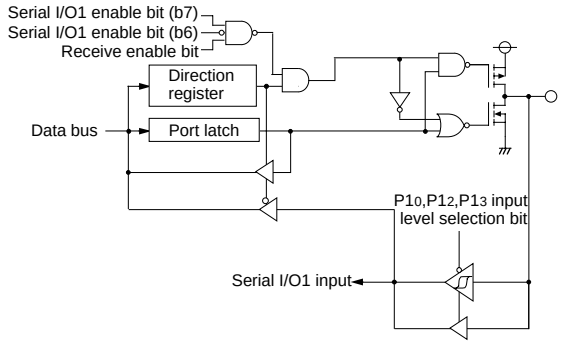
2: The $P2_6$/AN_6 and $P2_7$/AN_7 pins do not exist for the 32-pin version.

3: The $P3_5$ and $P3_6$/INT_1 pins do not exist for the 32-pin version.

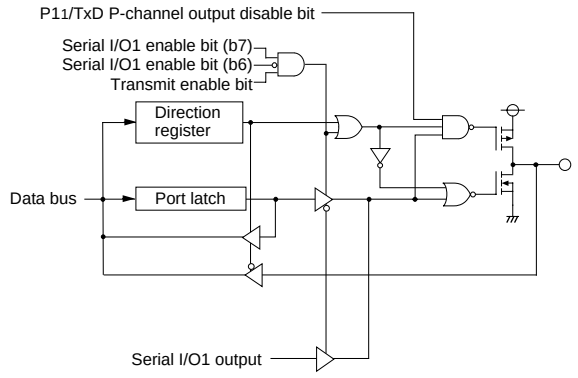
(1) Port P0



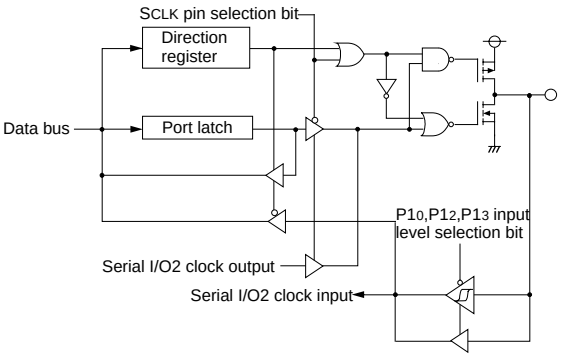
(2) Port P1$_0$



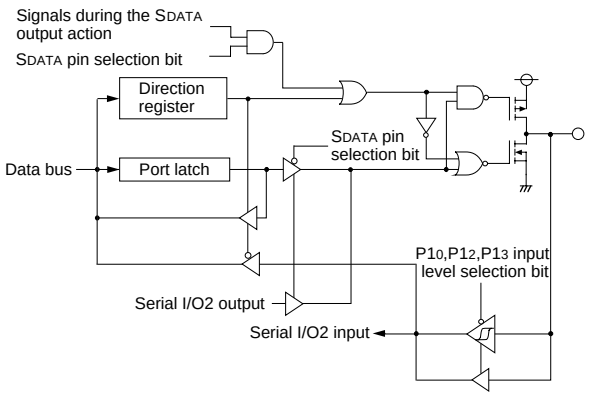
(3) Port P1$_1$



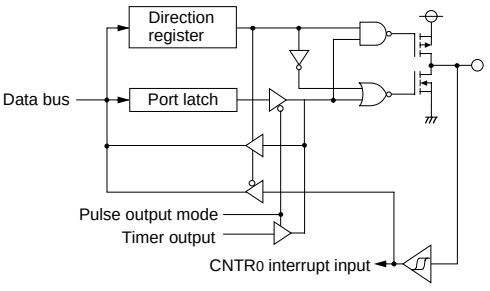
(4) Port P1$_2$



(5) Port P1$_3$



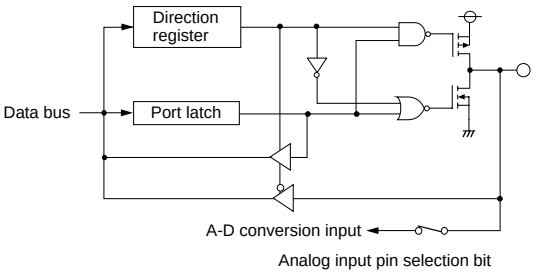
(6) Port P1$_4$



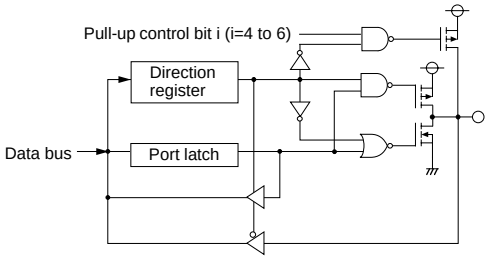
P1$_0$, P1$_2$, P1$_3$, P3$_6$, and P3$_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 15 Block diagram of ports (1)

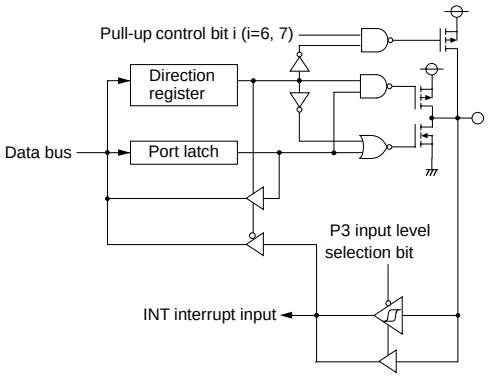
(7) Ports $P2_0$ – $P2_7$



(8) Ports $P3_0$ – $P3_5$



(9) Ports $P3_6$, $P3_7$



$P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 16 Block diagram of ports (2)

Interrupts

Interrupts occur by 12 different sources : 4 external sources, 7 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.

It becomes usable by switching $CNTR_0$ and AD conversion interrupt sources with bit 7 of the interrupt edge selection register, timer 2 and serial I/O2 interrupt sources with bit 6, timer X and key-on wake-up interrupt sources with bit 5, and serial I/O1 transmit and INT_1 interrupt sources with bit 4.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0, INT_1,$CNTR_0$) is set, the interrupt request bit may be set.

Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of $CNTR_0$: Timer X mode register)
3. Clear the set interrupt request bit to "0".
4. Enable the external interrupt which is selected.

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O1 receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O1 data receive	Valid when serial I/O1 is selected
Serial I/O1 transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid when serial I/O1 is selected
INT_1 (Note 3)				At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Timer X	5	$FFF5_{16}$	$FFF4_{16}$	At timer X underflow	
Key-on wake-up				At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
Timer 1	6	$FFF3_{16}$	$FFF2_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	7	$FFF1_{16}$	$FFF0_{16}$	At timer 2 underflow	
Serial I/O2				At completion of transmit/receive shift	
$CNTR_0$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	
BRK instruction	9	$FFED_{16}$	$FFEC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

3: It is an interrupt which can use only for 36 pin version.

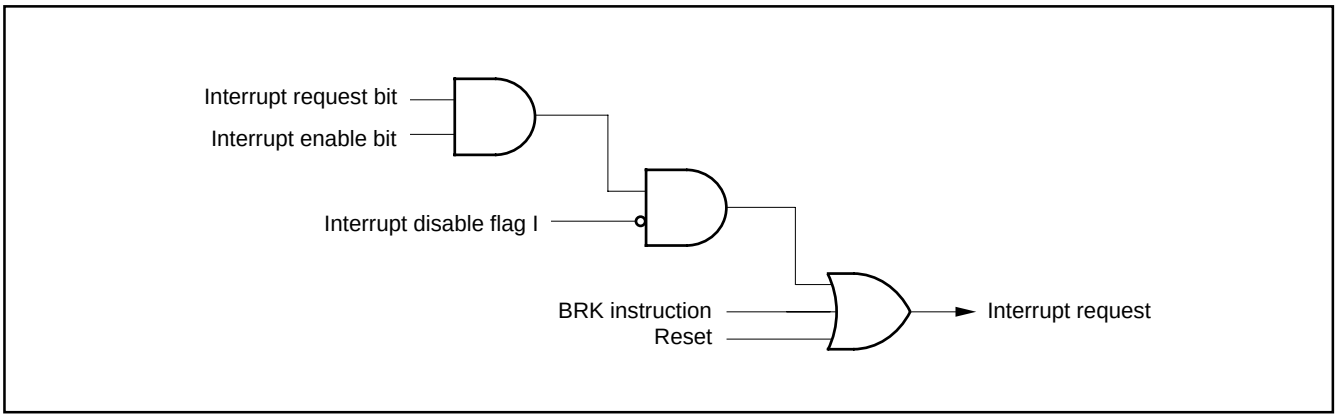


Fig. 17 Interrupt control

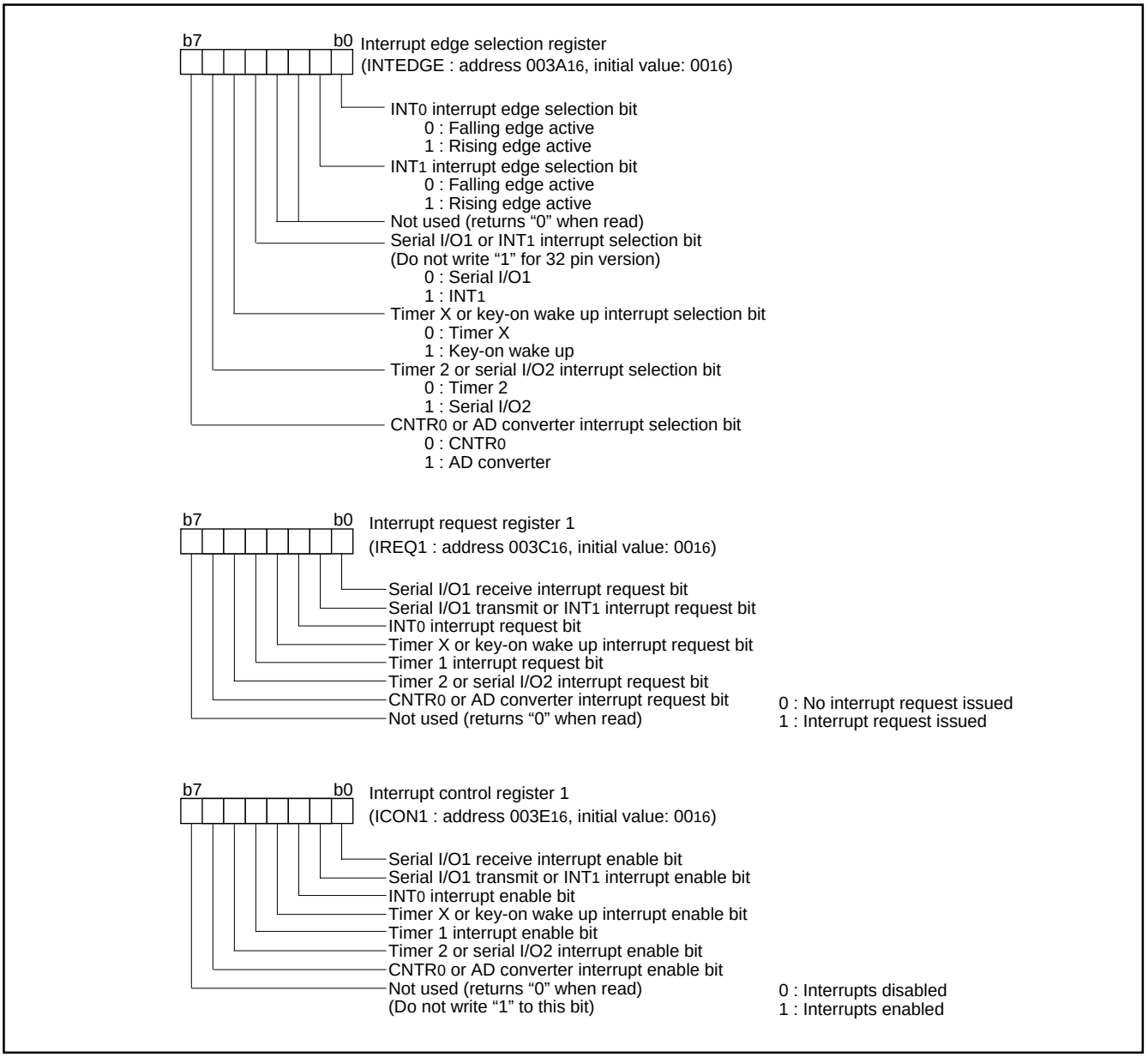


Fig. 18 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0$_0$ to P0$_3$ as input ports.

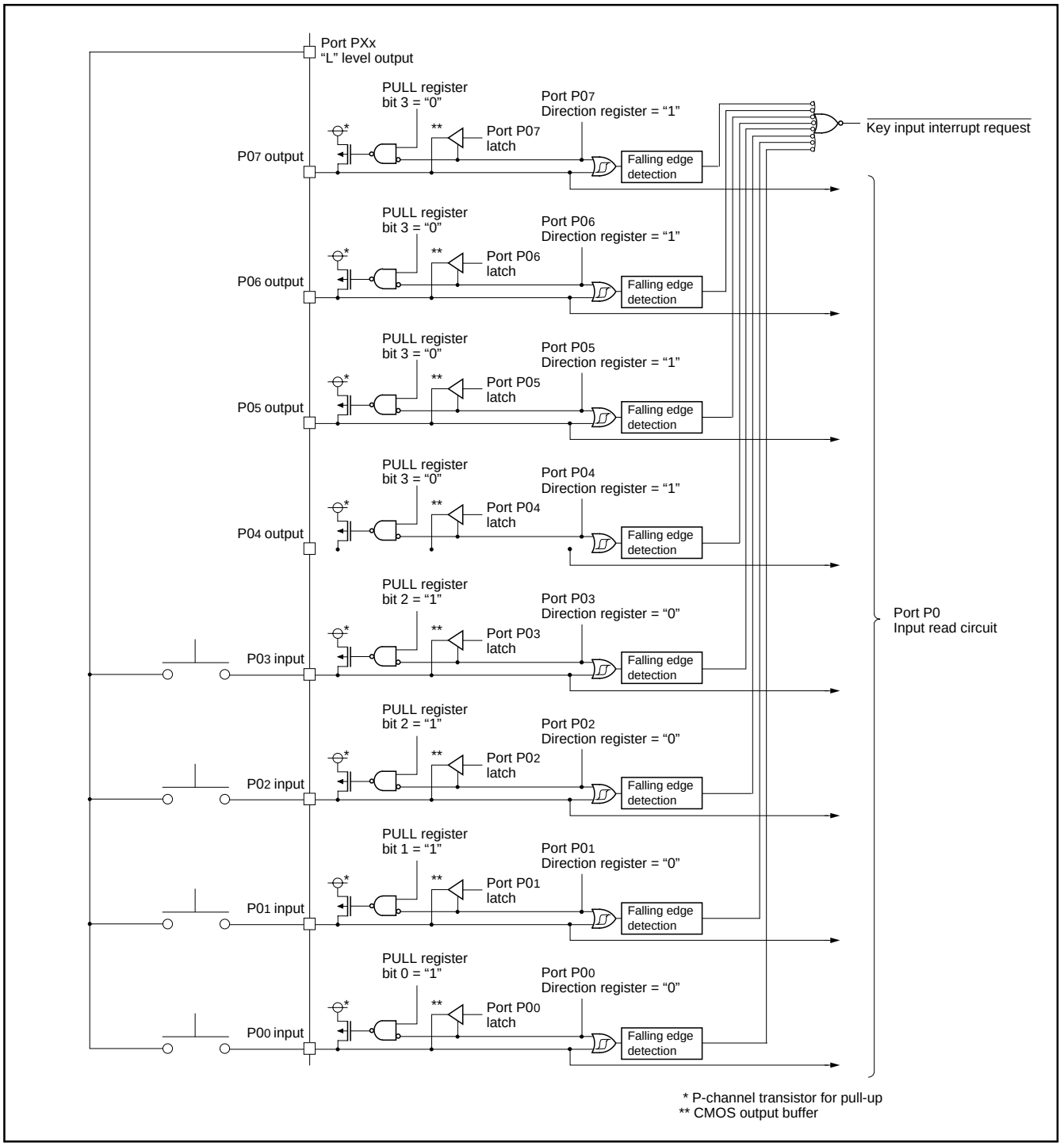


Fig. 19 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7531 Group has 3 timers: timer X, timer 1 and timer 2.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches “0”, an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to “1”.

●Timer 1, Timer 2

Prescaler 12 always counts f(XIN)/16. Timer 1 and timer 2 always count the prescaler output and periodically sets the interrupt request bit.

●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

• Timer Mode

The timer counts the signal selected by the timer X count source selection bit.

• Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bit, and outputs a signal whose polarity is inverted each time the timer value reaches “0”, from the CNTR0 pin.
When the CNTR0 active edge switch bit is “0”, the output of the CNTR0 pin is started with an “H” output.
At “1”, this output is started with an “L” output. When using a timer in this mode, set the port P14 direction register to output mode.

• Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the CNTR0 pin.
When the CNTR0 active edge switch bit is “0”, the timer counts the rising edge of the CNTR0 pin. When this bit is “1”, the timer counts the falling edge of the CNTR0 pin.

• Pulse Width Measurement Mode

When the CNTR0 active edge switch bit is “0”, the timer counts the signal selected by the timer X count source selection bit while the CNTR0 pin is “H”. When this bit is “1”, the timer counts the signal while the CNTR0 pin is “L”.
In any mode, the timer count can be stopped by setting the timer X count stop bit to “1”. Each time the timer overflows, the interrupt request bit is set.

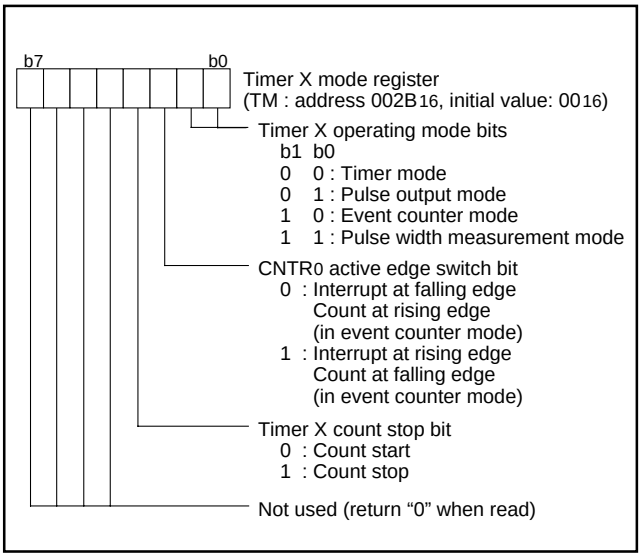


Fig. 20 Structure of timer X mode register

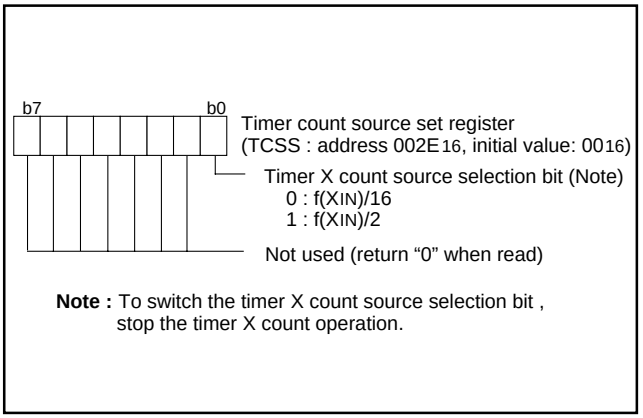


Fig. 21 Timer count source setting register

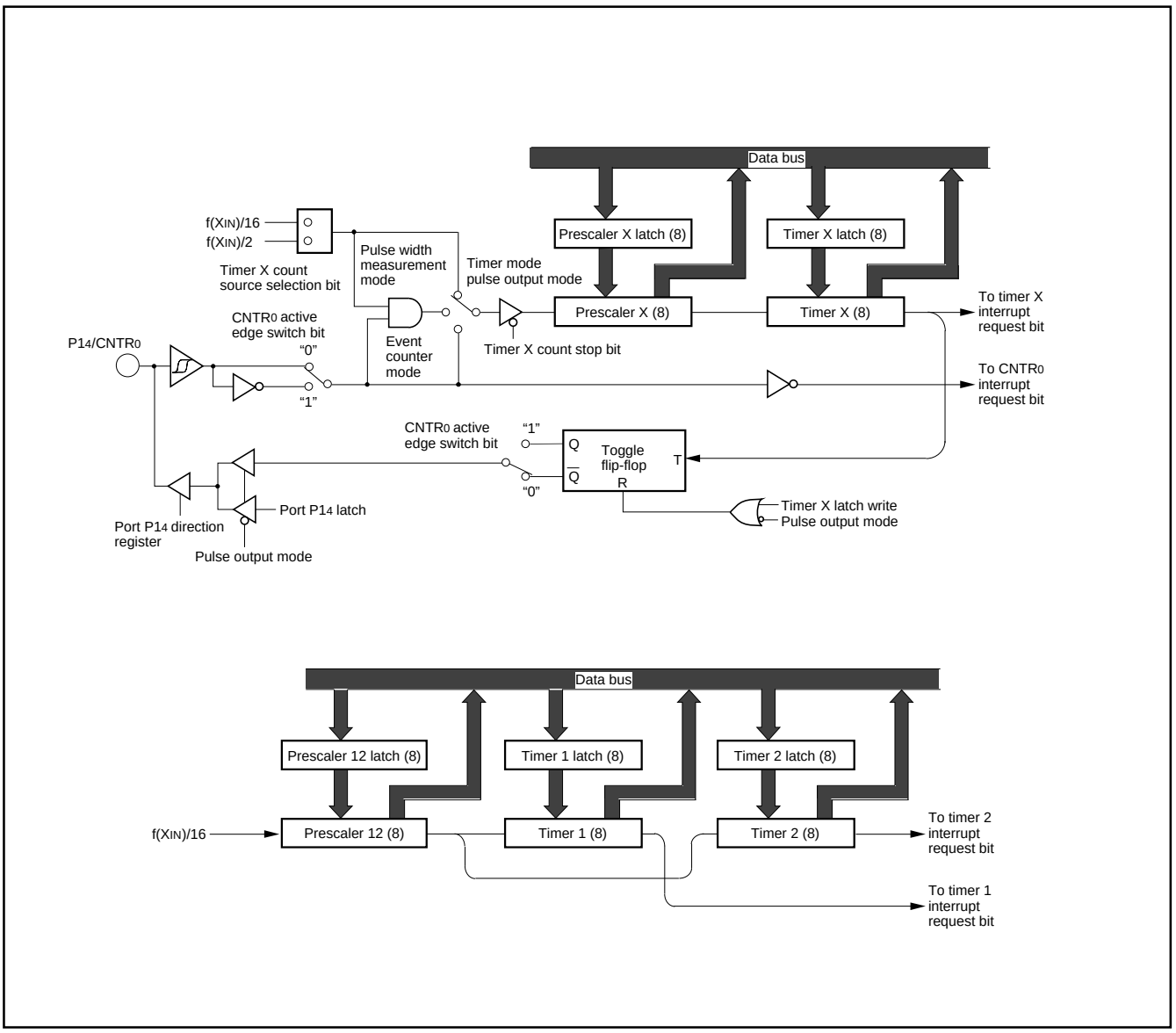


Fig. 22 Block diagram of timer X, timer 1 and timer 2

Serial I/O

●Serial I/O1

Serial I/O1 can be used as an asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O1 is in operation.

Eight serial data transfer formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical.

Each of the transmit and receive shift registers has a buffer register (the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the respective buffer registers. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession.

By selecting “1” for continuous transmit valid bit (bit 2 of SIO1CON), continuous transmission of the same data is made possible.

This can be used as a simplified PWM.

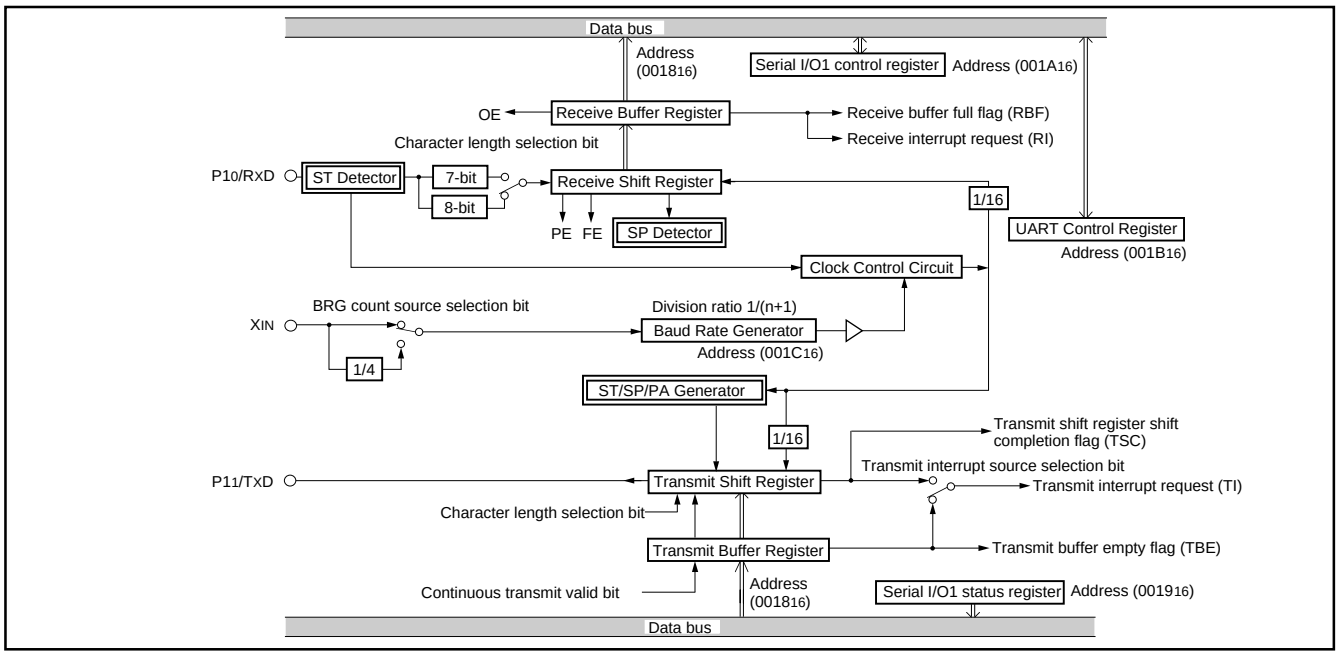
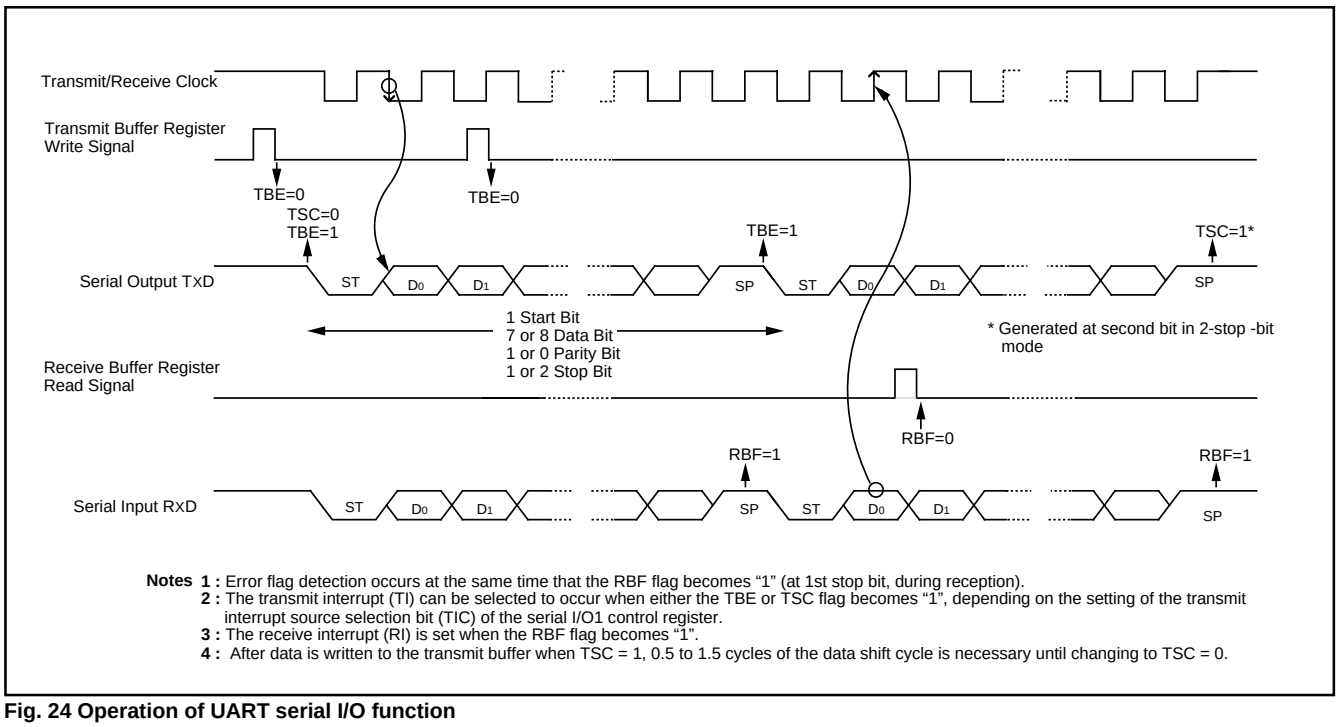


Fig. 23 Block diagram of UART serial I/O



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes “1”, depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes “1”.
4 : After data is written to the transmit buffer when TSC = 1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC = 0.

Fig. 24 Operation of UART serial I/O function

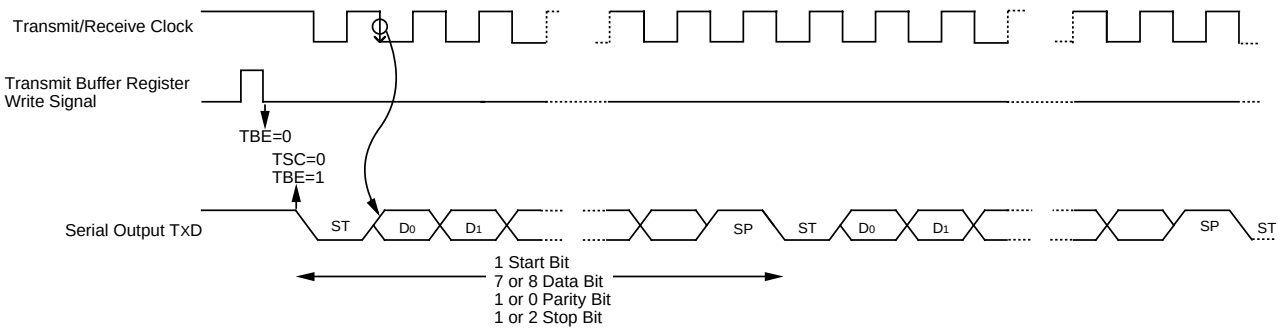
[Serial I/O1 control register] SIO1CON
The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register] UARTCON
The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P1_1$/TxD pin.

[Serial I/O1 status register] SIO1STS
The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “11” to bits 7 and 6 of the serial I/O1 control register initializes this register.
All bits of the serial I/O1 status register are initialized to “81_{16}” at reset.

[Transmit/Receive buffer register] TB/RB
The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7-bit, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator] BRG
The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.



Notes 1 : When the serial I/O1 enable bit (b7) is “1”, the transmit enable bit is “1”, and continuous transmit valid bit is “1”, writing on the transmit buffer initiates continuous transmission of the same data.
2 : Select 0 for continuous transmit valid bit to stop continuous transmission.
The TXD pin will stop at high level after completing transmission of 1 byte.
3 : If the transmit buffer contents are rewritten during a continuous transmission, transmission of the rewritten data will be started after completing transmission of 1 byte.

Fig. 25 Continuous transmission operation of UART serial I/O

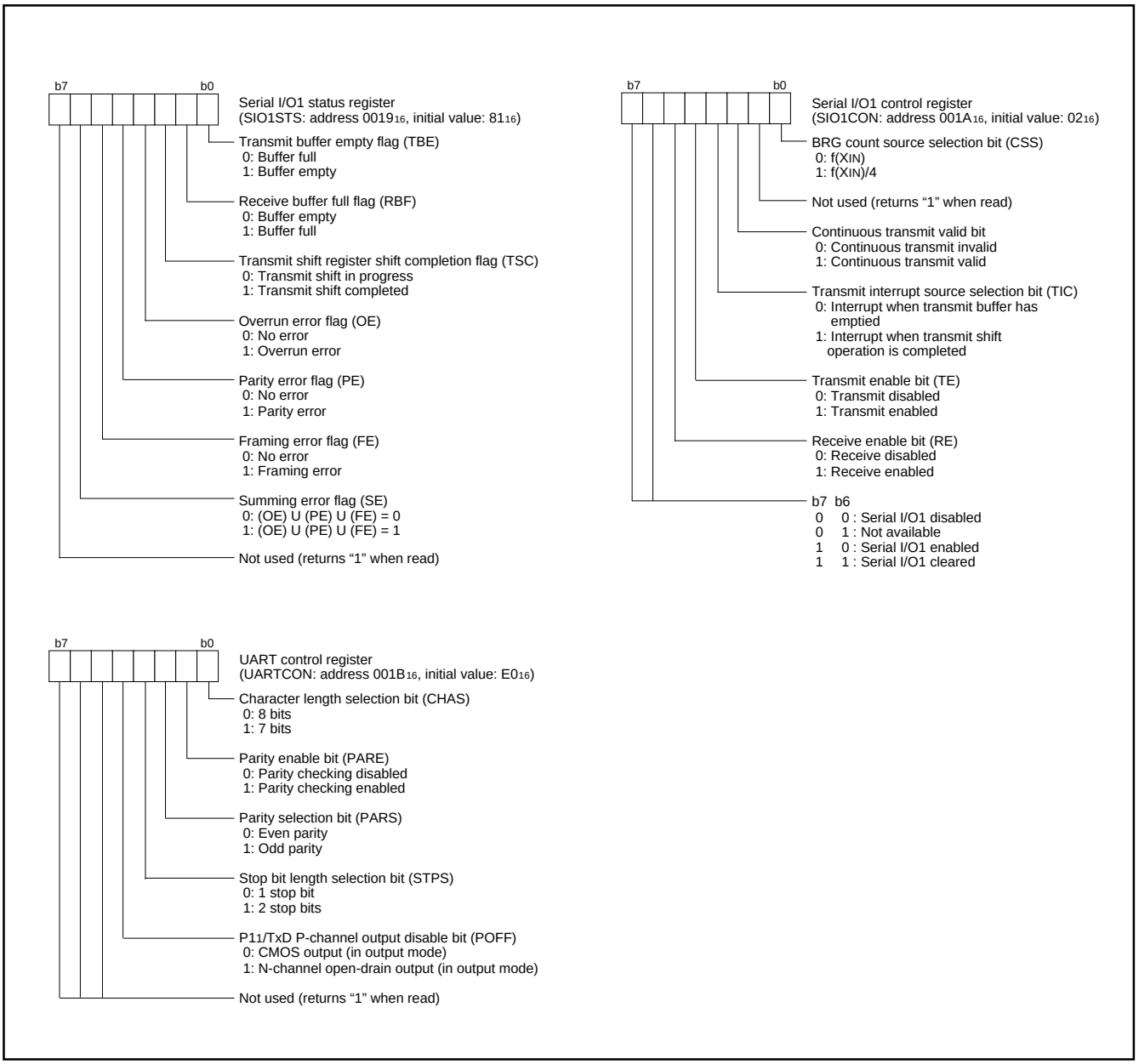


Fig. 26 Structure of serial I/O1-related registers (1)

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

•Set "0" to bit 3 to receive.

•At reception, clear bit 7 to "0" by writing a dummy data to the serial I/O2 register after completion of shift.

•Bit 7 is set to "1" a half cycle (of the shift clock) earlier than completion of shift operation. Accordingly, when using this bit to confirm shift completion, a half cycle or more of the shift clock must pass after confirming that this bit is set to "1", before performing read/write to the serial I/O2 register.

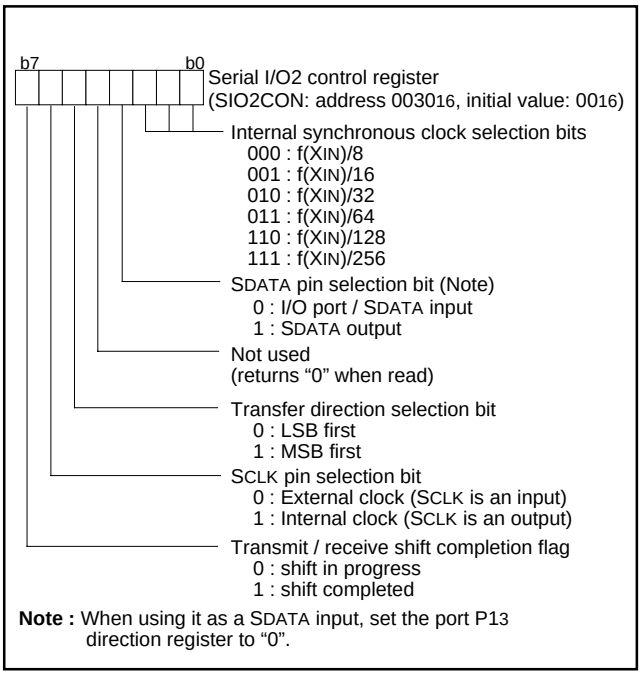


Fig. 27 Structure of serial I/O2 control registers

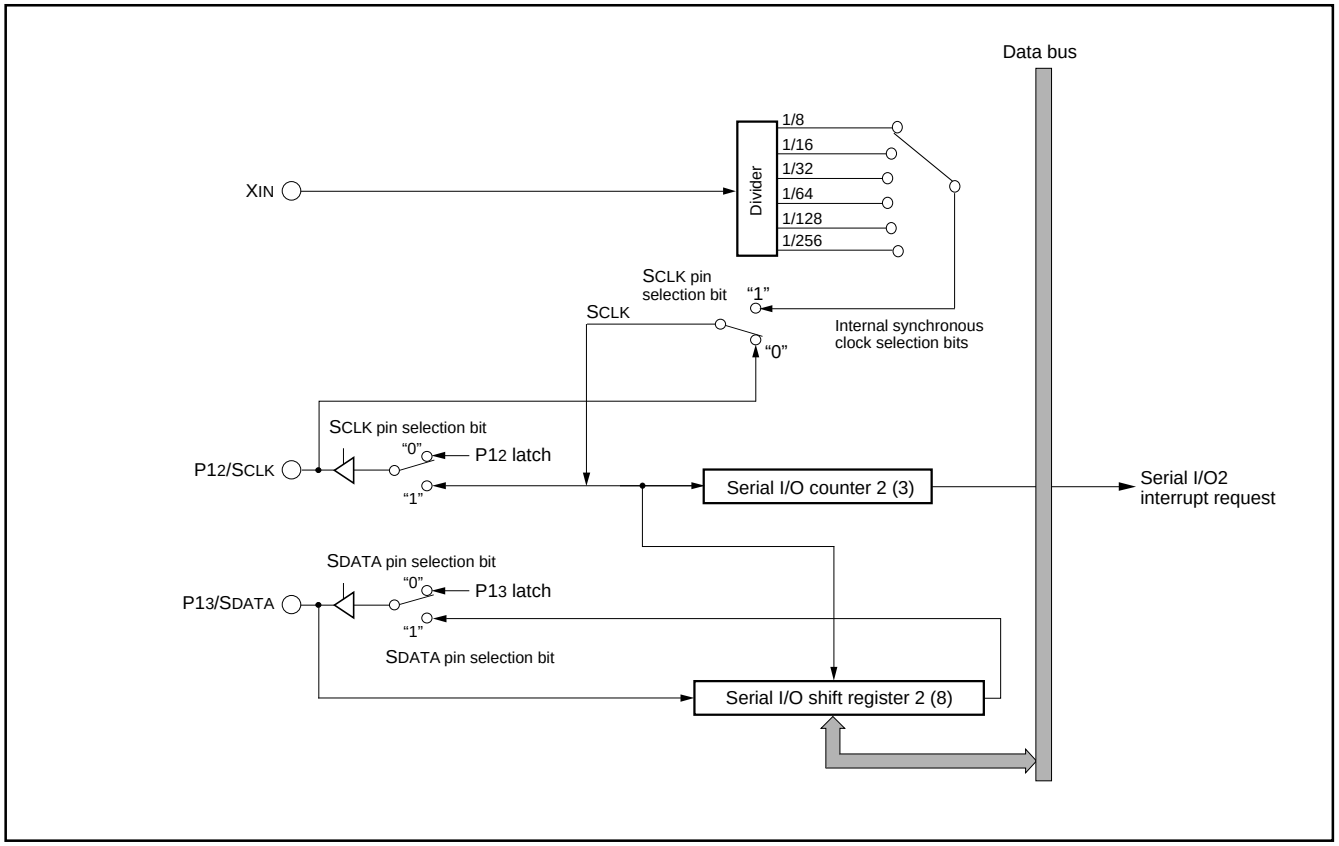


Fig. 28 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register (address 0031_{16}) the serial I/O2 counter is set to "7".

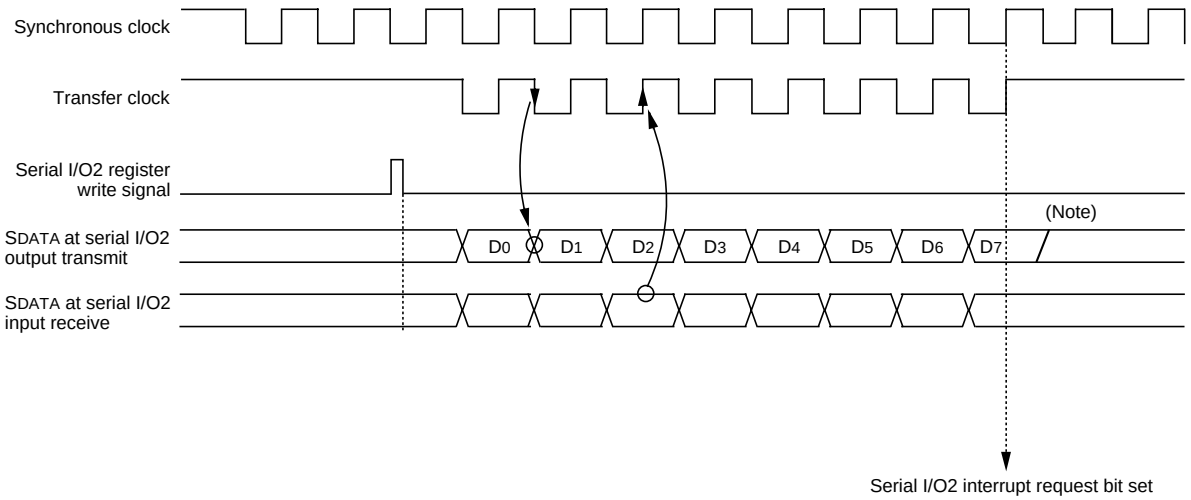
After writing, the SDATA pin outputs data every time the transfer clock shifts from a high to a low level. And, as the transfer clock shifts from a low to a high, the SDATA pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to "0".
- Transfer clock stops at an "H" level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA pin is in a high impedance state after the data transfer is complete (refer to Figure 29).

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA pin is not in a high impedance state on the completion of data transfer.



Note : When the internal clock is selected as the transfer and the direction register of P13/SDATA pin is set to the input mode, the SDATA pin is in a high impedance state after the data transfer is completed.

Fig. 29 Serial I/O2 timing (LSB first)

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion.
A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between V_{SS} and V_{REF} by 1024 by a resistor ladder, and outputs the divided voltages. Since the generator is disconnected from V_{REF} pin and V_{SS} pin, current is not flowing into the resistor ladder.

[Channel Selector]

The channel selector selects one of ports $P2_7/AN_7$ to $P2_0/AN_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set f(X_{IN}) to 500 kHz or more during A-D conversion.

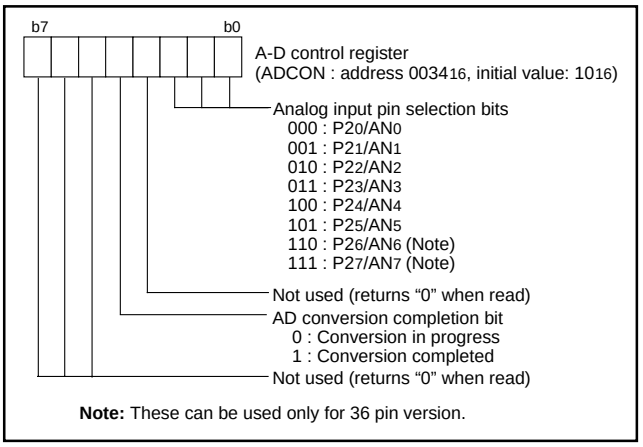


Fig. 30 Structure of A-D control register

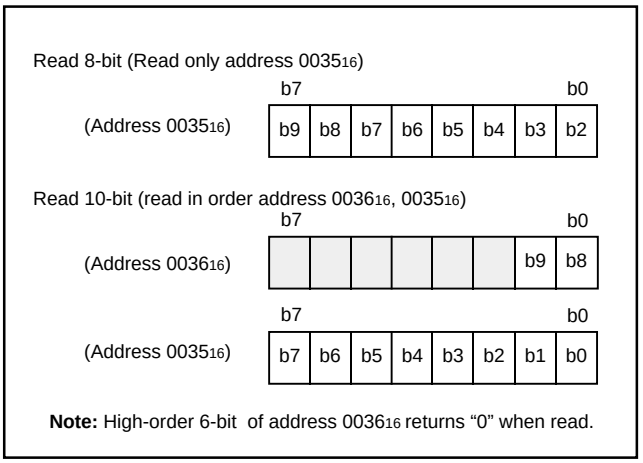


Fig. 31 Structure of A-D conversion register

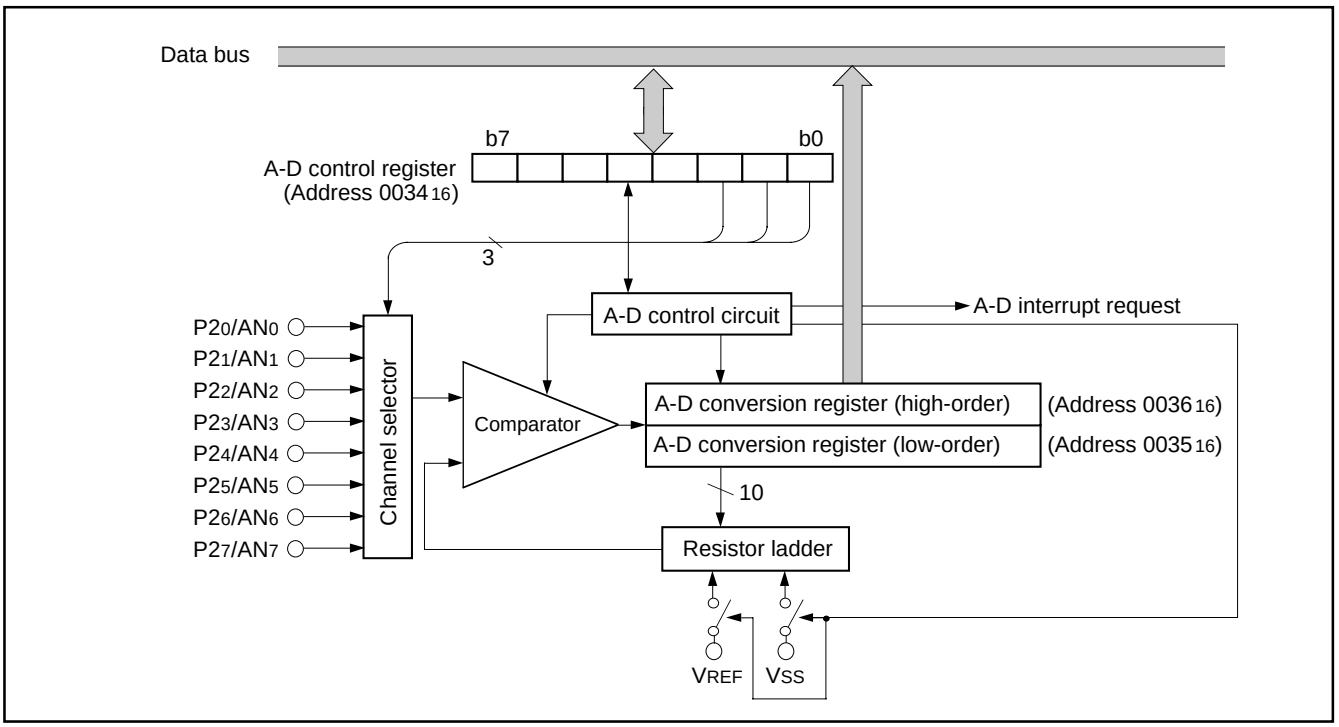


Fig. 32 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.

When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(XIN)=8 MHz.

When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 512 µs at f(XIN)=8 MHz.

This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

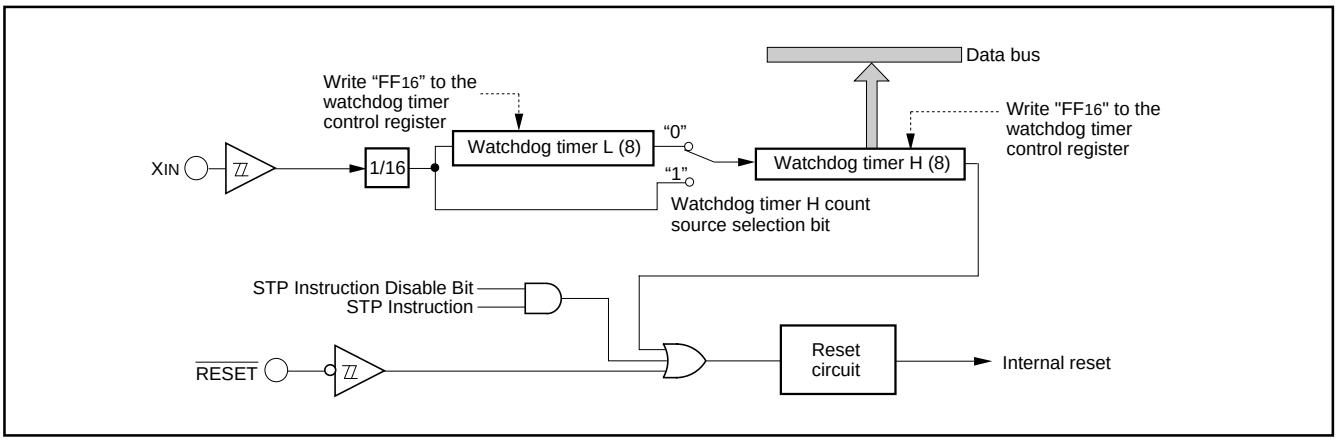


Fig. 33 Block diagram of watchdog timer

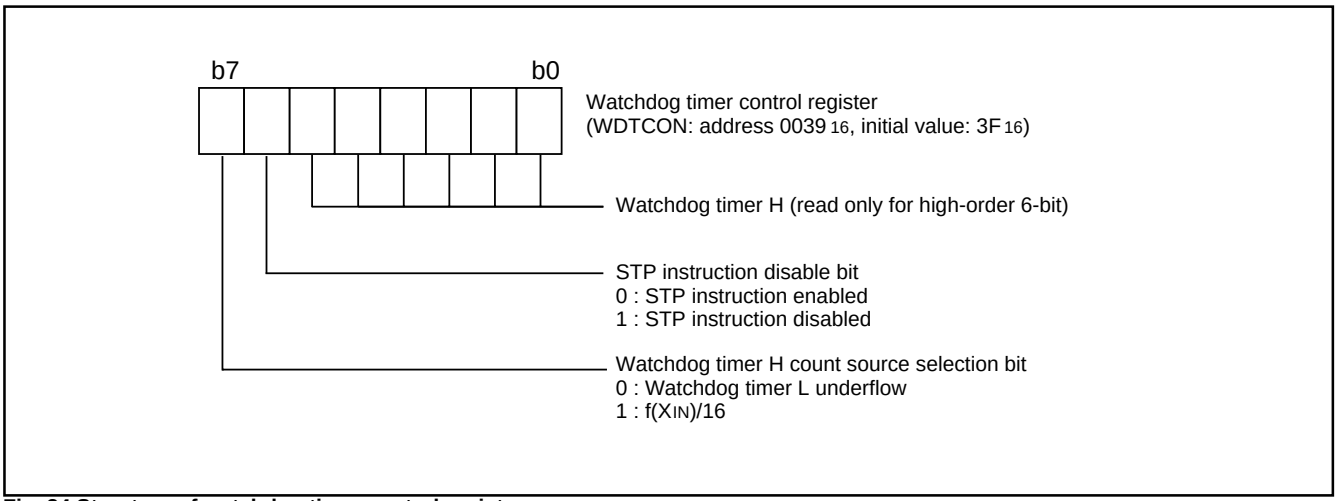


Fig. 34 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the "L" level for the following interval or more according to the power source voltage and X_{IN} is in stable oscillation.
After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the "H" level. The program starts from the address having the contents of address $FFFD_{16}$ as high-order address and the contents of address $FFFC_{16}$ as low-order address.
When V_{CC} = 2.2 to 5.5 V, reset input "L" interval is 45 μs or more
When V_{CC} = 2.4 to 5.5 V, reset input "L" interval is 35 μs or more
When V_{CC} = 4.0 to 5.5 V, reset input "L" interval is 15 μs or more

In the case of f(ϕ) ≤ 4 MHz, the reset input voltage must be 0.8 V or less when the power source voltage passes 4.0 V.
In the case of f(ϕ) ≤ 2 MHz, the reset input voltage must be 0.48 V or less when the power source voltage passes 2.4 V.
In the case of f(ϕ) ≤ 1 MHz, the reset input voltage must be 0.44 V or less when the power source voltage passes 2.2 V.

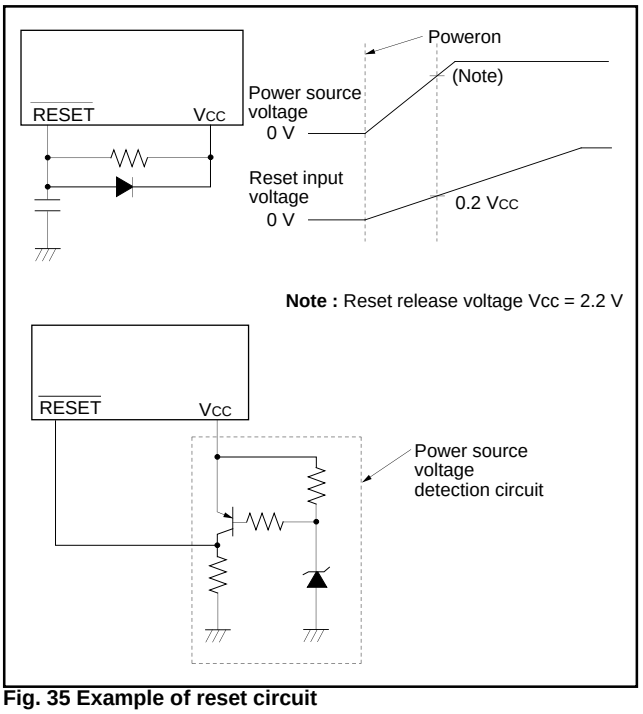


Fig. 35 Example of reset circuit

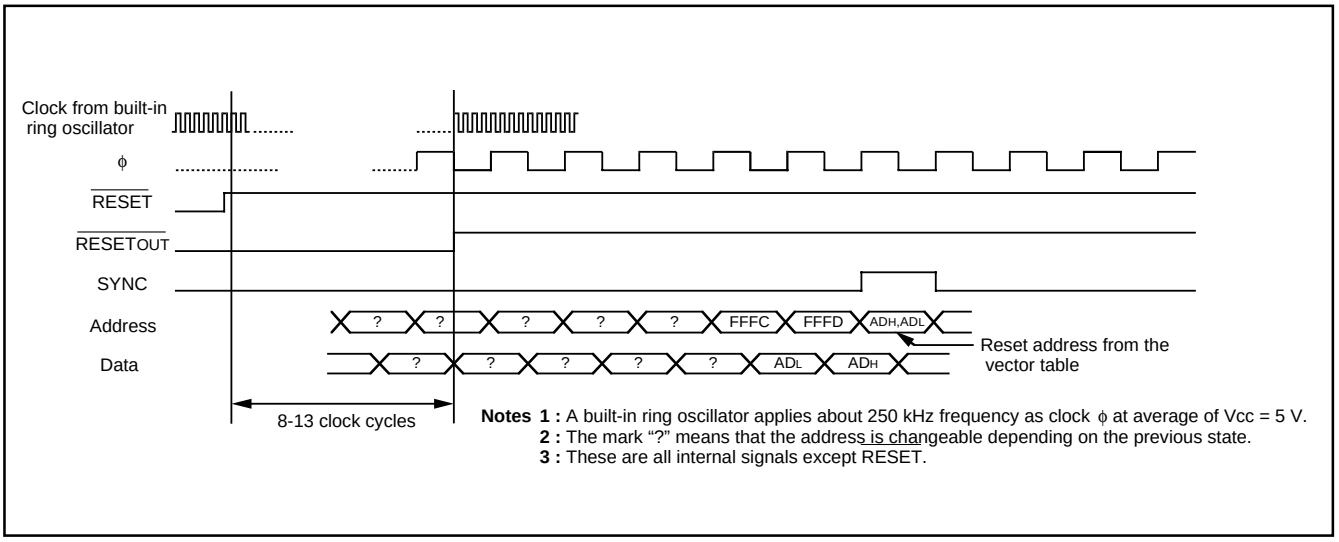


Fig. 36 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register	0001_{16}	00_{16}
(2) Port P1 direction register	0003_{16}	X X X 0 0 0 0 0
(3) Port P2 direction register	0005_{16}	00_{16}
(4) Port P3 direction register	0007_{16}	00_{16}
(5) Pull-up control register	0016_{16}	FF_{16}
(6) Port P1P3 control register	0017_{16}	00_{16}
(7) Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 1
(8) Serial I/O1 control register	$001A_{16}$	02_{16}
(9) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(10) Prescaler 12	0028_{16}	FF_{16}
(11) Timer 1	0029_{16}	01_{16}
(12) Timer 2	$002A_{16}$	00_{16}
(13) Timer X mode register	$002B_{16}$	00_{16}
(14) Prescaler X	$002C_{16}$	FF_{16}
(15) Timer X	$002D_{16}$	FF_{16}
(16) Timer count source set register	$002E_{16}$	00_{16}
(17) Serial I/O2 control register	0030_{16}	00_{16}
(18) A-D control register	0034_{16}	10_{16}
(19) MISRG	0038_{16}	00_{16}
(20) Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(21) Interrupt edge selection register	$003A_{16}$	00_{16}
(22) CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(23) Interrupt request register 1	$003C_{16}$	00_{16}
(24) Interrupt control register 1	$003E_{16}$	00_{16}
(25) Processor status register	(PS)	X X X X X 1 X X
(26) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

Note X : Undefined

Fig. 37 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT}, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip.

Set the constants of the resistor and capacitor when an RC oscillator is used, so that a frequency variation due to LSI variation and resistor and capacitor variations may not exceed the standard input frequency.

●Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock f stops at an "H" level and the X_{IN} oscillator stops. At this time, timer 1 is set to "01_{16}" and prescaler 12 is set to "FF_{16}" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 12 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(X_{IN})/16 is forcibly connected to the input of prescaler 12. When an external interrupt is accepted, oscillation is restarted but the internal clock f remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock f is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable.

• Wait mode

If the WIT instruction is executed, the internal clock f stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting clock which is X_{IN} divided by 16, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

●Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

The bit 5 can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.

●Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

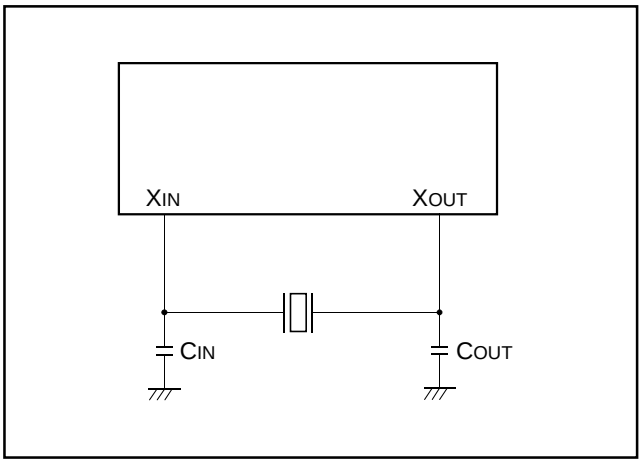


Fig. 38 External circuit of ceramic resonator

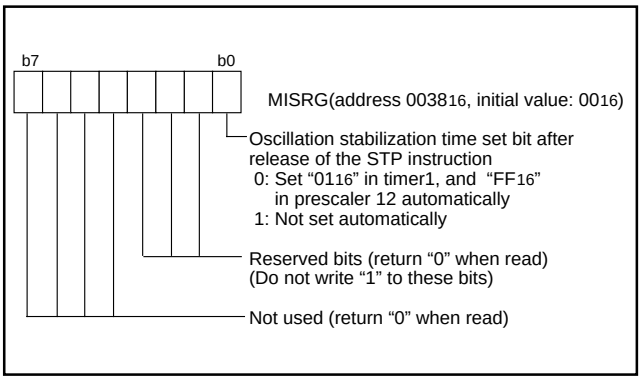


Fig. 41 Structure of MISRG

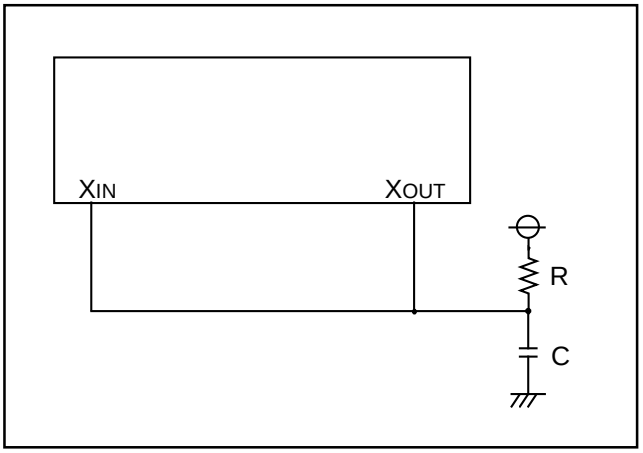


Fig. 39 External circuit of RC oscillation

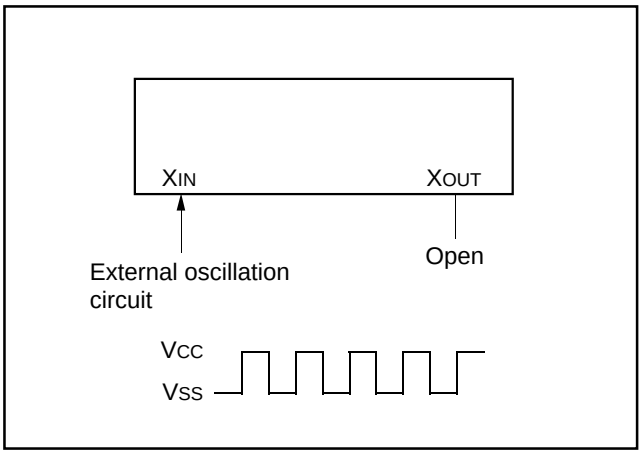


Fig. 40 External clock input circuit

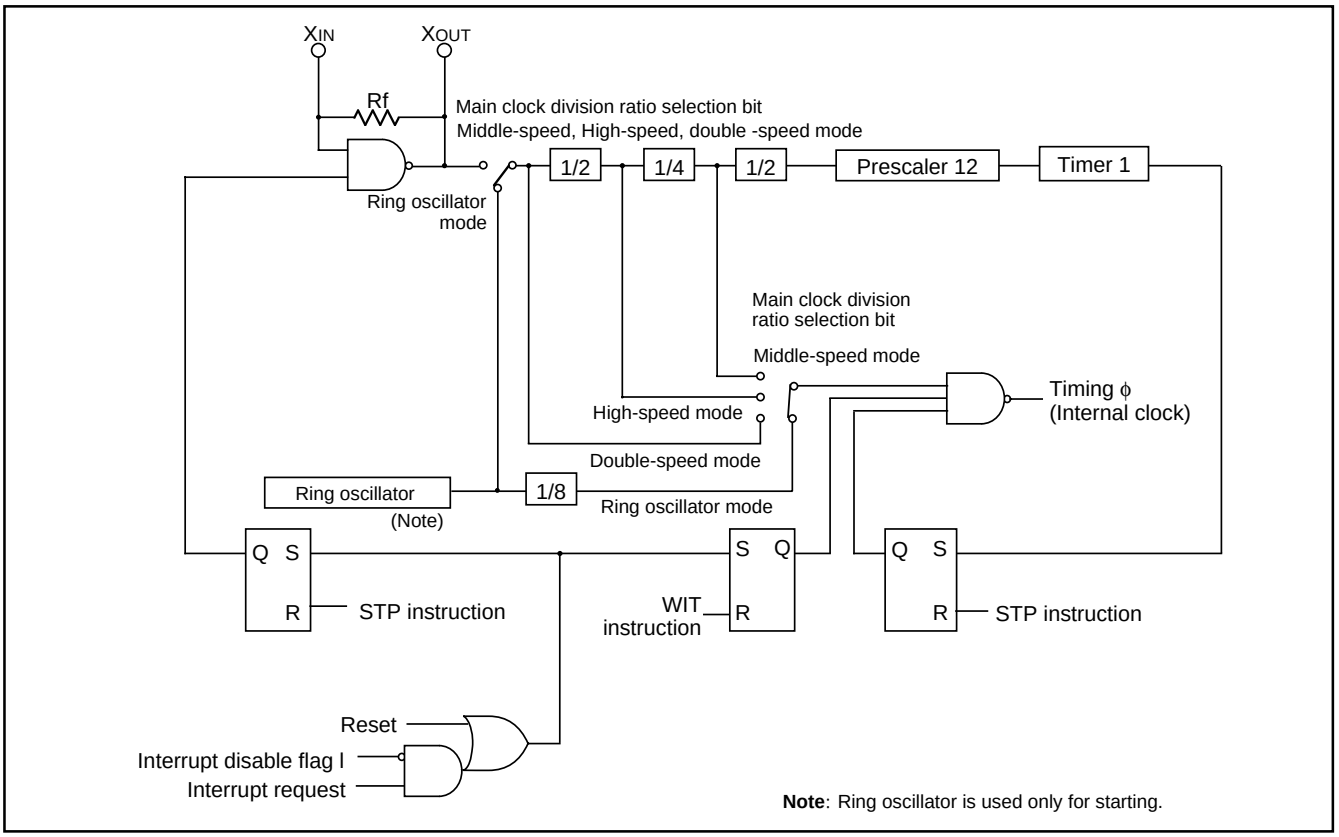


Fig. 42 Block diagram of internal clock generating circuit (for ceramic resonator)

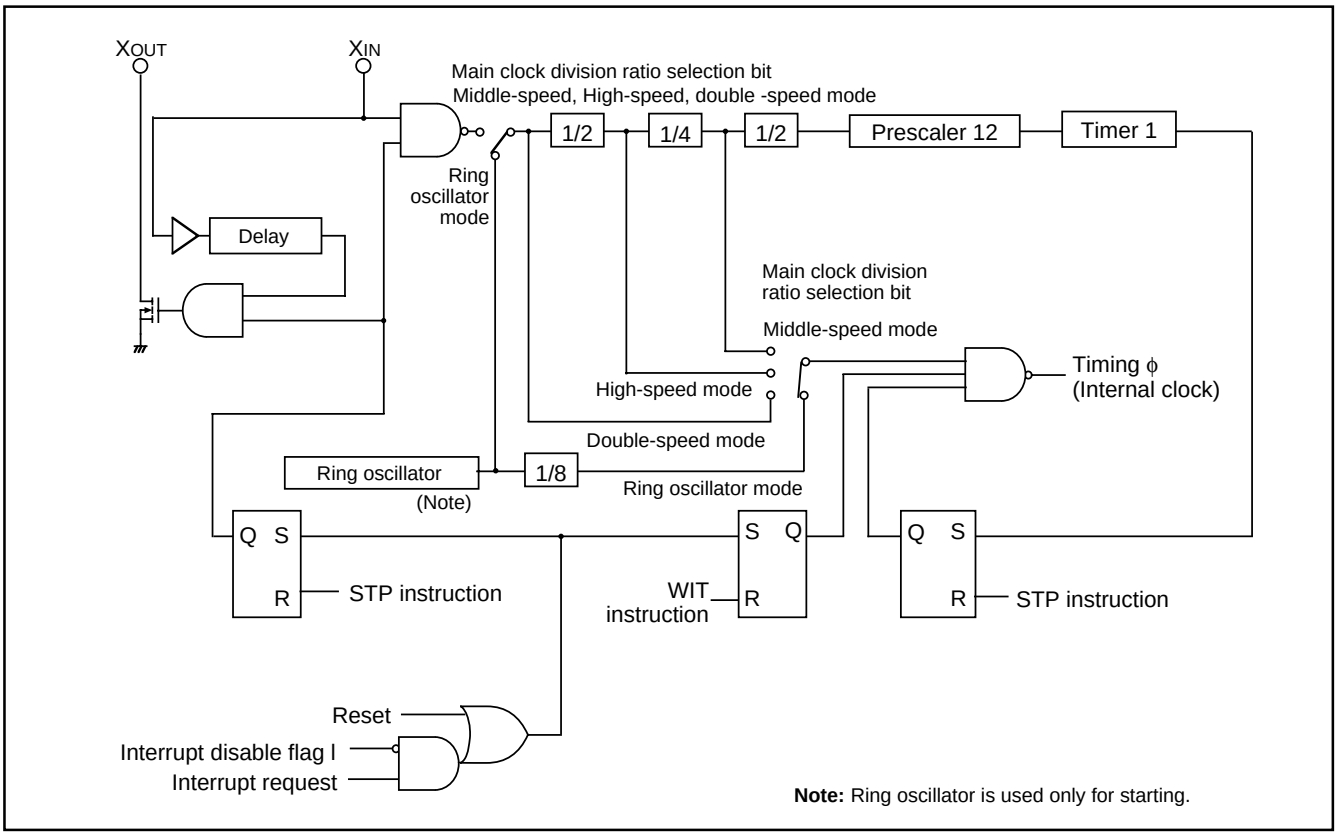


Fig. 43 Block diagram of internal clock generating circuit (for RC oscillation)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When a count source of timer X is switched, stop a count of timer X.

Ports

- The values of the port direction registers cannot be read.
  That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
  It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
  For setting direction registers, use the LDM instruction, STA instruction, etc.
- Set "1" to each bit 6 of the port P3 direction register and the port P3 register.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(X_{IN}) is 500kHz or more during A-D conversion.
Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.
When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF to 0.1 µF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form
(three identical copies)

DATA REQUIRED FOR ROM PROGRAMMING ORDERS

The following are necessary when ordering a ROM writing:

(1) ROM Programming Confirmation Form
(2) Mark Specification Form (for Special Mark)
(3) Data to be written to ROM, in EPROM form
(three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 7 Special programming adapter

Package	Name of Programming Adapter
32P4B	PCA7435SP
32P6B-A	PCA7435GP
36P2R-A	PCA7435FP

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 44 is recommended to verify programming.

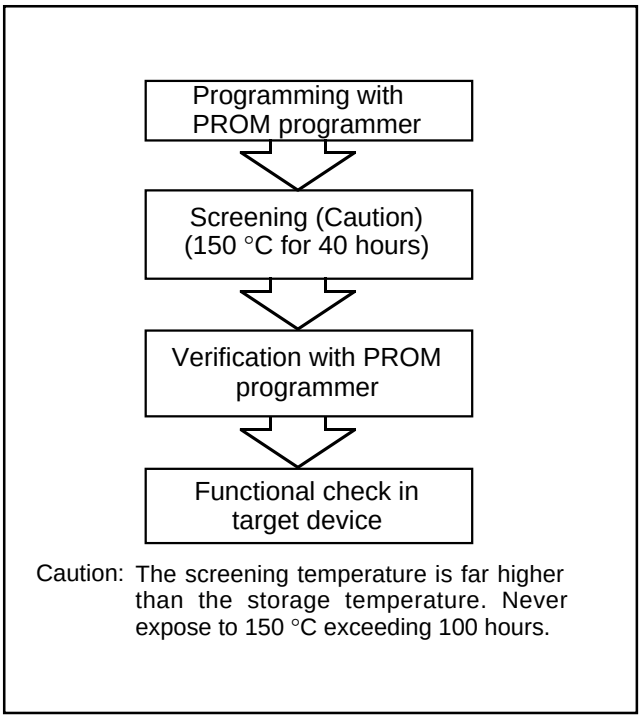


Fig. 44 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

(1) 7531 Group (General purpose)
Applied to: M37531M4-XXXFP/SP/GP, M37531M8-XXXFP/SP/GP, M37531E4FP/SP/GP, M37531E8FP/SP

Table 8 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Note 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6B package product.

Table 9 Recommended operating conditions (1)

(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	$f(X_{IN})$ = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (CR)	$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		0.3V_{CC}	V
V_{IL}	"L" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 10 Recommended operating conditions (2)

(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Table 11 Electrical characteristics

(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK}, S_{DATA} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current	High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"			5.0	8.0	mA
		High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V Output transistors "off"			0.5	1.5	mA
		Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"			5.0	8.0	mA
		Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"			2.0	5.0	mA
		f(X_{IN}) = 8 MHz (in WIT state) Functions except timers 1 and 2 stop Output transistors "off"			1.6	3.2	mA
		f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state) Output transistors "off"			0.2		mA
		Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD, S_{CLK}, S_{DATA}, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Table 12 A-D Converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	$t_{c(XIN)}$
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Table 13 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	15			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	80			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time	200			ns

Table 14 Timing requirements (2)

(V_{CC} = 2.2 to 5.5 V or 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	V_{CC} = 2.2 to 5.5 V	45			µs
		V_{CC} = 2.4 to 5.5 V	35			µs
$t_{C(XIN)}$	External clock input cycle time	V_{CC} = 2.2 to 5.5 V	500			ns
		V_{CC} = 2.4 to 5.5 V	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	V_{CC} = 2.2 to 5.5 V	1000			ns
		V_{CC} = 2.4 to 5.5 V	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	V_{CC} = 2.2 to 5.5 V	4000			ns
		V_{CC} = 2.4 to 5.5 V	2000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time		400			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time		400			ns

Table 15 Switching characteristics (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output “H” pulse width	tC(SCLK)/2–30			ns
tWL(SCLK)	Serial I/O2 clock output “L” pulse width	tC(SCLK)/2–30			ns
td(SCLK–SDATA)	Serial I/O2 output delay time			140	ns
tv(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			30	ns
tf(SCLK)	Serial I/O2 clock output falling time			30	ns
tr(CMOS)	CMOS output rising time (Note 1)		10	30	ns
tf(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 16 Switching characteristics (2)

(Vcc = 2.2 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output “H” pulse width	tC(SCLK)/2–50			ns
tWL(SCLK)	Serial I/O2 clock output “L” pulse width	tC(SCLK)/2–50			ns
td(SCLK–SDATA)	Serial I/O2 output delay time			350	ns
tv(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			50	ns
tf(SCLK)	Serial I/O2 clock output falling time			50	ns
tr(CMOS)	CMOS output rising time (Note 1)		20	50	ns
tf(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

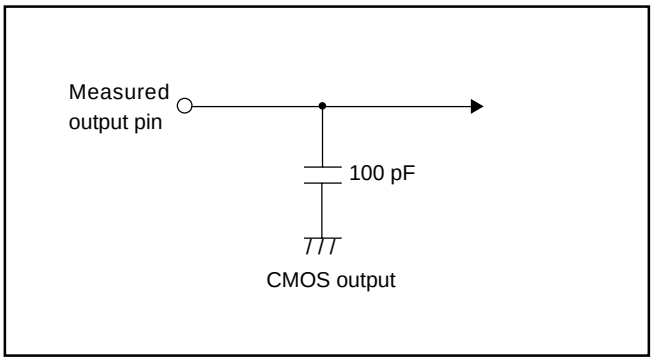


Fig. 45 Switching characteristics measurement circuit diagram (General purpose)

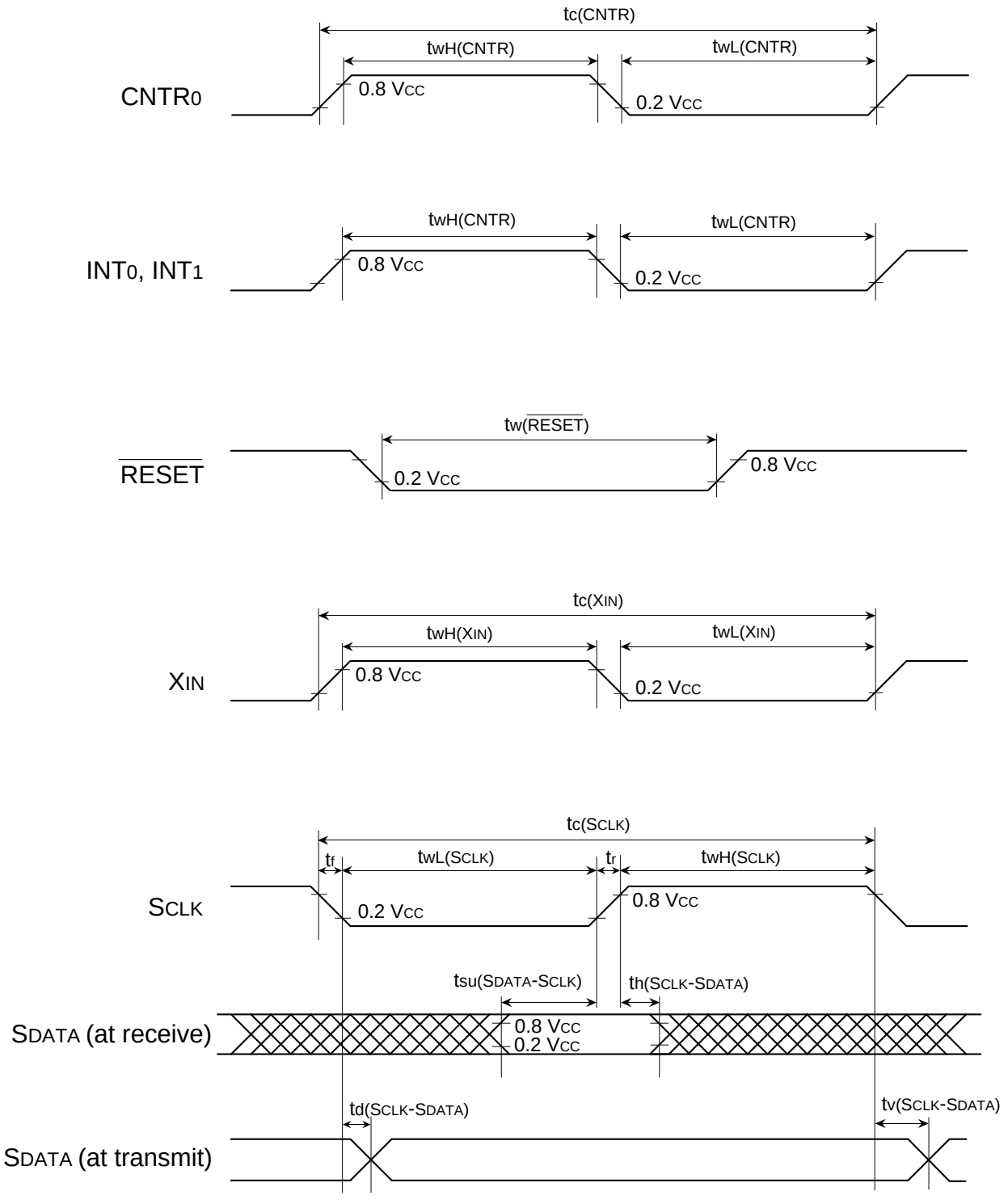


Fig. 46 Timing chart (General purpose)

(2) 7531 Group (Extended operating temperature version)
Applied to: M37531M4T-XXXFP/SP/GP, M37531E4T-XXXGP

Table 17 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature			–40 to 85	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6B package version.

Table 18 Recommended operating conditions (1)

(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\sum I_{OH(peak)}$	“H” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\sum I_{OH(avg)}$	“H” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\sum I_{OL(avg)}$	“L” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\sum I_{OL(avg)}$	“L” total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 19 Recommended operating conditions (2)

(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Table 20 Electrical characteristics

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.4 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 10 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, INT_1 (Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK}, S_{DATA} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current	High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"			5.0	8.0	mA
		High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V Output transistors "off"			0.5	1.5	mA
		Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"			5.0	8.0	mA
		Middle-speed mode, f(X_{IN}) = 8 MHz, Output transistors "off"			2.0	5.0	mA
		f(X_{IN}) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"			1.6	3.2	mA
		f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V (in WIT state) Output transistors "off"			0.2		mA
		Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Notes 1: $P1_1$ is measured when the $P1_1/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD, S_{CLK}, S_{DATA}, INT_0 and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Table 21 A-D Converter characteristics

(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	$t_{c(XIN)}$
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Table 22 Timing requirements (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	15			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0, INT_1 input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0, INT_1 input “L” pulse width	80			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time	200			ns

Table 23 Timing requirements (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	35			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0, INT_1 input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0, INT_1 input “L” pulse width	230			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time	400			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time	400			ns

Table 24 Switching characteristics (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK)}/2–30$			ns
$t_{WL(SCLK)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK)}/2–30$			ns
$t_{d(SCLK–SDATA)}$	Serial I/O2 output delay time			140	ns
$t_{v(SCLK–SDATA)}$	Serial I/O2 output valid time	0			ns
$t_{r(SCLK)}$	Serial I/O2 clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O2 clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 1)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin X_{OUT} is excluded.

Table 25 Switching characteristics (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK)}/2–50$			ns
$t_{WL(SCLK)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK)}/2–50$			ns
$t_{d(SCLK–SDATA)}$	Serial I/O2 output delay time			350	ns
$t_{v(SCLK–SDATA)}$	Serial I/O2 output valid time	0			ns
$t_{r(SCLK)}$	Serial I/O2 clock output rising time			50	ns
$t_{f(SCLK)}$	Serial I/O2 clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 1)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin X_{OUT} is excluded.

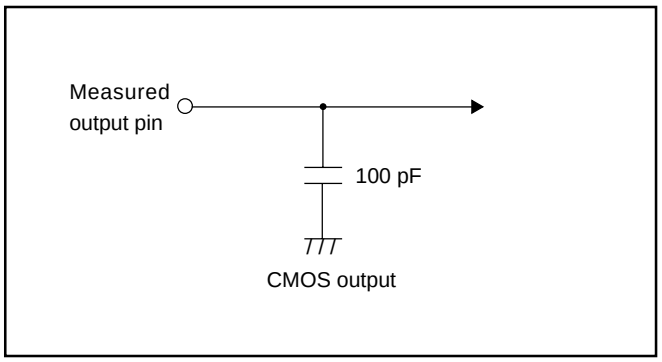


Fig. 47 Switching characteristics measurement circuit diagram
(Extended operating temperature version)

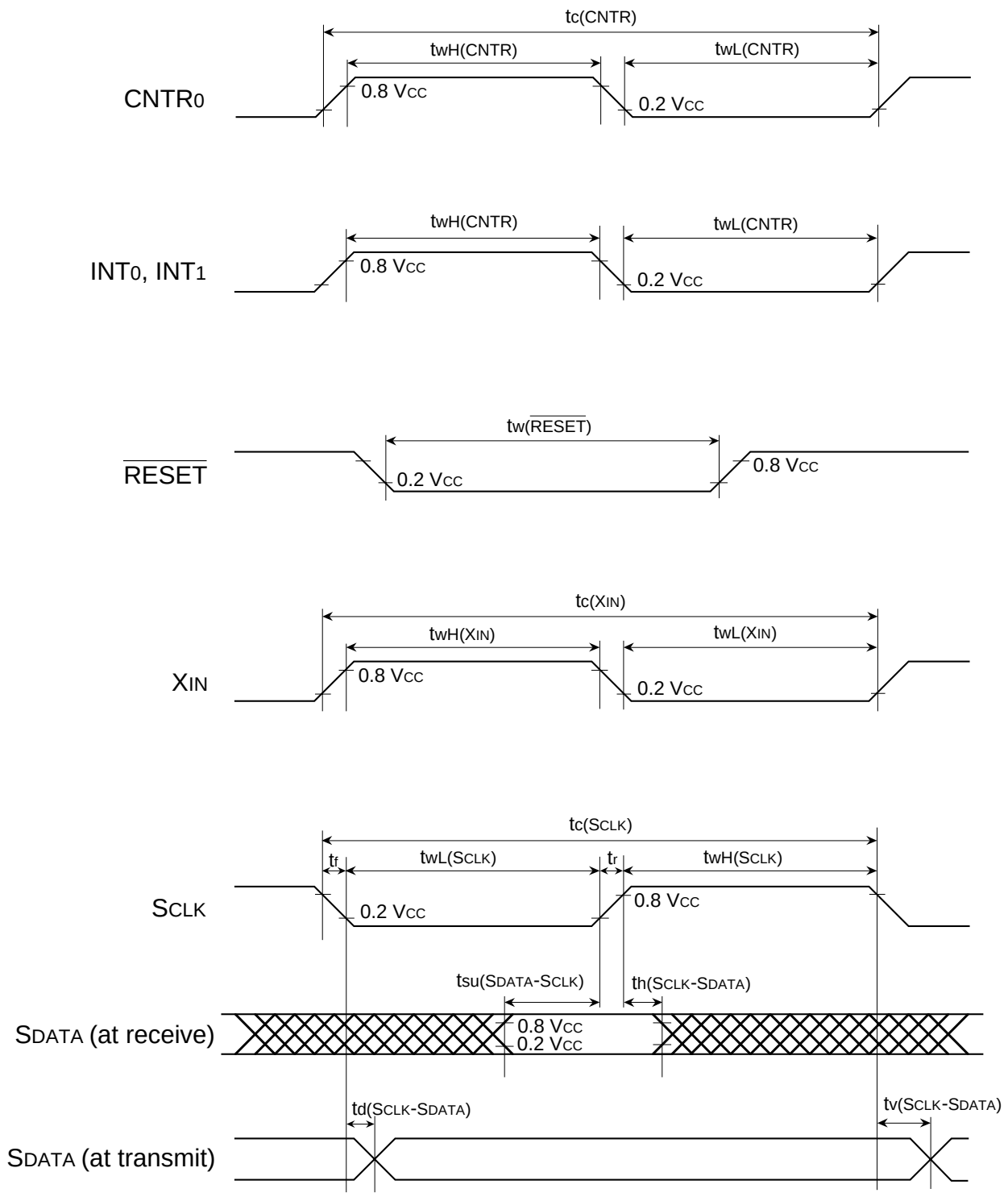


Fig. 48 Timing chart (Extended operating temperature version)

(3) 7531 Group (Extended operating temperature 125 °C version)
Applied to: M37531M4V-XXXGP, M37531E4V-XXXGP

Table 26 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	200	mW
T_{opr}	Operating temperature (Note 2)			–40 to 125	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: The total time is limited as follows:
6000 hours at 55 to 85 °C, 1000 hours at 85 to 125 °C

Table 27 Recommended operating conditions (1)

(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2)	$P3_0$–$P3_4$			60	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2)	$P3_0$–$P3_4$			30	mA

Note 1: Vcc = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 28 Recommended operating conditions (2)

(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_4$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_4$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Table 29 Electrical characteristics

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.4 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_4$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 10 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, (Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK}, S_{DATA} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current	High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"			5.0	8.0	mA
		High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V Output transistors "off"			0.5	1.5	mA
		Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"			5.0	8.0	mA
		Middle-speed mode, f(X_{IN}) = 8 MHz, Output transistors "off"			2.0	5.0	mA
		f(X_{IN}) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"			1.6	3.2	mA
		f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V (in WIT state) Output transistors "off"			0.2		mA
		Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
			Ta = 125 °C			50	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD, S_{CLK}, S_{DATA}, and INT_0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Table 30 A-D Converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	$t_{c(XIN)}$
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Table 31 Timing requirements (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	15			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0 input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0 input “L” pulse width	80			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time	200			ns

Table 32 Timing requirements (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	35			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, INT_0, input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, INT_0, input “L” pulse width	230			ns
$t_{C(SCLK)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SCLK–SDATA)}$	Serial I/O2 input set up time	400			ns
$t_{h(SCLK–SDATA)}$	Serial I/O2 input hold time	400			ns

Table 33 Switching characteristics (1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output “H” pulse width	tC(SCLK)/2–50			ns
tWL(SCLK)	Serial I/O2 clock output “L” pulse width	tC(SCLK)/2–50			ns
td(SCLK–SDATA)	Serial I/O2 output delay time			200	ns
tv(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			50	ns
tf(SCLK)	Serial I/O2 clock output falling time			50	ns
tr(CMOS)	CMOS output rising time (Note 1)		10	50	ns
tf(CMOS)	CMOS output falling time (Note 1)		10	50	ns

Note 1: Pin XOUT is excluded.

Table 34 Switching characteristics (2)

(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output “H” pulse width	tC(SCLK)/2–80			ns
tWL(SCLK)	Serial I/O2 clock output “L” pulse width	tC(SCLK)/2–80			ns
td(SCLK–SDATA)	Serial I/O2 output delay time			400	ns
tv(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			80	ns
tf(SCLK)	Serial I/O2 clock output falling time			80	ns
tr(CMOS)	CMOS output rising time (Note 1)		20	80	ns
tf(CMOS)	CMOS output falling time (Note 1)		20	80	ns

Note 1: Pin XOUT is excluded.

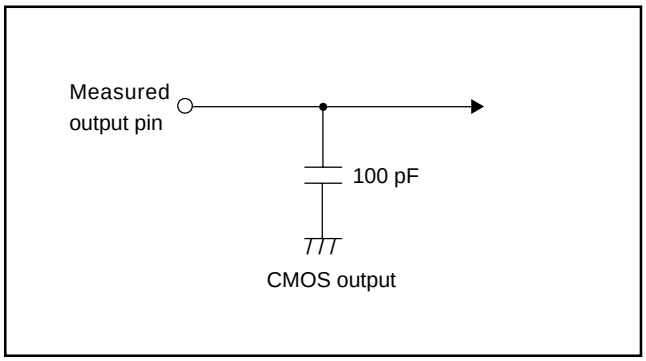


Fig. 49 Switching characteristics measurement circuit diagram
(Extended operating temperature 125 °C version)

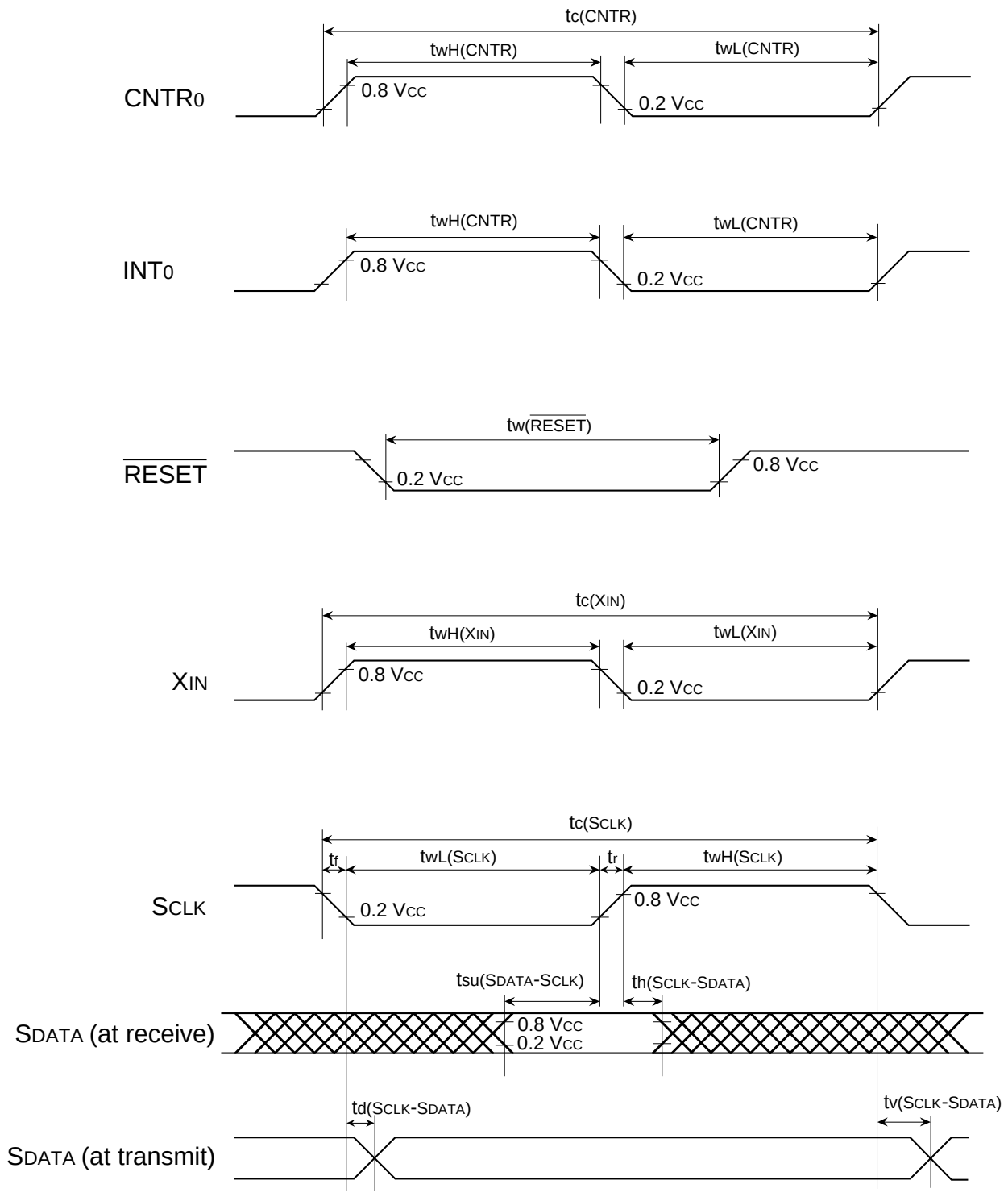


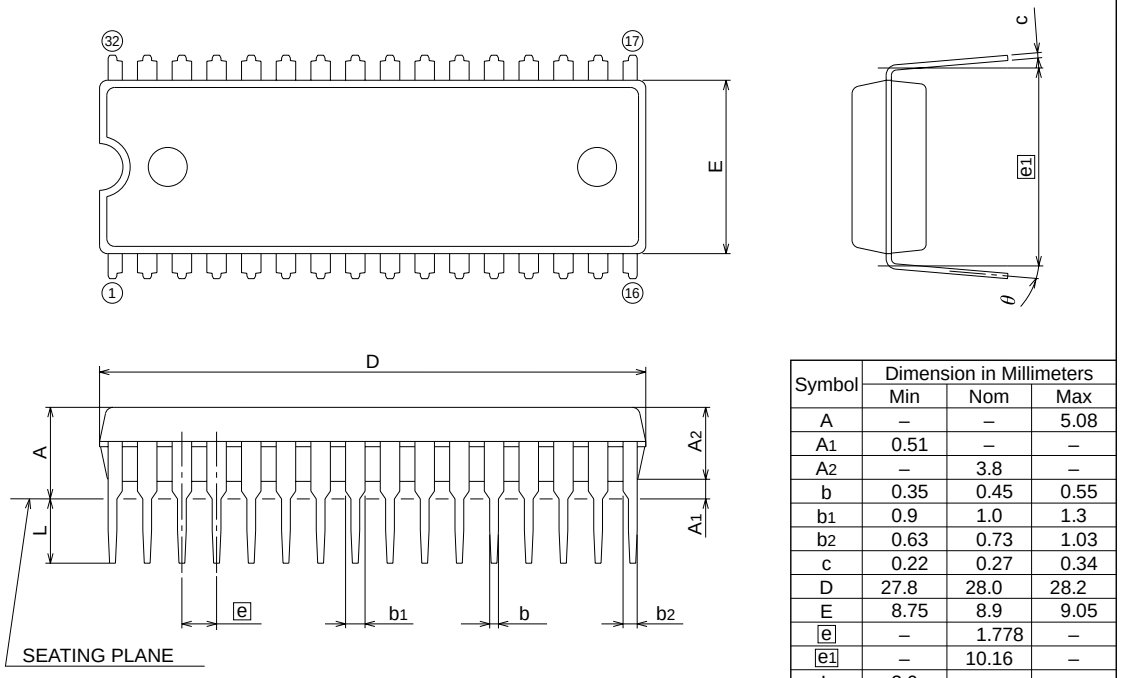
Fig. 50 Timing chart (Extended operating temperature 125 °C version)

PACKAGE OUTLINE

32P4B

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy

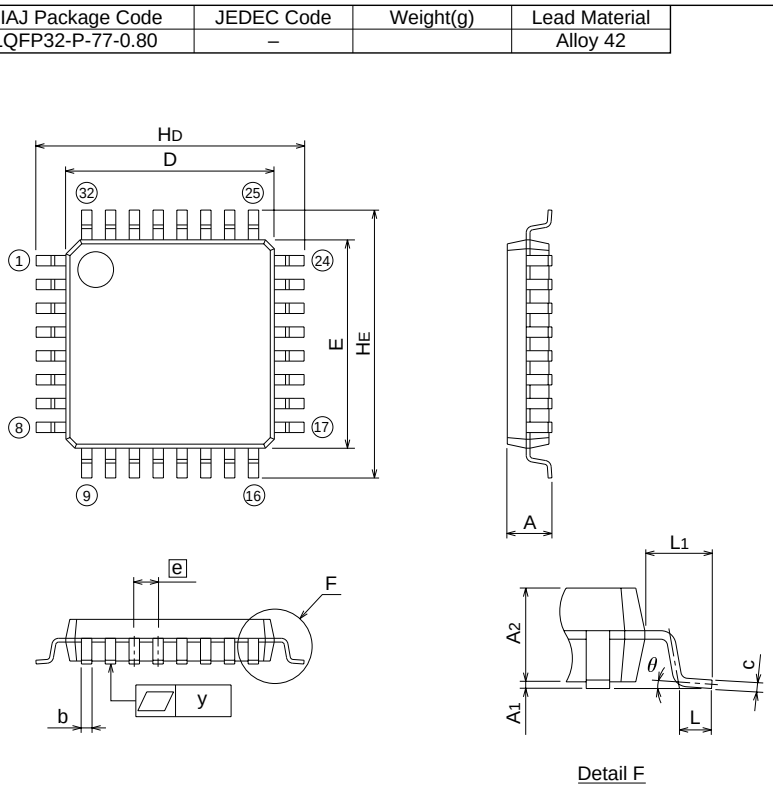


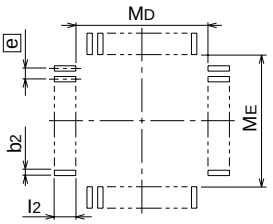
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

32P6B-A

Plastic 32pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-77-0.80	–		Alloy 42





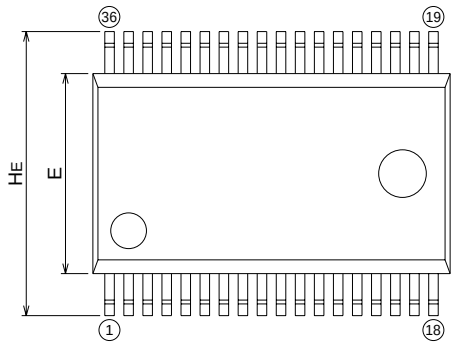
Recommended Mount Pad

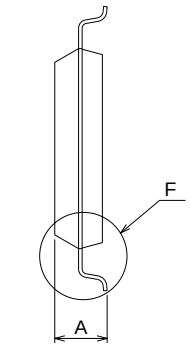
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

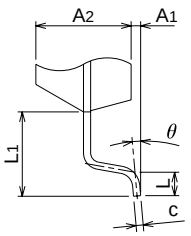
36P2R-A

Plastic 36pin 450mil SSOP

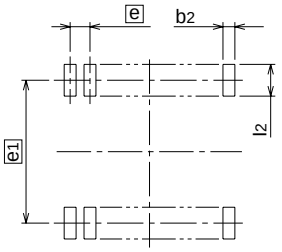
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	–	0.53	Alloy 42







Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
l_2	1.27	–	–

7531 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

New publication, effective Nov. 1999.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC

REVISION DESCRIPTION LIST	7531 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	970822
2.0	Page 1; FEATURES In Programmable I/O ports, the pin number of 32-pin version is added. In Power source voltage, two conditions are added and two are revised. Page 8; Central Processing Unit (CPU) The name of manual, 740 Family Software Manual, is revised. Fig. 11; Note is added. Page 11; [Direction registers] PiD The sentences are revised: Pins set to input are floating, and permit reading pin values. Fig. 12; Bit function and the initial value are added. Fig. 13; The figure name is revised: port P1P3 control register. Page 15; Interrupt operation The order of No. 3 and 4 is revised. Fig. 17; Four bit names are revised: Serial I/O1. Page 21; [Serial I/O1 status register] SIO1STS Explanations are partly revised. Fig. 25; Bits 6 and 7 explanations of serial I/O1 control register are revised. Page 23; [Serial I/O2 control register] SIO2CON Explanations are partly revised. Fig. 26; Bit 3 explanations are revised. Note is partly revised. Page 27; Reset Circuit Explanations are partly revised: In the case of f(f)... Fig. 35; The waveform of clock from built-in ring oscillator is revised. Note 1 is revised. Fig. 36; (6) Port P1P3 control register is added. Page 32; A-D Converter Explanations are partly revised: The WIT instruction is eliminated. Page 33; DATA REQUIRED FOR ROM PROGRAMMING ORDERS This clause is added. Table 7; Characteristics of Vcc is revised. Table 8; Characteristics of f(X_{IN}) is revised. Table 9; Characteristics of Icc is revised. Table 12; Characteristics of $t_{C}(X_{IN})$, $t_{WH}(X_{IN})$, $t_{WL}(X_{IN})$, t_{C}(CNTR), t_{WH}(CNTR), t_{WL}(CNTR), $t_{C}(S_{CLK})$, $t_{WH}(S_{CLK})$ and $t_{WL}(S_{CLK})$ are revised. Pages 42 to 45; MASK ROM CONFIRMATION FORM These are added. Pages 46 and 47; ROM PROGRAMMING CONFIRMATION FORM These are added.	980220

REVISION DESCRIPTION LIST	7531 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
2.0	Pages 48 to 51; MARK SPECIFICATION FORM These are added. Pages 52 and 53; PACKAGE OUTLINE These are added.	980220
2.1	Pages 37, 46, 47; Some words are corrected. Pages 42 to 47; The numbers of Mask ROM and ROM Programming Confirmation Forms are revised. Page 49; 32P6B Mark Specification Form is revised.	980702
3.0	All pages; “PRELIMINARY Notice: This is ... ” eliminated. All register structures; Initial values are added. Page 1; Explanations are partly revised. Page 1 and 2; Product names are added into the pin configurations. Page 3; Pin configuration of 42S1M is added. Page 8; Explanations of Figure 8 and Table 2 are partly revised. Page 9; Explanations of Figures 9 and 10 are partly revised. Page 11; The register name (Timer count souce set register) is revised. Page 16; Table 4; The contents of “Remarks” is partly revised. Page 20; Explanation is revised. Page 21; The some word is added. Page 24; The some word is added. Explanation is revised. Page 26; Explanation is added. Page 27; Figure 34; Explanation is revised. Page 28; Period is added. Page 32; Figure titles of Figures 42 and 43 are revised. Page 33; Explanation is revised. Page 36 to 59; “ELECTRICAL CHARACTERISTICS” are all revised. “ELECTRICAL CHARACTERISTICS” of Extended operating temperature version is added. “ELECTRICAL CHARACTERISTICS” of Extended operating temperature 125 °C version is added. Page 60 to 71; “MASK ROM CONFIRMATION FORM” and “ROM PROGRAMMING CONFIRMATION FORM” are all revised. “SHRINK DIP MARK SPECIFICATION FORM” eliminated.	990212
4.0	Most of the contents (Functional Description, Electrical characteristics, and so on) are updated.	991115

REVISION DESCRIPTION LIST	7531 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
4.1	Page 1: Power dissipation to 25 mW Operating temperature range; **Note** deleted Page 8: Fig. 8 “Under development” revised Page 10: Fig.11 Start address of Interrupt vector area to FFEC16 Page 25: Fig.29 Note revised Page 28: Description revised; $\overline{\text{RESET}}$ “L” pulse width 2 μs → 15 μs Page 32: Fig.42 Rd resistor connected to XOUT pin eliminated Page 39: Table 12 Absolute accuracy (excluding quantization error) → Linearity error Page 40: Table 13 tw($\overline{\text{RESET}}$) revised; 2 μs → 15 μs Table 14 tw($\overline{\text{RESET}}$) revised; 2 μs → 45 μs at VCC = 2.2 to 5.5 V, 35 μs at VCC = 2.4 to 5.5 V Page 47: Table 21 Absolute accuracy (excluding quantization error) → Linearity error Page 48: Table 22 tw($\overline{\text{RESET}}$) revised; 2 μs → 15 μs Table 23 tw($\overline{\text{RESET}}$) revised; 2 μs → 35 μs Page 55: Table 30 Absolute accuracy (excluding quantization error) → Linearity error Page 56: Table 31 tw($\overline{\text{RESET}}$) revised; 2 μs → 15 μs Table 32 tw($\overline{\text{RESET}}$) revised; 2 μs → 35 μs	000615