CMOS 4-Bit Microcontroller

TMP47P443VN TMP47P443VM TMP47P443VDM

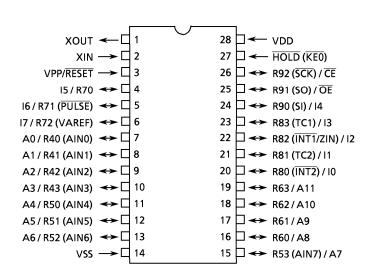
The TMP47P443V is the system evaluation LSI of TMP47C243/443 with a 32 Kbit one-time PROM. The TMP47P443V programs / verifies using an adapter socket to connect with PROM programmer, as it is in

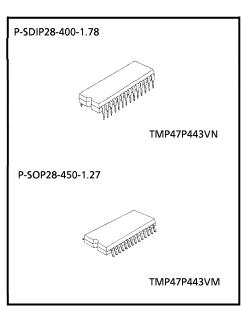
In addition, the TMP47P443V and the TMP47C243/443 are pin compatible. The TMP47P443V operates as the same as the TMP47C243/443 by programming to the internal PROM.

Part No.	ROM	RAM	Rackage	Adapter Socket
TMP47P443VN	OTP		P-SDIP28-400-1.78	BM11100
TMP47P443VM	•	256 × 4-bit	P-SOP28-450-1.27	BM11101
TMP47P443VDM	4096 × 8-bit		P-SSOP30-56-0.65	BM11115

Pin Assignment (Top View)

P-SDIP28-400-1.78 / P-SOP28-450-1.27





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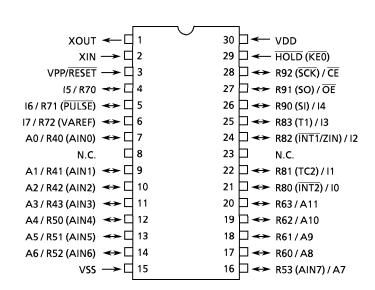
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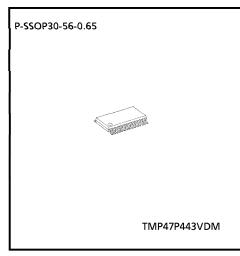
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Pin Assignment (Top View)

P-SSOP30-56-0.65





Pin Function

The TMP47P443V has MCU mode and PROM mode.

(1) MCU mode The TMP47C243/443 and the TMP47P443V are pin compatible.

(2) PROM mode

Pin Name	Input / Output	Functions	Pin Name (MCU mode)
A11 to A8			R63 to R60
A7 to A4	Input	Address inputs	R53 to R50
A3 to A0			R43 to R40
17 to 15			R72 to R70
14	I/O	Data inputs / outputs	R90
13 to 10			R83 to R80
CE	Input	Chip Enable input	R92
ŌĒ		Output Enable input	R91
VPP		+ 12.5 V / 5 V (Program supply voltage)	RESET
vcc	Power supply	+ 5 V	VDD
VSS		0 V	VSS
HOLD	Input	PROM mode setting pin. Be fixed to low level.	
XIN	Input	Input the clock from the external oscillator. (6 MHz typ.)	
XOUT	Input	Be pulled down to VSS level. (750 Ω typ.)	

Operational Description

The following is an explanation of hardware configuration and operation in relation to the TMP47P443V. The TMP47P443V is the same as the TMP47C243/443 except that an OTP is used instead of a built-in mask ROM.

1. Operation mode

The TMP47P443V has a MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by attaching a resonator between the XIN and Xout pins. Operation in the MCU mode is the same as for the TMP47C243/443. In the TMP47P443V, RC oscillation is impossible.

1.1.1 Program Memory

The program storage area is the same as for the TMP47C443. Data conversion tables must be set in two locations when using the TMP47P443V to check TMP47C243 operation.

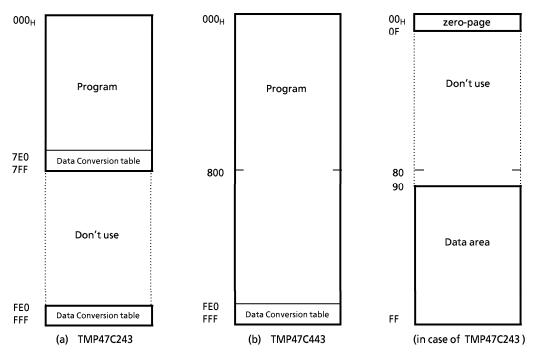


Figure 1-1. Program area (ROM)

Figure 1-2. RAM addressing

1.1.2 Data Memory

The TMP47P443V has 256×4 -bit of data memory (RAM). When the TMP47P443V is used as the TMP47C243 evaluator, programming should be performed assuming that the RAM is assigned to address 00 to 0F_H and 90 to FF_H as show in Figure 1-2. When the BM47C443 (emulator) is used as the TMP47C243 evaluator, it is same.

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Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins		Ratings	Unit
Supply Voltage	V_{DD}			– 0.3 to 6.5	V
Program Voltage	V_{PP}	RESET / VPP pin		– 0.3 to 13.0	V
Input Voltage	V_{IN}			- 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT}			– 0.3 to V _{DD} + 0.3	V
Output Current (Par 1 nin)	I _{OUT1}	Port R5, R6	30	mA	
Output Current (Per 1 pin)	I _{OUT2}	Port R4, R7, R8, R9	3.2		
Output Current (Total)	Σ I _{OUT}	Port R4, R5, R6, R7, R8, R9		120	mΑ
			DIP	300	
Power Dissipation [Topr = 70°C]	PD		SOP	180	mW
			SSOP	145	
Soldering Temperature (time)	Tsld			260 (10 s)	°C
Storage Temperature	Tstg		•	– 55 to 125	°C
Operating Temperature	Topr		•	– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions $| (V_{SS} = 0)|$

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			fc = 8.0 MHz	2.7		
Supply Voltage	V_{DD}		fc = 4.2 MHz	2.2	5.5	V
			In the HOLD mode	2.0		
	V_{IH1}	Except Hysteresis Input	In the normal	$V_{DD} \times 0.7$		
· · ·	V_{IH2}	Hysteresis Input	operating area	$V_{DD} \times 0.75$	V_{DD}	V
	V _{IH3}		In the HOLD mode	$V_{DD} \times 0.9$		
	V_{IL1}	Except Hysteresis Input	In the normal		$V_{DD} \times 0.3$	
Input Low Voltage	V_{IL2}	Hysteresis Input	operating area	0	$V_{DD} \times 0.25$	V
	V _{IL3}		In the HOLD mode		$V_{DD} \times 0.1$	
Clash Fasanianan	fc	XIN, XOUT	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	0.4	8.0	N/ILI-
Clock Frequency	10	AIN, AUUT	$V_{DD} = 2.2 \text{ to } 5.5 \text{ V}$	0.4	4.2	MHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{SS} = 0 \

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis Input		_	0.7	_	V
	I _{IN1}	RESET, HOLD					
Input Current	I _{IN2}	Open drain output ports	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V} / 0 \text{ V}$	_	-	± 2	μA
Input Resistance	R _{IN}	RESET		100	220	450	kΩ
Output Leakage Current	I _{LO}	Open drain output ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	-	-	2	μΑ
Output Low			$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	-	0.4	
Voltage	V _{OL}	Port R4, R7, R8, R9	$V_{DD} = 2.2 \text{ V}, \ I_{OL} = 20 \ \mu\text{A}$	_	_	0.1	V
Output Low Current	I _{OL1}	Port R5, R6	V _{DD} = 4.5 V, V _{OL} = 1.0 V	7	20	_	mA
Supply Current			$V_{DD} = 5.5 \text{ V}, \text{ fc} = 4 \text{ MHz}$	_	2	4	
(in the Normal	I _{DD}		$V_{DD} = 3.0 \text{ V}, \text{ fc} = 4 \text{ MHz}$	-	1	2	mA
operating mode)			V _{DD} = 3.0 V, fc = 400 kHz	_	0.5	1	
Supply Current (in the HOLD operating mode)	I _{DDH}		V _{DD} = 5.5 V	_	0.5	10	μΑ

Note 1: Typ. values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current l_{IN1} : The current through resistor is not included. Note 3: Supply Current: The analog supply current (l_{REF}) is not included.

Note 4: Supply Current: $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V} (V_{DD} = 5.5 \text{ V}), 2.8 \text{ V} / 0.2 \text{ V} (V_{DD} = 3.0 \text{ V})$

AD Conversion Characteristics

 $(Topr = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		V _{DD} – 1.5	_	V _{DD}	V
Analog Reference Voltage Range	ΔV_{AREF}	V _{AREF} - V _{SS}	2.7	_	_	V
Analog Input Voltage	V _{AIN}		V _{SS}	_	V _{DD}	V
Analog Supply current	I _{REF}		_	0.5	1.0	mA
Nonlinearity Error			_	_	± 1	
Zero Point Error		$V_{DD} = 2.7 \text{ to } 5.5 \text{ V},$	_	_	± 1	LSB
Full Scale Error		$V_{AREF} = V_{DD} \pm 0.001 V$	_	_	± 1	LJB
Total Error		$V_{SS} = \pm 0.001 \text{ V}$	_	_	± 2	

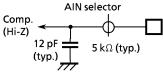
AC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Со	nditions	Min	Тур.	Max	Unit			
			$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$	1.0						
Instruction Cycle Time	tcy		V _{DD} = 2.2 to 5.5 V	1.9	_	20	μ S			
			V _{DD} ≧ 2.7 V	60						
High level clock pulse width	t _{WCH}	For external	V _{DD} <2.7 V	120	_	_				
		clock (XIN input)	V _{DD} ≧ 2.7 V	60			ns			
Low level clock pulse width	t _{WCL}	t _{WCL}	t_{WCL}	(XIII III pasy	(**************************************	V _{DD} <2.7 V	120			
AD Conversion Time	t _{ADC}		•	-	24 tcy	_	μ \$			
AD Sampling Time	t _{AIN}			-	2 tcy	_	μ3			
Shift data Hold Time	t _{SDH}			0.5 tcy – 0.3	_	_	μ S			

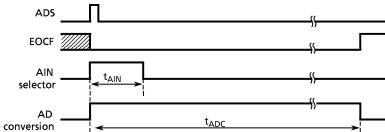
Note 1: AD conversion timing:

Internal circuit for pins AINO to 7



Electrical change inust be loaded into the buit-in condensen during t_{AIN} for normal AD conversion.

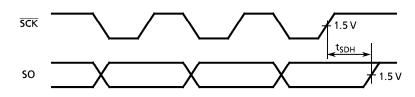
AD conversion timing



Note 2: Shift data Hold Time: External circuit for pins

SCK and SO o VDD 10 $k\Omega$ 50 pF





Zero-Cross Detection Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Characteristics are equivalent to the TMP47C243/443's.

Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.2 \text{ to } 5.5 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$

Recommended oscillating conditions of the TMP47P443V are equal to the TMP47C243/443's but RC oscillation is impossible.

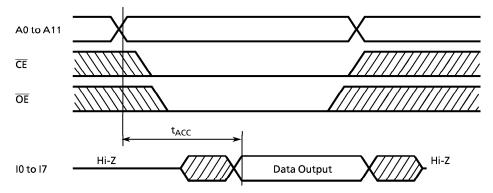
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DC/AC Characteristics

 $(V_{SS} = 0 V)$

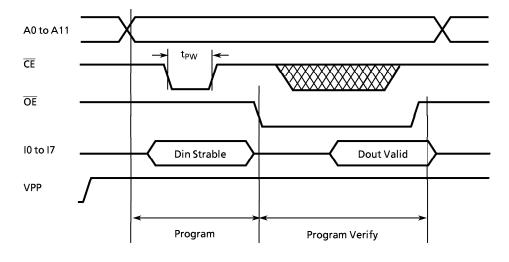
(1) Read Operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Output Level High Voltage	V _{IH4}		V _{CC} × 0.7	-	V _{CC}	٧
Output Level Low Voltage	V _{IL4}		0	_	V _{CC} × 0.3	V
Supply Voltage	V _{CC}		4.75		6.0	V
Programming Voltage	V _{PP}		4.75	-	6.0	v
Address Access Time	t _{ACC}	$V_{CC} = 5.0 \pm 0.25 \text{ V}$	0	-	350	ns



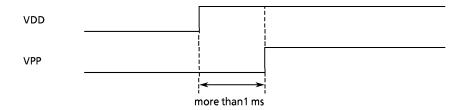
(2) High Speed Programming Operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Input High Voltage	V _{IH4}		V _{CC} × 0.7	-	V _{CC}	V
Input Low Voltage	V _{IL4}		0	_	V _{CC} × 0.3	V
Supply Voltage	V _{CC}		4.75	-	6.0	V
V _{PP} Power Supply Voltage	V _{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t _{PW}	V _{CC} = 6.0 ± 0.25 V	0.95	1.0	1.05	ms



Note: There are some PROM programmer types which cannot program OTP.

In TMP47P443V, VPP pin is also used as RESET pin. To set a mode, REST/VPP pin must be set to "low" during 1 ms and more after the rising of power-on and the rising of VDD electrical power.



Recommended EPROM programmer

TYPE

R4945 (ADVANTEST) UNISITE (DATA I/O) AF – 9706 (ANDO) PECKER – 11 (AVAL DATA)