

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT32P, TC74ACT32F, TC74ACT32FN, TC74ACT32FT

QUAD 2-INPUT OR GATE

The TC74ACT32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

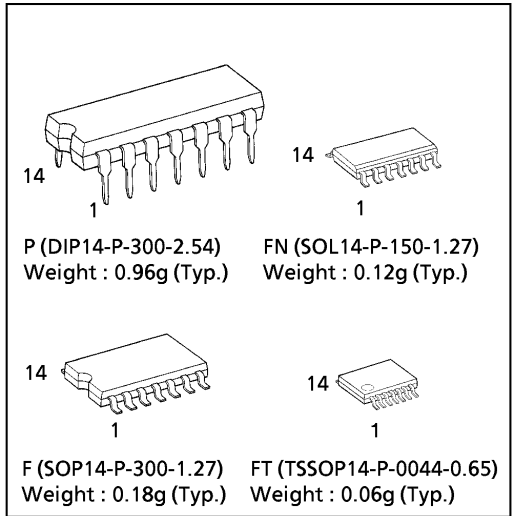
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

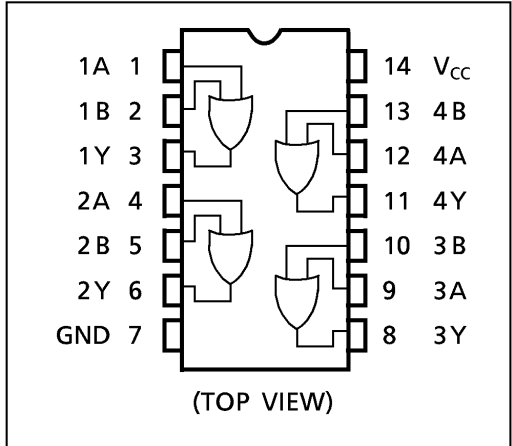
FEATURES :

- High Speed..... $t_{pd} = 4.5ns(\text{typ.})$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A(\text{Max.})$ at $T_a = 25^\circ C$
- Compatible with TTL outputs.... $V_{IL} = 0.8V(\text{Max.})$
 $V_{IH} = 2.0V(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24mA(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F32

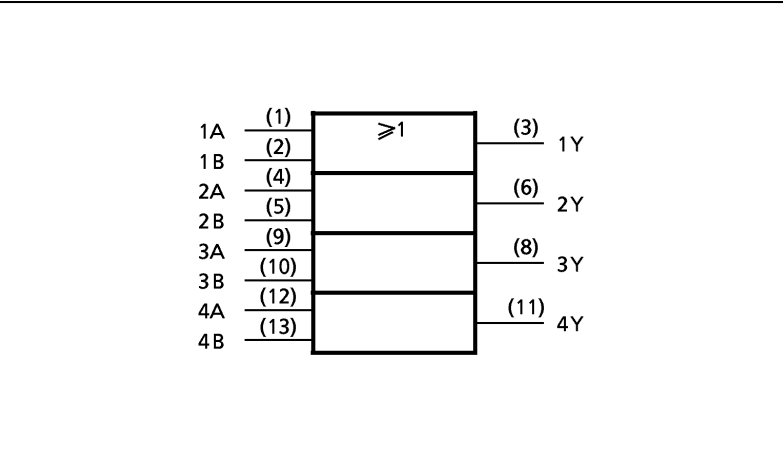
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±50	mA
DC Output Current	I _{OUT}	±50	mA
DC V _{CC} /Ground Current	I _{CC}	±100	mA
Power Dissipation	P _D	500 (DIP)* /180 (SOP/TSSOP)	mW
Storage Temperature	T _{stg}	-65~150	°C

*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	4.5~5.5	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		4.5 } 5.5	2.0	-	-	2.0	-	V	
Low - Level Input Voltage	V _{IL}		4.5 } 5.5	-	-	0.8	-	0.8	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.4	4.5	-	4.4	-	V
			I _{OH} = -24mA	4.5	3.94	-	-	3.80	-	
			I _{OH} = -75mA*	5.5	-	-	-	3.85	-	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IL}	I _{OL} = 50μA	4.5	-	0.0	0.1	-	0.1	V
			I _{OL} = 24mA	4.5	-	-	0.36	-	0.44	
			I _{OL} = 75mA*	5.5	-	-	-	-	1.65	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	-	-	±0.1	-	±1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	-	-	4.0	-	40.0		
	I _C	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND	5.5	-	-	1.35	-	1.5	mA	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.2	7.9	1.0	9.0	ns
Input Capacitance	C _{IN}		—	5	10	—	10		pF
Power Dissipation Capacitance	C _{PD} (1)		—	22	—	—	—		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

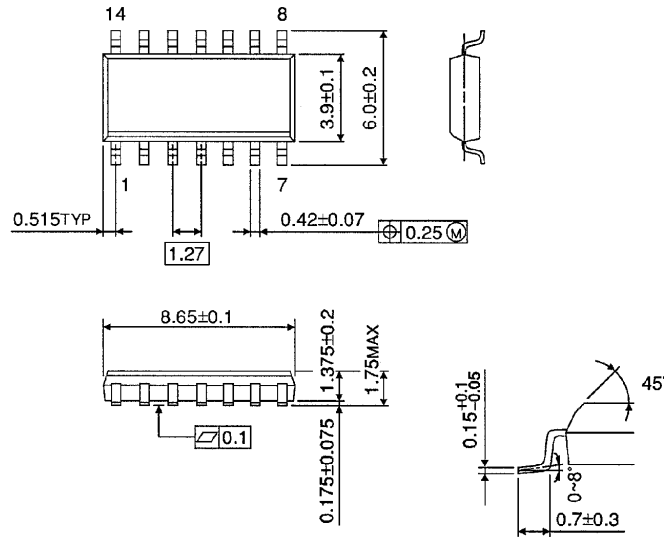
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

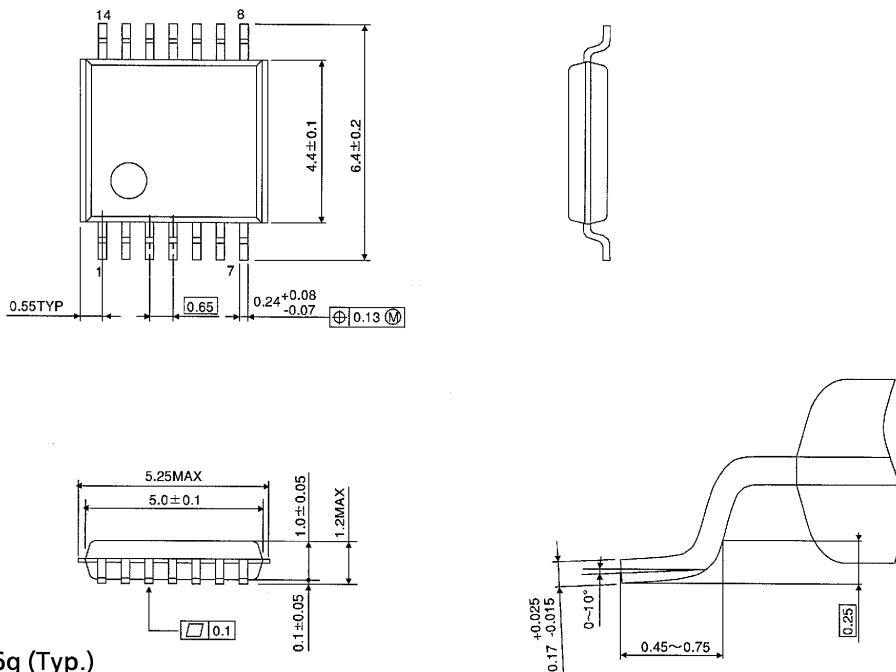
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) OUTLINE DRAWING (TSSOP14-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)