DS05-11407-3E

MEMORY

CMOS

2 × 512 K × 16 BIT / 2 × 256 K × 32 BIT SINGLE DATA RATE I/F FCRAM™

Consumer/Embedded Application Specific Memory for SiP

MB81ES171625/173225-12/-15

■ DESCRIPTION

The Fujitsu MB81ES171625/173225 is a Fast Cycle Random Access Memory (FCRAM*) containing 16,777,216 bit memory cells accessible in a 2×512K×16 bit / 2×256K×32 bit format. The MB81ES171625/173225 features a fully synchronous operation referenced to a positive edge clock same as that of SDRAM operation, whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB81ES171625/173225 is utilized using a Fujitsu advanced FCRAM core technology and designed for low power consumption and low voltage operation than regular synchronous DRAM (SDRAM).

The MB81ES171625/173225 is dedicated for SiP (System in a Package), and ideally suited for various embedded/consumer applications including digital AVs, and image processing where a large band width and low power consumption memory is needed.

* : FCRAM is a trademark of Fujitsu Limited, Japan.

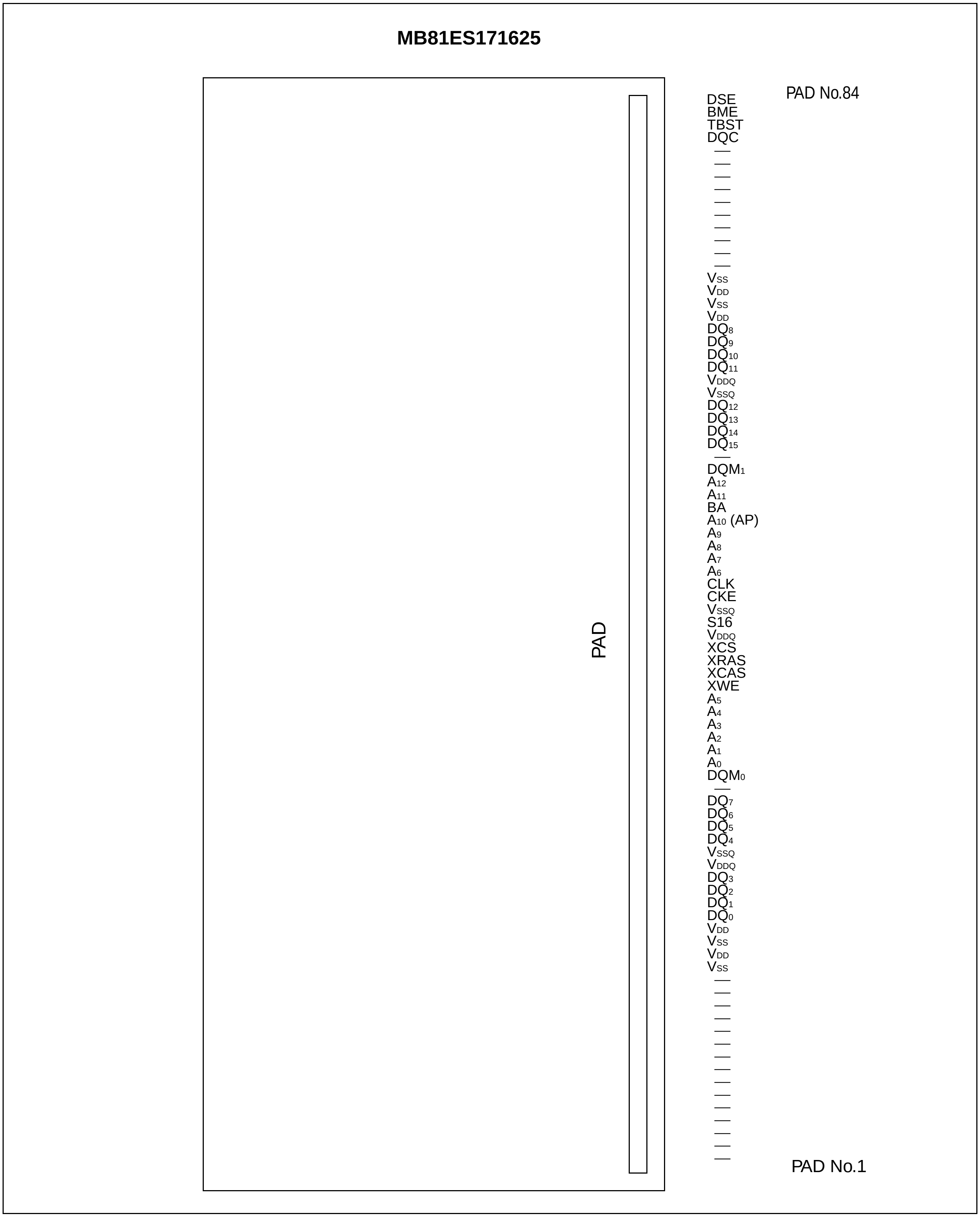
■ PRODUCT LINEUP

Parameter		MB81ES171625/173225	
		-12	-15
Clock Frequency (Max)		85 MHz	66.7 MHz
Burst Mode Cycle Time (Min)	CL = 1	23.4 ns	30 ns
	CL = 2	11.7 ns	15 ns
Access Time From Clock (Max)	CL = 1	21.9 ns	27 ns
	CL = 2	10.2 ns	12 ns
XRAS Cycle Time (Min)		75 ns	75 ns
Operating Current (Max) (I_{DD1})		30 mA	30 mA
Power Down Mode Current (Max) (I_{DD2P})		1 mA	1 mA
Self-refresh Current (Max) (I_{DD6})		5 mA	5 mA

■ FEATURES

- FCRAM core with Single Data Rate SDRAM interface
- 512 K word × 16 bit × 2 bank or 256 K word × 32 bit × 2 bank organization
- Single +1.8 V Supply ±0.15 V tolerance
- CMOS I/O interface
- Programmable burst type, burst length, and CAS latency
  Burst type : Sequential Mode, Interleave Mode
  Burst length : 1, 2, 4, 8, full column (64 : ×16 bit, 32 : ×32 bit)
  CAS latency
  MB81ES171625/173225-12
  CL = 1 (Min t_{CK} = 23.4 ns, Max 42.7 MHz)
  CL = 2 (Min t_{CK} = 11.7 ns, Max 85 MHz)
- 2 K refresh cycles every 16 ms
- Auto- and Self-refresh
- CKE power down mode
- Output Enable and Input Data Mask
- Burst Stop command at full column burst
- Burst read/write
- 85 MHz/66.7 MHz Clock frequency

■ PAD LAYOUT



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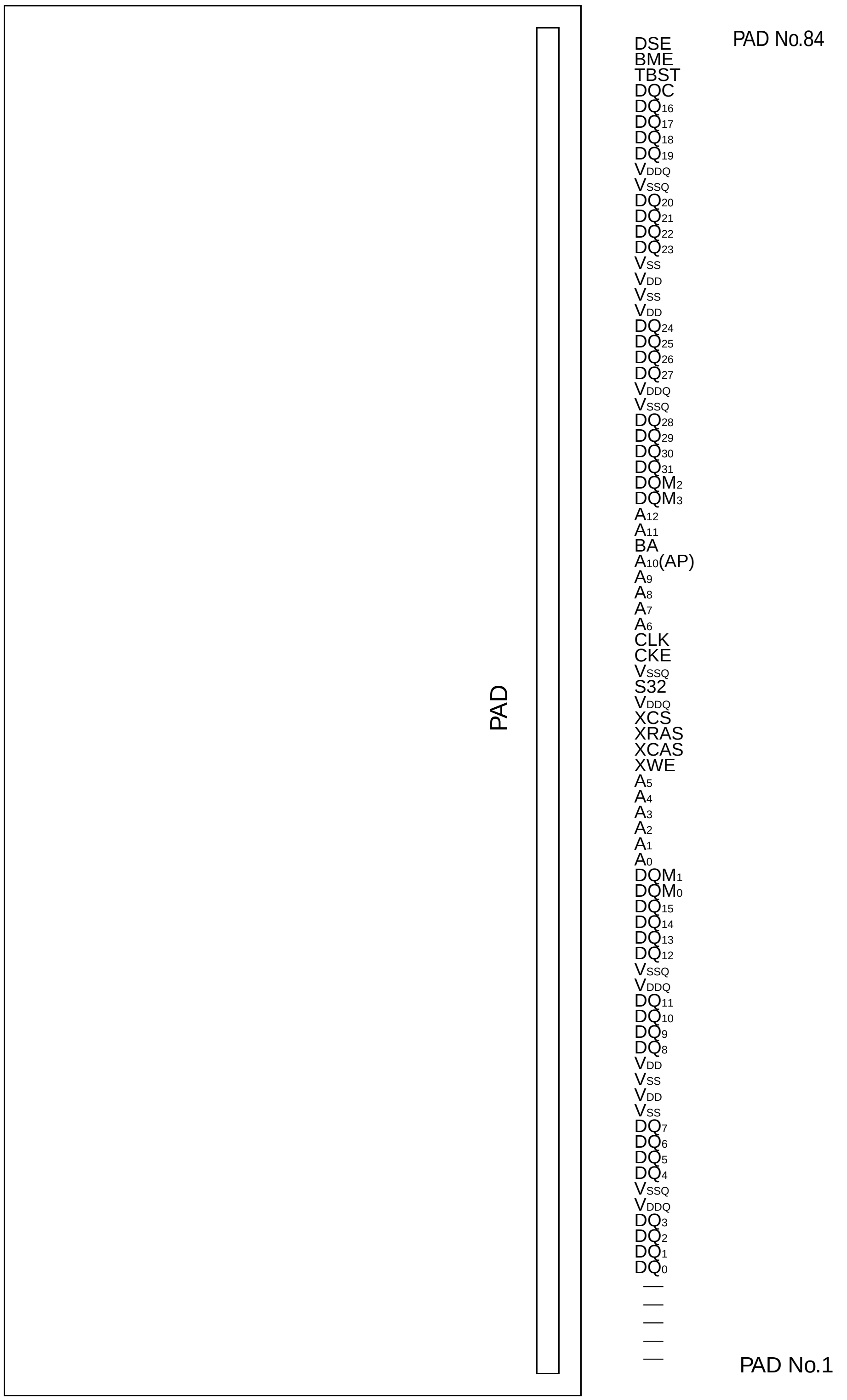
MB81ES173225



■ PAD DESCRIPTIONS

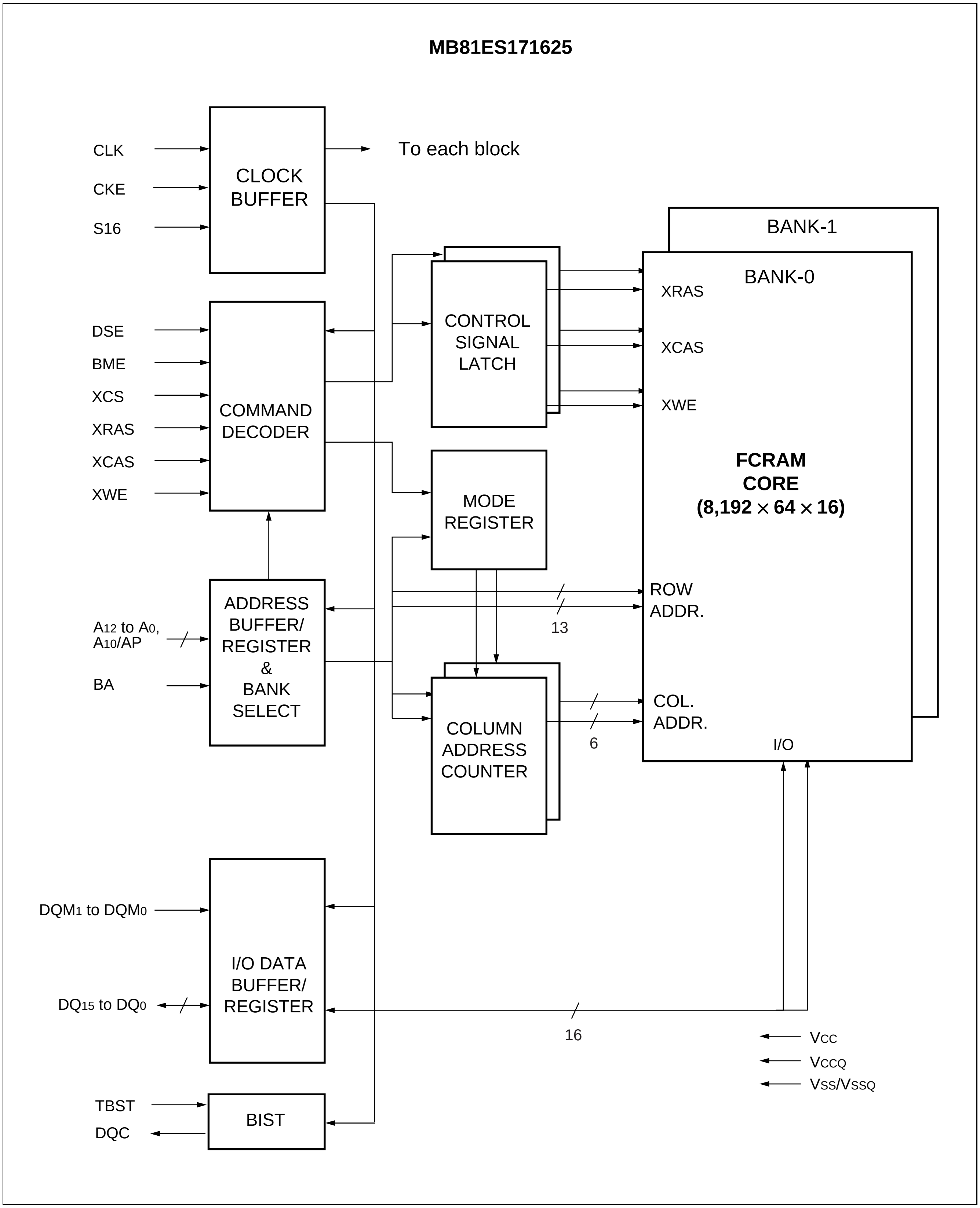
• **MB81ES171625**

Symbol	Function
V_{DD}, V_{DDQ}	Supply Voltage
V_{SS}, V_{SSQ}	Ground
DQ_{15} to DQ_0	Data I/O
DQM_1 to DQM_0	DQ MASK
XWE	Write Enable
XCAS	Column Address Strobe
XRAS	Row Address Strobe
XCS	Chip Select
BA	Bank Select
AP	Auto Precharge Enable
$A_{12}A_0$	Address Input • Row : A_{12} to A_0 • Column : A_5 to A_0
CKE	Clock Enable
CLK	Clock Input
TBST	BIST Control
BME	Burn In Enable
DSE	Disable
DQC	BIST Output
S16	$\times$ 16 Select

• **MB81ES173225**

Symbol	Function
V_{DD}, V_{DDQ}	Supply Voltage
V_{SS}, V_{SSQ}	Ground
DQ_{31} to DQ_0	Data I/O
DQM_3 to DQM_0	DQ MASK
XWE	Write Enable
XCAS	Column Address Strobe
XRAS	Row Address Strobe
XCS	Chip Select
BA	Bank Select
AP	Auto Precharge Enable
A_{12} to A_0	Address Input • Row : A_{12} to A_0 • Column : A_4 to A_0
CKE	Clock Enable
CLK	Clock Input
TBST	BIST Control
BME	Burn In Enable
DSE	Disable
DQC	BIST Output
S32	$\times$ 32 Select

■ BLOCK DIAGRAM



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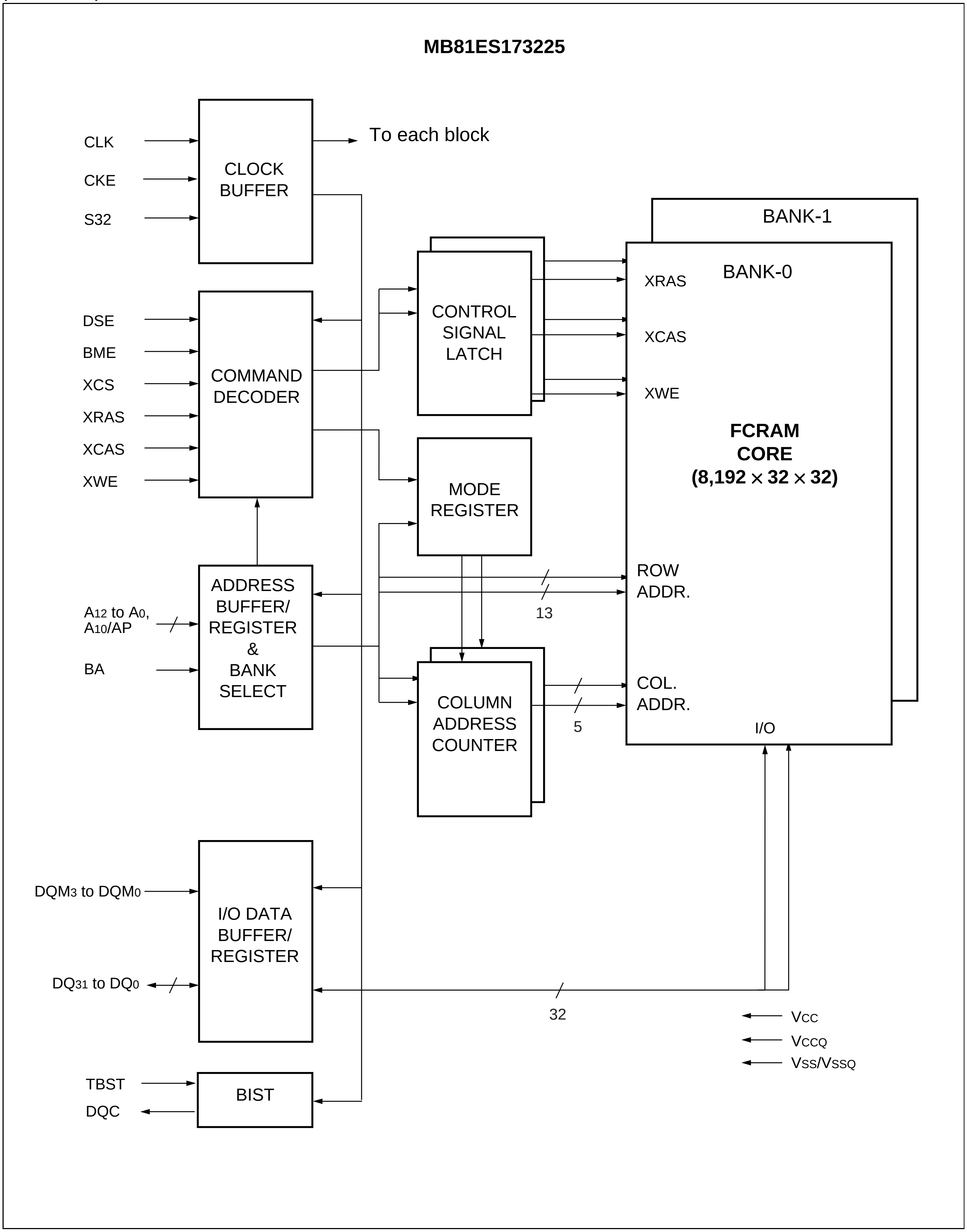
MB81ES173225
CLK
CKE
S32
CLOCK BUFFER
To each block
DSE
BME
XCS
XRAS
XCAS
XWE
COMMAND DECODER
CONTROL SIGNAL LATCH
MODE REGISTER
BANK-1
BANK-0
XRAS
XCAS
XWE
FCRAM CORE (8,192 × 32 × 32)
ROW ADDR.
13
A12 to A0, A10/AP
BA
ADDRESS BUFFER/ REGISTER & BANK SELECT
COLUMN ADDRESS COUNTER
COL. ADDR.
5
I/O
DQM3 to DQM0
DQ31 to DQ0
I/O DATA BUFFER/ REGISTER
32
VCC
VCCQ
VSS/VSSQ
TBST
DQC
BIST

■ FUNCTIONAL TRUTH TABLE

1. Command Truth Table

Function		Com-mand	CKE		XCS	XRAS	XCAS	XWE	BA	A_{10} (AP)	A_{12} to A_6	A_5	A_4 to A_0
			n-1	n									
Device Deselect*1		DESL	H	X	H	X	X	X	X	X	X	X	X
No Operation*1		NOP	H	X	L	H	H	H	X	X	X	X	X
Burst Stop*2		BST	H	X	L	H	H	L	X	X	X	X	X
Read*3	X16	READ	H	X	L	H	L	H	V	L	X	V	V
	X32		H	X	L	H	L	H	V	L	X	X	V
Read with Auto-pre-charge*3	X16	READA	H	X	L	H	L	H	V	H	X	V	V
	X32		H	X	L	H	L	H	V	H	X	X	V
Write*3	X16	WRIT	H	X	L	H	L	L	V	L	X	V	V
	X32		H	X	L	H	L	L	V	L	X	X	V
Write with Auto-pre-charge*3	X16	WRITA	H	X	L	H	L	L	V	H	X	V	V
	X32		H	X	L	H	L	L	V	H	X	X	V
Bank Active*4		ACTV	H	X	L	L	H	H	V	V	V	V	V
Precharge Single Bank*5		PRE	H	X	L	L	H	L	V	L	X	X	X
Precharge All Banks*5		PALL	H	X	L	L	H	L	X	H	X	X	X
Mode Register Set*5, *6		MRS	H	X	L	L	L	L	L	L	V	V	V

V = Valid, L = Logic Low, H = Logic High, X = either L or H.
n = State at current clock cycle, n–1 = state at 1 clock cycle before n.

*1: NOP and DESL commands have the same effect on the part. At DESL command (XCS = "H") , all input signal are ignored, but hold the internal state. NOP command (XCS = "L", XRAS = XCAS = XWE = "H") is no effect on device operation and the internal state continue.

*2: BST command is effective on every Burst Length. (BL = 1, 2, 4, 8, full column)

*3: READ, READA, WRIT and WRITA commands should be issued only after the corresponding bank has been activated (ACTV command) .
Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)."

*4 ACTV command should be issued only after the corresponding bank has been precharged (PRE or PALL command) .

*5: Required after power up. Refer to "17. Power-Up Initialization" in "■ FUNCTIONAL DESCRIPTION."

*6: MRS command should be issued only after all banks have been precharged (PRE or PALL command) and DQ is in High-Z. Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)."

Notes:
- All commands assumes no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.
- TBST,BME and DSE should be held Low.
- S16 should be held V_{IH}, and S32 should be held V_{IL}.

2. DQM Truth Table

Function	Command	CKE		DQM
		n-1	n	
Data Write/Output Enable	ENBL	H	X	L
Data Mask/Output Disable	MASK	H	X	H

V = Valid, L = Logic Low, H = Logic High, X = either L or H.
n = State at current clock cycle, n–1 = state at 1 clock cycle before n.

Notes:
- MB81ES171625; DQM_0 and DQM_1 controls DQ_7 to DQ_0 and DQ_{15} to DQ_8, respectively.
- MB81ES173225; DQM_0, DQM_1, DQM_2 and DQM_3 controls DQ_7 to DQ_0, DQ_{15} to DQ_8, DQ_{23} to DQ_{16}, and DQ_{31} to DQ_{24}, respectively.
- TBST, BME and DSE should be held Low.
- S16 should be held V_{IH}, and S32 should be held V_{IL}.
- All commands assumes no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.

3. CKE Truth Table

Current State	Function	Com-mand	CKE		XCS	XRAS	XCAS	XWE	BA	A_{10} (AP)	A_{12} to A_0
			n-1	n							
Bank Active	Clock Suspend Mode Entry *1	CSUS	H	L	X	X	X	X	X	X	X
Any (Except Idle)	Clock Suspend Continue *1	—	L	L	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit	—	L	H	X	X	X	X	X	X	X
Idle	Auto-refresh Command *2	REF	H	H	L	L	L	H	X	X	X
Idle	Self-refresh Entry *2, *3	SELF	H	L	L	L	L	H	X	X	X
Self Refresh	Self-refresh Exit *4	SELFX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Power Down Entry *3	PD	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Power Down	Power Down Exit	—	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X

V = Valid, L = Logic Low, H = Logic High, X = either L or H.
n = State at current clock cycle, n–1 = state at 1 clock cycle before n.

*1: CSUS command requires that at least one bank is active. Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)."

*2: REF and SELF commands should be issued only after all banks have been precharged (PRE or PALL command) . Refer to "■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)."

*3: SELF and PD commands should be issued only after the last read data have been appeared on DQ.

*4: CKE should be held High during t_{REFC}.

Notes:
- TBST,BME and DSE should be held Low.
- S16 should be held V_{IH}, and S32 should be held V_{IL}.
- All commands assumes no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.

4. Operation Command Table (Applicable to single bank)

Current State	XCS	XRAS	XCAS	XWE	Addr	Command	Function
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	NOP*1
	L	H	L	H	BA, CA, AP	READ/READA	Illegal*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}
	L	L	H	L	BA, AP	PRE	NOP
	L	L	H	L	AP	PALL	NOP*1
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-reresh*3, *5
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC}) *3, *6
Bank Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal*2
	L	L	H	L	BA, AP	PRE	Precharge
	L	L	H	L	AP	PALL	Precharge*1
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, NewRead; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP*4
	L	L	H	H	BA, RA	ACTV	Illegal*2
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge → Idle
	L	L	H	L	AP	PALL	Terminate Burst, Precharge → Idle*1
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	

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Current State	XCS	XRAS	XCAS	XWE	Addr	Command	Function
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP*4
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal*2
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge → Idle
	L	L	H	L	AP	PALL	Terminate Burst, Precharge → Idle*1
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE	
	L	L	H	L	AP	PALL	Illegal
	L	L	L	H	X	REF/SELF	
	L	L	L	L	MODE	MRS	
Write with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE	
	L	L	H	L	AP	PALL	Illegal
	L	L	L	H	X	REF/SELF	
	L	L	L	L	MODE	MRS	

(Continued)

Current State	XCS	XRAS	XCAS	XWE	Addr	Command	Function
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE	NOP*7
	L	L	H	L	AP	PALL	NOP*1
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	NOP (Bank Active after t_{RCD}) *1
	L	H	L	H	BA, CA, AP	READ/READA	Illegal*2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE	
	L	L	H	L	AP	PALL	Illegal
	L	L	L	H	X	REF/SELF	
	L	L	L	L	MODE	MRS	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after t_{REFC})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	H	X	X	ACTV/ PRE/PALL	
	L	L	L	X	X	REF/SELF/ MRS	

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Current State	XCS	XRAS	XCAS	XWE	Addr	Command	Function
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after t_{RSC})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/SELF/ MRS	

ABBREVIATIONS :

V = Valid, L = Logic Low, H = Logic High, X = either L or H.
n = State at current clock cycle, n–1 = state at 1 clock before n.
RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

*1: Entry may affect other bank.

*2: Illegal to the bank in specified state; entry may be legal to the bank specified by BA, depending on the state of that bank.

*3: Illegal if any bank is not idle.

*4: Must satisfy bus contention, bus turn around, and/or write recovery requirements.
Refer to “11. READ Interrupted by WRITE (Example @ CL = 2, BL = 4)” and “12. WRITE to READ Timing (Example @ CL = 1, BL = 4)” in “■ TIMING DIAGRAMS.”

*5: SELF command should be issued only after the last read data has been appeared on DQ.

*6: MRS command should be issued only when all DQ are in High-Z.

*7: NOP in precharging or idle state. PRE may affect to the bank specified by BA and AP.

Notes:
- TBST,BME and DSE should be held Low.
- S16 should be held V_{IH}, and S32 should be held V_{IL}.
- All entries in OPERATION COMMAND TABLE assume that the CKE was High during the proceeding clock cycle and the current clock cycle.
- Illegal means that the device operation and/or data-integrity are not guaranteed. If used, power up sequence will be asserted after power shut down.
- All commands assume no CSUS command on previous rising edge of clock.
- All commands are assumed to be valid state transitions.
- All inputs are latched on the rising edge of the clock.

5. Command Truth Table for CKE

Current State	CKE (n-1)	CKE (n)	XCS	XRAS	XCAS	XWE	Addr	Function
Self-refresh	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{REFC})
	L	H	L	H	H	H	X	
	L	H	L	H	H	L	X	Illegal
	L	H	L	H	L	X	X	
	L	H	L	L	X	X	X	
	L	L	X	X	X	X	X	Maintain Self-refresh
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid
	H	H	H	X	X	X	X	Idle after t_{REFC}
	H	H	L	H	H	H	X	
	H	H	L	H	H	L	X	Illegal
	H	H	L	H	L	X	X	
	H	H	L	L	X	X	X	
	H	L	X	X	X	X	X	Illegal*1
Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle
	L	H	L	H	H	H	X	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)
	L	H	L	L	X	X	X	Illegal
	L	H	L	H	L	X	X	
	L	H	L	H	H	L	X	
All Banks Idle	H	H	H	X	X	X	V	Refer to “Operation Command Table”.
	H	H	L	H	X	X	V	
	H	H	L	L	H	X	V	
	H	H	L	L	L	H	X	Auto-refresh
	H	H	L	L	L	L	V	Refer to “Operation Command Table”.
	H	L	H	X	X	X	X	Power Down
	H	L	L	H	H	H	X	
	H	L	L	H	H	L	X	Illegal
	H	L	L	H	L	X	X	
	H	L	L	L	H	X	X	
	H	L	L	L	L	H	X	Self-refresh*2
	H	L	L	L	L	L	X	Illegal
	L	X	X	X	X	X	X	Invalid

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Current State	CKE (n-1)	CKE (n)	XCS	XRAS	XCAS	XWE	Addr	Function
Bank Active Bank Activating Read/Write	H	H	X	X	X	X	X	Refer to “Operation Command Table”.
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle
	L	X	X	X	X	X	X	Invalid
Clock Suspend	H	X	X	X	X	X	X	
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle
	L	L	X	X	X	X	X	Maintain Clock Suspend
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid
	H	H	X	X	X	X	X	Refer to “Operation Command Table”.
	H	L	X	X	X	X	X	Illegal

V = Valid, L = Logic Low, H = Logic High, X = either L or H.
n = State at current clock cycle, n–1 = state at 1 clock cycle before n.

*1: CKE should be held High for t_{REFC} period.

*2: SELF command should be issued only after the last data has been appeared on DQ.

Notes: • TBST,BME and DSE should be held Low.
• S16 should be held V_{IH}, and S32 should be held V_{IL}.
• All entries in “5. Command Truth Table for CKE” are specified at CKE (n) state and CKE input from CKE (n–1) to CKE (n) state must satisfy the corresponding setup and hold time for CKE.

■ FUNCTIONAL DESCRIPTION

1. SDR I/F FCRAM Basic Function

Three major differences between SDR I/F FCRAMs and conventional DRAMs are : a synchronized operation, a burst mode, and a mode register.

The **synchronized operation** is the fundamental difference. SDR I/F FCRAM uses a clock input for synchronization, while DRAM is basically asynchronous memory although it has been using two clocks, XRAS and XCAS. Each operation of DRAM is determined by their timing phase differences while each operation of the SDR I/F FCRAM is determined by commands and all operations are referenced to a rising edge of a clock.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column address for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode registe**r is to configure SDR I/F FCRAM operation and function into desired system conditions. "■ MODE REGISTER TABLE" shows how the SDR I/F FCRAM can be configured for system requirements by mode register programming.

The program to the mode resister should be excuted after all banks are precharged.

2. FCRAM™

MB81ES171625/173225 utilizes FCRAM core technology. The FCRAM is an acronym for Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

3. Clock (CLK) Input and Clock Enable (CKE)

All input and output signals of the SDR I/F FCRAM use register type buffers. CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a rising edge of CLK. All outputs are validated by a rising edge of CLK. CKE is a high active clock enable signal. CKE controls the internal clock generator. CKE is latched by a rising edge of clock. CKE should become High level on the previous clock cycle when a basic command is issued. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged) , the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

4. Chip Select (XCS)

XCS enables all command inputs, XRAS, XCAS, XWE and address inputs. When XCS is High, command signals are negated but internal operations such as a burst cycle will not be suspended. If such a control isn't needed, XCS can be tied to ground level.

5. Command Input (XRAS, XCAS and XWE)

Unlike a conventional DRAM, XRAS, XCAS, and XWE do not directly imply SDR I/F FCRAM operations, such as Row address strobe by XRAS. Instead, each combination of XRAS, XCAS, and XWE input in conjunction with XCS input at the rising edge of the CLK determines SDR I/F FCRAM operations. Refer to "■ FUNCTIONAL TRUTH TABLE."

6. Address Input (A_{12} to A_0)

Address input selects an arbitrary location of each memory cell matrix, 524,288 (×16 bit) or 262,144 (×32 bit) . A total of 19(× 16 bit) or 18 (× 32 bit) address input signals are required to decode 13 bit Row addresses and 6 bit (×16 bit) or 5 bit (×32 bit) Column addresses matrix. The SDR I/F FCRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV) , 13 bit Row addresses are initially latched and the remainder of 6 bit (× 16 bit) or 5 bit (× 32 bit) Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or a Write command (WRIT or WRITA) . A_{10} selects READ or READA, WRIT or WRITA and PRE or PALL.

7. Bank Select (BA)

This SDR I/F FCRAM has two banks.
Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA) , write (WRIT or WRITA) , and precharge commands (PRE or PALL) .

8. Data Inputs and Ooutputs (DQ_{15} to DQ_0/DQ_{31} to DQ_0)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input :

t_{RAC}; from the bank active command when t_{RCD} (Min) is satisfied. (This parameter is reference only.)
t_{CAC}; from the read command when t_{RCD} is greater than t_{RCD} (Min) at CL = 1.
t_{AC} ; from the rising edge of the clock after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of input data. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}) .

Refer to "■ AC CHARACTERISTICS".

9. Data I/O Mask (DQM_1, DQM_0/DQM_3 to DQM_0)

DQM is an active high enable input and has an output disable and input mask function. During burst cycle and when DQM = High is latched by a clock, input is masked at the same clock and output will be masked at the CL later while internal burst counter will increment by one or will go to the next stage depending on the burst type.

10. Burst Mode Operation

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatically generating column address. Access time and cycle time of Burst mode is specified as t_{CAC}/t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and the burst count length of 1, 2, 4, 8 bits of boundary or full column. In order to terminate or move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required :

(1) Burst Type

The burst type can be selected either sequential or interleave mode. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps around to the least significant address (= 0) . The interleave mode is a scrambled decoding scheme for A_0 through A_2. If the first access of column address is even (0) , the next address will be odd (1) , or vice-versa.

(2) Burst Mode Termination and Method of Next Stage Set

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after ℓ_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

(3) **Counter Operation of Sequential Mode and Interleave Mode**

Burst Length	Starting Column Address			Sequential Mode	Interleave Mode
	A_2	A_1	A_0		
2	X	X	0	0 – 1	0 – 1
	X	X	1	1 – 0	1 – 0
4	X	0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X	0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X	1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X	1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

11. Full Column Burst and Burst Stop Command (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same row. If burst mode reaches the end of column address, then it wraps around to the first column address (= 0) and continues to count until interrupted by the new read (READ) /write (WRIT) , precharge (PRE) , or burst stop (BST) commands. The selection of Auto-precharge option is illegal during the full column burst operation.

BST command is applicable to terminate the burst operation. If BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When a read mode is interrupted by BST command, the output will be in High-Z.
For the detailed rule, please refer to "8. READ Interrupted by Burst Stop (Example @ BL = Full Column) " in "■ TIMING DIAGRAMS."
When a write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

12. Precharge and Precharge Option (PRE, PALL)

The SDR I/F FCRAM memory core is the same as a conventional DRAM's, requiring precharge and refresh operations. Precharge rewrites the bit line and reset the internal Row address line and is executed by the Precharge command (PRE) . With the Precharge command, SDR I/F FCRAM will automatically be in standby state after precharge time (t_{RP}) .

The precharged bank is selected by combination of AP and BA when the Precharge command is asserted. If AP = High, all banks are precharged regardless of BA (PALL) . If AP = Low, a bank to be selected by BA is precharged (PRE) .
The auto-precharge enters precharge mode at the end of burst mode of read or write without the Precharge command assertion.
This auto precharge is entered by AP = High when a read or write command is asserted. Refer to "■ FUNCTIONAL TRUTH TABLE."

13. Auto-Refresh (REF)

The Auto-refresh uses the internal refresh address counter. SDR I/F FCRAM Auto-refresh command (REF) generates the Precharge command internally. All banks of SDR I/F FCRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 7.8 µs or a total 2048 refresh commands within a 16 ms period.

14. Self-Refresh Entry (SELF)

The Self-refresh function provides automatic refresh by an internal timer as well as the Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF) . Once SDR I/F FCRAM enters the self-refresh mode, all inputs except for CKE will be “don’t care” (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should be issued only after the last read data has been appeared on DQ.

Note : When the burst refresh method is used, a total of 2048 auto-refresh commands must be asserted within 1 ms prior to the self-refresh mode entry.

15. Self-Refresh Exit (SELFX)

To exit the Self-refresh mode, apply minimum t_{SI} after CKE brought high, and then the No operation command (NOP) or the Deselect command (DESL) should be asserted within one t_{REFC} period. CKE should be held High within one t_{REFC} period after t_{SI}. Refer to “16. Self-Refresh Entry and Exit Timing” in “■ TIMING DIAGRAMS” for the detail.

It is recommended to assert an Auto-refresh command just after t_{REFC} period to avoid the violation of refresh period.

Note : When the burst refresh method is used, a total of 2048 auto-refresh commands must be asserted within 1 ms after the Self-refresh exit.

16. Mode Register Set (MRS)

The mode register of the SDR I/F FCRAM provides a variety of operations. The register consists of 3 operation fields; Burst Length, Burst Type, and CAS latency. Refer to “■ MODE REGISTER TABLE.”

The mode register can be programmed by the Mode Register Set command (MRS) . Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power) . MRS command should be issued only when DQ is in High-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of the SDR I/F FCRAM. Refer to “17. Power-Up Initialization”.

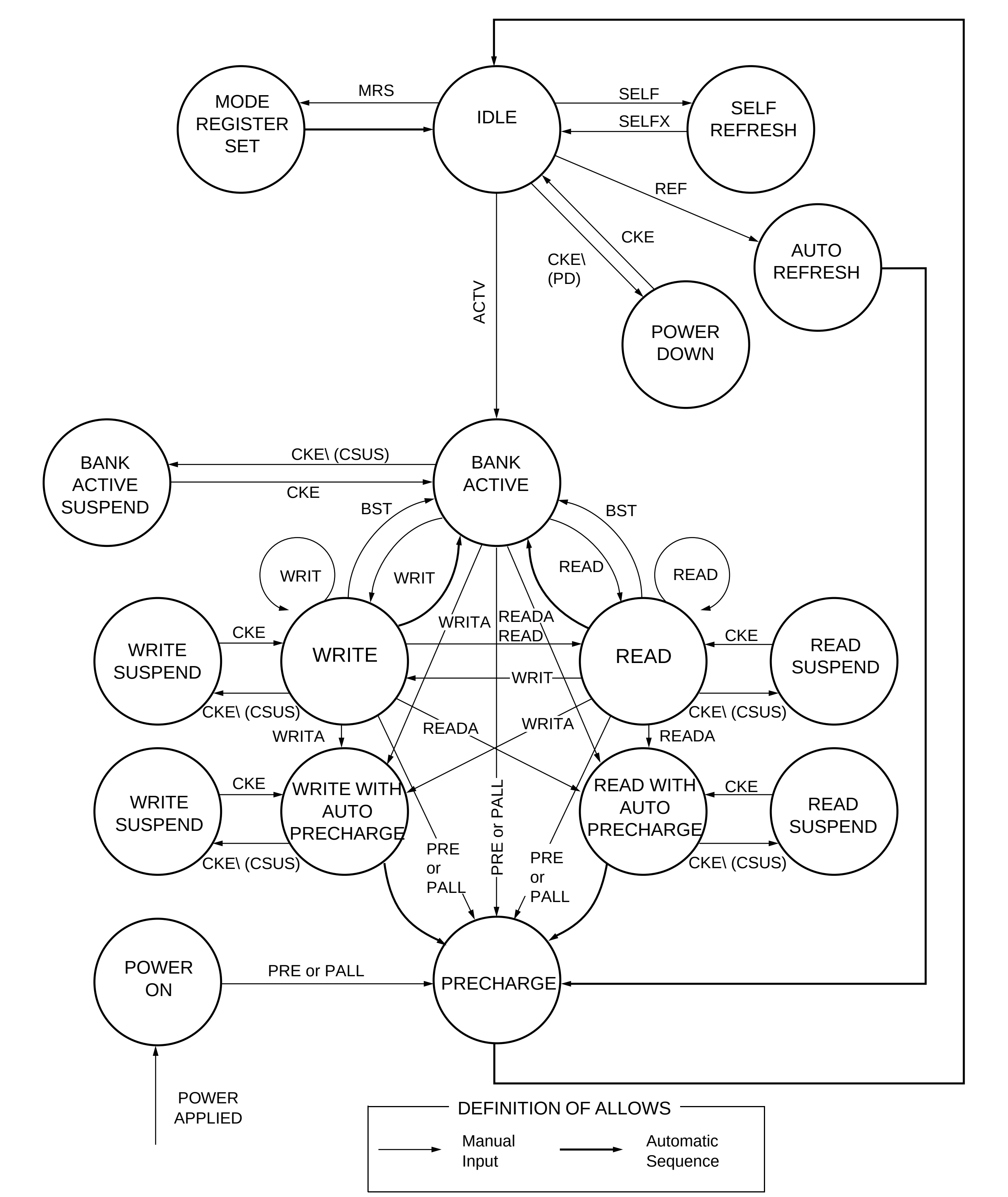
17. Power-Up Initialization

SDR I/F FCRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply the power and start the clock. Attempt to maintain either the NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 500 µs.
3. Precharge all banks by the Precharge (PRE) or Precharge All command (PALL) .
4. Assert minimum of 2 Auto-refresh commands (REF) .
5. Program the mode register by the Mode Register Set command (MRS) .

In addition, it is recommended that DQM and CKE track V_{DD} to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 2 Auto-refresh commands (REF) . It is possible to execute 5 before 4.

■ STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)



Note : CKE\ means CKE goes Low-level from High-level.

■ BANK OPERATION COMMAND TABLE

• Minimun Clock Latency or Delay Time for Single Bank Operation

First command \ Second command (same bank)	MRS	ACTV	READ	READA	WRIT	WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV			t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}			1
READ			1	1	*4 1	*4 1	*3 1	*3 1			1
READA	*1, *2 BL + t_{RP}	*1 BL + t_{RP}					*3 BL + t_{RP}	*3 BL + t_{RP}	*1 BL + t_{RP}	*1 BL + t_{RP}	*1 BL + t_{RP}
WRIT			t_{WR}	t_{WR}	1	1	*3 t_{DPL}	*3 t_{DPL}			1
WRITA	*1, *2 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}					*3 BL-1 + t_{DAL}	*3 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}
PRE	*1, *2 t_{RP}	t_{RP}					1	*3 1	*1 t_{RP}	*1, *5 t_{RP}	1
PALL	*2 t_{RP}	t_{RP}					1	1	t_{RP}	*5 t_{RP}	1
REF	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

*1: Assume all banks are in idle state.

*2: Assume output is in High-Z state.

*3: Assume t_{RAS} (Min) is satisfied.

*4: Assume no I/O conflict.

*5: Assume the last data have been appeared on DQ.

▢ Illegal Command.

• **Minimum Clock Latency or Delay Time for Multi Bank Operation**

Second command (other bank) / First command	MRS	ACTV	*4 READ	*4 READA	*4 WRIT	*4 WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV		*1 t_{RRD}	*6 1	*6 1	*6 1	*6 1	*5, *6 1	*6 t_{RAS}			1
READ		*1, *3 1	1	1	*8 1	*8 1	*5 1	*5 1			1
READA	*1, *2 BL + t_{RP}	*1, *3 1	*5 1	*5 1	*5, *8 1	*5, *8 1	*5 1	*5 BL + t_{RP}	*1 BL + t_{RP}	*1 BL + t_{RP}	*1 BL + t_{RP}
WRIT		*1, *3 1	1	1	1	1	*5 1	*5 t_{DPL}			1
WRITA	*1, *2 BL-1 + t_{DAL}	*1, *3 1	*5 1	*5 1	*5 1	*5 1	*5 1	*5 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}	*1 BL-1 + t_{DAL}
PRE	*1, *2 t_{RP}	*1, *3 1	*6 1	*6 1	*6 1	*6 1	*5, *6 1	*6 1	*1 t_{RP}	*1, *7 t_{RP}	1
PALL	*2 t_{RP}	t_{RP}					1	1	t_{RP}	*7 t_{RP}	1
REF	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}
SELFX	t_{REFC}	t_{REFC}					t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}

*1: Assume all banks are in idle state.

*2: Assume output is in High-Z state.

*3: t_{RRD} (Min) of other bank (the second command will be asserted) is satisfied.

*4: Assume other bank is in active, read or write state.

*5: Assume t_{RAS} (Min) is satisfied.

*6: Assume other banks are not in READA/WRITA state.

*7: Assume the last data have been appeared on DQ.

*8: Assume no I/O conflict.

Illegal Command.

■ MODE REGISTER TABLE

MODE REGISTER SET

BA	A_{12}	A_{11}	A_{10}	A_9	A_8*2	A_7*2	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0 or 1					0	0	CL			BT	BL			MODE REGISTER

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT = 0	BT = 1 *1
0	0	0	1	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_3	Burst Type
0	Sequential
1	Interleave

*1: BL = 1 and Full Column are not applicable to the interleave mode.

*2: A_7 and A_8 = 1 are reserved for vender test.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of V_{CC} Supply Relative to V_{SS}	V_{DD}, V_{DDQ}	–0.5	+3.0	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	+3.0	V
Short Circuit Output Current	I_{OUT}	–13	+13	mA
Storage Temperature	T_{STG}	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

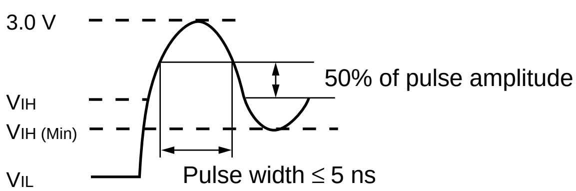
■ RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

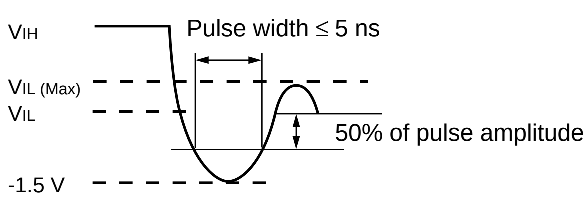
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage*1	V_{DD}, V_{DDQ}	1.65	1.8	1.95	V
	V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage*2	V_{IH}	V_{DDQ}–0.4	—	V_{DDQ} + 0.3	V
Input Low Voltage*3	V_{IL}	–0.3	—	0.4	V
Ambient Temperature	T_A	0	—	+70	°C
Junction Temperature*4	Tj	0	—	+100	°C

*1 : All voltages are referenced to V_{SS}.

*2 : Overshoot limit: V_{IH} (Max)
= 3.0 V for pulse width ≤ 5 ns
acceptable,pulse width measured at 50% of
pulse amplitude.



*3 : Undershoot limit: V_{IL} (Min)
= V_{SS} –1.5 V for pulse width ≤ 5 ns
acceptable,pulse width measured at 50% of
pulse amplitude.



*4 : The maximum junction temperature of FCRAM (Tj) should not be more than +100 °C.
Tj is represented by the power consumption of FCRAM (P_{FCRAM}) and Logic LSI(P_D),the thermal resistance of the package(θja),and the maximum ambient temperature of the SiP($T_A$max).

$$Tjmax[\ °C] = T_A max[\ °C] + \theta ja[\ °C/W] \times \Sigma\ Pmax[W]$$
$$\Sigma\ Pmax[W] = P_{FCRAM} + P_D$$

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

(f = 1 MHz, T_A = +25 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance, Except for CLK	C_{IN1}	2.0	—	5.0	pF
Input Capacitance for CLK	C_{IN2}	2.0	—	5.0	pF
I/O Capacitance	$C_{I/O}$	2.0	—	5.0	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output High Voltage	$V_{OH(DC)}$	I_{OH} = –2 mA	V_{DDQ} –0.2	—	V
Output Low Voltage	$V_{OL(DC)}$	I_{OL} = 2 mA	—	0.2	V
Input Leakage Current (Any Input)	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}; All other pins not under test = 0 V	–5	5	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}; Data out disabled	–5	5	µA
Average Power Supply Current (Operating Current)	I_{DD1}	Burst Length = 1, t_{RC} = Min for BL = 1, t_{CK} = Min, One bank active, Output pin open, Addresses changed up to one time during t_{CK} (Min) , 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{DDQ}	—	30	mA
Power Supply Current (Precharge Standby Current)	I_{DD2P}	CKE = 0 V, All banks idle, t_{CK} = Min, Power down mode, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	1	mA
	I_{DD2PS}	CKE = 0 V, All banks idle, CLK = V_{DDQ} or 0 V, Power down mode, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	1	mA
Power Supply Current (Precharge Standby Current)	I_{DD2N}	CKE = V_{DDQ} , All banks idle, t_{CK} = Min, NOP command only, Input signals (except to CMD) are changed one time during 30 ns, V_{IL}=0 V, V_{IH} = V_{DDQ}	—	4	mA
	I_{DD2NS}	CKE = V_{DDQ} , All banks idle, CLK = V_{DDQ} or 0 V, Input signal are stable, V_{IL}=0 V, V_{IH} = V_{DDQ}	—	1	mA

(Continued)

(Continued)

Parameter		Symbol	Condition	Value Min	Value Max	Unit
Power Supply Current (Active Standby Current)		I_{DD3P}	CKE = 0 V, Any bank active, t_{CK} = Min, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	1	mA
		I_{DD3PS}	CKE = 0 V, Any bank active, CLK = V_{DDQ} or 0 V, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	1	mA
	MB81ES171625/ 173225-12	I_{DD3N}	CKE = V_{DDQ}, Any bank active, t_{CK} = Min, NOP command only, Input signals (except to CMD) are changed one time during 30 ns, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	13	mA
	MB81ES171625/ 173225-15			—	10	mA
		I_{DD3NS}	CKE = V_{DDQ}, Any bank active, CLK = V_{DDQ} or 0 V, Input signals are stable, V_{IL} = 0 V, V_{IH} = V_{DDQ}	—	1	mA
Average Power Supply Current (Burst mode Current)	MB81ES171625/ 173225-12	I_{DD4}	t_{CK} = Min, Burst Length = 4, Output pin open, All-banks active, Gapless data, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{DDQ}	—	51	mA
	MB81ES171625/ 173225-15			—	40	mA
Average Power Supply Current (Auto Refresh Current)		I_{DD5}	Auto-refresh; t_{CK} = Min, t_{REFC} = Min, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{DDQ}	—	73	mA
Average Power Supply Current (Self Refresh Current)		I_{DD6}	Self-refresh; CLK = V_{DDQ} or 0 V, CKE= 0 V, 0 V ≤ V_{IN} ≤ V_{IL} Max, V_{IH} Min ≤ V_{IN} ≤ V_{DDQ}	—	5	mA

Notes:
- All voltages are referenced to V_{SS},V_{SSQ}.
- DC characteristics are measured after following “17. Power-Up Initialization” procedure in ■FUNCTIONAL DESCRIPTION.
- I_{DD} depends on output termination, load conditions, clock rate, number of address and/or command change within certain period. The specified values are obtained with the output open.

■ AC CHARACTERISTICS

(1) Basic AC Characteristics

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	MB81ES171625/173225				Unit
			-12		-15		
			Min	Max	Min	Max	
Clock Period	CL = 1	t_{CK1}	23.4	1000	30	1000	ns
	CL = 2	t_{CK2}	11.7		15		ns
Clock High Time *1		t_{CH}	4.5	—	6	—	ns
Clock Low Time *1		t_{CL}	4.5	—	6	—	ns
Input Setup Time *1		t_{SI}	3	—	3	—	ns
Input Hold Time *1		t_{HI}	2	—	2	—	ns
XRAS Access Time *2		t_{RAC}	—	51.9	—	57	ns
XCAS Access Time *1, *3		t_{CAC}	—	21.9	—	27	ns
Access Time from Clock (t_{CK} = Min) *1, *3, *4	CL = 1	t_{AC1}	—	21.9	—	27	ns
	CL = 2	t_{AC2}	—	10.2		12	ns
Output in Low-Z *1		t_{LZ}	0	—	0	—	ns
Output in High-Z *1, *5	CL = 1	t_{HZ1}	2.5	10	2.5	10	ns
	CL = 2	t_{HZ2}	2.5	10	2.5	10	ns
Output Hold Time *1, *3		t_{OH}	2.5	—	2.5	—	ns
Time between Auto-Refresh command interval *2		t_{REFI}	—	7.8	—	7.8	µs
Time between Refresh		t_{REF}	—	16	—	16	ms
Transition Time		t_T	0.5	5	0.5	5	ns

*1: If input signal transition time (t_T) is longer than 1 ns; [(t_T / 2) – 0.5] ns should be added to t_{CAC} (Max) , t_{AC} (Max) , t_{HZ} (Max) , and t_{SI} (Min) spec values, [(t_T / 2) – 0.5] ns should be subtracted from t_{LZ} (Min) , t_{HZ} (Min) , and t_{OH} (Min) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min) , t_{CL} (Min) , t_{SI} (Min) , and t_{HI} (Min) spec values.

*2: This value is for reference only.

*3: Measured under AC test load circuit shown in " (5) Measurement Condition of AC Characteristics (Load Circuit) ".

*4: t_{AC} also specifies the access time at burst mode except for first access at CL = 1.

*5: Specified where output buffer is no longer driven.

Notes:
- AC characteristics are measured after following "17. Power-Up Initialization" procedure in ■FUNCTIONAL DESCRIPTION.
- AC characteristics assume t_T = 1 ns ,10 pF of capacitive and 50 Ω of terminated load. Refer to " (5) Measurement Condition of AC Characteristics (Load Circuit) ".
- 0.9 V is the reference level for measuring timing of input/output signals.
- Transition times are measured between V_{IH} (Min) and V_{IL} (Max) . Refer to " (6) Set up, Hold and Delay Time".

(2) Base Values for Clock Count/Latency

Parameter	Symbol	MB81ES171625/173225				Unit
		-12		-15		
		Min	Max	Min	Max	
XRAS Cycle Time *	t_{RC}	75	—	75	—	ns
XRAS Precharge Time	t_{RP}	30	—	30	—	ns
XRAS Active Time	t_{RAS}	45	110000	45	110000	ns
XRAS to XCAS Delay Time	t_{RCD}	30	—	30	—	ns
Write Recovery Time	t_{WR}	11.7	—	15	—	ns
XRAS to XRAS Bank Active Delay Time	t_{RRD}	11.7	—	15	—	ns
Data-in to Precharge Lead Time	t_{DPL}	11.7	—	15	—	ns
Data-in to Active/ Refresh Command Period	t_{DAL}	1cyc+ t_{RP}	—	1cyc+ t_{RP}	—	ns
Refresh Cycle Time	t_{REFC}	75	—	75	—	ns
Mode Resister Set Cycle Time	t_{RSC}	45	—	45	—	ns

*: t_{RC} (Min) is not sum of t_{RAS} (Min) and t_{RP} (Min) . Actual clock count of t_{RC} (ℓ_{RC}) must satisfy t_{RC} (Min) , t_{RAS} (Min) and t_{RP} (Min) .

(3) Clock Count Formula

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round up to a whole number)}$$

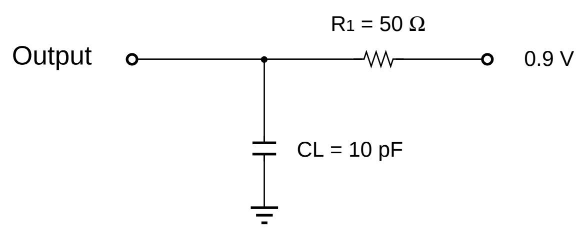
Note: All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula : clock count equals base value divided by clock period (round up to a whole number) .

(4) Latency - Fixed Values

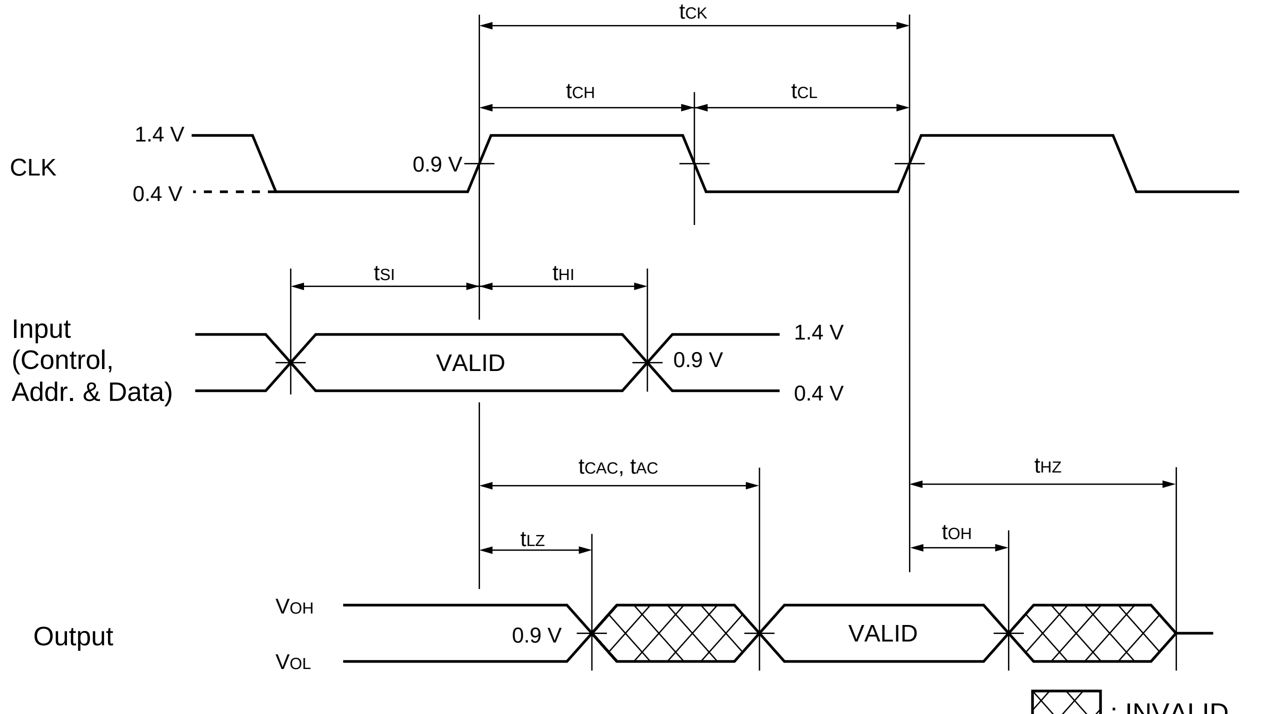
(The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	MB81ES171625/173225		Unit
			-12	-15	
CKE to Clock Disable		ℓ_{CKE}	1	1	cycle
DQM to Output in High-Z	CL = 1	ℓ_{DQZ1}	1	1	cycle
	CL = 2	ℓ_{DQZ2}	2	2	cycle
DQM to Input Data Delay		ℓ_{DQD}	0	0	cycle
Last Output to Write Command Delay		ℓ_{OWD}	2	2	cycle
Write Command to Input Data Delay		ℓ_{DWD}	0	0	cycle
Precharge to Output in High-Z Delay	CL = 1	ℓ_{ROH1}	1	1	cycle
	CL = 2	ℓ_{ROH2}	2	2	cycle
Burst Stop Command to Output in High-Z Delay	CL = 1	ℓ_{BSH1}	1	1	cycle
	CL = 2	ℓ_{BSH2}	2	2	cycle
XCAS to XCAS Delay (Min)		ℓ_{CCD}	1	1	cycle
XCAS Bank Delay (Min)		ℓ_{CBD}	1	1	cycle

(5) Measurement Condition of AC Characteristics (Load Circuit)

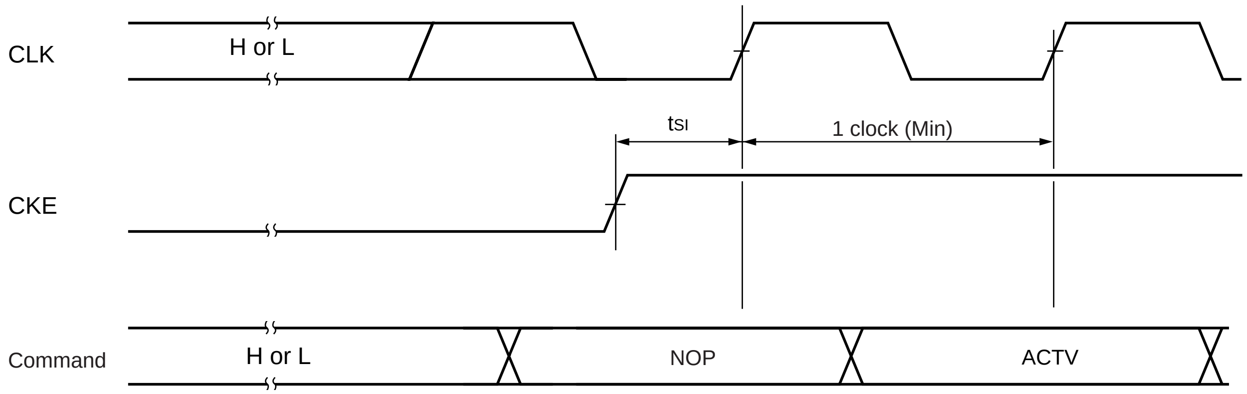


(6) Setup, Hold and Delay Time

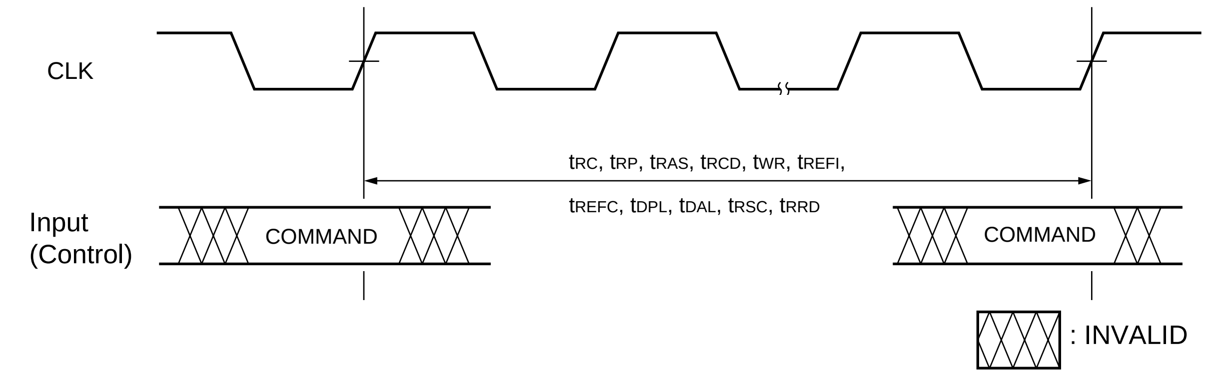


Notes :
- Reference level of input/output signal is 0.9 V.
- Access time is measured at 0.9 V.
- AC characteristics are also measured in this condition.

(7) Delay Time for Power Down Exit

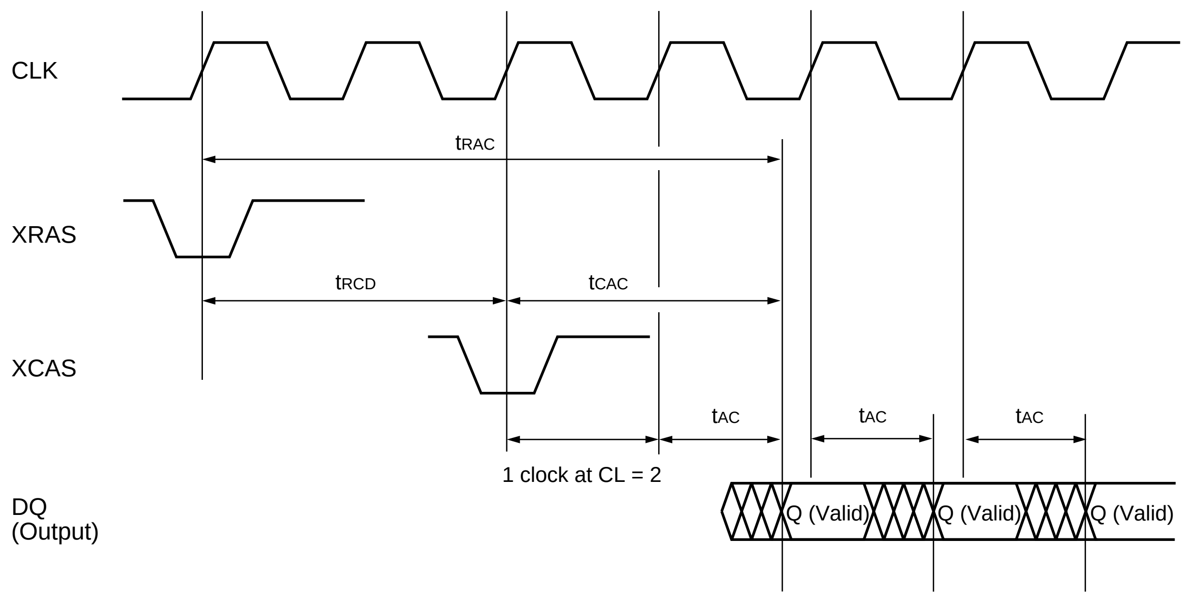


(8) Pulse Width



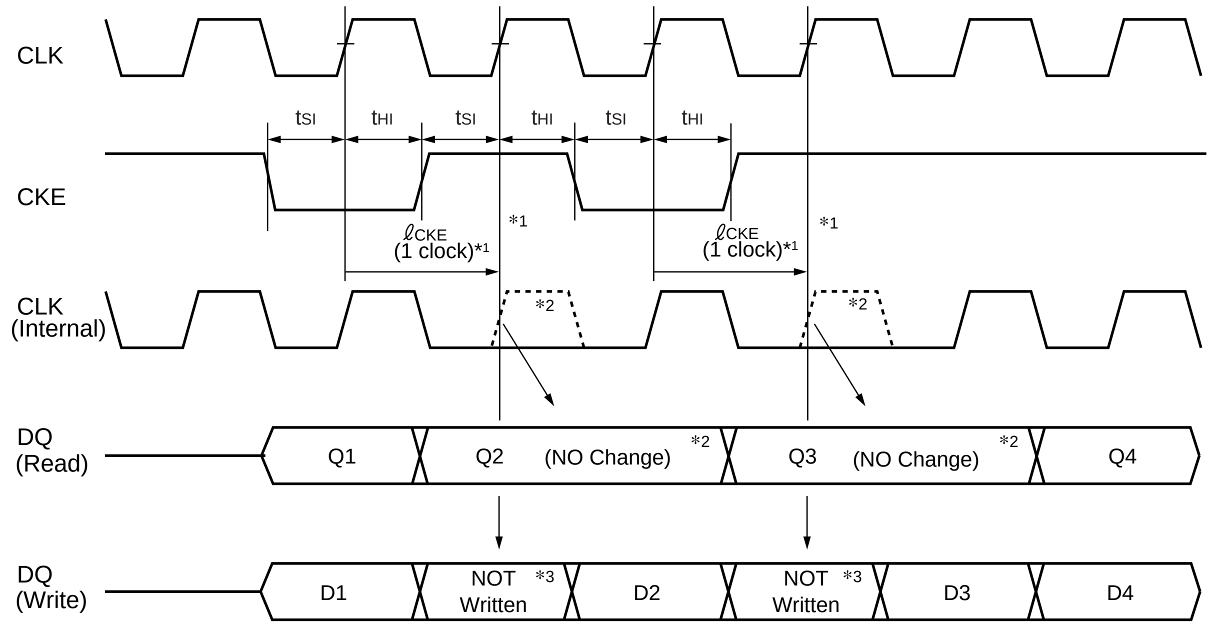
Notes : • These parameters are a limit value of the rising edge of the clock from one command input to the next input.
• Measurement reference voltage is 0.9 V.

(9) Access Time



■ TIMING DIAGRAMS

1. Clock Enable - READ and WRITE Suspend (@ BL = 4)

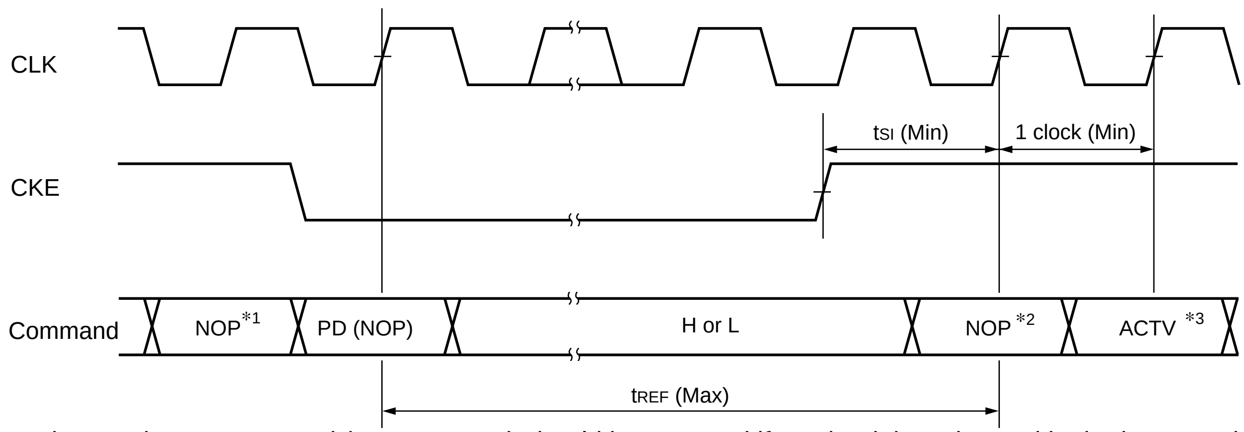


*1: The latency of the CKE (ℓ CKE) is one clock.

*2: During the read mode, burst counter will not be increased/decreased at the next clock of the CSUS command. Output data remains the same data.

*3: During the write mode, data at the next clock of the CSUS command is ignored.

2. Clock Enable - Power Down Entry and Exit

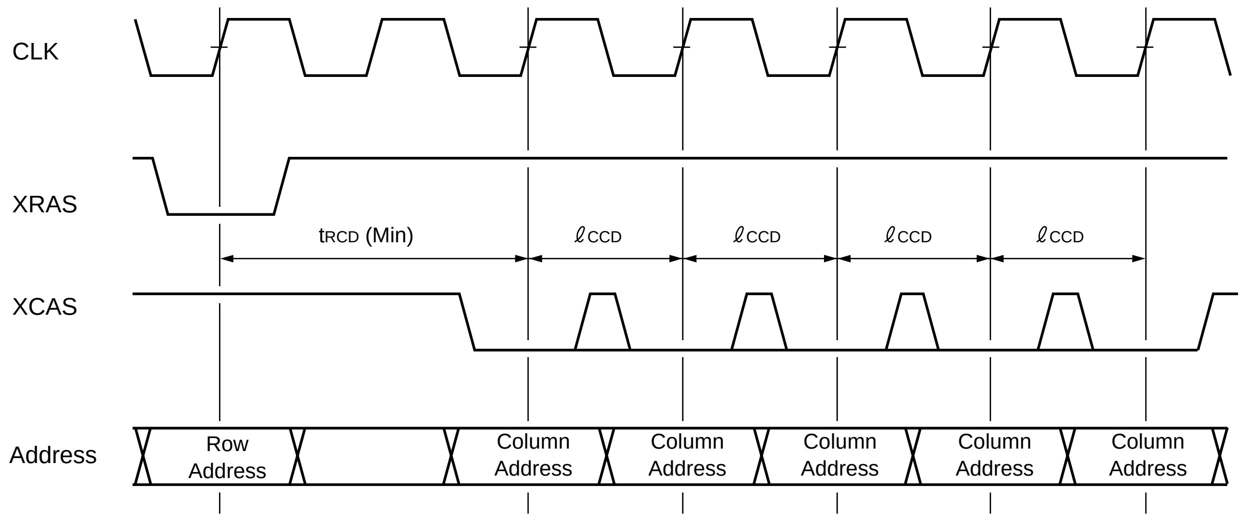


*1: The Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.

*2: The NOP command should be asserted in conjunction with CKE.

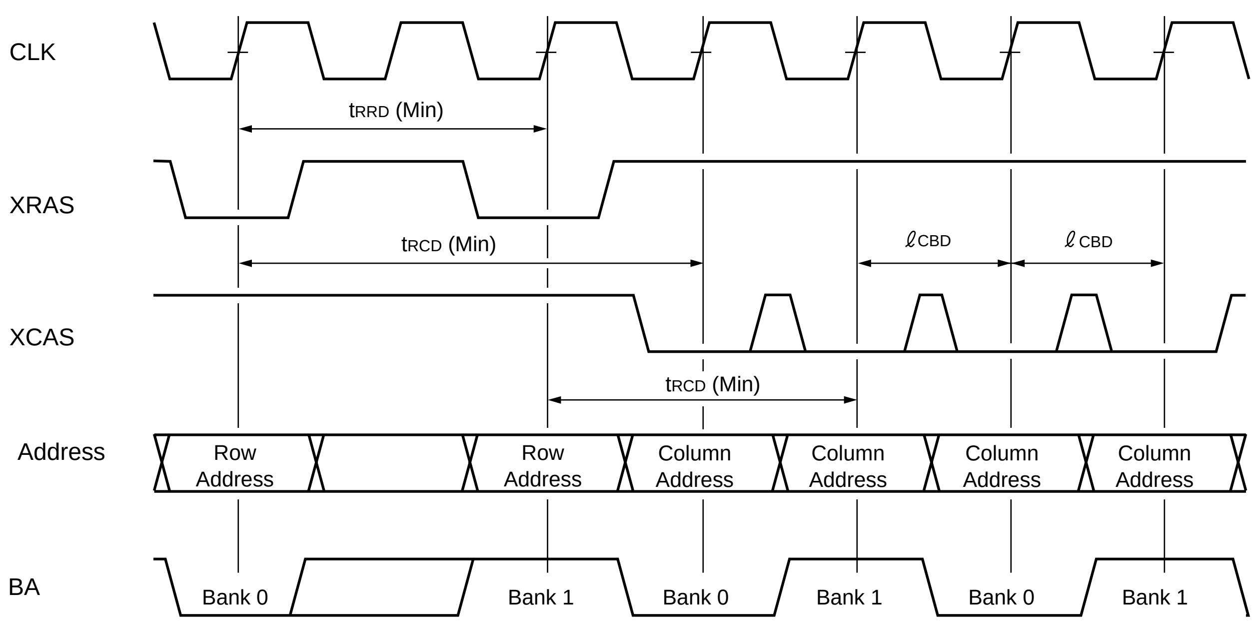
*3: The ACTV command can be latched after t_{SI} + 1 clock (Min) .

3. Column Address to Column Address Input Delay



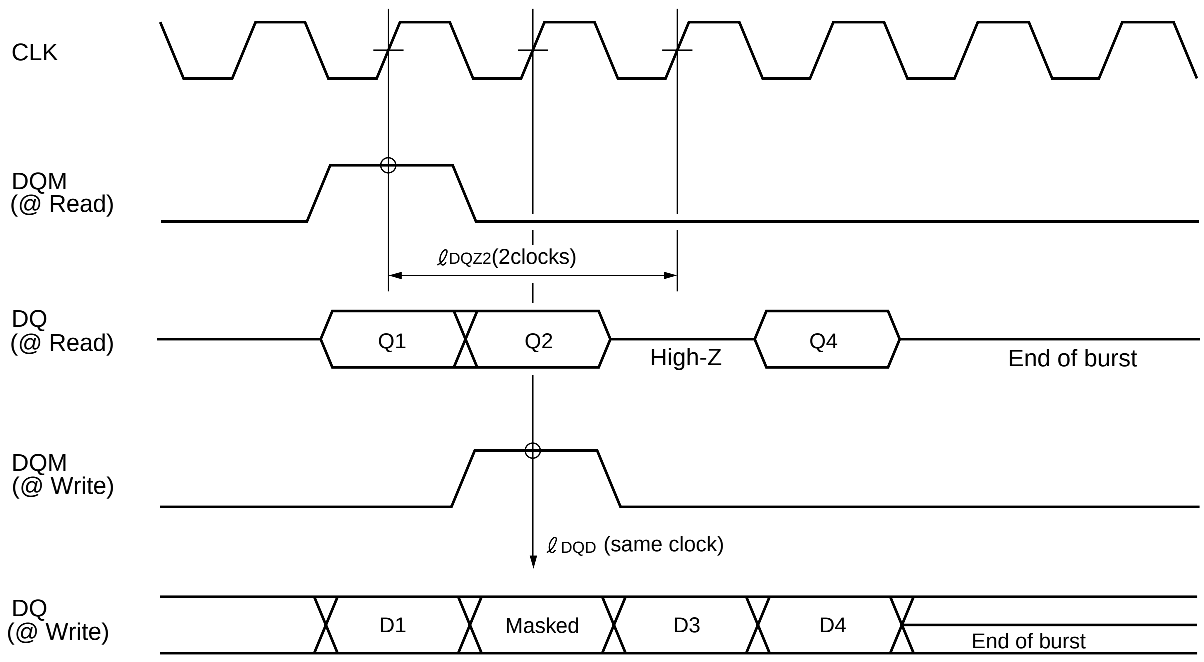
Note : XCAS to XCAS delay (ℓ CCD) can be one or more clock period.

4. Different Bank Address Input Delay

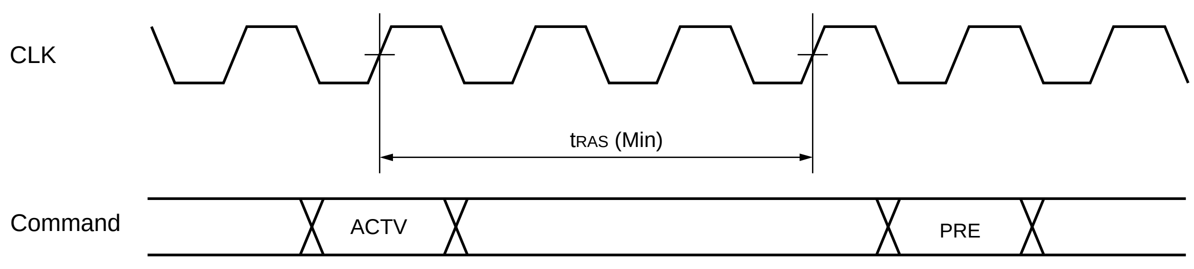


Note : XCAS Bank delay (ℓ CBD) can be one or more clock period.

5. DQM - Input Mask and Output Disable (@ CL = 2, BL = 4)

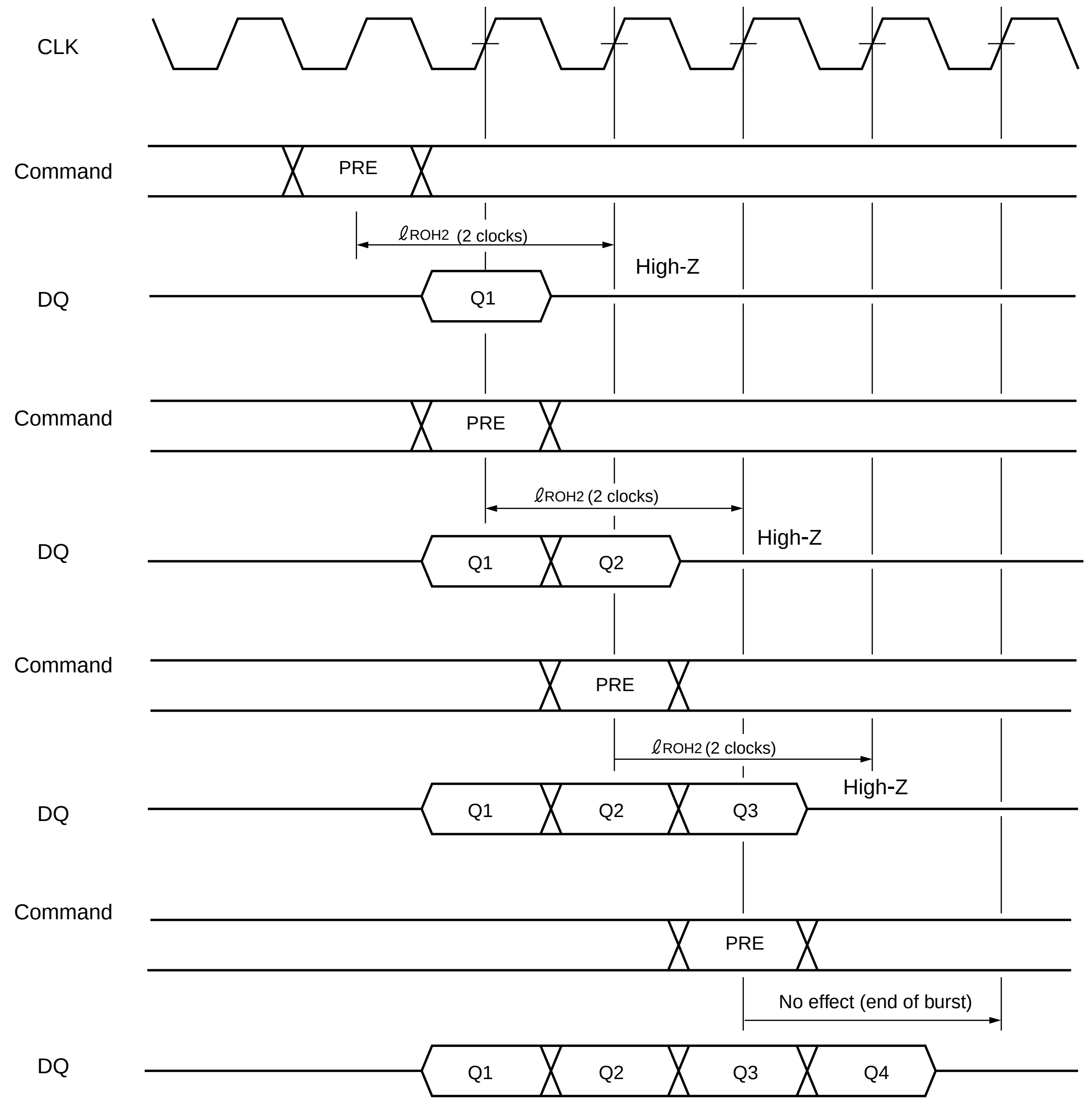


6. Precharge Timing (Applied to the Same Bank)



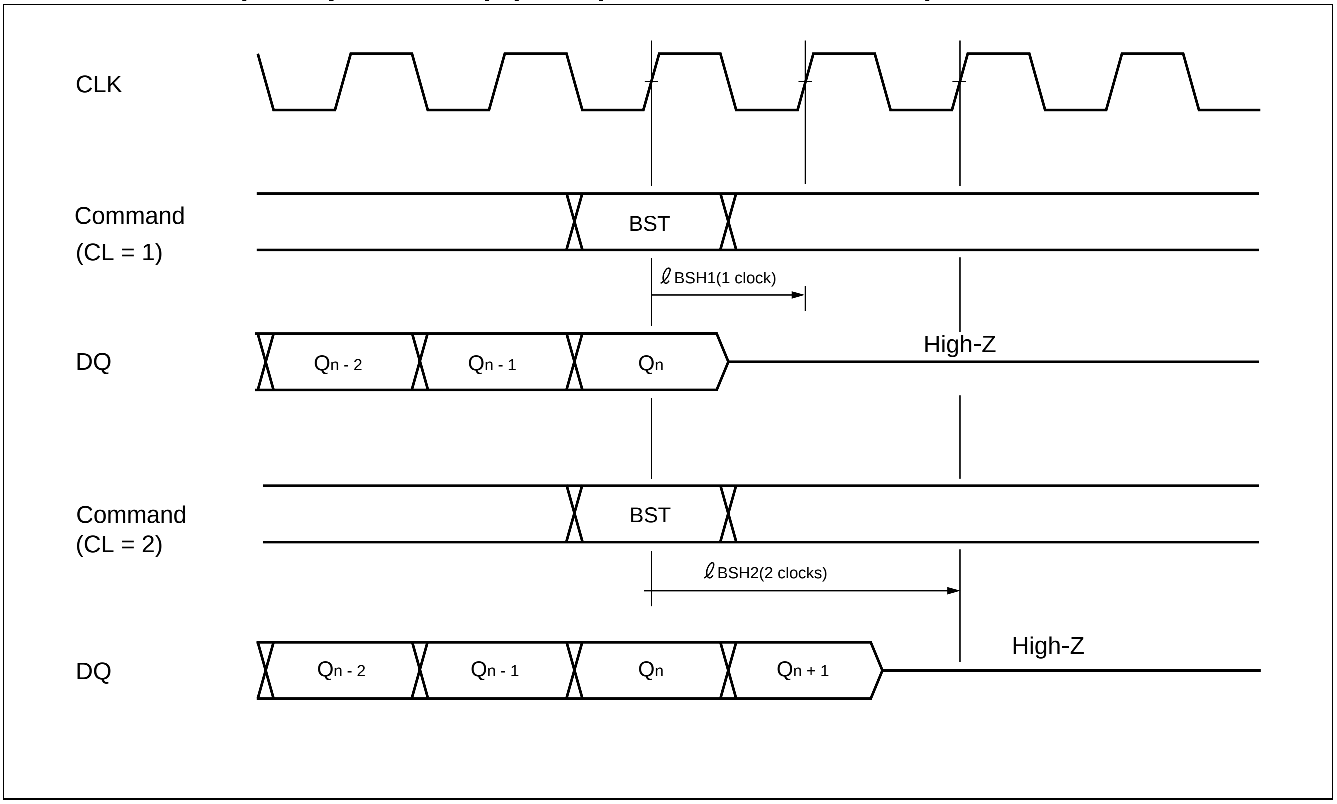
Note : PRE means 'PRE' or 'PALL'.

7. READ Interrupted by Precharge (Example @ CL = 2, BL = 4)

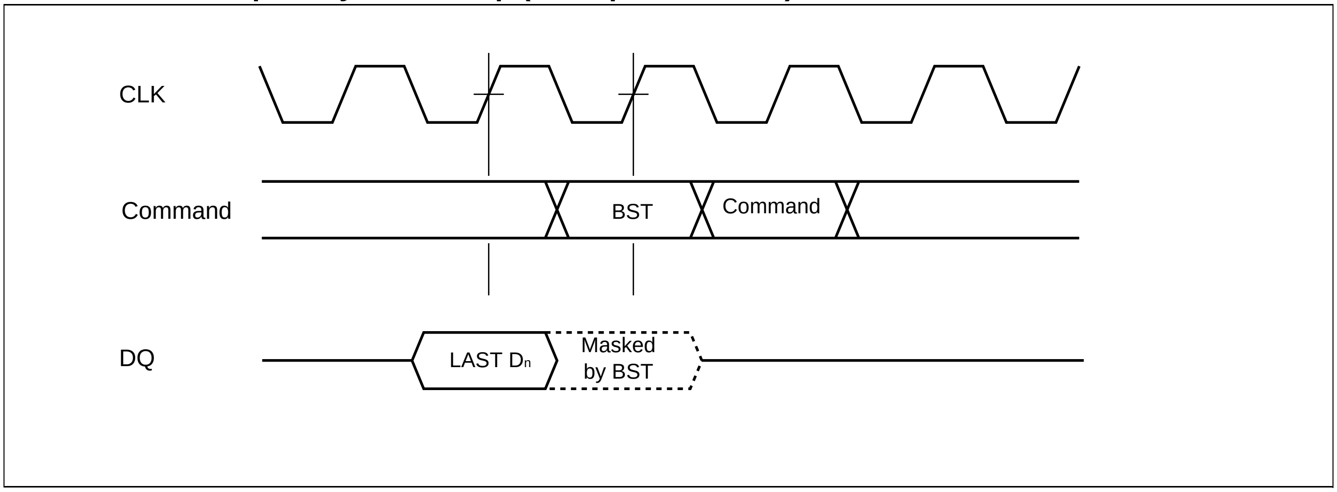


Notes :
- In case of CL = 1, the ℓ_{ROH1} is 1 clock.
- In case of CL = 2, the ℓ_{ROH2} is 2 clocks.
- PRE means ‘PRE’ or ‘PALL’.

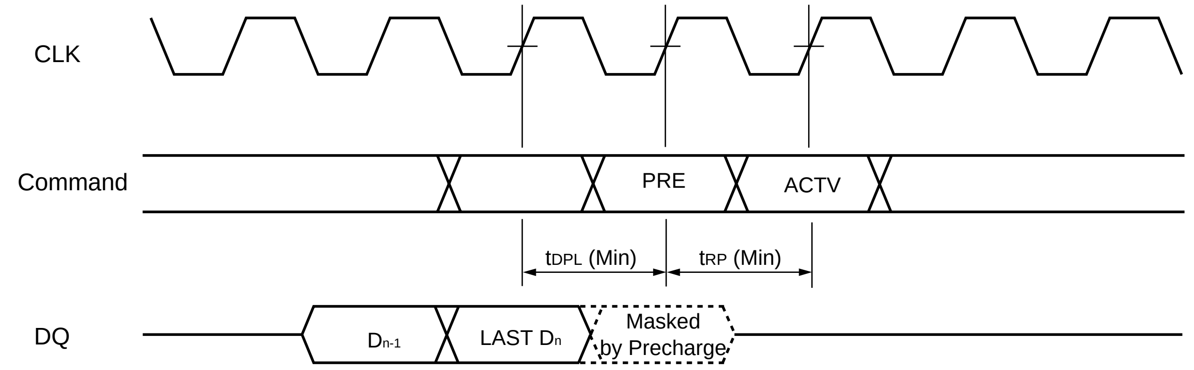
8. READ Interrupted by Burst Stop (Example @ BL = Full Column)



9. WRITE Interrupted by Burst Stop (Example @ BL = 2)

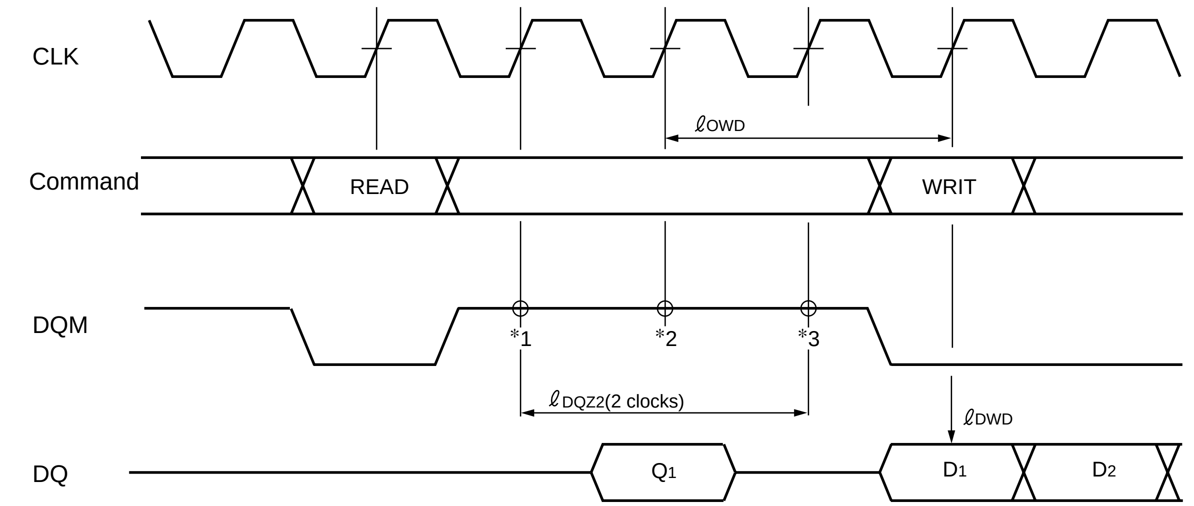


10. WRITE Interrupted by Precharge



Note : The precharge command (PRE) should be issued only after the t_{DPL} of final data input is satisfied. PRE means 'PRE' or 'PALL'.

11. READ Interrupted by WRITE (Example @ CL = 2, BL = 4)

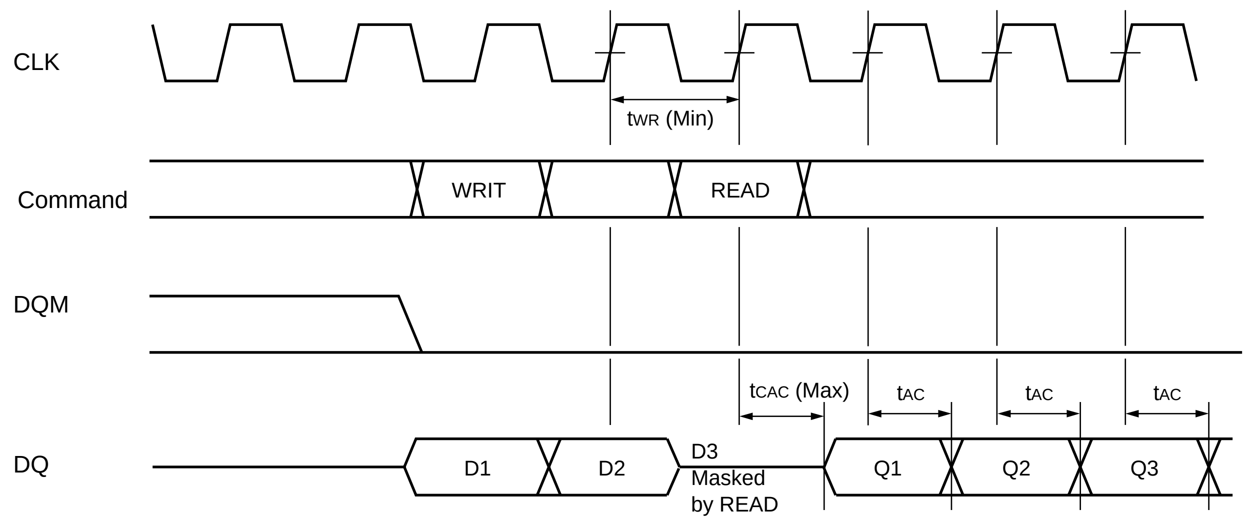


*1: The First DQM makes high-impedance state High-Z between the last output and the first input data.

*2: The Second DQM makes internal output data mask to avoid bus contention.

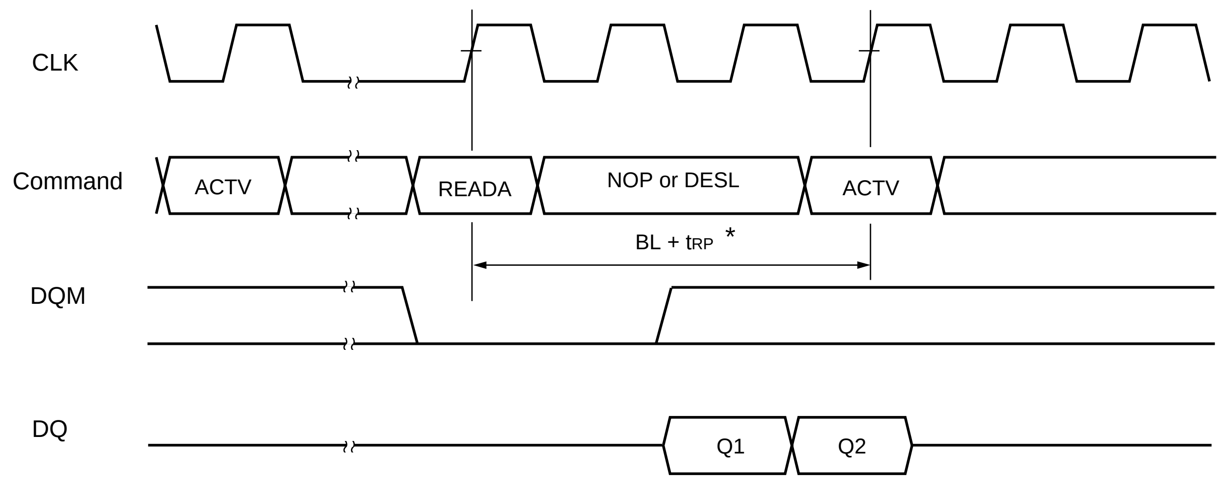
*3: The Third DQM in illustrated above also makes internal output data mask. If burst read ends (the final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

12. WRITE to READ Timing (Example @ CL = 1, BL = 4)



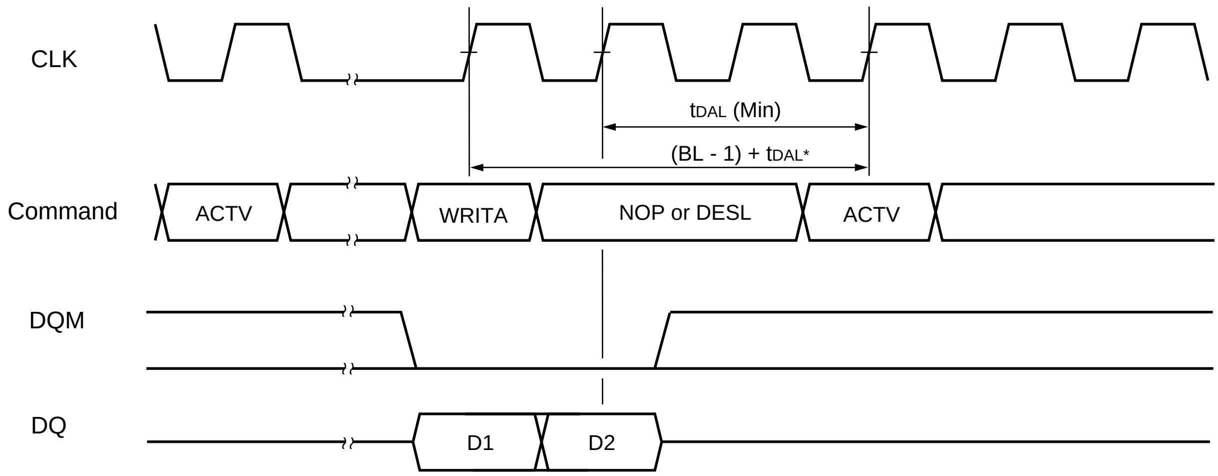
Notes : • The Read command should be issued after t_{WR} of the final data input is satisfied.
• The write data after the READ command is masked by the READ command.

13. READ with Auto-Precharge (Example @ CL = 2, BL = 2 Applied to same bank)



*: The Next ACTV command should be issued after BL + t_{RP} from the READA command.

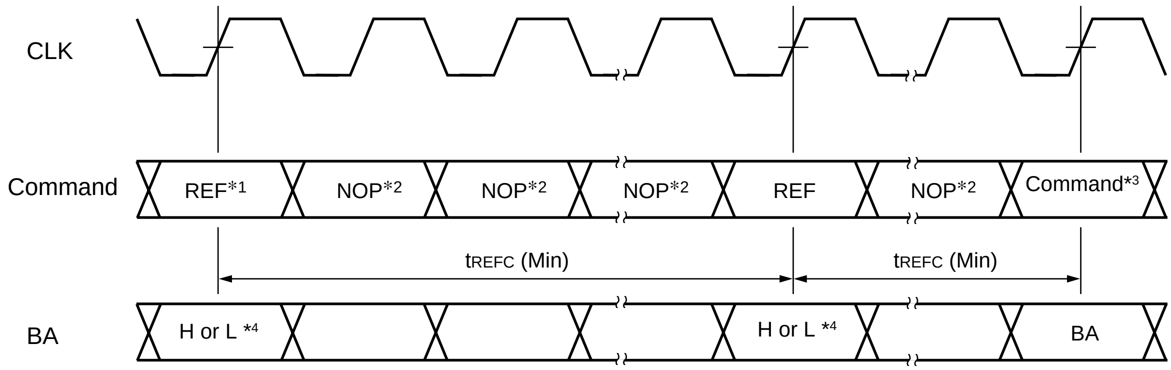
14. WRITE With Auto-Precharge (Example @ CL = 2, BL = 2 Applied to same bank)



*: The Next command should be issued after (BL – 1) + t_{DAL} from the WRITA command.

Notes:
- If the final data is masked by DQM, the precharge does not start at the clock of the final data input.
- Once the auto precharge command is asserted, no new command within the same bank can be issued.
- The Auto-precharge command can not be invoked at full column burst operation.

15. Auto-Refresh Timing



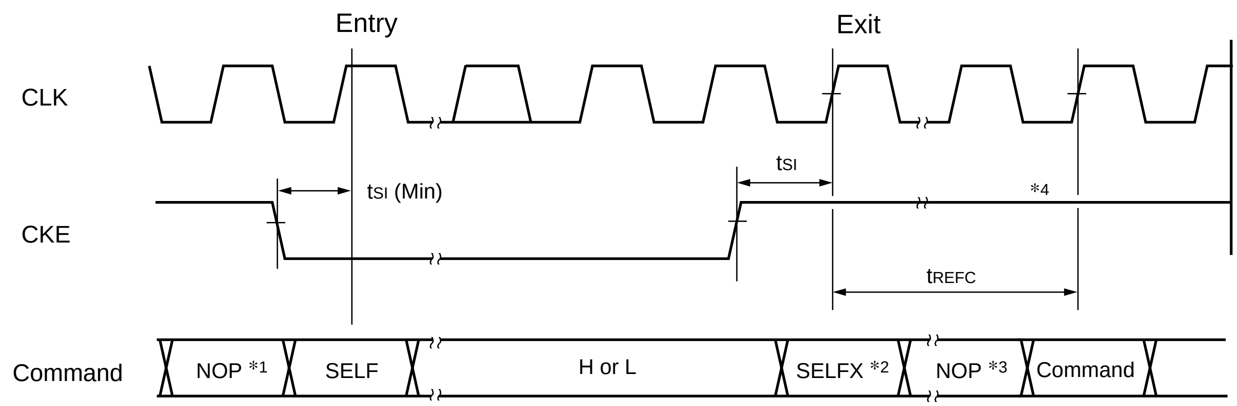
*1: All banks should be precharged prior to the first Auto-refresh command (REF) .

*2: Either the NOP or DESL command should be asserted within t_{REFC} period while Auto-refresh mode.

*3: Any activation command such as the ACTV or MRS commands other than the REF command should be asserted after t_{REFC} from the last REF command.

*4: Bank select is ignored at REF command. The refresh address and bank select are selected by the internal refresh counter.

16. Self-Refresh Entry and Exit Timing



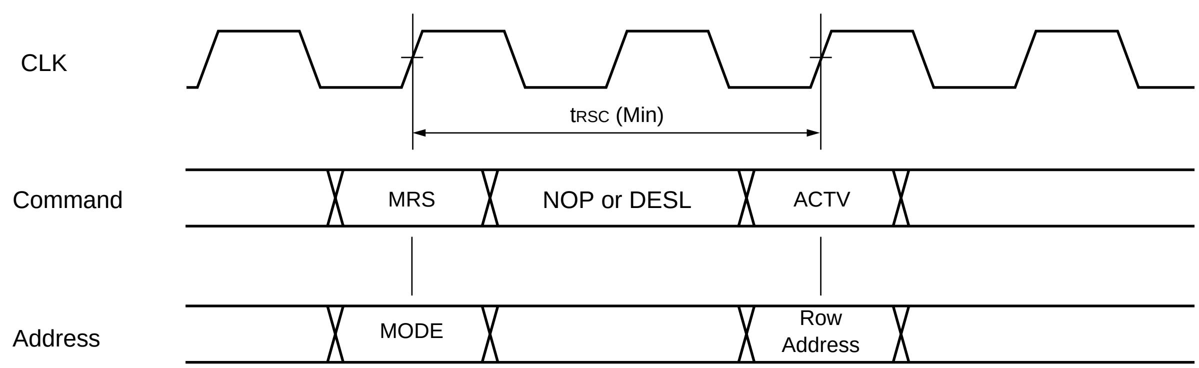
*1: The Precharge command (PRE or PALL) should be asserted if any bank is active prior to the Self-refresh Entry command (SELF) .

*2: The Self-refresh Exit command (SELFX) is latched after t_{SI}.

*3: Either the NOP or DESL command can be used during t_{REFC} period.

*4: CKE should be held high for at least one t_{REFC} period after t_{SI}.

17. Mode Register Set Timing



Note : The Mode Register Set command (MRS) should be asserted only after all banks have been precharged and DQ is in High-Z.

■ ORDERING INFORMATION

Part number	Configuration	Shipping form	Remarks
MB81ES171625-12WFKT	512 K word × 16 bit × 2 bank	Wafer	
MB81ES171625-15WFKT	512 K word × 16 bit × 2 bank	Wafer	
MB81ES173225-12WFKT	256 K word × 32 bit × 2 bank	Wafer	
MB81ES173225-15WFKT	256 K word × 32 bit × 2 bank	Wafer	

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