M66255FP

8192 × 10-BIT LINE MEMORY (FIFO)

DESCRIPTION

The M66255FP is a high-speed line memory with a FIFO (First In First Out) structure of 8192-word × 10-bit configuration which uses high-performance silicon gate CMOS process technology.
It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

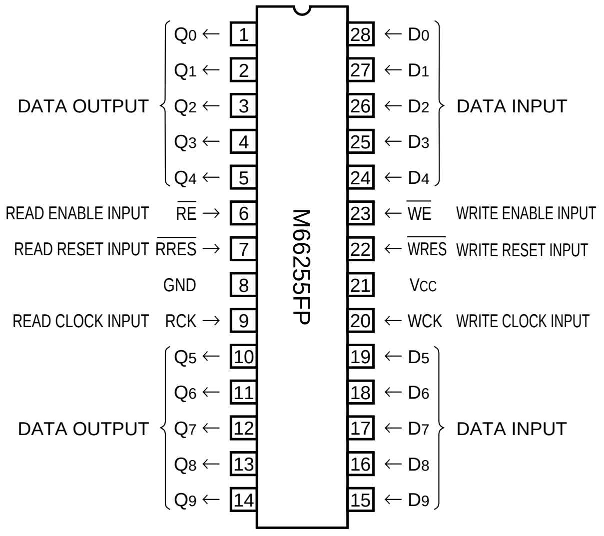
FEATURES

- Memory configuration of 8192 words × 10 bits (dynamic memory)
- High-speed cycle .... 30ns (Min.)
- High-speed access .... 25ns (Max.)
- Output hold .... 5ns (Min.)
- Fully independent, asynchronous write and read operations
- Variable length delay bit
- Output ....3 states

APPLICATION

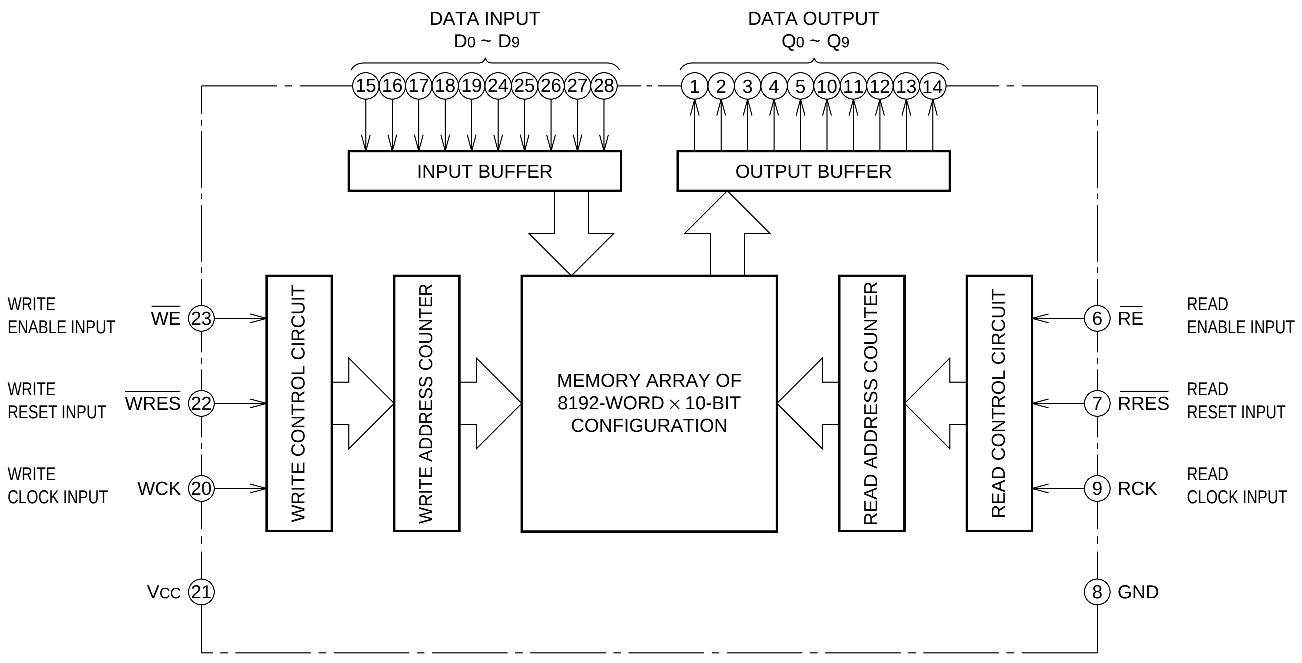
Digital photocopiers, high-speed facsimile, laser beam printers.

PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C

BLOCK DIAGRAM



FUNCTION

When write enable input $\overline{WE}$ is “L”, the contents of data inputs D_0 to D_9 are written into memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter is also incremented simultaneously.
The write functions given below are also performed in synchronization with rise edge of WCK.
When $\overline{WE}$ is “H”, a write operation to memory is inhibited and the write address counter is stopped.
When write reset input $\overline{WRES}$ is “L”, the write address counter is initialized.

When read enable input $\overline{RE}$ is “L”, the contents of memory are output to data outputs Q_0 to Q_9 in synchronization with rise edge of read clock input RCK. At this time, the read address counter is also incremented simultaneously.
The read functions given below are also performed in synchronization with rise edge of RCK.
When $\overline{RE}$ is “H”, a read operation from memory is inhibited and the read address counter is stopped. The outputs are in the high impedance state.
When read reset input $\overline{RRES}$ is “L”, the read address counter is initialized.

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	A value based on GND pin	–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
P_d	Maximum power dissipation	T_a = 25°C	825 (Note 1)	mW
T_{stg}	Storage temperature		–65 ~ 150	°C

Note 1: $T_a \geq$ 40°C are derated at –9.7mW/°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
T_{opr}	Operating ambient temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	“H” input voltage			2.0			V
V_{IL}	“L” input voltage					0.8	V
V_{OH}	“H” output voltage	I_{OH} = –4mA		V_{CC}–0.8			V
V_{OL}	“L” output voltage	I_{OL} = 4mA				0.55	V
I_{IH}	“H” input current	V_I = V_{CC}	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 ~ D_9			1.0	μA
I_{IL}	“L” input current	V_I = GND	$\overline{WE}$, $\overline{WRES}$, WCK, $\overline{RE}$, $\overline{RRES}$, RCK, D_0 ~ D_9			–1.0	μA
I_{OZH}	Off state “H” output current	V_O = V_{CC}				5.0	μA
I_{OZL}	Off state “L” output current	V_O = GND				–5.0	μA
I_{CC}	Operating mean current dissipation	V_I = V_{CC}, GND, Output open t_{WCK}, t_{RCK} = 30ns				150	mA
C_I	Input capacitance	f = 1MHz				10	pF
C_O	Off state output capacitance	f = 1MHz				15	pF

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V)

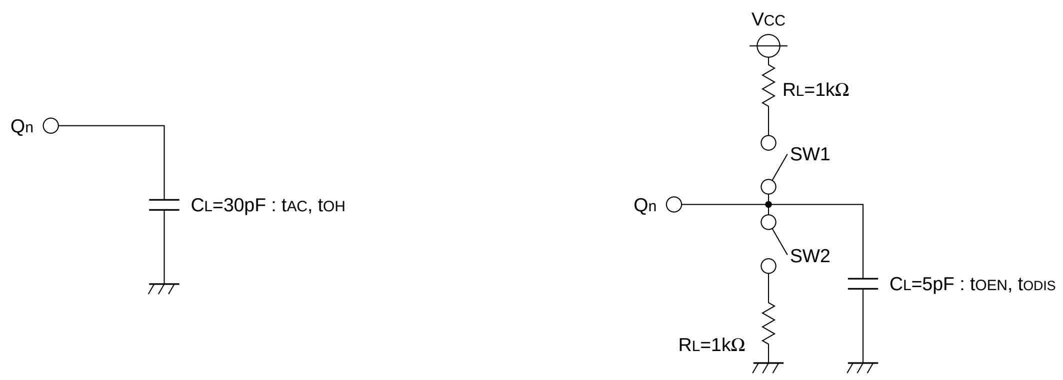
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Access time			25	ns
t_{OH}	Output hold time	5			ns
t_{OEN}	Output enable time	5		25	ns
t_{ODIS}	Output disable time	5		25	ns

TIMING CONDITIONS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle	30			ns
t_{WCKH}	Write clock (WCK) “H” pulse width	12			ns
t_{WCKL}	Write clock (WCK) “L” pulse width	12			ns
t_{RCK}	Read clock (RCK) cycle	30			ns
t_{RCKH}	Read clock (RCK) “H” pulse width	12			ns
t_{RCKL}	Read clock (RCK) “L” pulse width	12			ns
t_{DS}	Input data setup time to WCK	5			ns
t_{DH}	Input data hold time to WCK	5			ns
t_{RESS}	Reset setup time to WCK or RCK	5			ns
t_{RESH}	Reset hold time to WCK or RCK	5			ns
t_{NRESS}	Reset nonselect setup time to WCK or RCK	5			ns
t_{NRESH}	Reset nonselect hold time to WCK or RCK	5			ns
t_{WES}	$\overline{WE}$ setup time to WCK	5			ns
t_{WEH}	$\overline{WE}$ hold time to WCK	5			ns
t_{NWES}	$\overline{WE}$ nonselect setup time to WCK	5			ns
t_{NWEH}	$\overline{WE}$ nonselect hold time to WCK	5			ns
t_{RES}	$\overline{RE}$ setup time to RCK	5			ns
t_{REH}	$\overline{RE}$ hold time to RCK	5			ns
t_{NRES}	$\overline{RE}$ nonselect setup time to RCK	5			ns
t_{NREH}	$\overline{RE}$ nonselect hold time to RCK	5			ns
t_r, t_f	Input pulse rise/fall time			20	ns
t_H	Data hold time (Note 1)			20	ms

Notes 1: For 1-line access, the following should be satisfied:
$\overline{WE}$ “H” level period ≤ 20ms – 8192 t_{WCK} – $\overline{WRES}$ “L” level period
$\overline{RE}$ “H” level period ≤ 20ms – 8192 t_{RCK} – $\overline{RRES}$ “L” level period
2: Perform reset operation after turning on power supply.

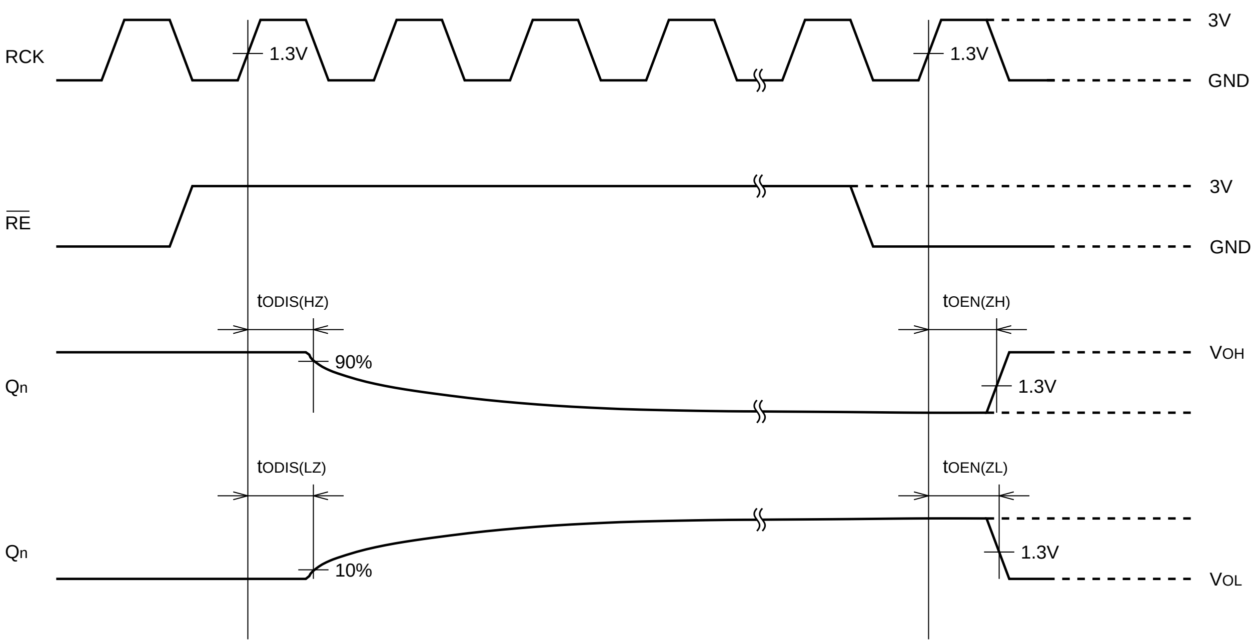
TEST CIRCUIT



Input pulse level : 0 ~ 3V
Input pulse rise/fall time : 3ns
Decision voltage input : 1.3V
Decision voltage output : 1.3V (However, $t_{ODIS(LZ)}$ is 10% of output amplitude and $t_{ODIS(HZ)}$ is 90% of that for decision).
The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

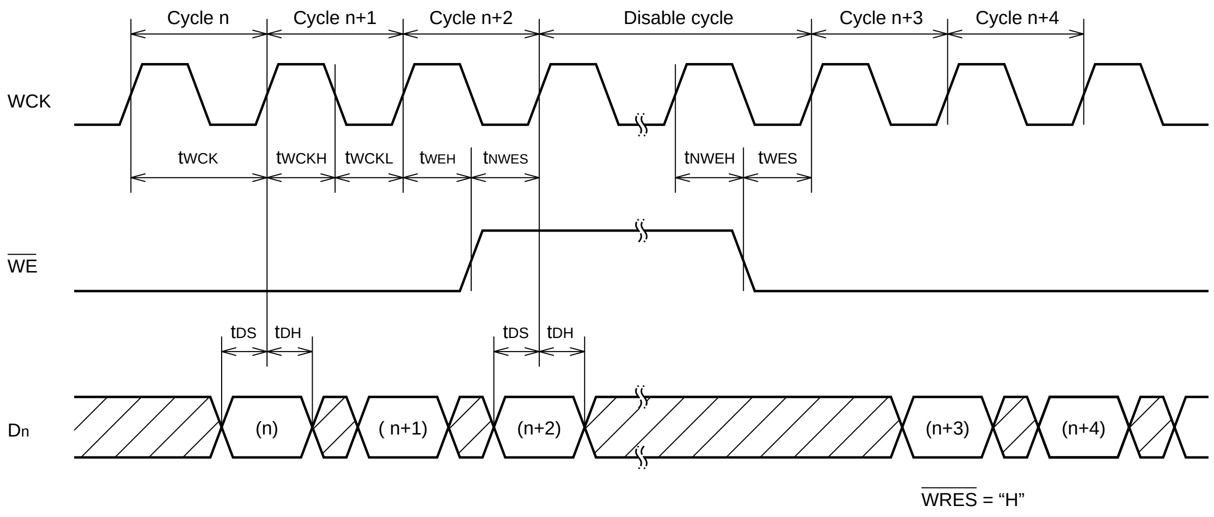
Parameter	SW1	SW2
$t_{ODIS(LZ)}$	Closed	Open
$t_{ODIS(HZ)}$	Open	Closed
$t_{OEN(ZL)}$	Closed	Open
$t_{OEN(ZH)}$	Open	Closed

t_{ODIS}/t_{OEN} TEST CONDITION

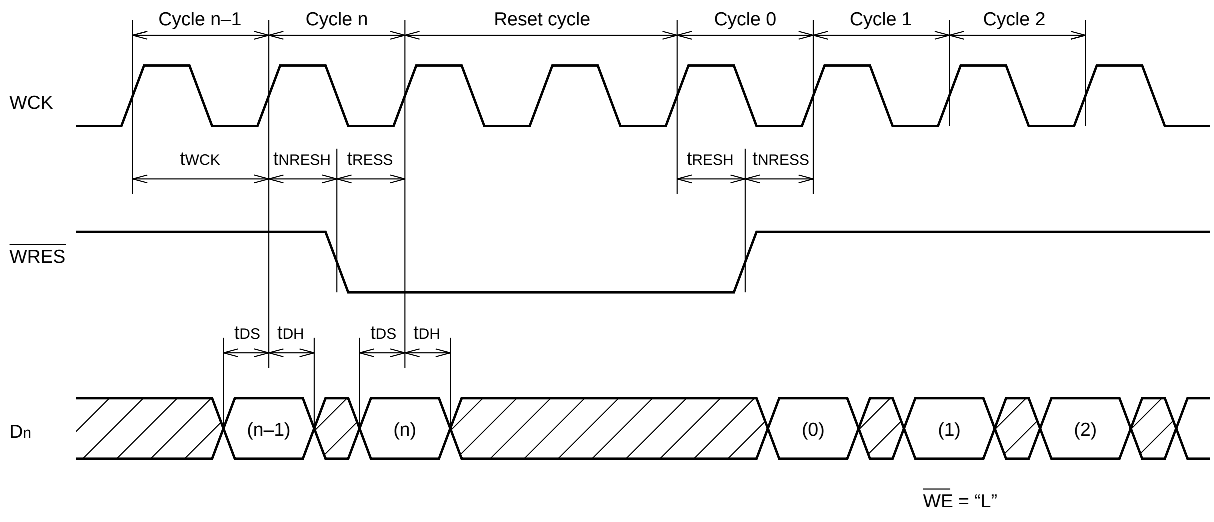


OPERATING TIMING

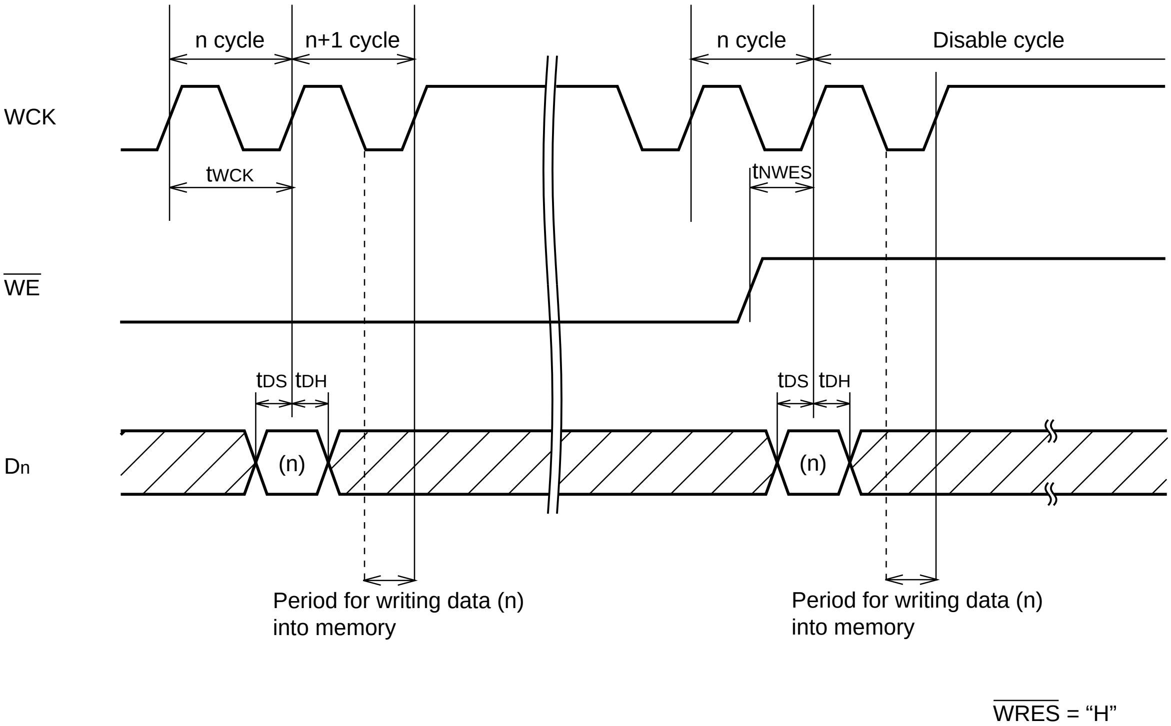
• Write cycle



• Write reset cycle

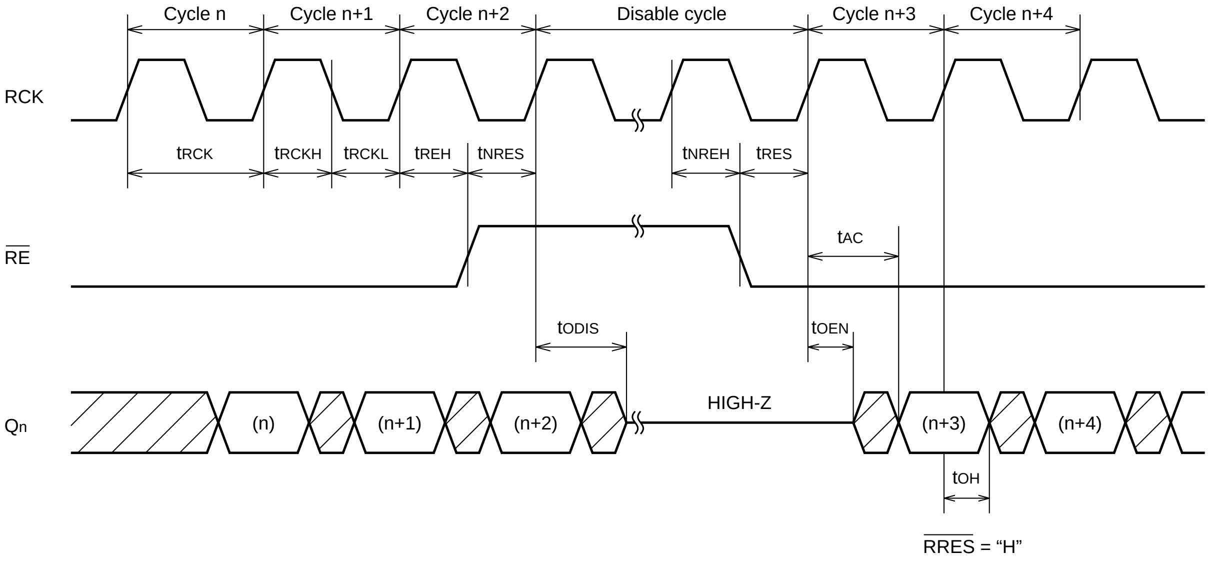


• Matters that needs attention when WCK stops

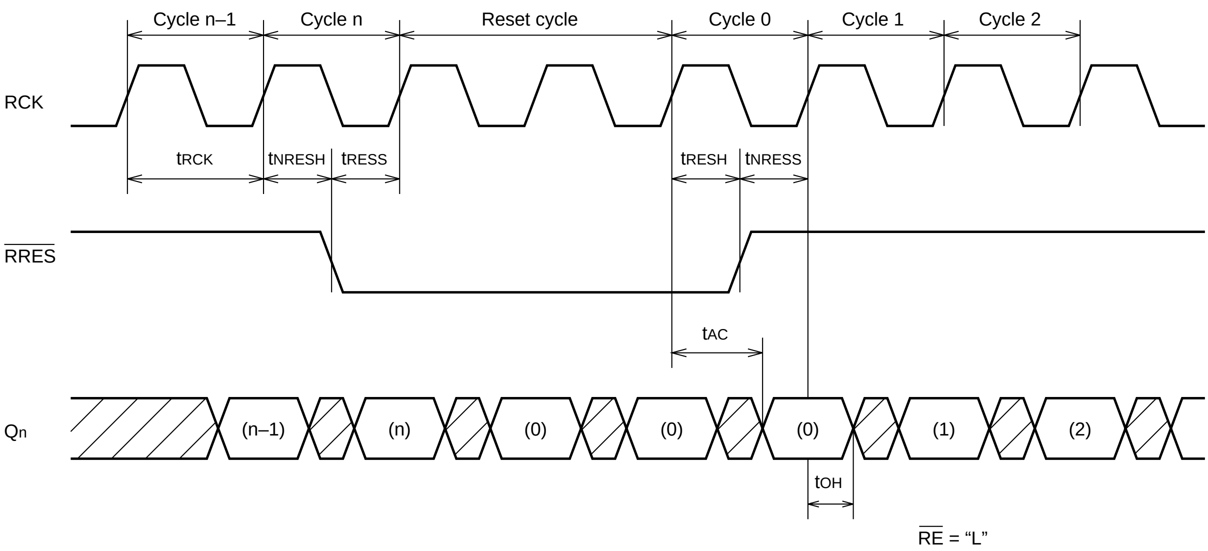


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n+1 cycle. The writing operation is complete at the falling edge after n+1 cycle.
To stop reading write data at n cycle, enter WCK before the rising edge after n+1 cycle.
When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

• Read cycle



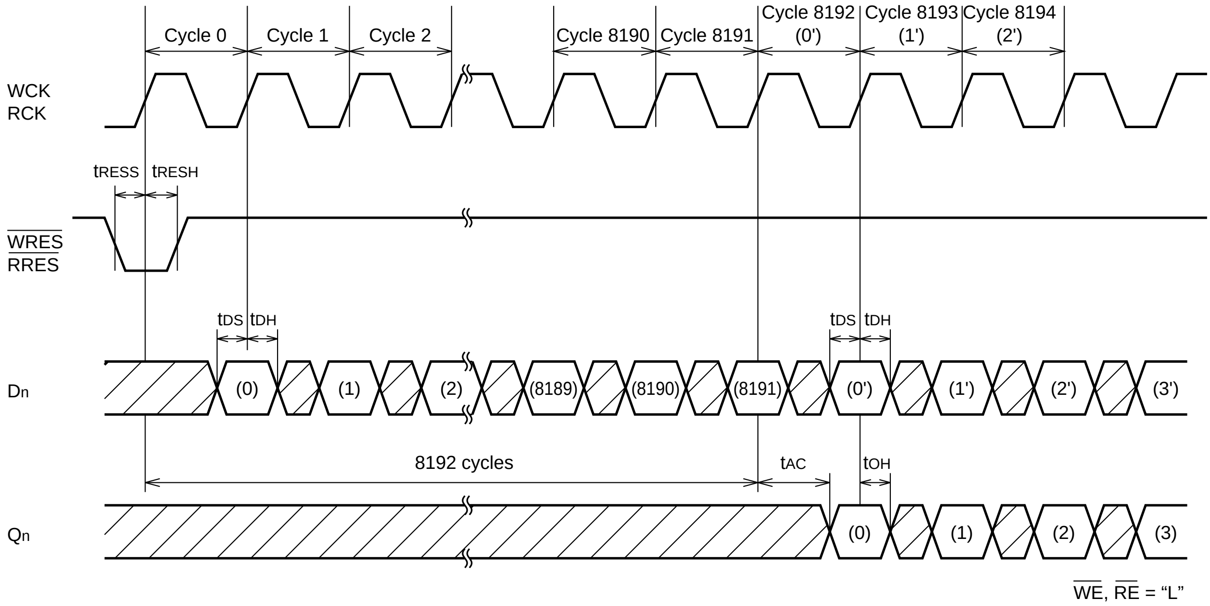
• Read reset cycle



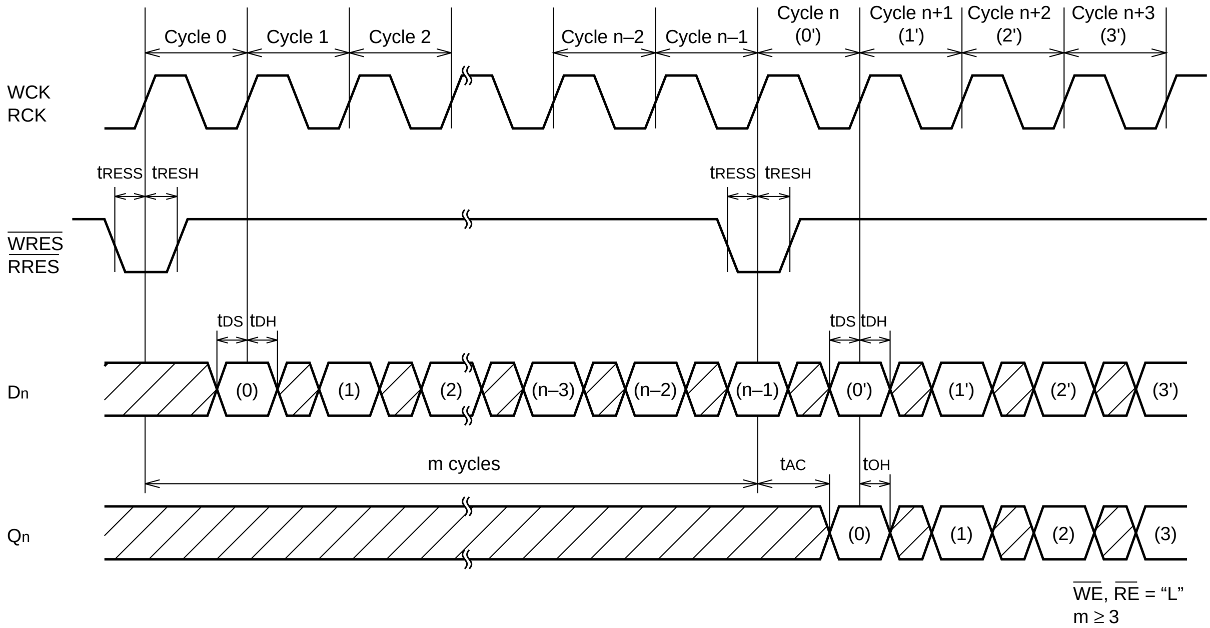
VARIABLE LENGTH DELAY BITS

• 1-line (8192 bits) delay

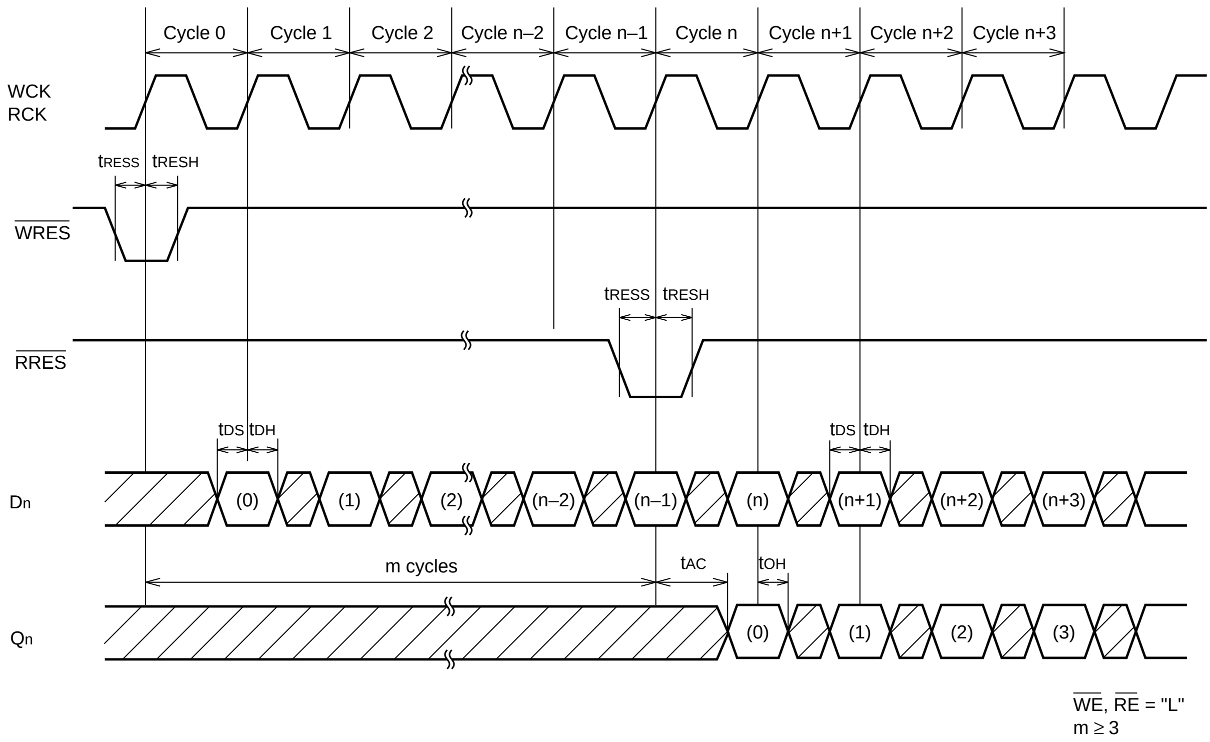
A write input data is written into memory at the second rise edge of WCK in the cycle, and a read output data is output from memory at the first rise edge of RCK in the cycle, so that 1-line delay can be made easily.



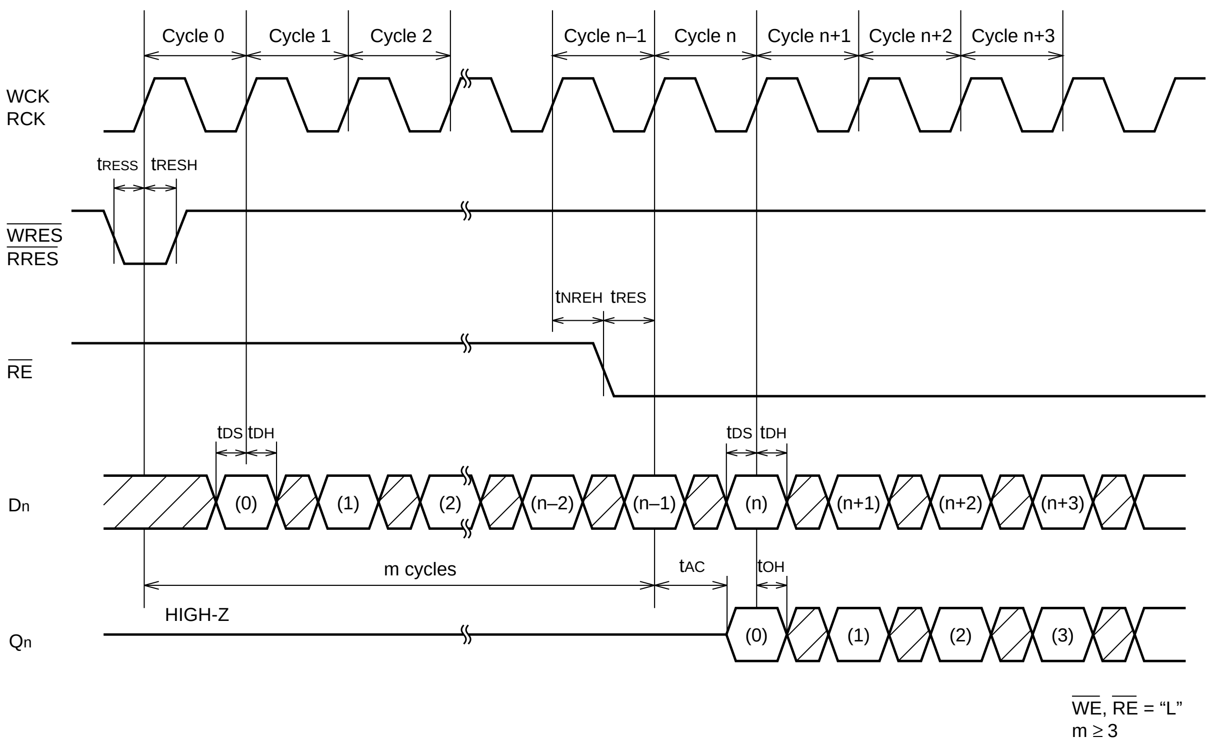
• N-bit delay bit
(Making a reset at a cycle corresponding to delay length)



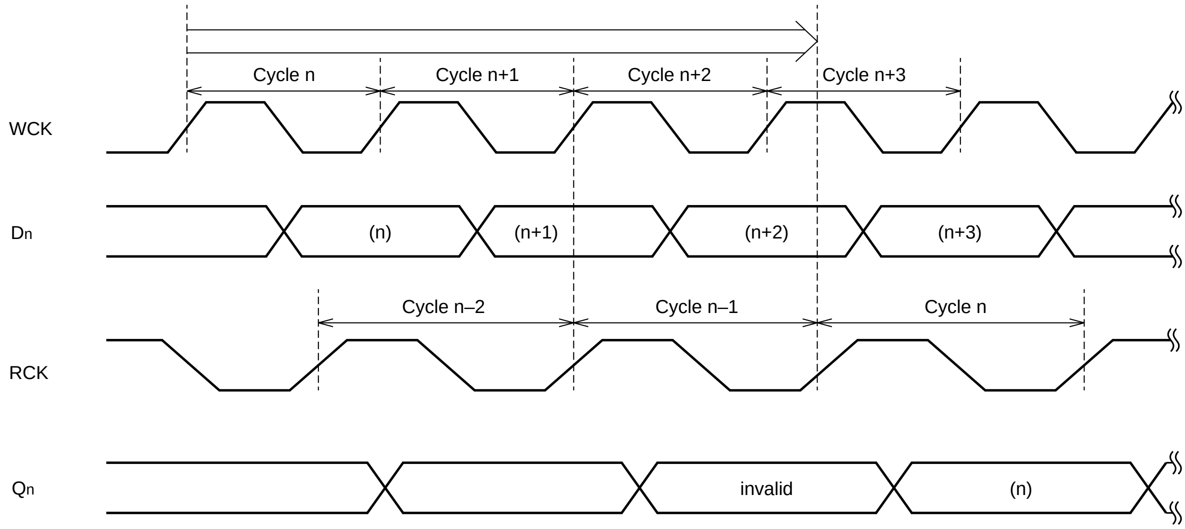
• N-bit delay 2
(Sliding $\overline{\text{WRES}}$ and $\overline{\text{RRES}}$ at a cycle corresponding to delay length)



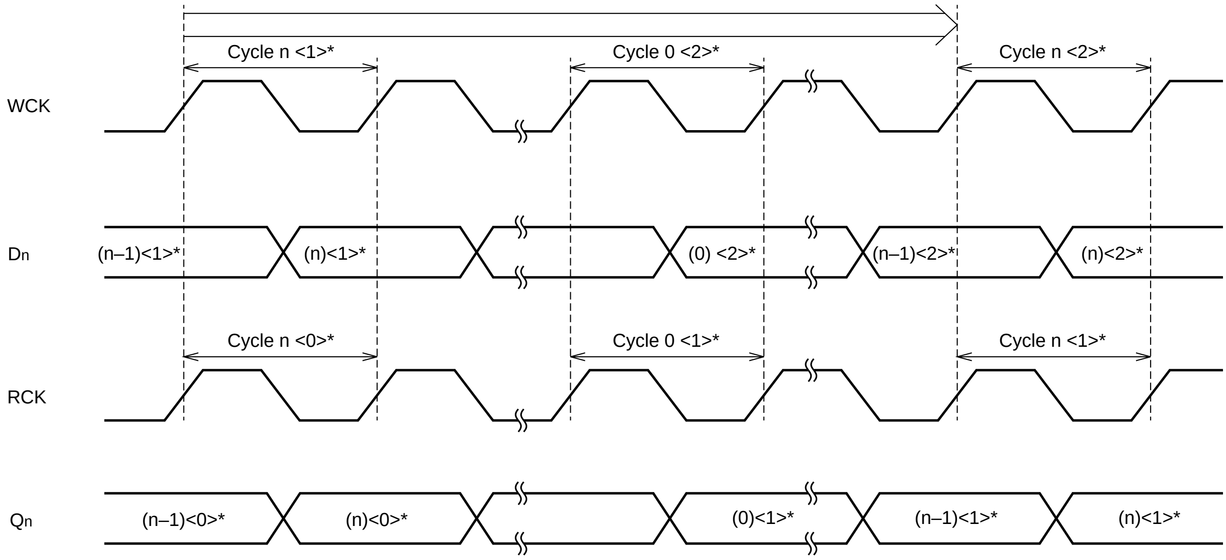
• N-bit delay 3
(Disabling $\overline{\text{RE}}$ at a cycle corresponding to delay length)



• Shortest read of data “n” written in cycle n
  Cycle n–1 on read side should be started after end of cycle n+1 on write side
When the start of cycle n–1 on read side is earlier than the end of cycle n+1 on write side, output Q_n of cycle n becomes invalid.
In the figure shown below, the read of cycle n–1 is invalid.



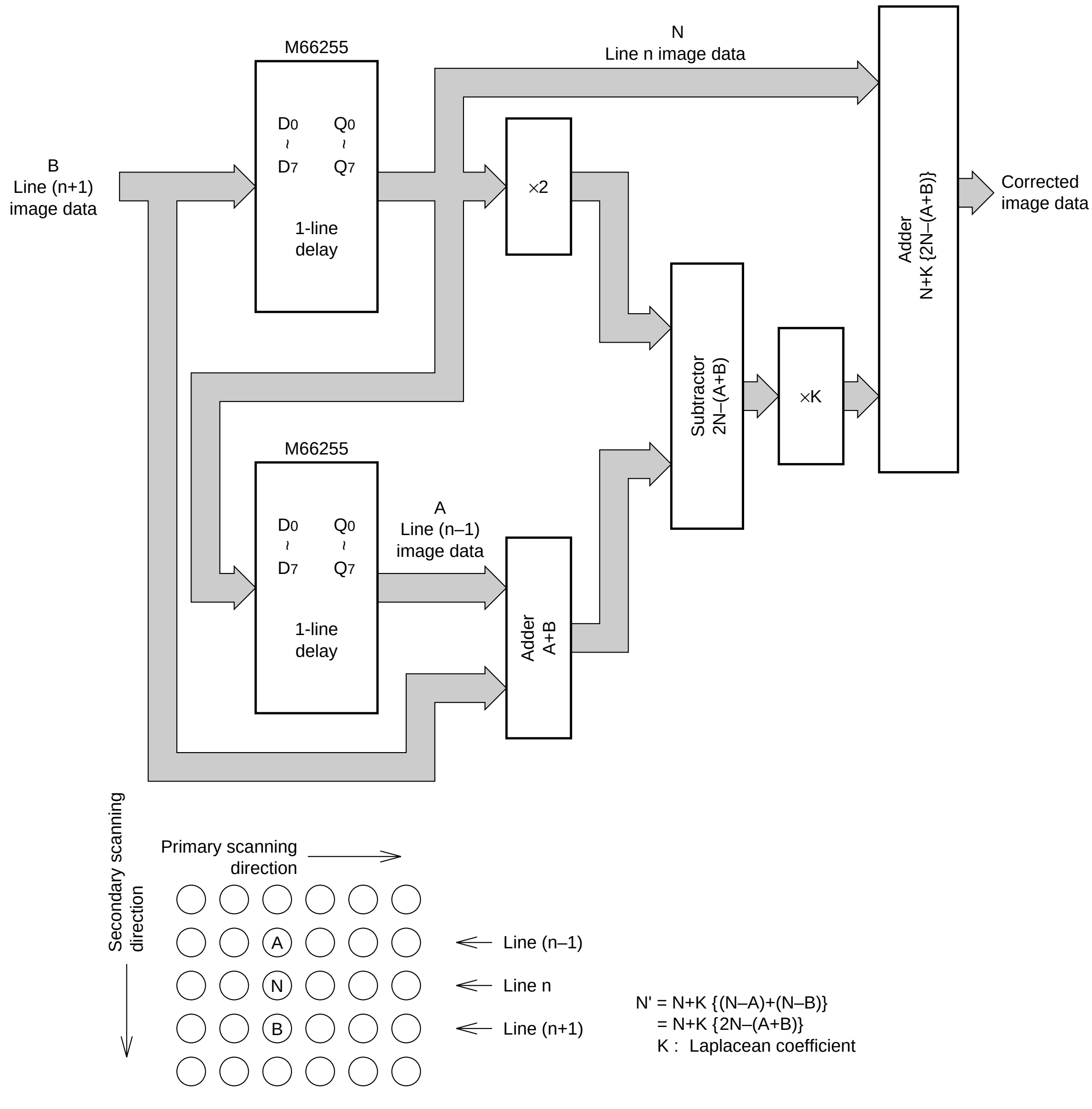
• Longest read of data “n” written in cycle n: 1-line delay
  Cycle n <1>* on read side should be started when cycle n <2>* on write is started
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1>* and the start of writing side n cycle <2>* overlap each other.



<0>*, <1>* and <2>* indicates a line value.

APPLICATION EXAMPLE

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction.



N' = N+K {(N–A)+(N–B)}
= N+K {2N–(A+B)}
K : Laplacean coefficient