International
IOR Rectifier

PD - 91721C

REPETITIVE AVALANCHE AND dv/dt RATED

HEXFET® TRANSISTORS
SURFACE MOUNT (LCC-18)

IRFE9110
100V, P-CHANNEL

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFE9110	-100V	1.2Ω	-2.5A

LCC-18

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Desinged to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

Features:

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-2.5	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-1.6	
I_{DM}	Pulsed Drain Current ①	-10	
P_D @ T_C = 25°C	Max. Power Dissipation	15	W
	Linear Derating Factor	0.12	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	102	mJ
I_{AR}	Avalanche Current ①	-	A
E_{AR}	Repetitive Avalanche Energy ①	-	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-14	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5 S)	
	Weight	0.42(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.08	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	V_{GS} = -10V, I_D = -1.6A ④
		—	—	1.38		V_{GS} = -10V, I_D = -2.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	0.9	—	—	S (℧)	V_{DS} > -15V, I_{DS} = -1.6A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS}= -80V, V_{GS}= 0V
		—	—	-250		V_{DS} =-80V V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} =-20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} =20V
Q_g	Total Gate Charge	—	—	15	nC	V_{GS} =-10V, ID= -2.5A V_{DS} =-50V
Q_{gs}	Gate-to-Source Charge	—	—	7.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	8.0		
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	V_{DD} =-50V, I_D = -2.5A, V_{GS} =-10V, R_G =7.5Ω
t_r	Rise Time	—	—	60		
$t_{d(off)}$	Turn-Off Delay Time	—	—	40		
t_f	Fall Time	—	—	40		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	214		pF	V_{GS} = 0V, V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	100	—		
C_{rss}	Reverse Transfer Capacitance	—	20	—		

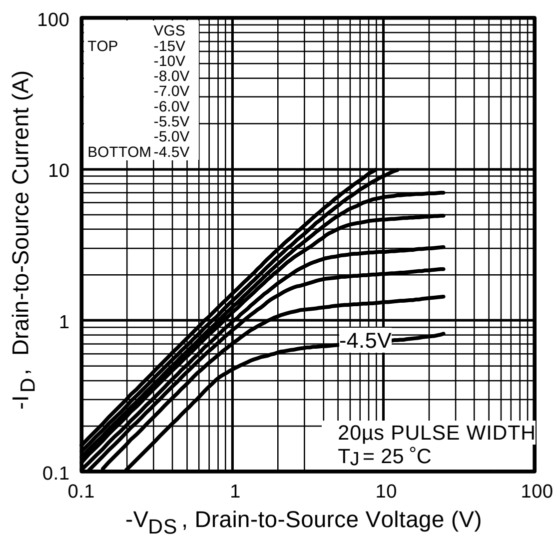
Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-10		
V_{SD}	Diode Forward Voltage	—	—	-5.5	V	T_j = 25°C, I_S = -2.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	200	nS	T_j = 25°C, I_F = -2.5A, di/dt ≤-100A/µs V_{DD} ≤ -50V ④
Q_{RR}	Reverse Recovery Charge	—	—	380	µc	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction to Case	—	—	8.3	°C/W	
$R_{thJ-PCB}$	Junction to PC Board	—	—	27		Soldered to a copper clad PC board

For footnotes refer to the last page



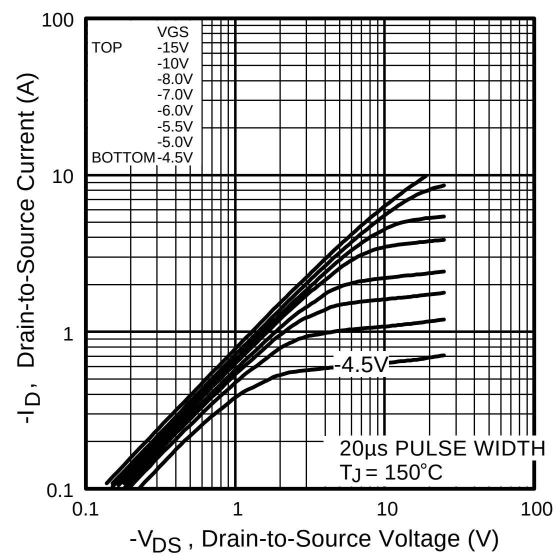


Fig 1. Typical Output Characteristics

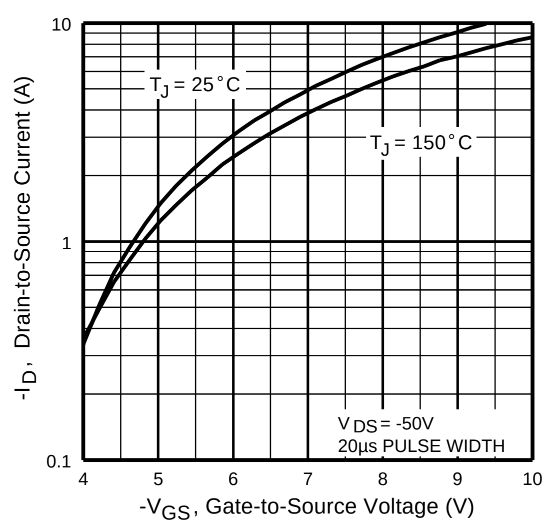


Fig 3. Typical Transfer Characteristics

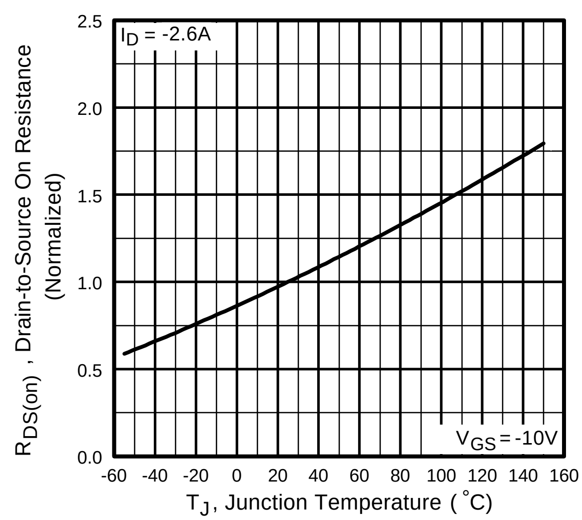


Fig 4. Normalized On-Resistance Vs. Temperature

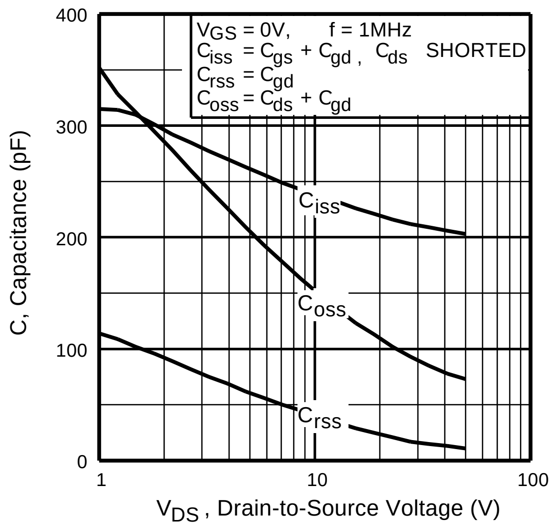


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

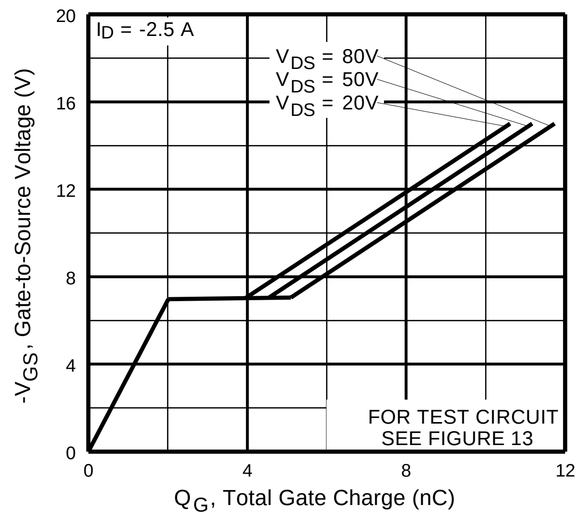


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

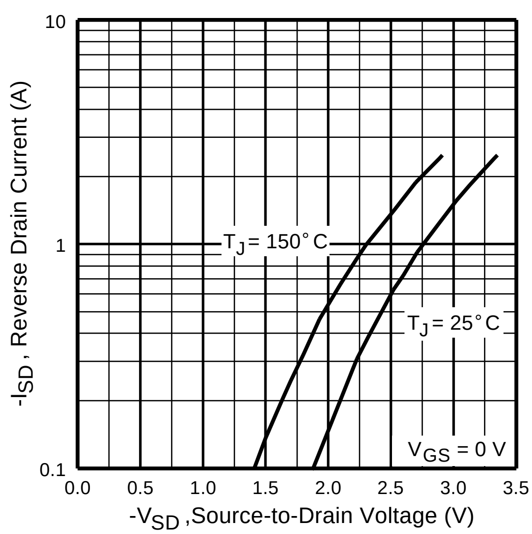


Fig 7. Typical Source-Drain Diode Forward Voltage

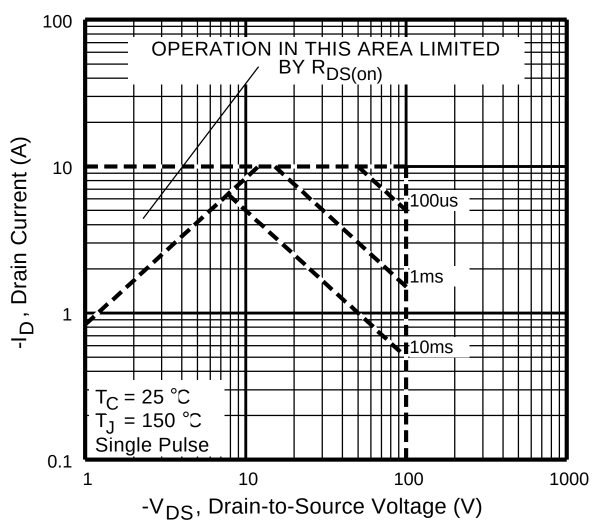


Fig 8. Maximum Safe Operating Area

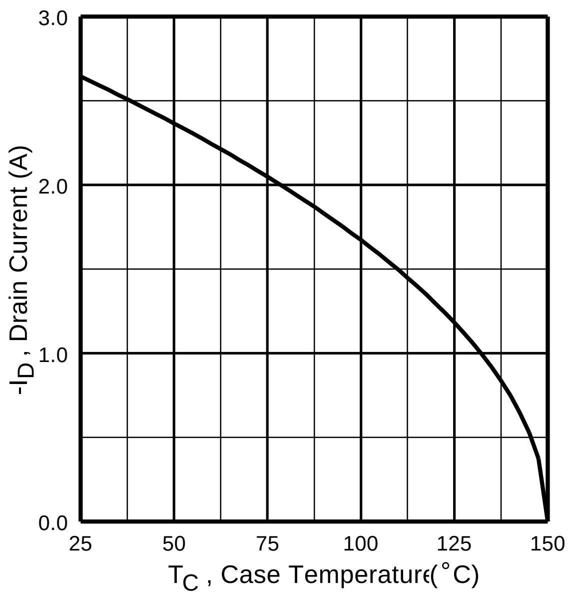


Fig 9. Maximum Drain Current Vs. Case Temperature

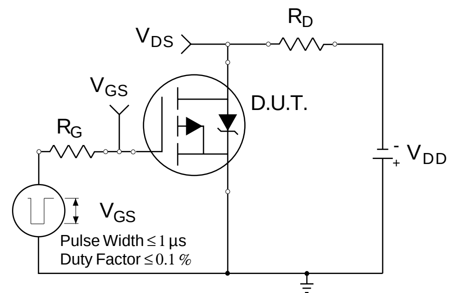


Fig 10a. Switching Time Test Circuit

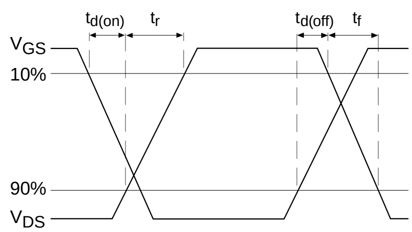


Fig 10b. Switching Time Waveforms

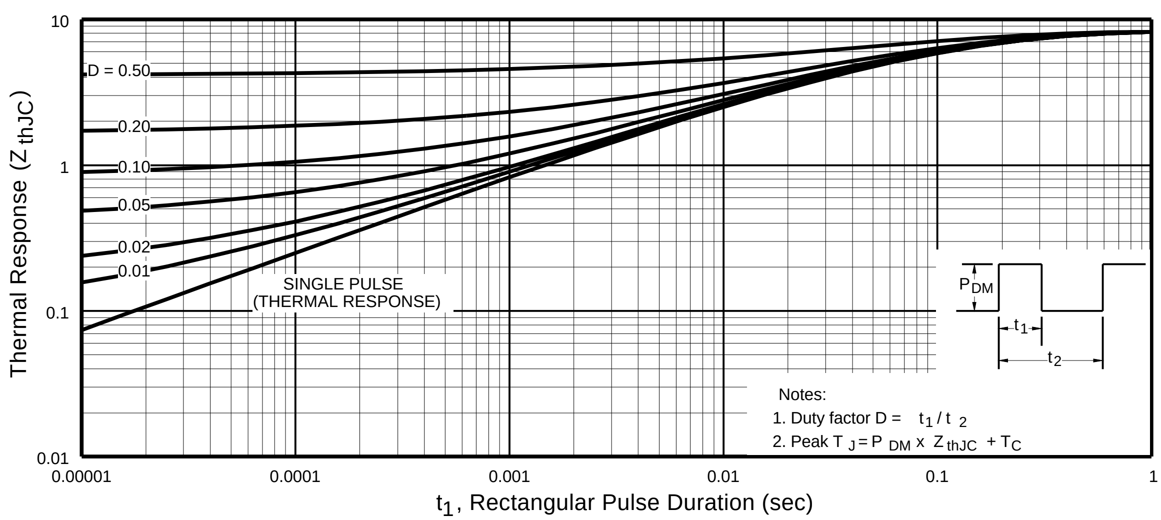


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

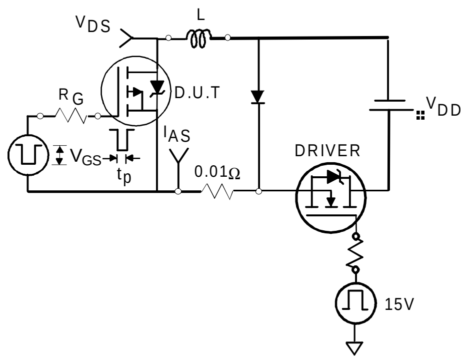


Fig 12a. Unclamped Inductive Test Circuit

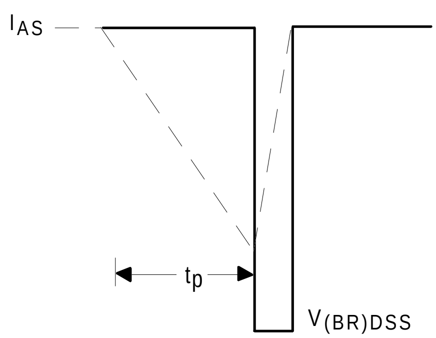


Fig 12b. Unclamped Inductive Waveforms

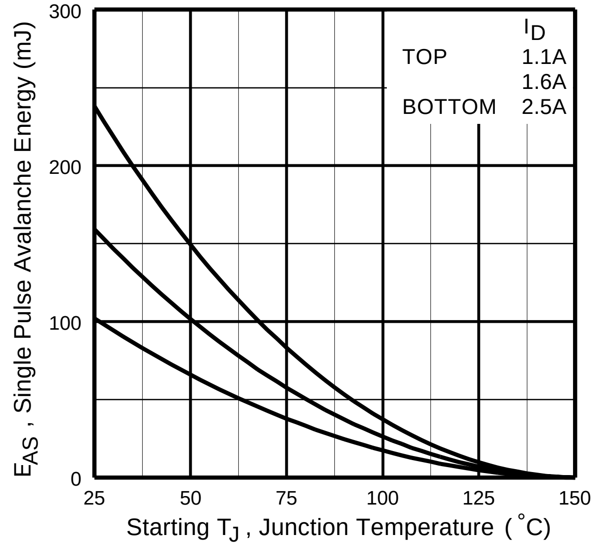


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

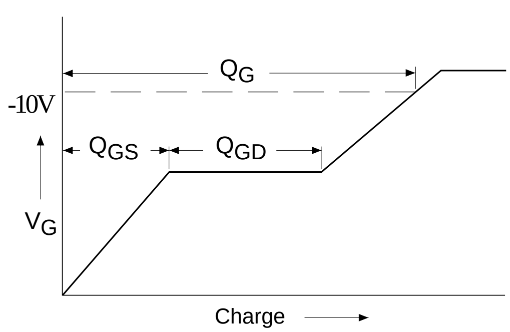


Fig 13a. Basic Gate Charge Waveform

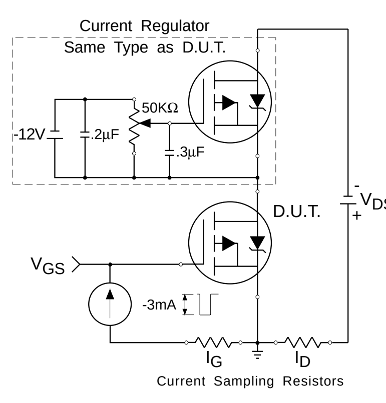


Fig 13b. Gate Charge Test Circuit

Foot Notes:

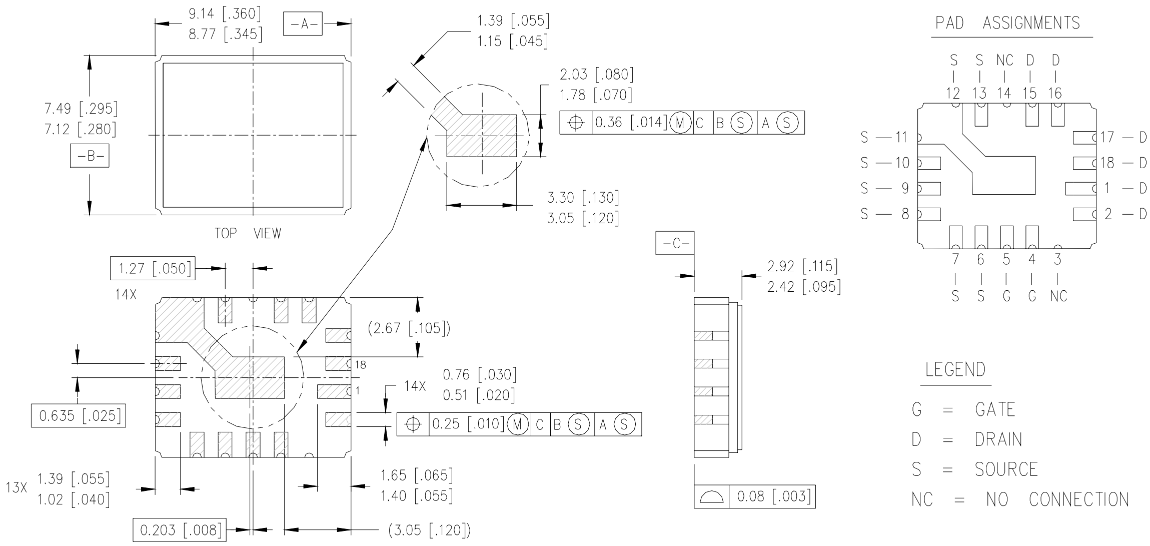
① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} =-25V, starting T_J = 25°C, Peak I_L = -2.5A, V_{GS} =- 10V

③ $I_{SD} \leq$ -2.5A, di/dt ≤– 285A/µs, $V_{DD} \leq$ -100V, $T_J \leq$ 150°C
Suggested RG =7.5 Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

Case Outline and Dimensions — LCC-18



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 10/01