ADVANCE INFORMATION

CDC1651F-E
Automotive Controller

Edition Jan. 27, 2005
6251-667-1AI

MICRONAS

Contents

1. Introduction

The device is a microcontroller for use in automotive applications. The on-chip CPU is a 65C816, an upgrade of the 65C02 with 16-bit internal data and 24-bit address bus. The chip consists of timer/counters, an interrupt controller, a multichannel A/D converter, a stepper motor and LCD driver, UARTs, a CAN interface and PWM outputs. This document provides ROM hardware-specific information. General information on operating the IC can be found in the document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

1.1. Features

Table 1–1: CDC16xxF Family Feature List

	This device:								
Item	**CDC1605F-E EMU**	**CDC1607F-E MCM Flash**	**CDC1631F-E Mask ROM**	**CDC1651F-E Mask ROM**	**CDC1605F-C EMU**	**CDC1607F-C MCM Flash**	**CDC1641F-C Mask ROM**	**CDC1652F-C Mask ROM**	**CDC1672F-C Mask ROM**
Core									
CPU	16-bit 65C816, featuring software compatibility with its 8-bit NMOS and CMOS 6502-series predecessors								
CPU-active operation modes	FAST, SLOW and DEEP SLOW				FAST and SLOW				
Power-saving operation modes (CPU inactive)	WAKE and IDLE				-				
EMI reduction mode	selectable in FAST mode								
Oscillators	4 to 12 MHz quartz, RC				4 to 12 MHz quartz				
RAM	6 Kbyte		2 Kbyte	4 Kbyte	6 Kbyte		2.75 Kbyte	4 Kbyte	6 Kbyte
ROM	ROMless, external program storage with up to 16 Mbyte, internal 2-Kbyte boot ROM	256-Kbyte Flash, bottom boot configuration, internal 2-Kbyte boot ROM	64 Kbyte	128 Kbyte, 2-Kbyte SF- ROM	ROMless, external program storage with up to 16 Mbyte, internal 2-Kbyte boot ROM	256-Kbyte Flash, bottom boot configuration, internal 2-Kbyte boot ROM	90 Kbyte	128 Kbyte	216 Kbyte

Table 1–1: CDC16xxF Family Feature List, continued

This device:

Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E Mask ROM	CDC1651F-E Mask ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Multiplier, 8 by 8 bit	✔				-				
Digital watchdog	✔								
Central clock divider	✔								
Interrupt controller expanding NMI	16 inputs,15 priority levels								
Port interrupts including slope selection	4 inputs								
Port wake-up inputs including slope / level selection	10				-				
Patch module	10 ROM locations		5 ROM locations	10 ROM locations			5 ROM locations	6 ROM locations	
Boot system	allows in-system downloading of code and data into RAM via serial link		-	allows in-system downloading of code and data into RAM via serial link			-		
Analog									
Reset/Alarm	combined input for regulator input supervision								
Clock and supply supervision	✔								
10-bit ADC, charge balance type	9 channels (5 channels selectable as digital input)								
ADC reference	VREF pin								
Comparators	P06COMP with 1/2 AVDD reference								
LCD	internal processing of all analog voltages for the LCD driver								

Table 1–1: CDC16xxF Family Feature List, continued

	This device:								
Item	**CDC1605F-E EMU**	**CDC1607F-E MCM Flash**	**CDC1631F-E Mask ROM**	**CDC1651F-E Mask ROM**	**CDC1605F-C EMU**	**CDC1607F-C MCM Flash**	**CDC1641F-C Mask ROM**	**CDC1652F-C Mask ROM**	**CDC1672F-C Mask ROM**
Communication									
DMA	1 DMA channel for serving the graphics bus interface		-	1 DMA channel for serving the graphics bus interface			-	1 DMA channel for serving the graphics bus interface	
UART	3: UART0, UART1 and UART2		1: UART0	2: UART0 and UART1	3: UART0, UART1 and UART2		1: UART0	3: UART0, UART1 and UART2	
Synchronous serial peripheral interfaces	2: SPI0 and SPI1		1: SPI0	2: SPI0 and SPI1			1: SPI0	2: SPI0 and SPI1	
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN000F)		1: CAN0 with 256-byte object RAM (LCAN000F)		3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN0009)		1: CAN0 with 256-byte object RAM (LCAN0009)	2: CAN0 and CAN1 with 256-byte object RAM each (LCAN0009)	
DIGITbus	1 master module		-		1 master module		-	1 master module	
Input & Output									
Universal ports selectable as 4:1-mux LCD segment/ backplane lines or digital I/O ports	up to 52 I/O or 48 LCD segment lines (=192 segments), in groups of two, configurable as I/O or LCD								
Universal port slew rate	HW-preselectable								
Stepper motor control modules with high-current ports	5 modules, 24 dI/dt-controlled ports								
8-bit PWM modules	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4		3 modules: PWM0, PWM1, PWM2	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4			2 modules: PWM0, PWM1	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4	
Audio module with auto-decay	✔								
SW-selectable clock outputs	2								

Table 1–1: CDC16xxF Family Feature List, continued

	This device:								
Item	**CDC1605F-E EMU**	**CDC1607F-E MCM Flash**	**CDC1631F-E Mask ROM**	**CDC1651F-E Mask ROM**	**CDC1605F-C EMU**	**CDC1607F-C MCM Flash**	**CDC1641F-C Mask ROM**	**CDC1652F-C Mask ROM**	**CDC1672F-C Mask ROM**
Polling/flash timer output	1 high-current port output operable in power-saving operation modes				-				
Timers & Counters									
16-bit free-running counters with capture/compare modules	CCC0 with 3 CAPCOM								
16-bit timers	1: T0								
8-bit timers	2: T1 and T2								
Real-time clock, delivering hours, minutes and seconds	✔				-				
Miscellaneous									
Scalable layout in CAN, RAM and ROM	-	✔			-	✔			
Various HW options selectable at random	most options SW-programmable, copy from user program storage during system start-up		mask-programmed according to user specification		most options SW-programmable, copy from user program storage during system start-up		mask-programmed according to user specification		
Core bond-out	✔	-			✔	-			
Supply voltage	4.5 V to 5.5 V								
Temperature range	T_{case}: 0 °C to +70 °C	T_{case}: –40 °C to +105 °C			T_{amb}: –40 °C to +85 °C				
Package									
Type	ceramic 177PGA	PMQFP100-1 0.65 mm pitch			ceramic 177PGA	PMQFP100-1 0.65 mm pitch			
Bonded pins	176	100			176	100			

1.2. Abbreviations

ADC	Analog-to-Digital Converter
AM	Audio Module
CAN	Controller Area Network
CAPCOM	Capture/Compare
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access
ERM	EMI Reduction Module
IR	Interrupt Controller
LCD	Liquid Crystal Display
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PSM	Power-Saving Module
PWM	Pulse Width Modulator
RTC	Real-Time Clock
SF-ROM	Special-Function ROM
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver/Transmitter

1.3. Block Diagram

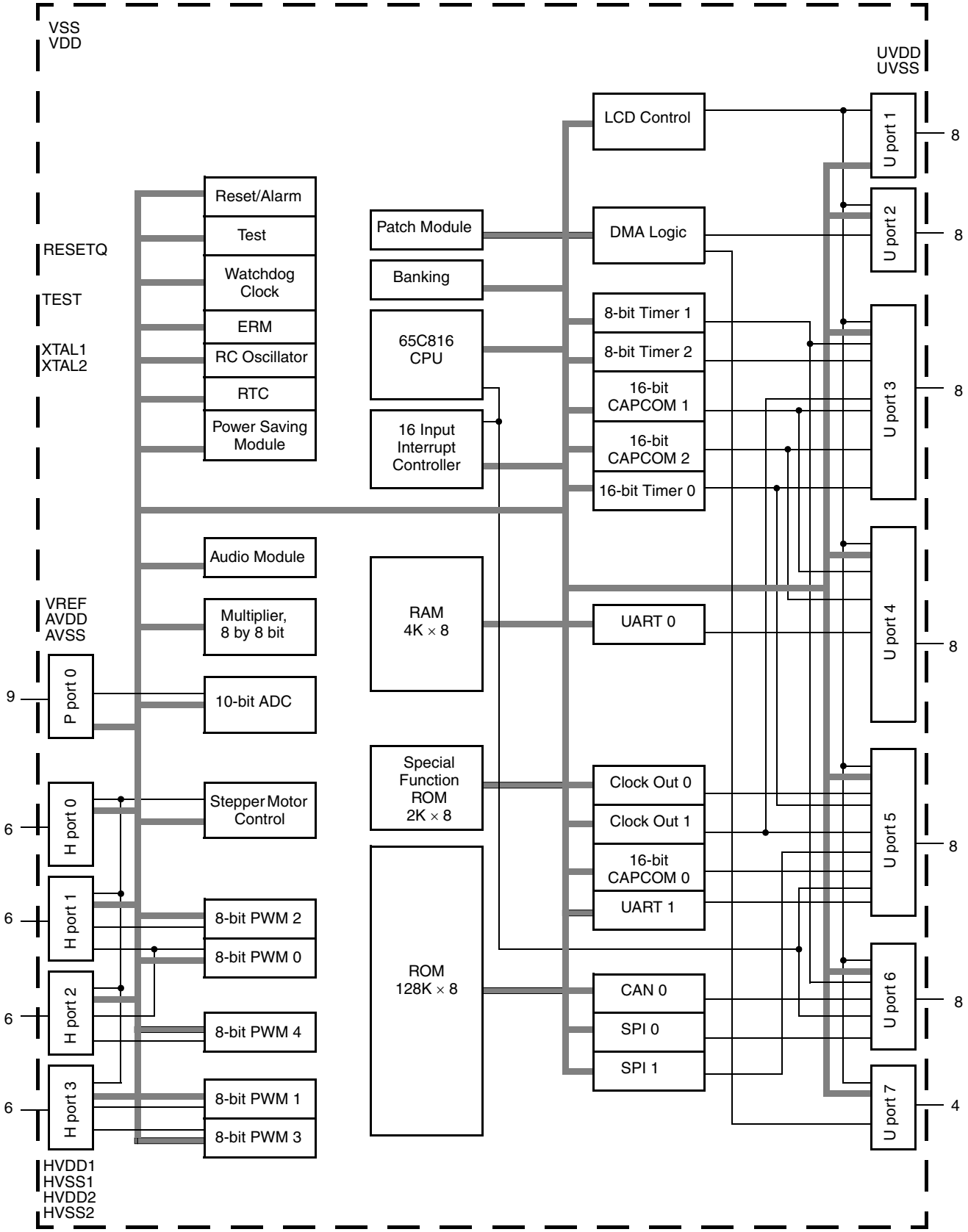
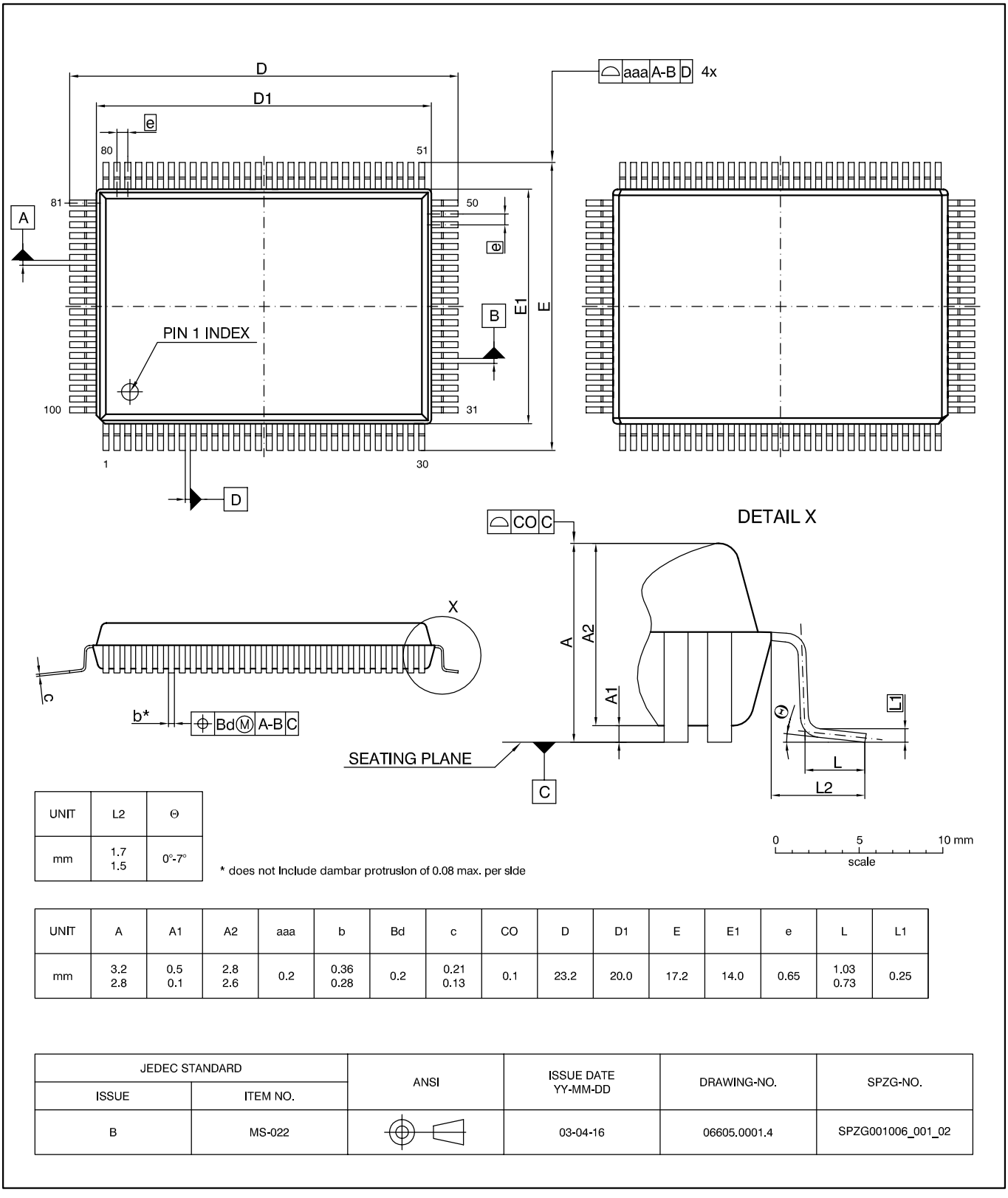


Fig. 1–1: CDC1651F-E block diagram

2. Package and Pins

2.1. Package Outline Dimensions



UNIT	L2	Θ
mm	1.7 1.5	0°-7°

* does not include dambar protrusion of 0.08 max. per side

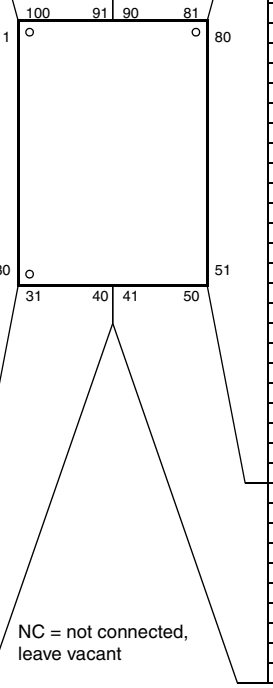
UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	3.2 2.8	0.5 0.1	2.8 2.6	0.2	0.36 0.28	0.2	0.21 0.13	0.1	23.2	20.0	17.2	14.0	0.65	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-04-16	06605.0001.4	SPZG001006_001_02

Fig. 2–1: PMQFP100-1: **P**lastic **M**etric **Q**uad **F**lat **P**ackage,
100 leads, 14 × 20 × 2.7 mm^3
Ordering code: QB
Weight approximately 1.7 g

2.2. Pin Assignment

Pin Functions						Pin No.
Bus Mode	LCD Mode	Port Special Out	Port Special In	Basic Function		
	SEG7.3	GWRQ		U7.3		91
	SEG7.2	GRDQ		U7.2		92
	SEG7.1			U7.1		93
	SEG7.0			U7.0		94
				UVSS		95
				UVDD		96
ADB7	SEG3.7	T2-OUT		U3.7		97
ADB6	SEG3.6	CC1-OUT		U3.6		98
ADB5	SEG3.5	SPI1-CLK-OUT	SPI1-CLK-IN	U3.5		99
ADB4	SEG3.4	T0-OUT	WP0	U3.4		100
ADB3	SEG3.3	CC2-OUT		U3.3		1
ADB2	SEG3.2			U3.2		2
ADB1	SEG3.1	CO1	SPI1-D-IN	U3.1		3
ADB0	SEG3.0	SPI1-D-OUT		U3.0		4
	SEG6.7	CAN0-TX	MULTI-TEST-IN	U6.7		5
	SEG6.6	PINT1-OUT	CAN0-RX/WP1	U6.6		6
	SEG6.5	T1-OUT	SPI0-D-IN	U6.5		7
	SEG6.4	SPI0-D-OUT		U6.4		8
				TEST		9
				RESETQ		10
				XTAL2		11
				XTAL1		12
				VSS		13
				VDD		14
	SEG6.3	SPI0-CLK-OUT	SPI0-CLK-IN	U6.3		15
	SEG6.2	T1-OUT	PINT2-IN/WP5	U6.2		16
	SEG6.1	LCD-CLK-OUT	PINT1-IN/WP4	U6.1		17
	SEG6.0	LCD-SYNC-OUT	PINT0-IN/WP3	U6.0		18
WEQ	SEG1.7			U1.7		19
CEQ	SEG1.6		WP2	U1.6		20
ITSTOUT	SEG1.5	LCD-CLK-OUT		U1.5		21
RWQ	SEG1.4	LCD-SYNC-OUT		U1.4		22
PH2	BP3			U1.3		23
OEQ	BP2			U1.2		24
BE	BP1			U1.1		25
RDY	BP0	ITSTOUT		U1.0		26
STOPCLK		SMB1+		H1.5		27
VPQ		SMB1-		H1.4		28
VPA		SMB2+		H1.3		29
VDA		SMB2-	SMB-COMP	H1.2		30
DB7		SME1+/PWM2		H1.1		31
DB6		SME1-/PWM0		H1.0		32
				HVDD1		33
				HVSS1		34
DB5		SME2+		H0.5		35
DB4		SME2-	SME-COMP	H0.4		36
DB3		SMA1+		H0.3		37
DB2		SMA1-		H0.2		38
DB1		SMA2+		H0.1		39
DB0		SMA2-	SMA-COMP	H0.0		40



Pin No.		Pin Functions				
		Basic Function	Port Special In	Port Special Out	LCD Mode	Bus Mode
90		U4.0	WP7	SME1+	SEG4.0	ADB8
89		U4.1			SEG4.1	ADB9
88		U4.2		SME1-	SEG4.2	ADB10
87		U4.3			SEG4.3	ADB11
86		U4.4	UART0-RX/WP8		SEG4.4	ADB12
85		U4.5		UART0-TX	SEG4.5	ADB13
84		U4.6	CC2-IN	CC1-OUT	SEG4.6	ADB14
83		U4.7	CC1-IN		SEG4.7	ADB15
82		U5.0	CC0-IN	CO1	SEG5.0	
81		U5.1	INT-TEST-IN	CC0-OUT	SEG5.1	
80		U5.2	LCD-CLK-IN	AM-PWM	SEG5.2	
79		U5.3	LCD-SYNC-IN	AM-OUT	SEG5.3	
78		U5.4	IRQ	UART1-TX	SEG5.4	
77		U5.5	ABORTQ	CO0	SEG5.5	
76		U5.6	PINT3/WP6	PWM2	SEG5.6	
75		U5.7	PINT3/UART1-RX	PINT0-OUT	SEG5.7	
74		U2.0/GD0			SEG2.0	ADB16
73		U2.1/GD1			SEG2.1	ADB17
72		U2.2/GD2			SEG2.2	ADB18
71		U2.3/GD3			SEG2.3	ADB19
70		U2.4/GD4			SEG2.4	ADB20
69		U2.5/GD5			SEG2.5	ADB21
68		U2.6/GD6			SEG2.6	ADB22
67		U2.7/GD7			SEG2.7	ADB23
66		AVSS				
65		AVDD				
64		VREF				
63		P0.1	P0.1 digital input			
62		P0.2	P0.2 digital input			
61		P0.3	P0.3 digital input			
60		P0.4	P0.4 digital input			
59		P0.5	P0.5 digital input			
58		P0.6	P0.6 Compar. inp.			
57		P0.7				
56		P0.8				
55		P0.9				
54		H2.0	SMC-COMP	SMC2-		
53		H2.1		SMC2+		
52		H2.2		SMC1-		
51		H2.3		SMC1+		
50		H2.4	WP9	PWM0		
49		H2.5/Pol		PWM4		
48		HVSS2				
47		HVDD2				
46		H3.0		PWM1		
45		H3.1		PWM3		
44		H3.2	SMD-COMP	SMD2-		
43		H3.3		SMD2+		
42		H3.4		SMD1-		
41		H3.5		SMD1+		

Fig. 2–2: Pin Assignment for **PMQFP100-1** Package

2.3. External Components

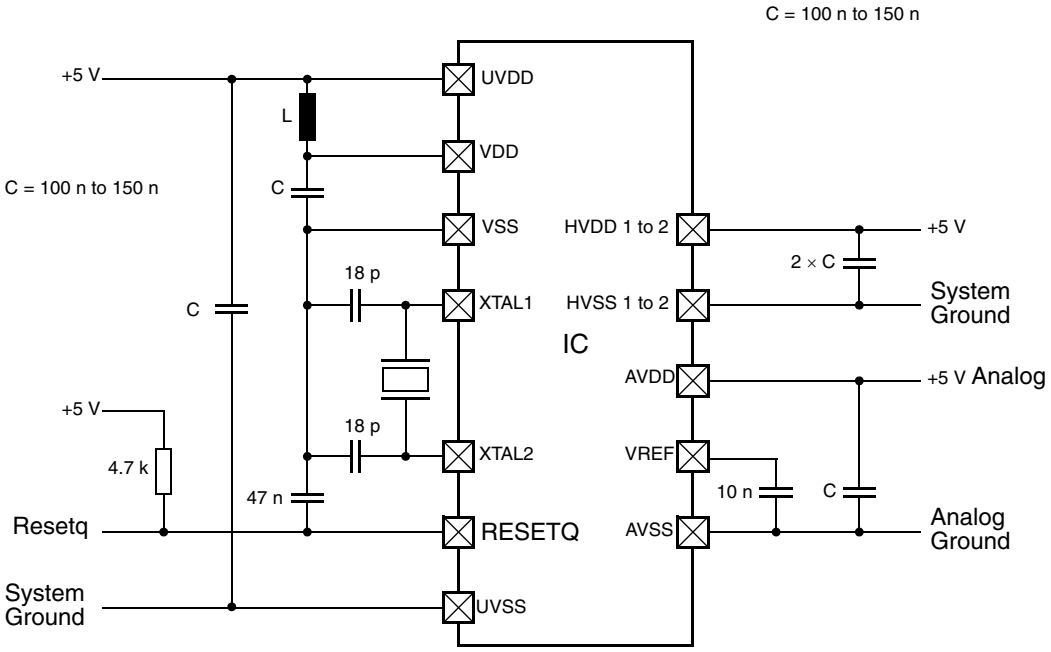


Fig. 2–3: Recommended external supply and quartz connection for low electromagnetic interference (EMI)

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. A frequency too low will reduce decoupling effectiveness, increase RF emissions and may affect device operation adversely.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other printed circuit board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47 nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of $\geq 200\ \mu s$, sufficient for proper Wake Reset functionality.

3. Electrical Data

3.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

Table 3–1: All voltages listed are referenced to ground (UV_{SS} = HV_{SSn} = AV_{SS} = 0 V), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Core supply voltage Port supply voltage Analog supply voltage SM supply voltage 1 SM supply voltage 2	VDD UVDD AVDD HVDD1 HVDD2	–0.3	6.0	V
ΔV_{DD}	Voltage difference between VDD and AVDD, resp. UVDD	VDD, AVDD UVDD	–0.5	0.5	V
I_{SUP}	Core supply current Port supply current	VDD, VSS UVDD, UVSS	–100	100	mA
IA_{SUP}	Analog supply current	AVDD, AVSS	–20	20	mA
IH_{SUP}	SM supply current @T_j = 105 °C, duty factor = 0.71 [1)]	HVDD1, HVSS1 HVDD2, HVSS2	–380	380	mA
V_{in}	Input voltage	U ports, XTAL,RESETQ, TEST	UV_{SS} – 0.5	UV_{DD} + 0.7	V
		P0 ports VREF	UV_{SS} – 0.5	AV_{DD} + 0.7	V
		H ports	HV_{SS} – 0.5	HV_{DD} + 0.7	V
I_{in}	Input current	all inputs	0	2	mA
I_o	Output current	U ports	–5	5	mA
		H ports	–60	60	mA
t_{oshsl}	Duration of short circuit in Port SLOW mode to UVSS or UVDD	U ports except U3.2 in DP mode		indefinite	s
T_j	Junction temperature under bias		–45	115	°C
T_s	Storage temperature		–45	125	°C
P_{max}	Maximum power dissipation			0.8	W

[1)] This condition represents the worst case load with regard to the intended application

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep UV_{DD} = AV_{DD} during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction.

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions” of this specification is not implied, may result in unpredictable behavior of the device and may reduce reliability and lifetime.

Table 3–2: All voltages listed are referenced to ground (UV_{SS} = HV_{SSn} = AV_{SS} = 0 V), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage Port supply voltage Analog supply voltage	VDD UVDD AVDD	4.5	5	5.5	V
HV_{DD}	SM supply voltage 1 SM supply voltage 2	HVDD1 HVDD2	4.75	5	5.25	V
ΔV_{DD}	Voltage difference between VDD and AVDD resp. UVDD	VDD, AVDD UVDD	−0.2		0.2	V
dAV_{DD}	AVDD ripple, peak-to-peak	AVDD			200	mV
f_{XTAL}	XTAL clock frequency	XTAL1	4		12	MHz
	XTAL clock frequency using ERM	XTAL1	4		10	MHz
V_{il}	Low input voltage	U ports H ports P0 ports TEST			$0.51 \times V_{DD}$	V
V_{ih}	High input voltage	U ports H ports P0 ports TEST	$0.86 \times V_{DD}$			V
RV_{il}	Reset active input voltage	RESETQ			0.9	V
WRV_{il}	Reset active input voltage during power-saving modes and Wake Reset	RESETQ			0.6	V
RV_{im}	Reset inactive and Alarm active input voltage	RESETQ	1.6		2.1	V
RV_{ih}	Reset inactive and Alarm inactive input voltage	RESETQ	2.9			V
WRV_{ih}	Reset inactive during power-saving modes	RESETQ	UV_{DD} − 0.4 V			V
V_{REFi}	ADC reference input voltage	VREF	2.56		AV_{DD}	V
$P0V_i$	P0 ADC input port input voltage	P0 ports	0		V_{REFi}	V

3.3. Characteristics

Listed are only those characteristics that differ from chapter 3.3 of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD). All not differing characteristics, that are not listed here, apply, but in a T_{CASE} temperature range extended to –40 °C to +105 °C.

Table 3–3: $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0$ V, 4.5 V < $V_{DD} = AV_{DD} = UV_{DD}$ < 5.5 V, 4.75 V < $HV_{DD1} = HV_{DD2}$ < 5.25 V, T_{CASE} = –40 °C to +105 °C, f_{XTAL} = 10 MHz.

Symbol	Parameter	Pin Name	Min.	Typ. [1]	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal resistance from junction to case			12.1		K/W	measured on Micronas typical 2-layer board, 1s1p, described in document “Integrated Circuits - Thermal Characterization of Packages” (6200-266-1E) (modified JESD-51.3)
R_{thja}	Thermal resistance from junction to ambient			41.0		K/W	
Supply Currents (CMOS levels on all inputs, no loads on outputs, difference between any two VDDs within ±0.2 V)							
I_{DDF}	VDD FAST mode supply current	VDD		35	65	mA	
I_{DDS}	VDD SLOW mode supply current	VDD		1.5	2.0	mA	all modules off [2] [3], all hardware options set to their reset values
I_{DDD}	VDD DEEP SLOW mode supply current	VDD		0.75	1.0	mA	all modules off [2] [3], all hardware options set to their reset values
I_{DDI}	VDD IDLE mode supply current	VDD		70	135	µA	f_{xtal} = 4 MHz [3]
				180	260	µA	f_{xtal} = 10 MHz [3]
				12	55	µA	internal RC oscill.
I_{DDW}	VDD WAKE mode supply current	VDD	0	1	50	µA	
UI_{DDa}	UVDD active supply current	UVDD			0.3	mA	no output activity, LCD module on
AI_{DDa}	AVDD active supply current	AVDD		0.2	0.4	mA	ADC on, ERM off
				1	2	mA	ERM on, f_{XTAL} = 8.4 MHz
AI_{DDq}	Quiescent supply current	AVDD	0	1	10	µA	ADC and ERM off
UI_{DDq}		UVDD	0	1	10	µA	no output activity, LCD module off
HI_{DDq}		sum of all HVDDn	0	1	20	µA	no output activity, SM module off

[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical recommended operating conditions applied, and are not 100% tested).

[2] Value may be exceeded with unusual hardware option setting
[3] Measured with external clock. Add 100 µA at 4 MHz, 115 µA at 10 MHz for operation on typical quartz with SR3.XTAL = 0 (Oscillator RUN mode).

3.4. Recommended Crystal Characteristics

See chapter 3.4 of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

4. CPU, RAM, ROM and Banking

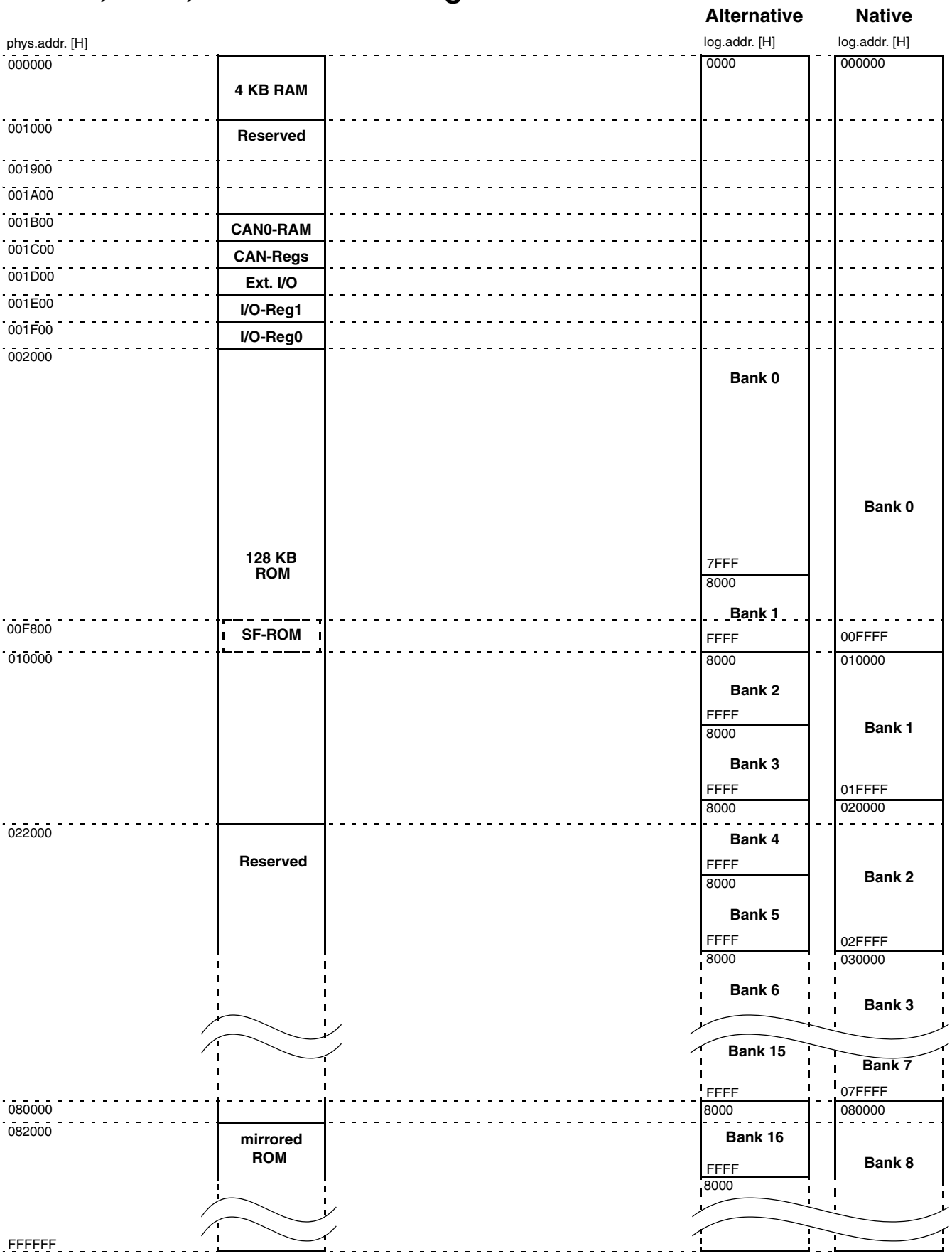


Fig. 4–1: Address Map

5. Core Logic

5.1. Control Register CR

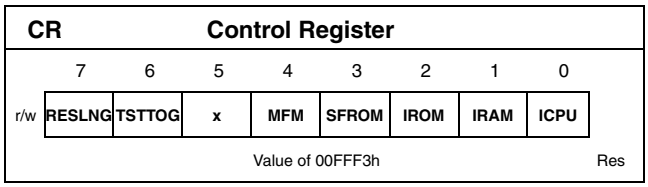
The control register CR serves to configure the ways by which certain system resources are accessed during operation. The main purpose is to obtain a variable system configuration during IC test.

Upon each high transition on the RESETQ pin, internal hardware reads data from the address location 00FFF3h and stores it to the CR. The state of the TEST pin at that time specifies which program storage source is accessed for this read:

Table 5–1: Control byte source

TEST	Control byte source
0 or NC	internal SF-ROM (standard for stand-alone operation)
1	external, via multifunction pins in bus mode (for test purposes only)

The system will thus start up according to the configuration defined in address location 00FFF3h, automatically copied to register CR.



RESLNG **Reset Pulse Length**
r/w1: Pulse length is $16/F_{XTAL}$
r/w0: Pulse length is $4096/F_{XTAL}$
This bit specifies the length of the reset pulse which is output at pin RESETQ following an internal reset. If pin TEST is 1 the first reset after power on is short. The following resets are as programmed by RESLNG. If pin TEST is 0, all resets are long.

TSTTOG **TEST Pin Toggle** (Table 5–2)
This bit is used for test purposes only. If TSTTOG is true in IC active mode, pin TEST can toggle the multifunction pins between bus mode and normal mode.

MFM **Multifunction Pin Mode**
(Table 5–2)

Table 5–2: TSTTOG and MFM usage

TSTTOG	MFM	TEST pin	Multifunction Pins
0	0	x	bus mode
1	0	0	bus mode
		1	normal mode
x	1	x	normal mode

SFROM **SF-ROM** (Table 5–3)

IROM **Internal ROM** (Table 5–3)

Table 5–3: SFROM and IROM usage

SFROM	IROM	selected program storage
1	1	internal ROM
0		internal SF-ROM
x	0	external via multifunction pins in bus mode

IRAM **Internal RAM**
r/w1: Enable internal RAM.
r/w0: Disable internal RAM.

ICPU **Internal CPU**
r/w1: Enable internal CPU.
r/w0: Disable internal CPU.

Table 5–4: Some commonly used settings for address location 00FFF3h. A copy is automatically transferred to the CR when exiting reset.

Code	TEST Pin	Operation Mode
FFh	0	Stand-alone with internal ROM
ABh	1	External program storage connected to multifunction pins in bus mode

6. Interrupt Controller (IR)

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

6.1. Interrupt Assignment

(cf. chapter 10.3 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

Table 6–1: INT-MUX 1 = HW Option addr. FFC0H

bit 1	bit 0	selects
0	0	CC0 COMP
0	1	Timer 2
1	0	V_{SS}
1	1	Timer 1

Table 6–2: INT-MUX 2 = HW Option addr. FFC0H

bit 3	bit 2	selects
0	0	V_{SS}
0	1	P06 COMP
1	0	SPI 0
1	1	Timer 1

Table 6–3: INT-MUX 4 = HW Option addr. FFC0H

bit 7	bit 6	selects
0	0	V_{SS}
0	1	SPI 0
1	0	DMA
1	1	PINT3-IN

Table 6–4: INT-MUX 6= HW Option addr. FFC1H

bit 3	bit 2	selects
0	0	Timer 2
0	1	V_{SS}
1	0	V_{SS}
1	1	PINT2-IN

Table 6–5: INT-MUX 9= HW Option addr. FFC2H

bit 1	bit 0	selects
0	0	V_{SS}
0	1	UART 1
1	0	IR-RTC
1	1	IR-WAPI

7. Hardware Options

7.1. Functional Description

Hardware options are available in several areas to adapt the IC function to the host system requirements:

– clock signal selection for most of the peripheral modules from f_{osc} to $f_{osc}/2^{17}$ plus some internal signals (see “Table 25-2: Clock Option Selection Code“ in Chapter “25. Hardware Options” of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD)).

– interrupt source selection for interrupt inputs 0, 1, 5, 6, 7, 10, 13, 14 and 15

– Special-out signal selection for some U and H ports

– Rx/Tx polarity selection for SPI and UART modules

– U Port Slow mode selection

In ROM parts, hardware options are not software-programmable.

The data in address locations 00FFA0H through 00FFC3H were used to define their respective, hard-wired hardware options during mask production and can only be altered by changing a production mask for this IC.

For verification purposes, it is recommended to have an application code in ROM that runs with Flash parts as well - which is automatically the case if Flash parts have been used for software development and tests before. This implies reading of locations 00FFA0h through 00FFC3h directly after reset, to activate the hardware options’ settings in Flash and EMU parts as well.

7.2. Listing of Dedicated Addresses and Corresponding Hardware Options

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

Table 7–1: Hardware-Option-Dedicated Addresses
(cf. chapter 25.2 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

7	6	5	4	3	2	1	0

00FFB4 UART0 Input and Output

UART0 Tx 0: direct 1: inverted	UART0 Rx 0: direct 1: inverted	x	x	x	x	x	x

00FFC0 Interrupt Sources Multiplexer 1 to 4

Mux4:		Mux3:		Mux2:		Mux1:	
00	V_{SS}	00	PINT3-IN	00	V_{SS}	00	CC0 COMP
01	SPI 0	01	SPI 1	01	P06 COMP	01	Timer 2
10	DMA	10	UART 1	10	SPI 0	10	V_{SS}
11	PINT3-IN	11	CC1 COMP	11	Timer 1	11	Timer 1

00FFC1 Interrupt Sources Multiplexer 5 to 8

Mux8:		Mux7:		Mux6:		Mux5:	
00	CC1OR	00	CC0OR	00	Timer 2	00	Timer 2
01	PINT2-IN	01	UART 1	01	V_{SS}	01	UART 1
10	IR-RTC	10	IR-RTC	10	V_{SS}	10	SPI 1
11	IR-WAPI	11	IR-WAPI	11	PINT2-IN	11	DMA

Table 7–1: Hardware-Option-Dedicated Addresses, continued
(cf. chapter 25.2 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

7	6	5	4	3	2	1	0
00FFC2	**Interrupt Sources Multiplexer 9 and Port Multiplexer**						
H-Port 1.1 0: SME 1: PWM2	x	H-Port 1.0 0: SME 1: PWM0	PINT3-IN 0: at U5.6 1: at U5.7	x	x	Mux9: 00 V_{SS} 01 UART 1 10 IR-RTC 11 IR-WAPI	

8. Register Cross-Reference Table

Table 8–1: CAN RAM, memory page 1B

Address (hex)	Mnemonic	Block
1B00 ... 1BFF	CAN0_RAM	CAN0-RAM

Table 8–2: CAN Registers, memory page 1C

Address (hex)	Mnemonic	Block
1C00	CAN0CTR	CAN0
1C01	CAN0STR	
1C02	CAN0ESTR	
1C03	CAN0IDX	
1C04	CAN0IDM	
1C05		
1C06		
1C07		
1C08	CAN0BT1	
1C09	CAN0BT2	
1C0A	CAN0BT3	
1C0B	CAN0ICR	
1C0C	CAN0OCR	
1C0D	CAN0TEC	
1C0E	CAN0REC	
1C0F	CAN0ESM	
1C10	CAN0CTIM	
1C11		

Table 8–3: I/O Registers, memory page 1E

Address (hex)	Mnemonic	Block
1E64	PAR0	Patch Module
1E65	PAR1	
1E66	PAR2	
1E67	PDR	
1E68	PER0	
1E69	PER1	
1E70	WUS	Power-Saving Module
1E71		
1E74	SSR	
1E75		
1E76		
1E78	SSC	
1E79		
1E7A		
1E7C	RTC	
1E7D		
1E7E		
1E80	WPM0	
1E81	WPM2	
1E82	WPM4	
1E83	WPM6	
1E84	WPM8	
1E88	WSC	
1E90	OSC	
1E94	RTCC	
1E98	POL	
1E99		
1E9C	SMX	

Table 8–3: I/O Registers, memory page 1E, continued

Address (hex)	Mnemonic	Block
1EA0	MULCAND	Multiplier
1EA1	MULPLIER	
1EA2	MULPROD	
1EA3		

Table 8–4: I/O Registers, memory page 1F

Address (hex)	Mnemonic	Block
1F00	CSW0	Core Logic
1F01	CR	
1F02	ERMC	ERM
1F08	SR0	Core Logic
1F09	SR1	
1F0A	SR2	
1F0B	SR3	
1F0C	DBG	Debug Register
1F0F	ABR	Memory Banking
1F10	SPI0D	SPI0
1F11	SPI0M	
1F12	SPI1D	SPI1
1F13	SPI1M	
1F14	CO0SEL	Core Logic
1F15	CO1SEL	
1F18	UA1D	UART1
1F19	UA1C	
1F1A	UA1BR0	
1F1B	UA1BR1	
1F1C	UA1IM	
1F1D	UA1CA	
1F1E	UA1IF	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F1F	IRE	Interrupt Controller
1F20	IRC	
1F21	IRRET	
1F22	IRPRI10	
1F23	IRPRI32	
1F24	IRPRI54	
1F25	IRPRI76	
1F26	IRPRI98	
1F27	IRPRIBA	
1F28	IRPRIDC	
1F29	IRPRIFE	
1F2A	IRP	
1F2B	IRPM0	
1F2C	IRPP	
1F2D	AMAS	Audio Module
1F2E	AMF	
1F2F	AMDEC	
1F30	U2D	Universal Port 2
1F32	U2SEG10	
1F33	U2M10	
1F34	U2SEG32	
1F35	U2M32	
1F36	U2SEG54	
1F37	U2M54	
1F38	U2SEG76	
1F39	U2M76	
1F4E	TIM0	Timer 0
1F4F		
1F50	PWM0	PWM
1F51	PWM1	
1F52	PWM2	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F54	TIM1	Timer 1, 2
1F55	TIM2	
1F5A	SMVC	Stepper Motor Module
1F5B	SMVSIN	
1F5C	SMVCOS	
1F5D	SMVCMP	
1F5E	PWM3	PWM
1F5F	PWM4	
1F60	CSW1	Core Logic
1F61	CSW2	
1F6C	CC0M	Capture Compare Module
1F6D	CC0I	
1F6E	CC0	
1F6F		
1F70	CC1M	
1F71	CC1I	
1F72	CC1	
1F73		
1F74	CC2M	
1F75	CC2I	
1F76	CC2	
1F77		
1F7C	CCC	
1F7D		
1F7E	P0PIN	Analog Input Port 0
1F80	H0NS	High Current Port 0
1F81	H0TRI	
1F82	H0D	
1F84	H1NS	High Current Port 1
1F85	H1TRI	
1F86	H1D	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F88	H2NS	High Current Port 2
1F89	H2TRI	
1F8A	H2D	
1F90	H3NS	High Current Port 3
1F91	H3TRI	
1F92	H3D	
1F98	U1D	Universal Port 1
1F99	U1SEG10	
1F9A	U1SEG32	
1F9B	U1M30	
1F9C	U1SEG54	
1F9D	U1M54	
1F9E	U1SEG76	
1F9F	U1M76	
1FA0	UA0D	UART0
1FA1	UA0C	
1FA2	UA0BR0	
1FA3	UA0BR1	
1FA4	UA0IM	
1FA5	UA0CA	
1FA6	UA0IF	
1FA8	AD0	AD Converter
1FA9	AD1	
1FAC	U3D	Universal Port 3
1FAE	U3SEG10	
1FAF	U3M10	
1FB0	U3SEG32	
1FB1	U3M32	
1FB2	U3SEG54	
1FB3	U3M54	
1FB4	U3SEG76	
1FB5	U3M76	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1FB8	U4D	Universal Port 4
1FBA	U4SEG10	
1FBB	U4M10	
1FBC	U4SEG32	
1FBD	U4M32	
1FBE	U4SEG54	
1FBF	U4M54	
1FC0	U4SEG76	
1FC1	U4M76	
1FC4	U5D	Universal Port 5
1FC6	U5SEG10	
1FC7	U5M10	
1FC8	U5SEG32	
1FC9	U5M32	
1FCA	U5SEG54	
1FCB	U5M54	
1FCC	U5SEG76	
1FCD	U5M76	
1FD0	U6D	Universal Port 6
1FD2	U6SEG10	
1FD3	U6M10	
1FD4	U6SEG32	
1FD5	U6M32	
1FD6	U6SEG54	
1FD7	U6M54	
1FD8	U6SEG76	
1FD9	U6M76	
1FDC	U7D	Universal Port 7
1FDE	U7SEG10	
1FDF	U7M10	
1FE0	U7SEG32	
1FE1	U7M32	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1FE8	DCS	DMA
1FE9	DIC	
1FEA	DSA	
1FEB		
1FEC		
1FED	DEA	
1FEE		
1FEF		
1FFD	TST3	TST
1FFE	TST1	
1FFF	TST2	

8.1. Modified Registers

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

8.1.1. Standby Registers

(cf. chapter 6.3 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

SR0 Standby Register 0

	7	6	5	4	3	2	1	0	
r/w	SM	PWM1	PWM0	x	SPI1	CAN0	CCC	SPI0	
	0	0	0	x	0	0	0	0	Res

SR2 Standby Register 2

	7	6	5	4	3	2	1	0	
r/w	TIM2	PWM3	PWM2	UART1	PWM4	x	EXTIR	ABM	
	0	x	0	x	x	x	0	0	Res

SR3 Standby Register 3

	7	6	5	4	3	2	1	0	
r/w	x	x	x	XTAL	WAID	FCLO	x	x	
	x	x	x	1	0*)	0	x	x	Res

*)Reset with pin reset or VDD power on

9. Data Sheet History

1. “CDC1651F-E Automotive Controller”, Jan. 27, 2005, 6251-667-1AI. First release of the advance information. Originally created for the HW version CDC1651F-E1.

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