PM73123

AAL1GATOR-8

REVISION A DEVICE ERRATA

PRELIMINARY

ISSUE 1: FEBRUARY 2001

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	February 2001	Document created.

CONTENTS

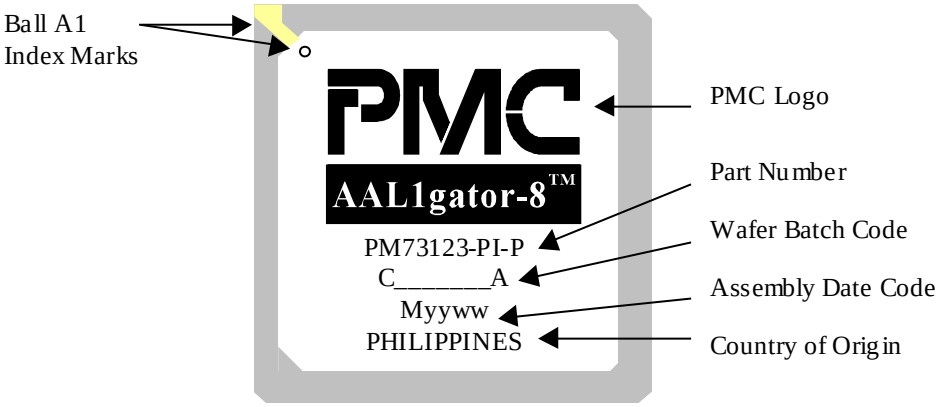
1 INTRODUCTION

This document lists the known functional errata for revision A of the PM73123 AAL1gator-8 as of the publication date of this document. Please refer to PMC's product web-page at www.pmc-sierra.com to check for the latest errata.

1.1 Device Identification

The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). The PM73123-PI is packaged in a custom 324 PBGA, with a 23 x 23 mm body size, and a ball pitch of 1.00 mm.

Figure 1. PM73123 AAL1gator-8 Branding Format.



1.2 Reference:

1. PMC-2000097 AAL1gator-8 Datasheet, Issue 1.

2 AAL1GATOR-8 REVISION A FUNCTIONAL DEFICIENCY LIST

This section lists the known functional deficiencies for Revision A of the AAL1gator-8 (as of the publication date of this document). For each deficiency, the known workaround is described as well as a comparison of the performance of the device with the workaround and without the workaround implemented.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

PMC-Sierra, Inc.
105-8555 Baxter Place
Burnaby, BC
Canada V5A 4V7
Tel: (604) 415-6000
App Support: (604) 415-4533
Fax: (604) 415-6001

Product information: info@pmc-sierra.com
Applications information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

2.1 Limited Dynamic Bandwidth CES and Non-DBCES Idle Detection

2.1.1 Description

Dynamic Bandwidth CES (DBCES) and Non-DBCES Idle Detection are techniques used by the AAL1gator-8 to remove timeslots from the AAL1 structure when those timeslots are detected to be inactive. The result is a savings in network bandwidth as compared to the constant bit rate generated using AAL1 CES without DBCES.

The AAL1gator is designed to support DBCES which is compliant to the ATM Forum standard AF-VTOA-0085.000 Dynamic Bandwidth Circuit Emulation Service (DBCES). The second method, Non-DBCES Idle Detection, is proprietary.

With DBCES, when an inactive state is detected in a specific time slot, the time slot is dropped from the next ATM structure and the bandwidth it was using may be reutilized for other services.

With Non-DBCES Idle Detection, cells are transmitted when *any* of the timeslots are active. Cells are not transmitted when *all* of the constituent time slots are inactive.

There are limitations with DBCES and Non-DBCES Idle Detection. It is recommended not to use these features with Rev A AAL1gator-8.

2.1.2 Workarounds:

Don't enable DBCES or Non-DBCES Idle Detection. The AAL1gator-8 operates normally as per ATM Forum's CES Specification.

2.1.3 Performance with workaround:

The AAL1gator-8 operates normally as per ATM Forum's CES Specification.

2.1.4 Performance without workaround:

The use of DBCES and non-DBCES Idle Detection is not recommended.

2.2 Robust SNP Feature

2.2.1 Description

The AAL1gator-8 is designed to support two algorithms for Sequence Number Processing (SNP): Fast SNP and Robust SNP. The Fast SNP feature is available in the current revision, Rev A, and functions exactly as in the PM73121 AAL1gator-II device. The Robust SNP feature is not functional in Rev A.

2.2.2 Workarounds:

Use Fast SNP, not Robust SNP.

2.2.3 Performance with workaround:

Fast SNP functions exactly as in the PM73121 AAL1gator-II device.

2.2.4 Performance without workaround:

Not applicable.

2.3 LOW_CDV Queue Does Not Activate/Deactivate Correctly

2.3.1 Description

For Unstructured Data Format (UDF) lines there is a LOW_CDV bit which can be set in the LIN_STR_MODE memory register which will cause cells to be scheduled every 47 bytes instead of every frame. This eliminates the CDV caused by the scheduler. This mode can only be used in UDF-ML mode when BYTES_PER_CELL is 47. In High Speed mode cells are always scheduled every 47 bytes which assumes that partial cells are never used in HS mode.

If a queue is "added" to the ADDQ_FIFO and LOW_CDV is set, data errors may result. In addition, if a queue is deactivated by clearing the TX_ACTIVE bit when LOW_CDV is set, the CSD can enter a lock condition.

2.3.2 Workarounds:

1. Don't use LOW_CDV mode (this is an optional mode, only valid for unstructured connections).

2. Software workaround in Beta Release 1.0. This software workaround is implemented in the AAL1gator-32/-8/-4 Beta Release 1.0 Software Driver which makes this deficiency virtually non-existent to the application. The workaround is described below to serve as a reference.

Beta Release 1.0 Software Workaround Description: Bring the connection up and down with LOW_CDV off and SUPPRESS_XMT set. Set LOW_CDV after connection is up but before sending cells.

Activate a LOW_CDV queue by doing the following:
a) When activating a line initialize LOW_CDV in the LIN_STR_MODE memory register to "0"
b) Configure the queue with SUPPRESS_XMT=1 in the TRANSMIT_CONFIG memory word (also set FRAMES_PER_CELL to 4 instead of 3)
c) Add the queue using ADDQ_FIFO
d) Set LOW_CDV
e) Set the CMD_ATTN bit in the An_CMD_REG (this will load LOW_CDV value) for that line
f) clear the SUPPRESS_XMT bit (after 250 us)

Deactivate a LOW_CDV queue by doing the following:
a) Set SUPPRESS_XMT in the TRANSMIT_CONFIG memory word
b) clear LOW_CDV
c) Set the CMD_ATTN bit for that line

d) Clear the TX_ACTIVE bit
e) Queue will be dequeued the next time a cell is processed (wait 16 ms to be safe)

Note when using this method, the first cell which the chip sends will not have SN=0.

An alternative method would be to do the same steps as above, but don't set the SUPPRESS_XMT bit when activating the queue. This will have the first cell have SN=0, but there will be a larger CDV value for the first cell until LOW_CDV is set. You may also get two cells sent close together when LOW_CDV takes effect.

2.3.3 Performance with workaround:

1. Scheduling is frame based not cell based (when LOW_CDV = 0).

2. Low CDV Mode operates normally.

2.3.4 Performance without workaround:

1. Data errors may result if adding and deleting queues when in Low CDV Mode.

2.4 RATM_CLK Must be Present even when Debugging Hardware

2.4.1 Description

In normal operation, a clock is present on RATM_CLK and this Errata 2.4 is not an issue.

When debugging and in those cases where no RATM_CLK is present (e.g. when running the AAL1gator-8 in internal UTOPIA loopback), there is a problem. In this scenario, when the A1SP is taken out of reset, the OAM queue and some of the receive data queues could detect cells even though nothing is connected to the UTOPIA interface. This will not happen if a clock signal is connected to the RATM_CLK pin.

2.4.2 Workarounds:

Ensure a clock exists on the RATM_CLK pin when chip is in reset.

2.4.3 Performance with workaround:

Operates normally.

2.4.4 Performance without workaround:

When the A1SP is taken out of reset, the OAM queue and some of the receive data queues could detect cells even though nothing is connected to the UTOPIA interface.

2.5 SRTS Queue Underrun Impacts Other Lines in A1SP

2.5.1 Description

When using the Synchronous Residual Time Stamp (SRTS) scheme in Unstructured Data Format (UDF) mode, if the SRTS queue (buffer which contains received SRTS nibbles) underruns for a specific line, a signal is sent to the internal clock synthesizer that indicates that *all* lines are in SRTS underrun. This causes all lines within the A1SP block to revert to nominal clocking.

2.5.2 Workarounds:

1. Software workaround in Beta Release 1.0. This software workaround is implemented in the AAL1gator-32/-8/-4 Beta Release 1.0 Software Driver which makes this deficiency virtually non-existent to the application. The workaround is described below to serve as a reference.

Beta Release 1.0 Software Workaround Description: One way to prevent this problem from occurring is to prevent the SRTS queue underrun event from occurring. The SRTS queue is only checked when EN_SRTS bit is set in the LIN_STR_MODE memory register. So the goal is to only have EN_SRTS set when the queue is already active and not in SRTS_UNDERRUN.

Startup:
1) When line is activated (set CMD_ATTN), make sure EN_SRTS is not set in LIN_STR_MODE. CLK_SOURCE_TX can stay at SRTS (will generate nominal or last clock with no SRTS data).
2) Initialize SRTS_CDVT to the normal value (ROUNDUP(R_CDVT/11.75)) plus 2. (this creates a gap between when the data buffer underruns and the SRTS queue underruns).
3) When line exits underrun (interrupt will occur), set SRTS_EN in LIN_STR_MODE for that line. Set CMD_ATTN in CMD_REG for it to take affect.

Now SRTS will work fine as long is there is not an SRTS underrun. A data buffer underrun is ok, as long as the SRTS queue does not underrun. To handle the underrun case, do the following steps when an underrun is detected (interrupt):

1) Clear SRTS_EN for that line, set CMD_ATTN.

2) Initialize SRTS read and write pointer to match SRTS_CDVT value.
3) When line exits underrun (interrupt will occur), set SRTS_EN in LIN_STR_MODE for that line. Set CMD_ATTN in CMD_REG for it to take affect.

Note that since the SRTS_CDVT value is set to 2 more than what would be normally set, this provides at least 3 ms to handle the interrupt. If more time is required, the initial SRTS_CDVT value should be set higher. Note the higher the SRTS_CDVT value is, the longer it will take to react to changes in clock frequency and it may take longer to lock.

2.5.3 Performance with workaround:

Operates normally. This software workaround is implemented in the AAL1gator-32/-8/-4 Beta Release 1.0 Software Driver which makes this deficiency virtually non-existent to the application.

2.5.4 Performance without workaround:

This software workaround is implemented in the AAL1gator-8 Beta Release 1.0 Software Driver which makes this deficiency virtually non-existent to the application and the device will operate normally.

2.6 When a Significant Number of Queues are Configured in TDM-to-TDM Loopback Cells May be Dropped

2.6.1 Description

A loopback FIFO exists in the A1SP block that allows cells destined for the UTOPIA bus to instead be looped directly back to the receive ATM logic. (TDM-to-TDM loopback). This errata is not relevant (i.e. cells are not dropped) if only a few queues are configured for TDM-to-TDM loopback. Unless more than approximately six queues are configured for TDM-to-TDM loopback in the A1SP, it is unlikely that this FIFO will overflow. If this FIFO fills and cells are sent to the FIFO, the cells will be dropped.

2.6.2 Workarounds:

This errata is not relevant (i.e. cells are not dropped) if only a few queues are configured for TDM-to-TDM loopback. Unless a significant amount of traffic for an A1SP is configured for TDM-to-TDM loopback, it is unlikely that the FIFOs will overflow. If this FIFO fills then cells will be dropped. There are no workarounds for this problem. .

2.6.3 Performance without workaround:

Looped back cells may be dropped. These cells will be replaced by dummy cells by the Receive ATM Processor (RALP).

2.7 MVIP-90 Mode is Not Functional

2.7.1 Description

The MVIP-90 option does not work correctly. *H-MVIP works correctly.*

2.7.2 Workarounds:

Use external glue logic to make an MVIP-90 signal appear to the AAL1gator-8 to be a typical direct mode signal (LINE_MODE=00 / MVIP_EN=0).

2.7.3 Performance with workaround:

With glue logic, the MVIP-90 signal appears to the AAL1gator-8 to be a typical direct mode signal, and therefore functions normally.

2.7.4 Performance without workaround:

MVIP-90 is not functional; however H-MVIP works correctly. Data will not have correct frame alignment.

2.8 REF_VAL_ENABLE in E1 SDF-MF Mode is not Functional

2.8.1 Description

This errata only applies when using E1 SDF-MF mode with all (up to 32) queues on the line configured for single DS0, full cells, with or without signalling; it does not apply to all other modes.

A new feature to minimize CDV for single-DS0 connections with signaling using full cells was introduced in the AAL1gator-8. As described in the “TxA1SP” and “Add Queue FIFO” sections of the datasheet for single DS0 queues with signaling enabled using full cells, cell clumping can occur in situations where cells from different VCs are scheduled such that they are to be segmented at the same instance in time.

The CDV introduced in this case can be minimized by setting REF_VAL_ENABLE to 1. With REF_VAL_ENABLE set to 1, and using different

offset values for each queue on a particular line, when adding an entry to the Add_Queue_FIFO, the scheduling of cell segmentation is distributed in such a manner as to minimize CDV. Note that the algorithm for distributing cell segmentation is based on the premise that all queues on a line are single DS0 full cell queues. See the datasheet for details.

This feature works for all modes except E1 SDF-MF mode.

2.8.2 Workaround:

Don't enable REF_VAL_ENABLE in E1 SDF-MF mode. All other modes support REF_VAL_ENABLE as documented in the datasheet.

With the REF_VAL_ENABLE bit cleared the CDV introduced by the AAL1gator-8 is the same as it is for the PM73121 AAL1gator-II.

2.8.3 Performance without workaround:

CDV introduced by the AAL1gator-8 is the same as it is for the PM73121 AAL1gator-II.

2.9 UTOPIA Registers - Read Timing Violation

2.9.1 Description

In the AAL1gator-8 Datasheet, the Microprocessor Interface Read Timing specifies that the AAL1gator-8 provides 5 ns of setup time from data valid to ACKB asserted low. For the UTOPIA registers (address 0x80120 -0x80125), the AAL1gator-8 Rev A actually provides negative 10 ns of setup time, i.e., AAL1gator-8 asserts ACKB low 10 ns *before* asserting data valid.

2.9.2 Workaround:

Read each UTOPIA register twice, discarding the read data from the first read.

2.9.3 Performance with workaround:

The data read from the UTOPIA registers will be correct.

2.9.4 Performance without workaround:

The data read from the UTOPIA registers may be invalid.

2.10 Setting HS_GEN_DS3_AIS Does Not Cause T_COND_CELL_CNT to Increment

2.10.1 Description

When the HS_GEN_DS3_AIS bit is set, the AAL1gator-8 generates cells with a framed DS3 AIS pattern, as a form of cell conditioning. The AAL1gator-8 should increment the T_COND_CELL_CNT instead of the T_CELL_CNT for each generated cell while HS_GEN_DS3_AIS is set. Instead the AAL1gator-8 erroneously continues to increment the T_CELL_CNT instead of the T_COND_CELL_CNT.

2.10.2 Workaround:

There is no workaround. See Section 2.10.3.

2.10.3 Performance without workaround:

T_COND_CELL_CNT does not indicate the number of conditioned cells generated. The number of conditioned cells generated can be approximated by multiplying the nominal cell rate by the amount of time that the HS_GEN_DS3_AIS bit was set.

2.11 Maintain Bit-Count-Integrity Through Underrun Feature is Not Functional

2.11.1 Description

For real-time applications such as voice, it may be desirable to have a shallow receive buffer to minimize delay - this is done by using a low R_CDVT value. With a low R_CDVT value, when as few as one cell is lost, the receive buffer can quickly underrun. For SDF-FR and SDF-MF queues, the Receive Adaptation Layer Processor (RALP) responds to this underrun by initiating a structure search which results in the RALP dropping all received cells until it finds the next structure pointer followed by dropping all cell bytes until if finds the start of the structure. The net result is a loss of bit-count-integrity on the CES connection. For UDF-ML queues, the RALP does not initiate a structure search, but does initiate the resume procedure in which RFTC plays out R_COND_DATA while RALP accumulates R_CDVT's worth of bits. This also results in a loss of bit-count-integrity on the CES connection.

With the Bit-Count-Integrity Through Underrun feature enabled by setting the BITI_UNDERRUN bit, the bit-count-integrity of the CES connection can be maintained. The RALP maintains bit-count-integrity because it does not initiate a

structure search or a resume procedure when cells are lost. (see the section on ”Sequence Number Processing” in the datasheet).

This feature is not functional in Rev A.

2.11.2 Workaround:

Use a larger value for R_CDVT when using sequence number processing so that underruns do not occur when cells are lost.

2.11.3 Performance without workaround:

R_CDVT must be set larger, when using sequence number processing. For small values of R_CDVT, the benefits of sequence number processing may not be realized.

3 CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-2000422 (P1), Issue date: February 2001