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Phison Electronics Corporation

PS4043S Controller Spec.

version 1.1

Document Number ：S-05007

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Contents

Revision History

Revision	History	Draft Date	Remark
1.0		14-Dec-04	Estan
1.1	1. New flash supported list table. 2. LGA pin description of J4 -- DV_CARD_PAD, Dual / High voltage selected.	10-Jan-05	Estan

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A. General Description

Phison's flash memory controller PS4043S is specially designed for the Secure Digital (SD) Card. It supports 16~512M byte of NAND flash memory and allows the selection of either SD or SPI mode. To store and transfer data securely, the PS4043S controller provides both data write protection and password protection. In addition, it has a built-in SRAM Buffer and a Dual Buffer mode to allow smooth reading and writing. Using this one chip solution, both RMA problems and manufacturing time between Research & Development and mass production will be significantly reduced.

PS4043S also extends the clock frequency to 50MHz for higher data transfer rate. The multiple (x1 bit, x4 bit) bus-width feature allows for host design flexibility and higher data transfer bandwidth.

B. Controller Features

- Support SD system specification version 1.01, 1.1
- Designed for read-only, read/write storage cards：
  – Support NAND type flash： 16~512 MBytes [Include MLC or Binary Flash]
- Support SD SPI mode
- Block read and block write supported [class 2 and class 4]
- Erase supported [class 5]
- Write protection supported [class 6]
- Lock card supported [class 7]
- CPRM(Content Protection for Recordable Media) of SD Card supported.
- Variable clock rate 0 - 50 MHz.
- High performance flash memory control with dual SRAM buffer mode
- Transmission speed：
  – SD-4bit interface Read / Write：12 MB/sec (Max) / 10 MB/sec (Max)
  – SD-1bit interface Read / Write：3.1 MB/sec (Max) / 2.9 MB/sec (Max).
- Voltage range for communication： 2.0 - 3.6V.
- ECC circuits to protect data communication.

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C. Main Features Guide

Main Features	PS4043S
Specifications support	SD1.01, SD1.1
CPRM support	Yes
Lock/unlock function support	Yes
SLC NAND Flash support : Small Block-- Large Block--	 128Mb~1Gb 1Gb~4Gb, 8Gb*1
MLC NAND Flash support : Small Block-- Large Block--	 512Mb~4Gb refer to flash supported list table as below
Maximum Storage Capacity(CSD) support	4GB
Number of NAND Flash support	4
Voltage Supports	Dual Voltage 1.8/3.3V
Flash I/O	8-bit/16-bit*2
IC Technology	0.18um
Controller Package (mm x mm)	LGA-52pin 3.0 x 7.6

***1 :** Dual die with dual nCE(2 chip enable pin)

***2 :** 2x8-bit parallel mode(Dual channel)

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D. Flash Supported Table

D1. Flash type list and definition :

SLC	Single-Level Cell	**1P**	1-plane
MLC	Multi-Level Cell	**2P**	2-plane
SB	Small Block = 2k+64bytes per page	**4P**	4-plane
LB	Large Block = 2k+64bytes per page(Toshiba)		
BB	Big Block = 2k+64bytes per page(Samsung)		

Type	SLC-SB	SLC-LB	MLC-SB	MLC-LB-Conv
Capacity	128Mb 1P	1Gb 1P	512Mb 4P	512Mb N.A
	256Mb 1P	2Gb 1P	1Gb 4P	1Gb N.A
	512Mb 1P	4Gb 1P	2Gb 4P	2Gb 1P
	1Gb 1P	8Gb 1P Note2	4Gb 4P	4Gb 2P
	512Mb 4P Note1			8Gb 2P
	1Gb 4P Note1			
Vendor	Hynix Samsung ST Toshiba	Micron Hynix Samsung ST Toshiba	Toshiba	Samsung Toshiba

Type	MLC-LB-ABL	AG-AND-LB	TwinNAND(NROM)-SB
Capacity	512Mb 1P	1Gb 4P	512Mb 1P
	1Gb 1P	2Gb 4P	
	2Gb 1P	4Gb 4P	
Vendor	Toshiba	Renesas	Infineon

Note1 : 4P structure only support with Toshiba and Samsung 512Mb/1Gb NAND flash

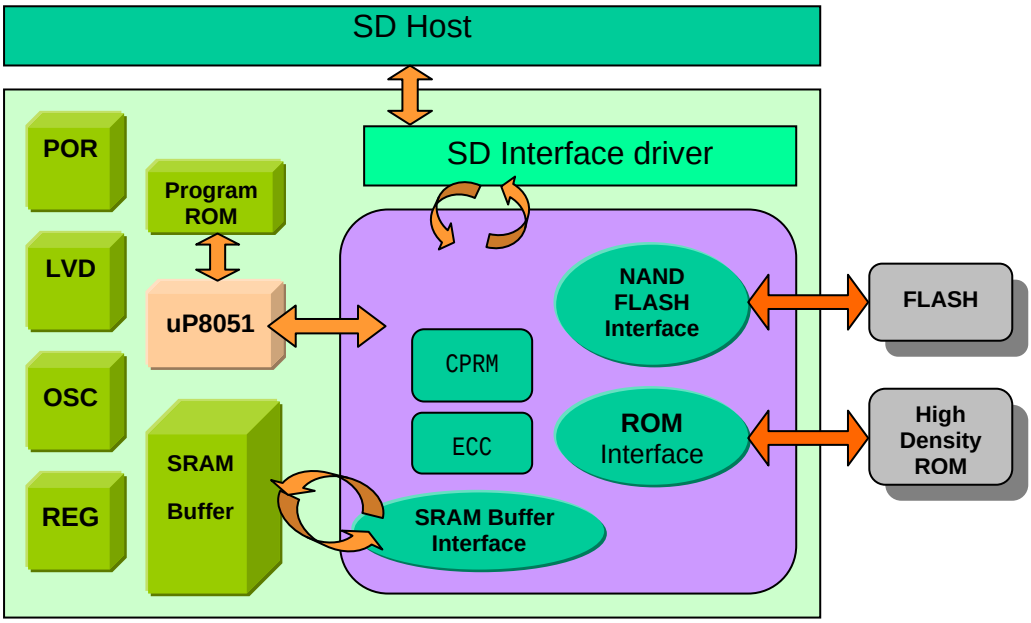
Note2 : Not the mono die, there was dual die with 2 chip enable pin

D2. Flash supported table :

F/W ver.		PS4043 CC	PS4043 CD	PS4043 CE
NAND Type	Mode	Support	Support	Support
SLC-SB-1P	x1	O	O	X
	x2	O	O	X
SLC-SB-4P (Toshiba/Samsung)	x1	O	O	X
	x2	X	X	X
SLC-LB	x1	O	O	X
	x2	O	O	X
MLC-SB-4P	x1	O	O	X
	x2	X	X	X
MLC-LB-Conv-1P	x1	X	O	X
	x2	X	X	X
MLC-LB-Conv-2P	x1	X	O	X
	x2	X	X	X
MLC-LB-ABL-1P	x1	X	O	X
	x2	X	X	X
MLC-LB-ABL-2P	x1	X	X	X
	x2	X	X	X
AG-AND-4P	x1	O support spec “B”	X	O support spec “B”, “C” & “D”
	x2		X	
TwinNAND	x1	O	X	X
	x2	X	X	X

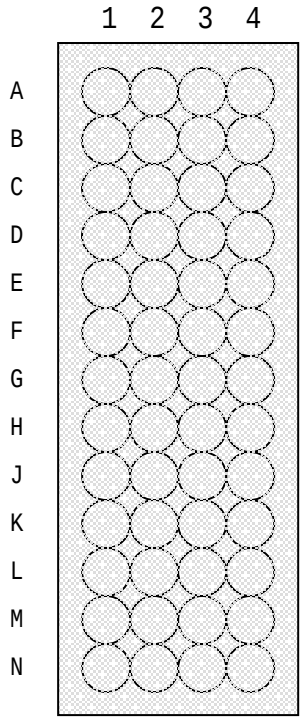
E. BLOCK DIAGRAM

SD CONTROLLER BLOCK DIAGRAM

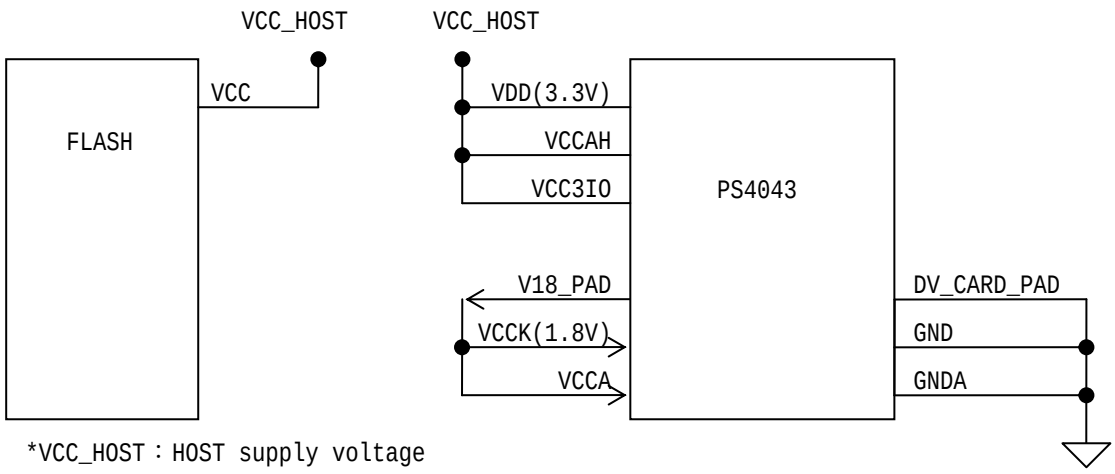


F. Pin Assignment and Description

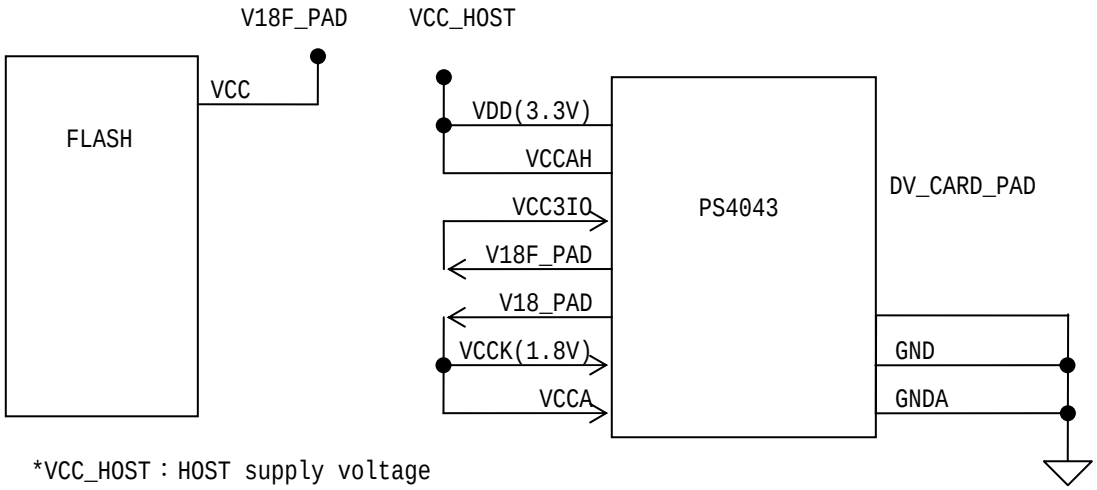
PS4043S LGA Top View：



F1. Pin Description of Power Setting Diagram (flash voltage 2.7V ~ 3.6V)



F2. Pin Description of Power Setting Diagram (flash voltage 1.7V ~ 1.95V)



*VCC_HOST：HOST supply voltage

F3. Pins Listed in Numeric Order & Pin Description：

BALL No.	BALL Name	Dir.	Description
A1	NC	-	No Connect
B1	FAD_PAD[5]	I/O	Flash IO
C1	FAD_PAD[6]	I/O	Flash IO
D1	AGAND_RST	O	AGAND flash reset
E1	FARDB_PAD	O	Flash read enable
F1	FCEB_PAD[2]	O	Flash chip enable
G1	FACLE_PAD	O	Flash command latch enable
H1	NC	-	No Connect
J1	GND	I	Ground
K1	VCCK(1.8V)	I	Power
L1	CLK_PAD	I	Clock
M1	DAT0_PAD	I/O	Data
N1	DAT7_PAD	I/O	Data
A2	FBD_PAD[7]	I/O	Flash IO
B2	FBD_PAD[6]	I/O	Flash IO
C2	FAD_PAD[4]	I/O	Flash IO
D2	FAD_PAD[7]	I/O	Flash IO
E2	FARDY_PAD	I	Flash ready/busy output
F2	FCEB_PAD[0]	O	Flash chip enable
G2	FCEB_PAD[3]	O	Flash chip enable
H2	FAWRB_PAD	O	Flash write enable
J2	MODE_PAD	I	VDD
K2	DAT4_PAD	I/O	Data
L2	DAT5_PAD	I/O	Data
M2	VDD(3.3V)	I	Power
N2	DAT6_PAD	I/O	Data

BALL No.	BALL Name	Dir.	Description
A3	FAD_PAD[1]	I/O	Flash IO
B3	FBD_PAD[3]	I/O	Flash IO
C3	FBD_PAD[5]	I/O	Flash IO
D3	FBD_PAD[1]	I/O	Flash IO
E3	FAD_PAD[2]	I/O	Flash IO
F3	FCEB_PAD[1]	O	Flash chip enable
G3	FAALE_PAD	O	Flash address latch enable
H3	NC	-	No Connect
J3	DAT2_PAD	I/O	Data
K3	DAT3_PAD	I/O	Data
L3	CMD_PAD	I/O	Command / Response
M3	VCCAH	I	Power
N3	V18_PAD	O	1.8v output
A4	FAD_PAD[0]	I/O	Flash IO
B4	NC	-	No Connect
C4	FBD_PAD[0]	I/O	Flash IO
D4	FBD_PAD[2]	I/O	Flash IO
E4	FBD_PAD[4]	I/O	Flash IO
F4	FAD_PAD[3]	I/O	Flash IO
G4	VCC3IO	I	Power
H4	FAWP_PAD	O	Flash write protect
J4	DV_CARD_PAD	I	Dual /High voltage select Connect to **Ground**: Dual(1.65~1.95/2.7~3.6) voltage supported. Connect to **Power**: High(2.7~3.6) voltage supported
K4	VCCA	I	Power
L4	DAT1_PAD	I/O	Data
M4	V18F_PAD	O	1.8v output
N4	GNDA	I	Ground

G. System Power Consumption

Table list as below is the power consumption of SD card with different type of flash memory. (PS4043S + Flash Memory)

Max Power up Current (uA)	Max Stand by Current (uA)	Max Read Current (mA)	Max Write Current (mA)
150	150	60 @ 3.6V	60 @ 3.6V

H. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+3.3	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	-25	+85	℃
4	Tst	Storage Temperature	-40	+85	℃

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	-25	+85	℃
V_{DD} Voltage	V_{DD}	2.0	3.6	V

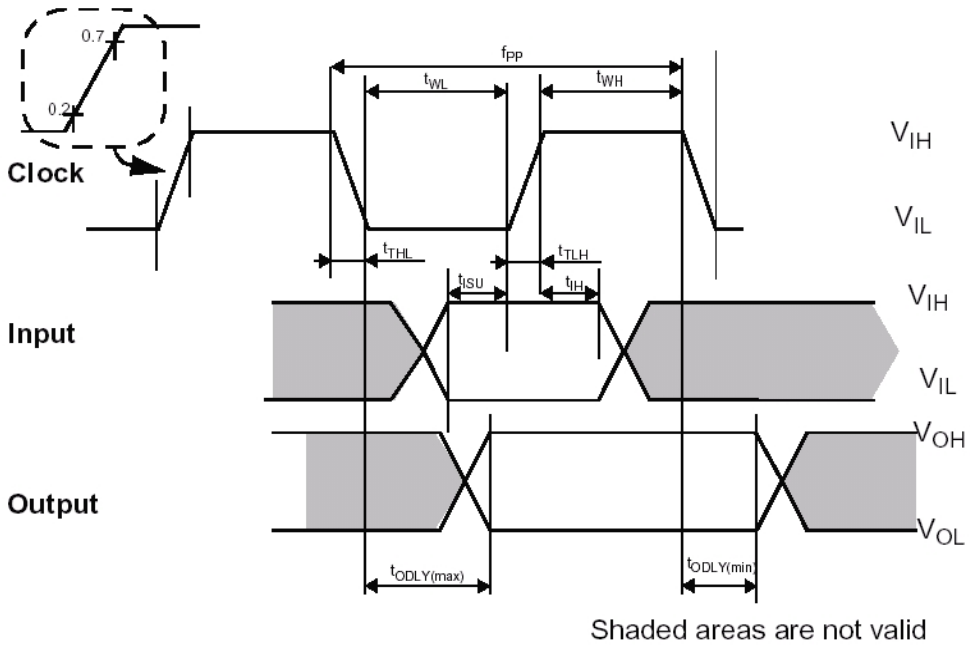
I. DC Characters

SD Controller DC Characteristics

Parameter	Symbol	Min.	Max	Unit	Condition
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA @VDD Min
Output Low Voltage	VOL		0.125*VDD	V	IOL=100uA @VDD Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25*VDD	V	

J. AC Characters

J1. SD Interface timing :



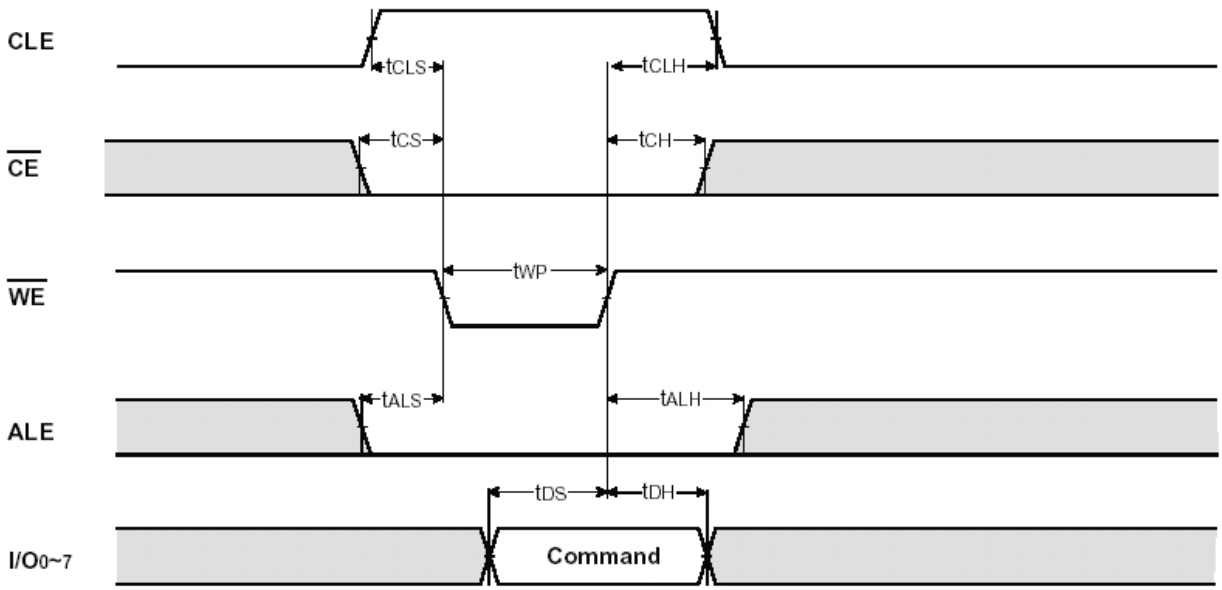
Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_L≤100 pF (7 cards)
Clock frequency Identification Mode(the low freq. is required for MultiMedia Card compatibility)	f_{OD}	0	400	KHz	C_L≤250 pF (21 cards)
Clock low time	t_{WL}	10		ns	C_L≤100 pF (7 cards)
Clock high time	t_{WH}	10		ns	C_L≤100 pF (7 cards)
Clock rise time	t_{TLH}		10	ns	C_L≤100 pF (7 cards)
Clock fall time	t_{THL}		10	ns	C_L≤100 pF (7 cards)
Clock low time	t_{WL}	50		ns	C_L≤250 pF (21 cards)
Clock high time	t_{WH}	50		ns	C_L≤250 pF (21 cards)
Clock rise time	t_{TLH}		50	ns	C_L≤250 pF (21 cards)
Clock fall time	t_{THL}		50	ns	C_L≤250 pF (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_L≤25 pF (1 cards)
Input hold time	t_{IH}	5		ns	C_L≤25 pF (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	C_L≤25 pF (1 cards)

J2. Flash Interface AC Characteristic：

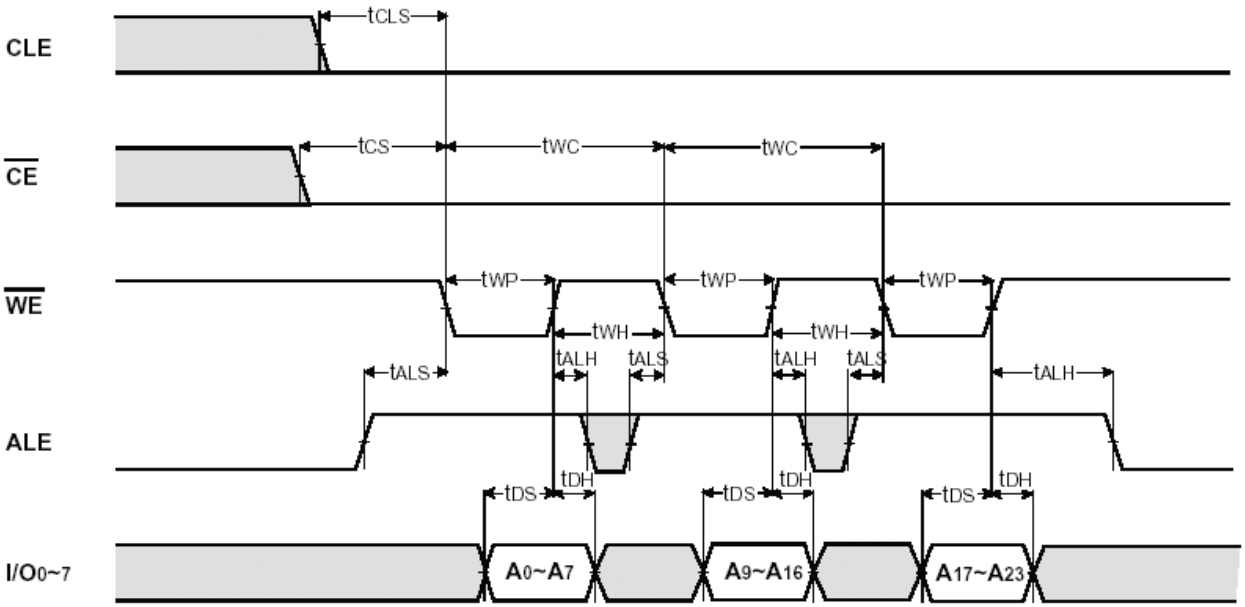
Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	60	-	ns
/CE Setup Time	t_{CS}	0	-	ns
/CE Hold Time	t_{CH}	120	-	ns
WE Pulse Width	t_{WP}	60	-	ns
ALE Setup Time	t_{ALS}	60	-	ns
ALE Hold Time	t_{ALH}	60	-	ns
Data Setup Time	t_{DS}	28	-	ns
Data Hold Time	t_{DH}	32	-	ns
Write Cycle Time	t_{WC}	60	-	ns
WE High Hold Time	t_{WH}	20	-	ns
Read Cycle Time	t_{RC}	60	-	ns
/RE Pulse Width	t_{RP}	40	-	ns
/RE High Hold Time	t_{REH}	20	-	ns
Ready to /RE Low	t_{RR}	120	-	ns

J3. Flash memory timing

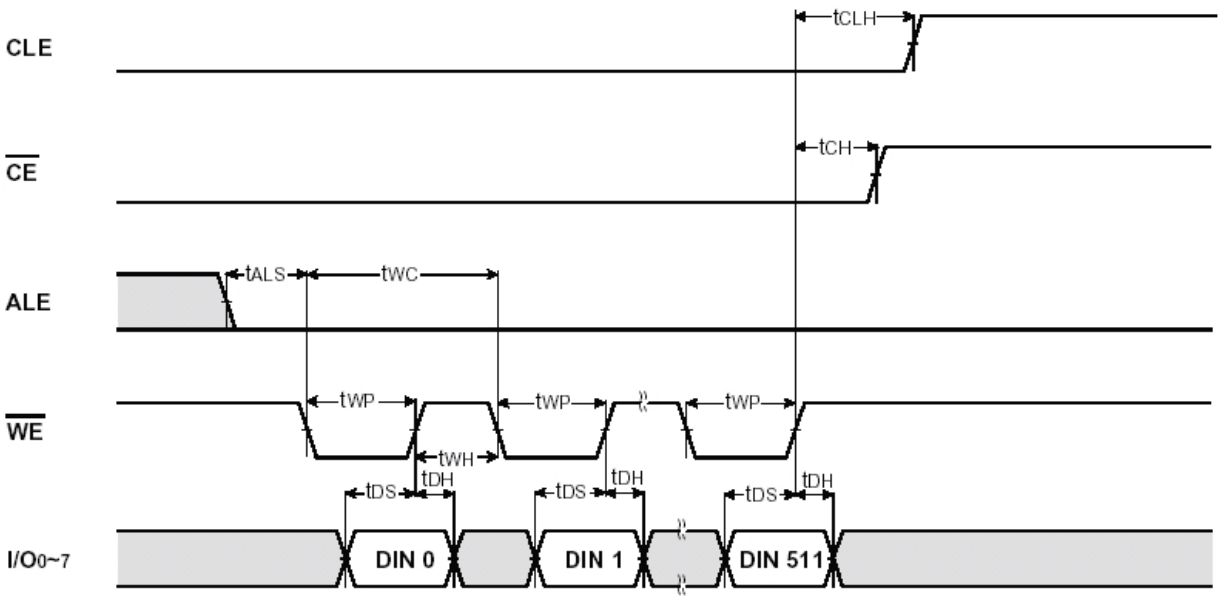
(a) Command Latch Cycle



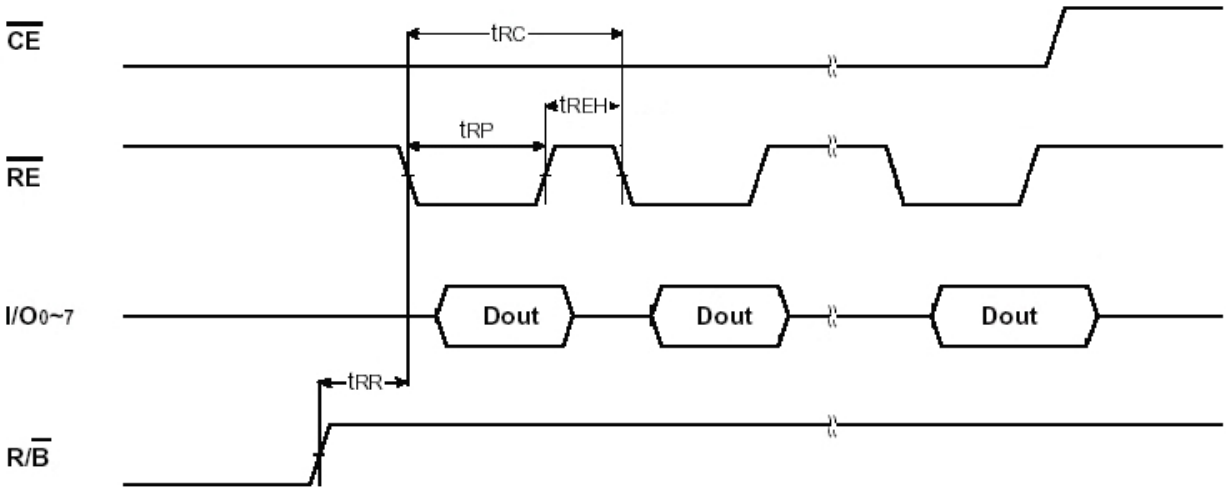
(b) Address Latch Cycle



(c) Input Data Latch Cycle



(d) Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



K. Package Information

1. **LGA 52 PIN 3.0 x 7.6 mm^2**
2. **0.5 mm PIN PITCH**
3. **ψ0.23 mm**
4. **T = 0.67 MAX**
5. **SBT = 0.21 mm**