OKI Semiconductor

This version: Jan. 1998
Previous version: Aug. 1996

MSM52V1001LP

131,072-Word × 8-Bit CMOS STATIC RAM

DESCRIPTION

The MSM52V1001LP is a 131,072-word by 8-bit CMOS static RAM featuring 3.0 V to 3.6 V power supply operation in the range of –40 °C to 85 °C and direct LVCMOS input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM52V1001LP can be used in the high-speed operation of an access time 100 ns due to adopting a high-performance CMOS technology and in the low current consumption of a standby current max. 50 µA when there is no chip selection. In addition, the MSM52V1001LP is the most suitable memory for microcomputer systems or data terminals because it is provided with a chip enable signal ($\overline{CE_1}$) suited to the expansion of a memory capacity, a chip enable signal (CE_2) suited to a battery back-up, and an output enable signal ($\overline{OE}$) suited to the I/O bus line control.

FEATURES

- 131,072-word × 8-bit configuration
- Power supply voltage: 3.0 V to 3.6 V
- Fully static operation
- Operating temperature range: Ta = –40°C to 85°C
- (Input/Output) LVCMOS compatible
- 3-state output
- Data retention available at power supply voltage 2 V
- Package options:

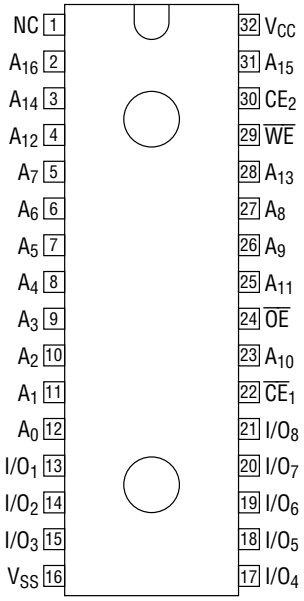
32-pin 600 mil plastic DIP	(DIP32-P-600-2.54)	(Product : MSM52V1001LP-xxRS)
32-pin 525 mil plastic SOP	(SOP32-P-525-1.27-K)	(Product : MSM52V1001LP-xxGS-K)
32-pin plastic TSOP (Type I)	(TSOPI32-P-820-0.50-K)	(Product : MSM52V1001LP-xxTS-K)
	(TSOPI32-P-820-0.50-L)	(Product : MSM52V1001LP-xxTS-L)

xx indicates speed rank.

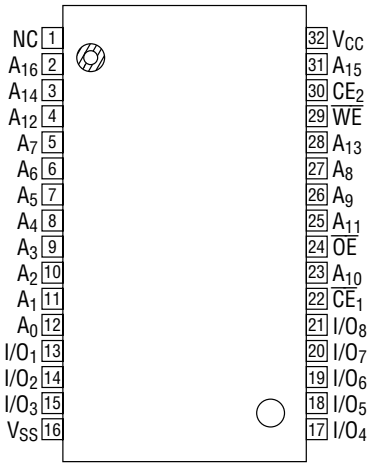
PRODUCT FAMILY

Family	Access Time (Max.)	Power Dissipation	
		Operating (Max.)	Standby (Max.)
MSM52V1001LP-10	100 ns	126 mW	0.18 mW
MSM52V1001LP-12	120 ns	108 mW	

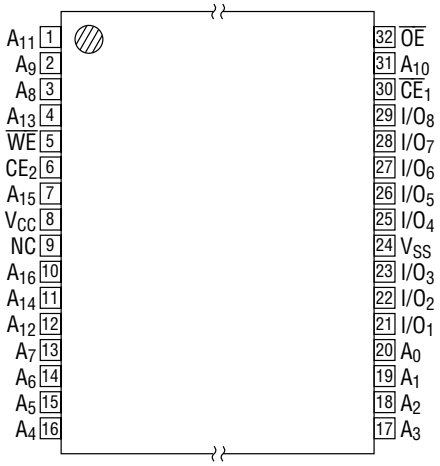
PIN CONFIGURATION (TOP VIEW)



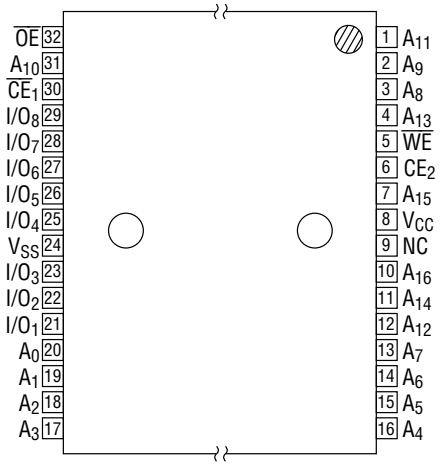
32-Pin Plastic DIP



32-Pin Plastic SOP



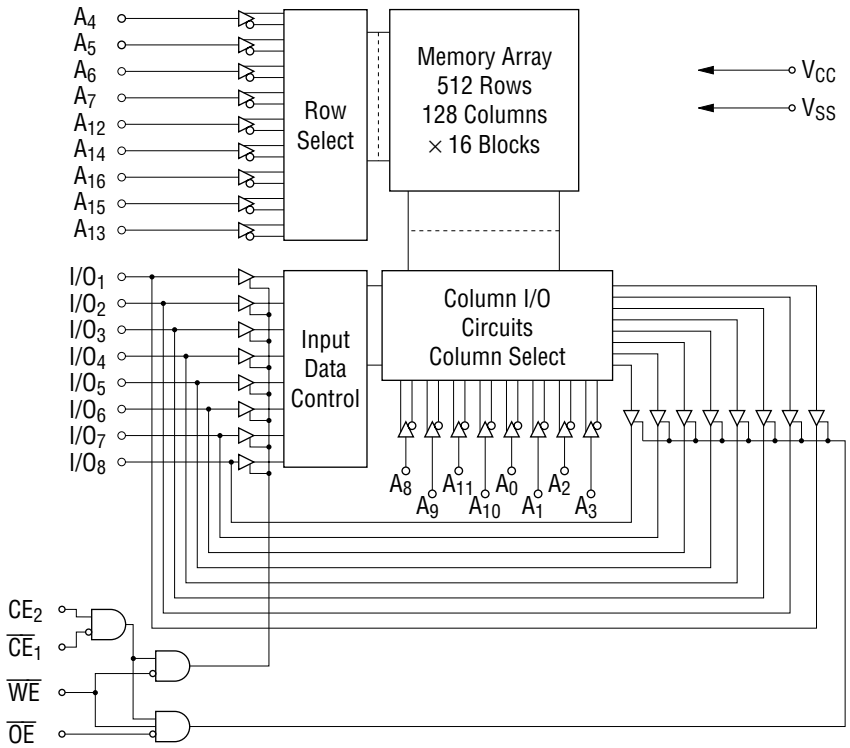
32-Pin Plastic TSOP (I)
(K Type)



32-Pin Plastic TSOP (I)
(L Type)

Pin Name	Function
A_0 - A_{16}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CE}_1$, CE_2	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Power Supply
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Operating Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Operating Contents	Power Mode
Read Cycle	H	*	*	*	Output Floating	Standby
	*	L	*	*		Standby
	L	H	H	H		Active
	L	H	H	L	Data Read	Active
Write Cycle	H	*	*	*	Output Floating	Standby
	*	L	*	*		Standby
	L	H	L	*	Data Write	Active

*Don't Care ("H" or "L")

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	Ta = 25°C, for V_{SS}	–0.5 to 4.6	V
Pin Voltage	V_T		–0.5* to V_{CC} + 0.5	V
Power Dissipation	P_D	Ta = 25°C	0.7	W
Operating Temperature	T_{opr}	—	–40 to 85	°C
Storage Temperature	T_{stg}	—	–55 to 125	°C

* –1.2 V Min. for pulse width less than 30 ns.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	—	3.0	—	3.6	V
	V_{SS}		0	0	0	V
Data Retention Voltage	V_{CCH}	—	2	—	3.6	V
Input High Voltage	V_{IH}	V_{CC} = 3.0 V to 3.6 V	2.4	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3*	—	0.4	V
Load Capacitance	C_L	—	—	—	100	pF
Fan Out	N	LVCMOS	—	—	1	—

* –1.2 V Min. for pulse width less than 30 ns.

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	V_I = 0 V	—	10	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	10	pF

Note: This parameter is periodically sampled and not 100% tested.

DC Characteristics

(V_{CC} = 3.0 V to 3.6 V, Ta = –40°C to 85°C)

Parameter	Symbol	Condition	MSM52V1001LP			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	–1.0	—	1.0	µA
Output Leakage Current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0 to V_{CC}	–1.0	—	1.0	µA
Output High Voltage	V_{OH}	I_{OH} = –100 µA	V_{CC} – 0.2	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	V
Standby Power Supply Current	I_{CCS}	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V, CE_2 ≥ V_{CC} – 0.2 V or 0 V ≤ CE_2 ≤ 0.2 V, V_{IN} = 0 to V_{CC}	—	—	50	µA
	I_{CCS1}	$\overline{CE_1}$ = V_{IH}, CE_2 = V_{IH} or CE_2 = V_{IL}	—	—	0.3	mA
Operating Power Supply Current	I_{CCA}	$\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}, V_{IN} = V_{IH} / V_{IL}, T_{CYC} = Min. cycle, I_{OUT} = 0 mA	—	—	①	mA
		$\overline{CE_1}$ ≤ 0.2 V, CE_2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V, T_{CYC} = 1 µs, I_{OUT} = 0 mA	—	—	10	mA

① 52V1001LP-10 35 mA
52V1001LP-12 30 mA

AC Characteristics

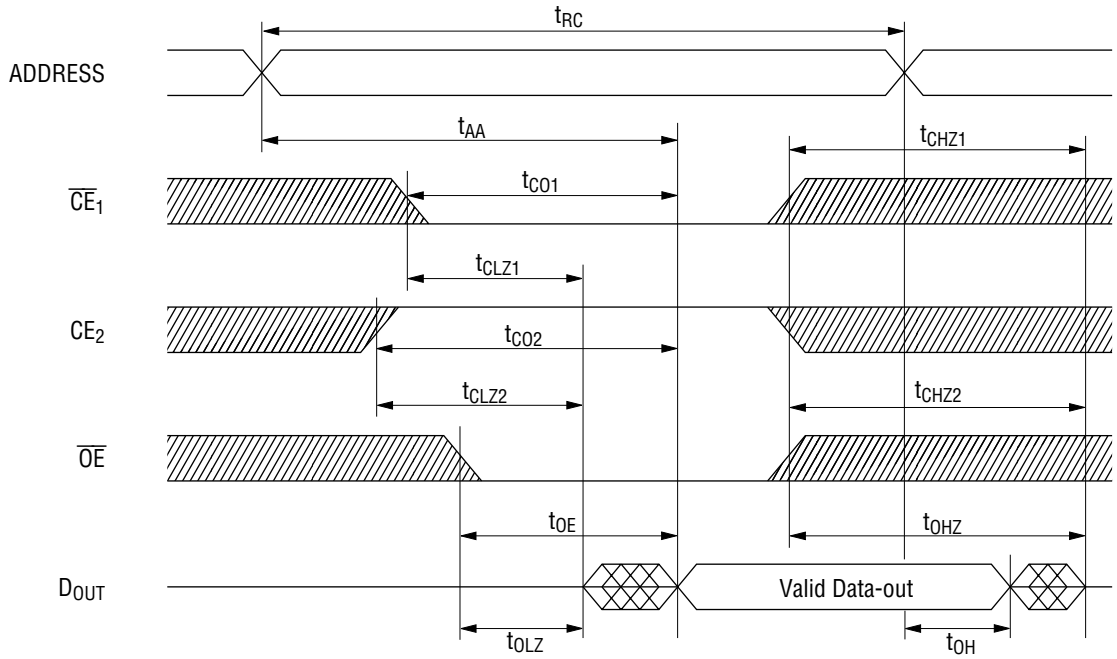
Test Conditions

Parameter	Condition
Input Pulse Level	V_{IH} = 2.4 V, V_{IL} = 0.4 V
Input Rise and Fall Times	5 ns
Input/Output Timing Level	1.4 V
Output Load	C_L = 100 pF, 1 LVCMOS

Read Cycle

(V_{CC} = 3.0 V to 3.6 V, Ta = –40°C to 85°C)

Parameter	Symbol	MSM52V1001LP-10		MSM52V1001LP-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	—	120	—	ns
Address Access Time	t_{AA}	—	100	—	120	ns
$\overline{CE}_1$, CE_2 Access Time	t_{CO1}	—	100	—	120	ns
	t_{CO2}	—	100	—	120	
$\overline{OE}$ Access Time	t_{OE}	—	50	—	60	ns
$\overline{CE}_1$, CE_2 to Output in Low-Z	t_{CLZ1}	10	—	10	—	ns
	t_{CLZ2}	10	—	10	—	
$\overline{OE}$ to Output in Low-Z	t_{OLZ}	5	—	5	—	ns
Output Hold Time from Address Change	t_{OH}	10	—	10	—	ns
$\overline{CE}_1$, CE_2 to Output in High-Z	t_{CHZ1}	—	35	—	35	ns
	t_{CHZ2}	—	35	—	35	
$\overline{OE}$ to Output in High-Z	t_{OHZ}	—	35	—	35	ns

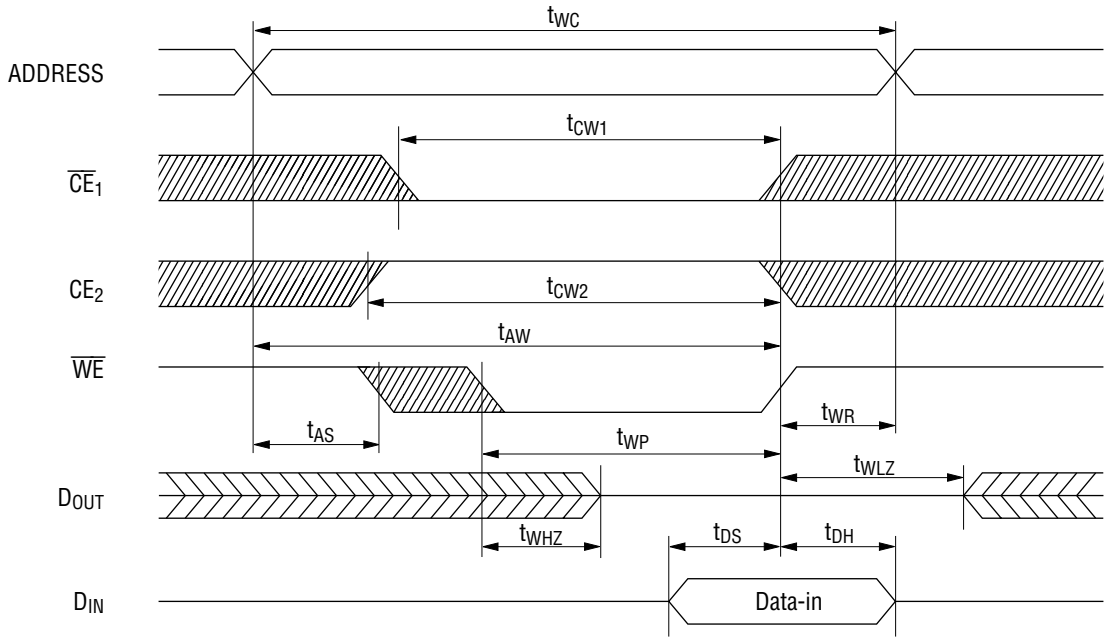


Notes:
1. A read cycle occurs during the overlap of $\overline{CE}_1$ = "L", CE_2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H".
2. t_{CLZ1} and t_{CLZ2} are specified from $\overline{CE}_1$ = "L" or CE_2 = "H", whichever occurs last.
3. t_{CHZ1} and t_{CHZ2} are specified from $\overline{CE}_1$ = "H" or CE_2 = "L", whichever occurs first.
4. t_{OHZ}, t_{CHZ1} and t_{CHZ2} are specified by the time when DATA is floating, not defined by the output level.

Write Cycle

(V_{CC} = 3.0 V to 3.6 V, Ta = –40°C to 85°C)

Parameter	Symbol	MSM52V1001LP-10		MSM52V1001LP-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100	—	120	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	75	—	90	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Setup Time	t_{DS}	40	—	50	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
$\overline{WE}$ to Output in High-Z	t_{WHZ}	—	35	—	35	ns
$\overline{CE}_1$, CE_2 to End of Write	t_{CW1}	90	—	100	—	ns
	t_{CW2}	90	—	100	—	
Address Valid to End of Write	t_{AW}	90	—	100	—	ns
Output Active from End of Write	t_{WLZ}	5	—	5	—	ns



Notes:
1. A write cycle occurs during the overlap of $\overline{CE}_1$ = "L", CE_2 = "H" and $\overline{WE}$ = "L".
2. $\overline{OE}$ may be either of "H" or "L" in the write cycle.
3. t_{AS} is specified from $\overline{CE}_1$ = "L", CE_2 = "H" or $\overline{WE}$ = "L", whichever occurs last.
4. t_{WP} is an overlap time of $\overline{CE}_1$ = "L", CE_2 = "H" and $\overline{WE}$ = "L".
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE}_1$ = "H", CE_2 = "L" or $\overline{WE}$ = "H", whichever occurs first.
6. t_{WHZ} is specified by the time when DATA output is floating, not defined by the output level.
7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

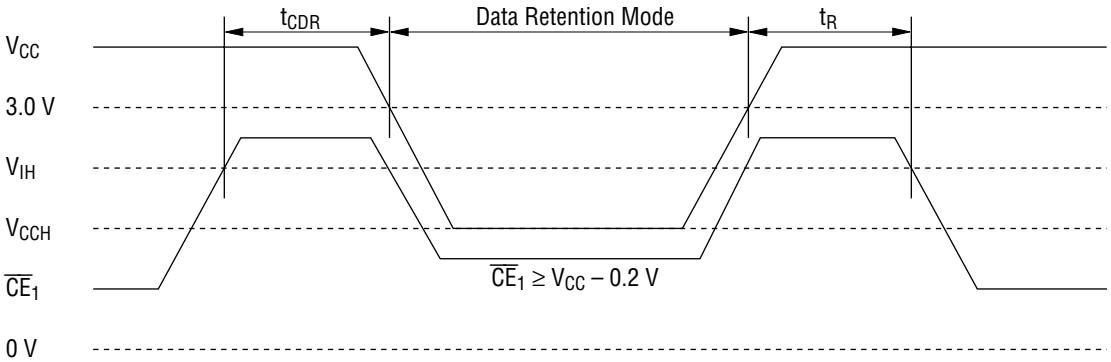
Data Retention Characteristics

(Ta = –40°C to 85°C)

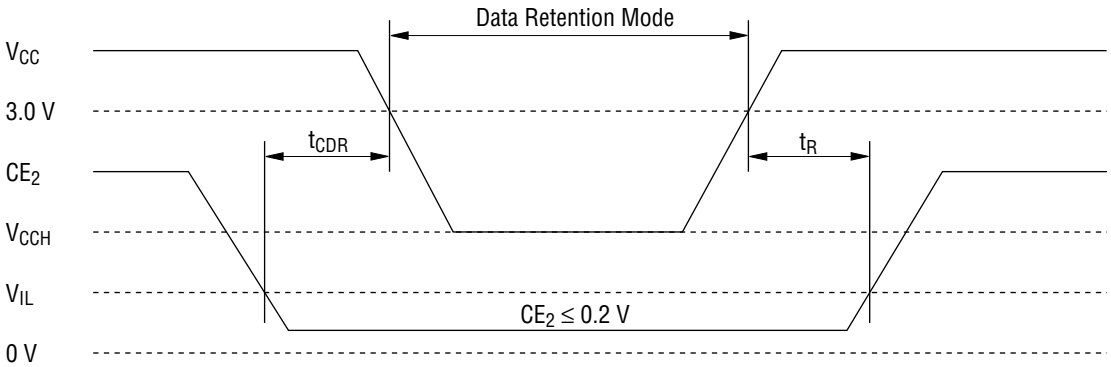
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V_{CCH}	$\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq CE_2 \leq 0.2$ V, $V_{IN} = 0$ to V_{CC}	2.0	—	—	V
Data Retention Power Supply Current	I_{CCH}	$V_{CC} = 3$ V, $V_{IN} = 0$ to V_{CC}, $\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq CE_2 \leq 0.2$ V	—	—	40*	µA
Chip Deselect to Data Retention Time	t_{CDR}	—	0	—	—	ns
Operation Recovery Time	t_R	—	50	—	—	ms

* 5 µA Max. when Ta = 0°C to 40°C.

$\overline{CE_1}$ Control



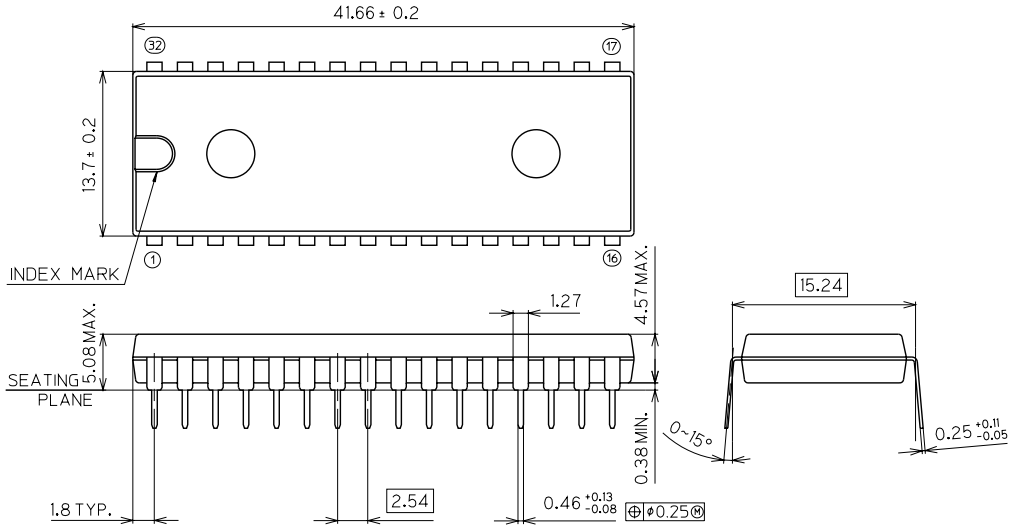
CE_2 Control



PACKAGE DIMENSIONS

(Unit : mm)

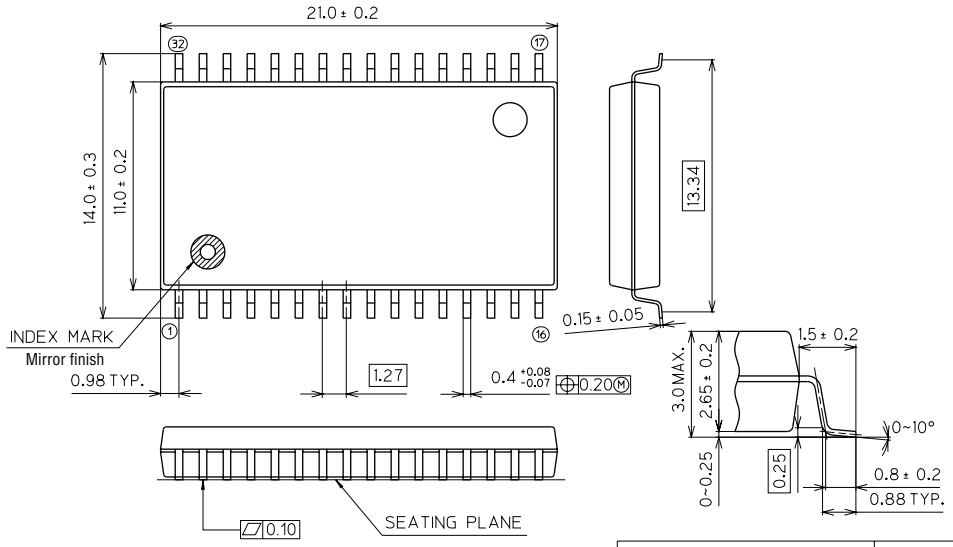
DIP32-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.70 TYP.

(Unit : mm)

SOP32-P-525-1.27-K



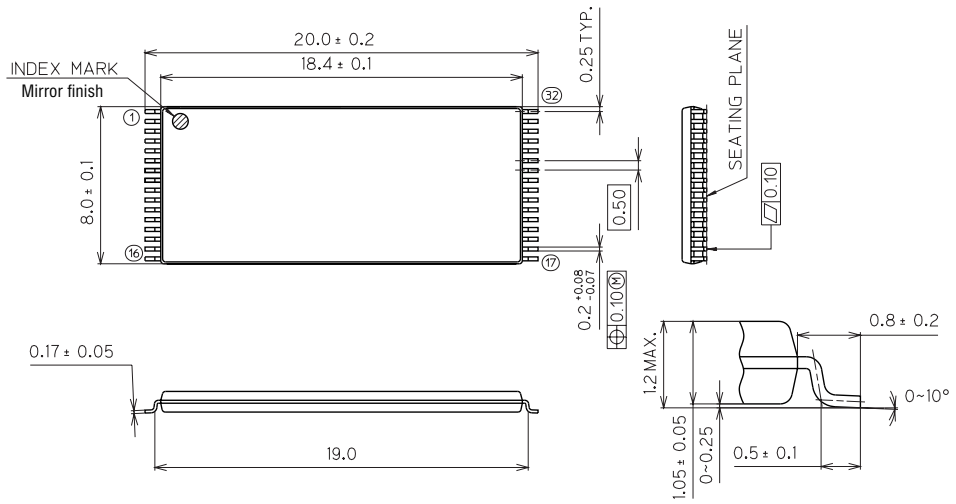
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.32 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPI32-P-820-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.40 TYP.

Notes for Mounting the Surface Mount Type Package

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