# MN863440

## TFT LCD Gate Driver with 200, 240, 256, or 263 Outputs

### ■ Overview

The MN863440 is a TFT LCD gate driver with 200, 240, 256, or 263 2-value outputs. The number of outputs can be selected to be any one of these by the user.

This IC implements 2-value (pseudo 3-value) drive, and provides a cascade-connection pin to support large-screen displays. It is provided in a TCP package.

### ■ Features

- Adopts a bidirectional shift register system
- Provides an expansion pin so that the number of output pins can be increased.
- Pulse width modulation function (OE1 to OE3)
- Driver operating frequency: 500 kHz (maximum)
- LCD drive voltage: $V_{EE} + 40$ V (maximum)
- Driver output levels: 2 levels (The low level can be modified.)
- Supports TCP mounting.
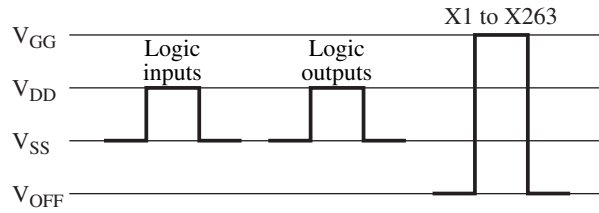
### ■ Applications

- LCD TV sets

### ■ Block Diagram
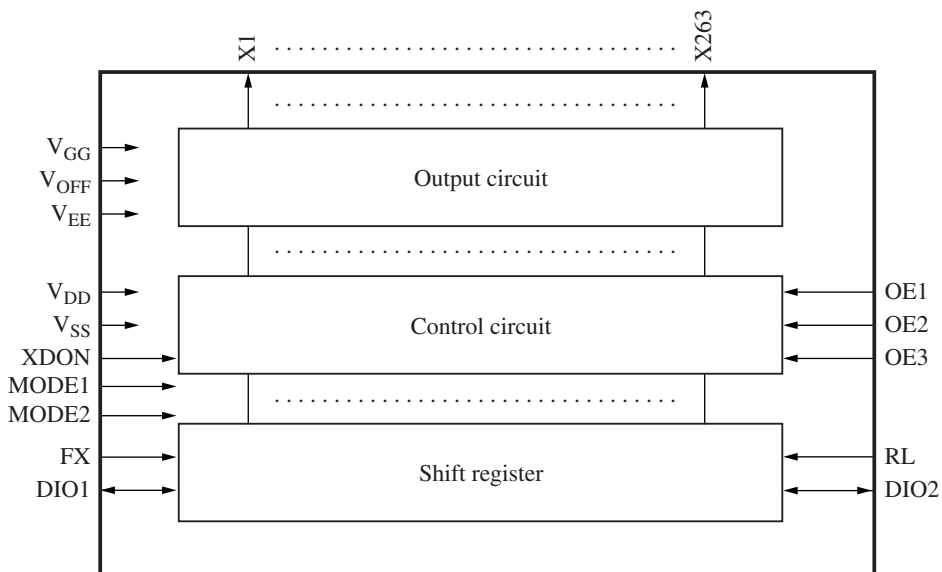
■ Functional Descriptions

1. LCD drive voltages

The MN863440 can provide LCD drive voltages that are negative relative to logic ground.



2. Operation

The MN863440 outputs either the display level ($V_{GG}$) or the off level ($V_{OFF}$) from the LCD driver outputs (X1 to X263) under control of the shift data and the OE input signal.

The data shift direction can be controlled with the shift direction switching pin (RL).

The DIO input signal is acquired on the rising edge of FX. The shift register operates and the drive voltages are output with this timing as well. The DIO output is synchronized with the falling edge of FX.

| RL | Start pulse input | Data transfer direction | Carry pulse output |
|---|---|---|---|
| RL = High | DIO1 | X1 → X263 | DIO2 |
| RL = Low | DIO2 | X263 → X1 | DIO1 |

■ Functional Descriptions (continued)

3. OE function

   The outputs can be forced to the display off level regardless of the data in the shift register in sets consisting of every third output pin by setting the OE1, OE2, and OE3 pins to the high level.

   This function operates asynchronously with the FX pin.

| 200 output TCP | | 240 output TCP | | 256 output TCP | | 263 output TCP | |
|---|---|---|---|---|---|---|---|
| MODE1 = Low | | MODE1 = Low | | MODE1 = High | | MODE1 = High | |
| MODE2 = Low | | MODE2 = High | | MODE2 = Low | | MODE2 = High | |
| X1 | (OE1) | X1 | (OE1) | X1 | (OE1) | X1 | (OE1) |
| X2 | (OE2) | X2 | (OE2) | X2 | (OE2) | X2 | (OE2) |
| X3 | (OE3) | X3 | (OE3) | X3 | (OE3) | X3 | (OE3) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| X98 | (OE2) | | | | | X98 | (OE2) |
| X99 | (OE3) | | | | | X99 | (OE3) |
| X100 | (OE1) | | | | | X100 | (OE1) |
| | | | | ⋮ | ⋮ | ⋮ | ⋮ |
| | | X118 | (OE1) | | | X118 | (OE1) |
| | | X119 | (OE2) | | | X119 | (OE2) |
| | | X120 | (OE3) | | | X120 | (OE3) |
| | | | | ⋮ | ⋮ | ⋮ | ⋮ |
| | | | | X126 | (OE3) | X126 | (OE3) |
| | | | | X127 | (OE1) | X127 | (OE1) |
| | | | | X128 | (OE2) | X128 | (OE2) |
| | | | | | | X129 | (OE3) |
| | | | | | | X130 | (OE1) |
| | | | | | | X131 | (OE2) |
| | | | | | | X132 | (OE3) |
| | | | | | | X133 | (OE1) |
| | | | | | | X134 | (OE2) |
| | | | | | | X135 | (OE3) |
| | | | | X136 | (OE3) | X136 | (OE1) |
| | | | | X137 | (OE1) | X137 | (OE2) |
| | | | | X138 | (OE2) | X138 | (OE3) |
| | | | | ⋮ | ⋮ | ⋮ | ⋮ |
| | | X144 | (OE1) | | | X144 | (OE3) |
| | | X145 | (OE2) | | | X145 | (OE1) |
| | | X146 | (OE3) | | | X146 | (OE2) |
| | | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |

■ Functional Descriptions (continued)

3. OE function (continued)

| 200 output TCP | 240 output TCP | | 256 output TCP | | 263 output TCP |
|---|---|---|---|---|---|
| X164　(OE2) | ⋮ | ⋮ | ⋮ | ⋮ | X164　(OE2) |
| X165　(OE3) | ⋮ | ⋮ | ⋮ | ⋮ | X165　(OE3) |
| X166　(OE1) | ⋮ | ⋮ | ⋮ | ⋮ | X166　(OE1) |
| ⋮　　⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮　　⋮ |
| X261　(OE3) | X261　(OE1) | | X261　(OE2) | | X261　(OE3) |
| X262　(OE1) | X262　(OE2) | | X262　(OE3) | | X262　(OE1) |
| X263　(OE2) | X263　(OE3) | | X263　(OE1) | | X263　(OE2) |

Here, (OEn) indicates which of OE1, OE2, and OE3 is the related signal.

4. XDON function

The outputs can be set to the output the display on potential ($V_{GG}$) regardless of the states of the OEn pins and the shift register data by setting the XDON pin to the low level.
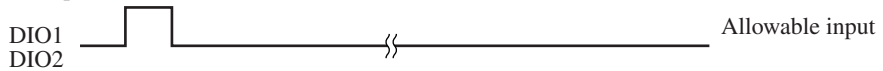
This function operates asynchronously with the FX pin. This pin is pulled up.
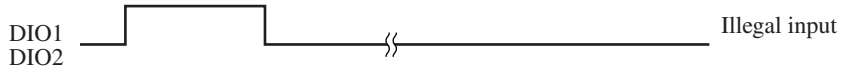
5. Carry input (DIO1, DIO2)

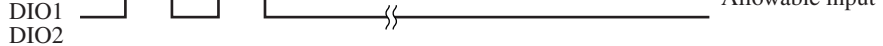The waveform input to the carry input must meet the following conditions.

FX　　1　2　3　4　5　　260 261 262 263
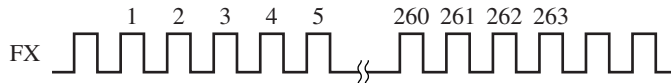
1) Single pulse width input

DIO1
DIO2　　　　　　　　　　　　　　　　　　Allowable input

2) Input with a width of 2 pulses or longer

DIO1
DIO2　　　　　　　　　　　　　　　　　　Illegal input

3) Double pulse input
Pulse spacing: An odd number
DIO1
DIO2　　　　　　　　　　　　　　　　　　Allowable input

4) Double pulse input
Pulse spacing: An even number
DIO1
DIO2　　　　　　　　　　　　　　　　　　Illegal input
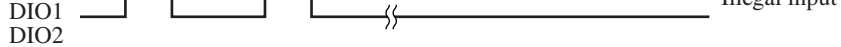
## ■ Pin Descriptions

| Pin Name | I/O | Function | Description |
|---|---|---|---|
| FX | I | Shift register clock input | The start pulse is acquired and the shift register shifted on the FX rising edge. The carry pulse is output on the FX falling edge. |
| RL | I | Right shift/left shift selection input | RL = High: X1 → X263 (Left shift)<br>RL = Low: X263 → X1 (Right shift) |
| DIO1<br>DIO2 | I/O | Start pulse input and carry pulse output | <table><tr><td></td><td>DIO1</td><td>DIO2</td></tr><tr><td>RL = High</td><td>I</td><td>O</td></tr><tr><td>RL = Low</td><td>O</td><td>I</td></tr></table> |
| MODE1<br>MODE2 | I | Output pin count switching inputs | <table><tr><td>MODE1</td><td>MODE2</td><td>LCD outputs</td></tr><tr><td>High</td><td>High</td><td>263</td></tr><tr><td>High</td><td>Low</td><td>256</td></tr><tr><td>Low</td><td>High</td><td>240</td></tr><tr><td>Low</td><td>Low</td><td>200</td></tr></table> |
| OE1 to OE3 | I | Display signal enable/disable inputs | When OEn is high, the corresponding LCD drive output pins are set to the display off potential ($V_{OFF}$) asynchronously with the FX pin, regardless of the states of the shift register and other input data.<br>See 3. OE function in the Functional Descriptions section. |
| X1 to X263 | O | LCD drive outputs | These pins output, in synchronization with the FX rising edge, either the $V_{GG}$ or the $V_{OFF}$ voltage level according to the shift register data and the states of the OE1 to OE3, DIO1, and DIO2 pins. |
| $V_{GG}$ | Power | LCD drive output block power supply<br>LCD drive supply 1 | Power su'pply for the level shifters and output buffers.<br>This supply is also used for the LCD drive voltage. |
| $V_{OFF}$ | Power | LCD drive supply 2 | Supplies an LCD drive voltage. |
| $V_{EE}$ | Power | $V_{GG}$ system ground | |
| $V_{DD}$ | Power | 3 V system logic power supply | Power supply used for the 3 V system logic circuits. |
| $V_{SS}$ | Power | $V_{DD}$ system ground | |

# Panasonic

■ Basic Waveforms

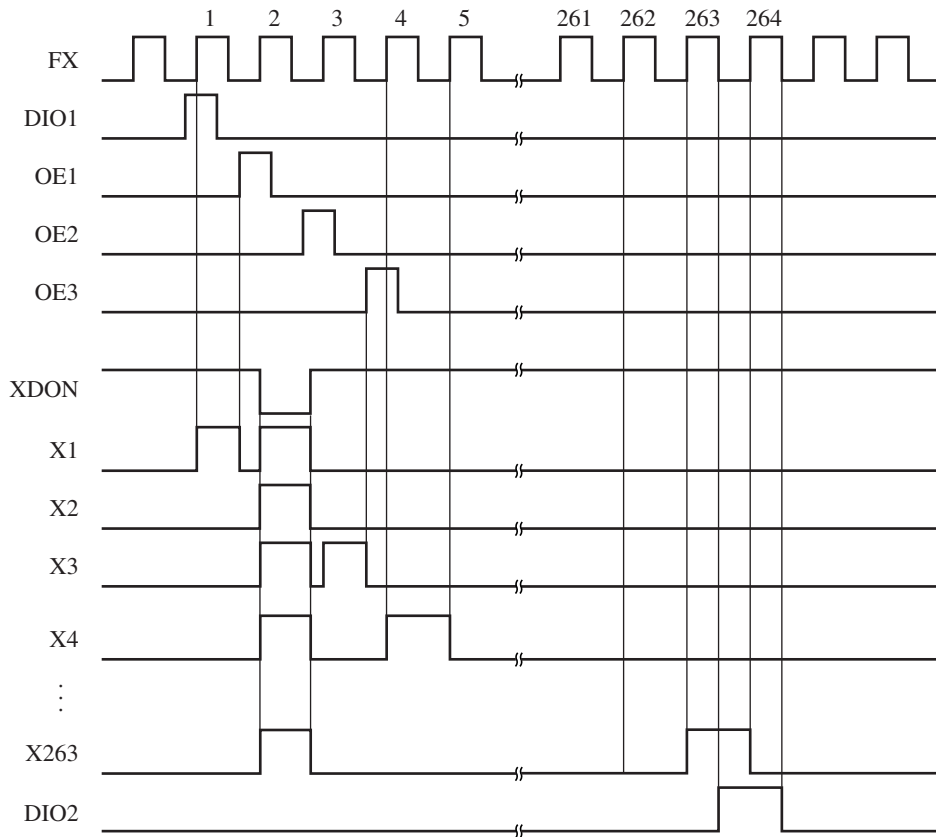1. RL = High, left shift, MODE1, MODE2 = high
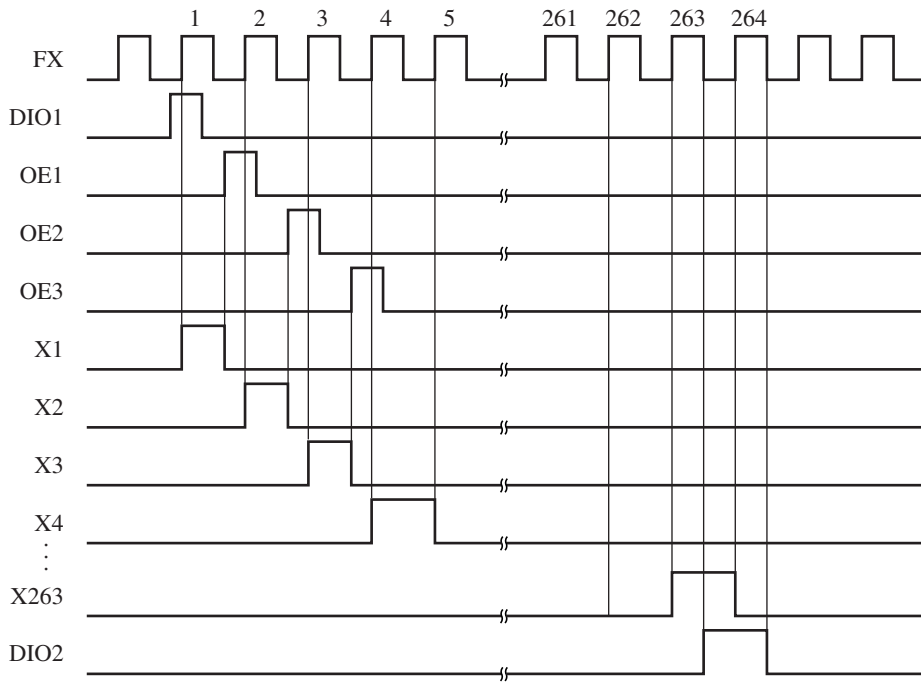


2. RL = Low, right shift, MODE1, MODE2 = high

SDF00033AEM
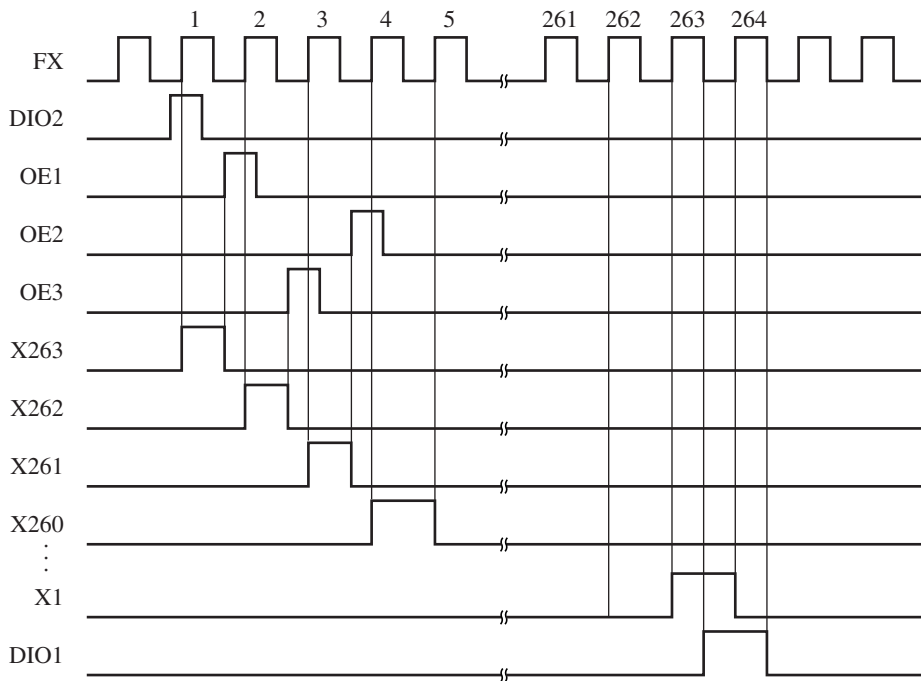
■ XDON Usage Example

• RL = High, left shift, MODE1, MODE2 = high

■ Electrical Characteristics

1.  Absolute Maximum Ratings at $V_{SS}$ = 0 V

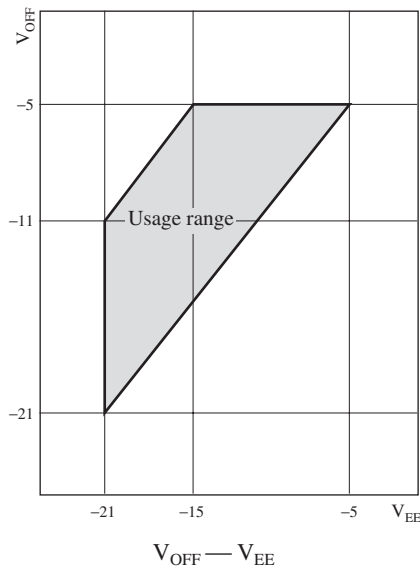| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage 1 | $V_{DD}$ | $-0.3$ to $+4.5$ | V |
| Supply voltage 2 | $V_{GG}$ | $V_{EE}$ to $V_{EE}$ $+44$ | V |
| Drive voltage | $V_{OFF}$ | $V_{EE} - 0.3$ to $V_{GG}$ $+0.3$ | V |
| Supply voltage 3 | $V_{EE}$ | $-24$ to $+0.3$ | V |
| Digital input voltage | $V_I$ | $-0.3$ to $V_{DD}$ $+0.3$ | V |
| Operating and storage temperature range | $T_a$ | $-30$ to $+85$ | °C |
| Operating ambient temperature | $T_{opr}$ | $-20$ to $+75$ | °C |
| Storage temperature | $T_{stg}$ | $-55$ to $+120$ | °C |

Note) 1. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.

    2. The operating and storage temperature range is the temperature range over which the chip will not be damaged even if operated. Note that performance is not guaranteed throughout this range.

    3. These ratings are guaranteed values when the standard Panasonic package is used.

    4. The power supply voltages must meet the condition $V_{EE} \leq V_{GG}$ at all times, including when power is being applied, during operation, and when power is being turned off.

    5. When power is applied, certain sequences of power application can cause large currents to flow and permanently damage the IC. To avoid this problem, first apply $V_{DD}$, and then, after $V_{DD}$ has reached 90% of its set voltage, apply $V_{EE}$, $V_{GG}$, and $V_{OFF}$.

2.  Operating Conditions at $V_{SS}$ = 0 V, $T_{opr}$ = -20°C to +75°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating supply voltage 1 | $V_{DD}$ | | 2.3 | — | 3.6 | V |
| Operating supply voltage 2 | $V_{GG}$ | | 10 | — | $V_{EE}$ $+40$ | V |
| Operating supply voltage 3 | $V_{EE}$ | | $-21$ | — | $-5$ | V |
| Operating supply voltage 3 | $V_{OFF}$ | $-21 \leq V_{EE} \leq -15$ | $V_{EE}$ | — | $V_{EE}$ $+10$ | V |
| | | $-15 < V_{EE} < -5$ | $V_{EE}$ | — | $-5$ | |

$V_{OFF}$ — $V_{EE}$

Note) These ratings are guaranteed values when the standard Panasonic package is used.

■ Electrical Characteristics (continued)

3. DC Characteristics at $V_{SS} = 0$ V, $T_{opr} = $ -20°C to +75°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating supply current ($V_{DD}$) | $I_{DD}$ | $f_{FX} = 15.7$ kHz<br>$f_{DIO} = 60$ Hz<br>$V_{DD} = 3.0$ V | — | — | 800 | μA |
| Operating supply current ($V_{GG}$) | $I_{GG}$ | $V_{OFF} = -15$ V<br>$V_{GG} = 15$ V<br>With no output load | — | — | 300 | μA |
| Standby mode current consumption ($V_{DD}$) | $I_{DS}$ | In standby mode<br>$V_{DD} = 3.0$ V | — | — | 600 | μA |
| Standby mode current consumption ($V_{GG}$) | $I_{GS}$ | $V_{OFF} = -15$ V<br>$V_{GG} = 15$ V | — | — | 100 | μA |
| 1) Input pins    RL, FX, OE1 to OE3, MODE1, MODE2 | | | | | | |
| High-level input voltage | $V_{IH1}$ | | $0.8 \times V_{DD}$ | — | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL1}$ | | 0 | — | $0.2 \times V_{DD}$ | V |
| Input leakage current | $I_{LI1}$ | | −10 | — | 10 | μA |
| 2) Pulled up input pins    XDON | | | | | | |
| High-level input voltage | $V_{IH2}$ | | $0.8 \times V_{DD}$ | — | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL2}$ | | 0 | — | $0.2 \times V_{DD}$ | V |
| Pull-up resistance | $R_{PU}$ | $V_{DD} = 3.0$ V | 10 | — | 100 | kΩ |
| 3) I/O pins    DIO1, DIO2 | | | | | | |
| High-level input voltage | $V_{IH3}$ | | $0.8 \times V_{DD}$ | — | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL3}$ | | 0 | — | $0.2 \times V_{DD}$ | V |
| High-level output voltage | $V_{OH}$ | $-100$ μA | $V_{DD} - 0.4$ | — | — | V |
| Low-level output voltage | $V_{OL}$ | $100$ μA | — | — | 0.4 | V |
| 4) LCD drive voltage input pin    $V_{OFF}$ | | | | | | |
| Input leakage current | $V_{LI1}$ | | −50 | — | 50 | μA |
| 5) LCD drive output pins    X1 ~ X263 | | | | | | |
| Output leakage current | $I_{LO1}$ | | −50 | — | 50 | μA |
| Output on resistance | RON-$V_{GG}$ | $V_{GG} = 15$ V<br>$V_{OFF} = -15$ V<br>$V_{OM} = V_{GG} - 0.5$ V<br>$V_{OM}$ is the X1 to X263 applied voltage. | 200 | 400 | 800 | Ω |
| | RON-$V_{OFF}$ | $V_{GG} = 15$ V<br>$V_{EE} = -15$ V<br>$V_{OFF} = -15$ V<br>$V_{OM} = V_{OFF} + 0.5$ V<br>$V_{OM}$ is the X1 to X263 applied voltage. | 200 | 400 | 800 | |

Note) These ratings are guaranteed values when the standard Panasonic package is used.

■ Electrical Characteristics (continued)

4. AC Characteristics at $V_{SS}$ = 0 V, $T_{opr}$ = -20°C to +75°C

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock period | $t_{FX}$ | | 2.0 | — | — | μs |
| Clock high-level pulse width | $t_{WH}$ | | 700 | — | — | ns |
| Clock low-level pulse width | $t_{WL}$ | | 700 | — | — | ns |
| DIO data setup time | $t_{su}$ | | 300 | — | — | ns |
| DIO data hold time | $t_h$ | | 300 | — | — | ns |
| DIO output delay time | $t_{pd1}$ | CL = 50 pF | — | — | 600 | ns |
| Xn output delay time | $t_{pd2}$ | CL = 300 pF | — | — | 800 | ns |

Note) These ratings are guaranteed values when the standard Panasonic package is used.

• AC Characteristics Timing Charts
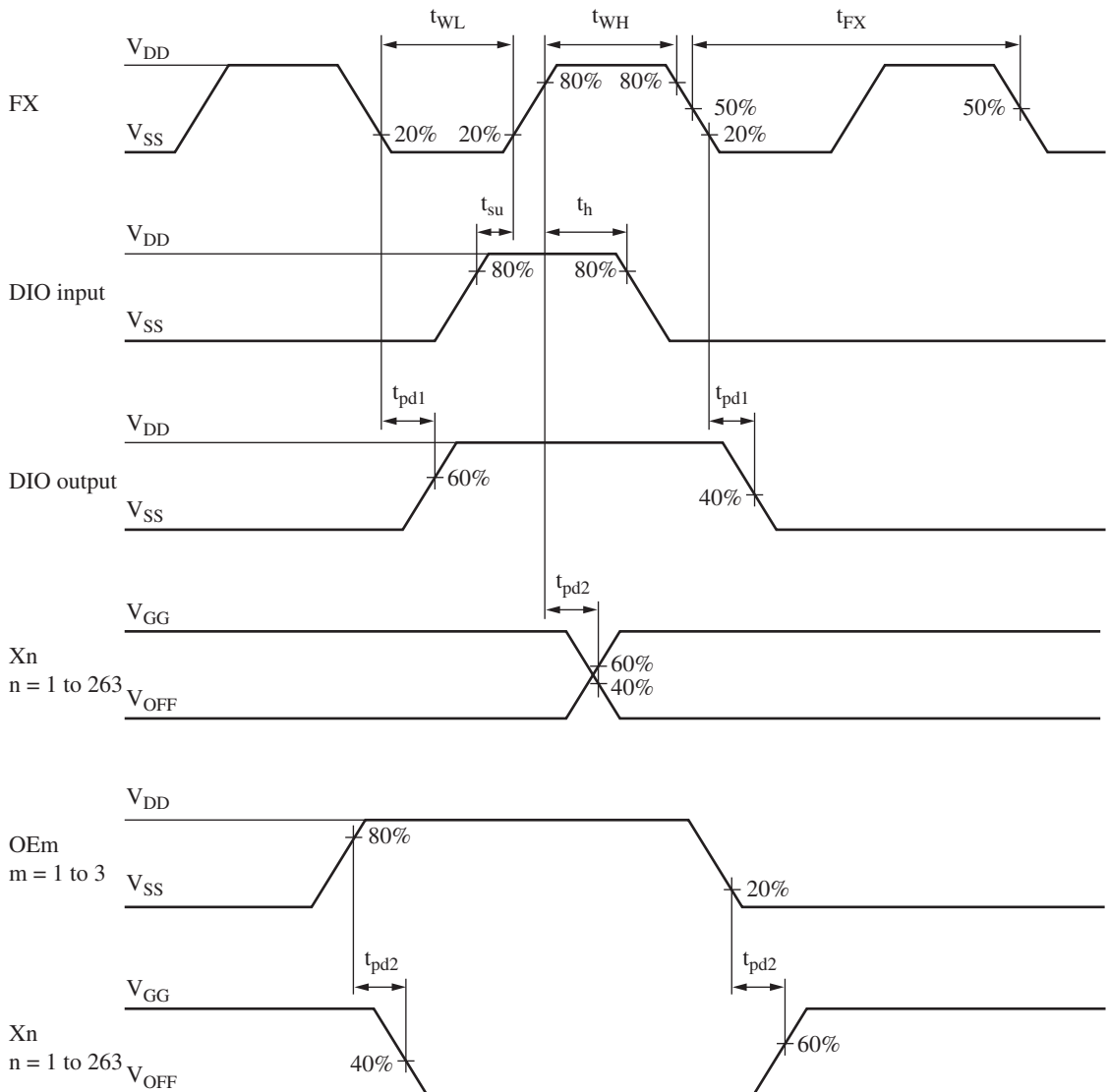
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