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IT8888G

PCI-to-ISA Bridge Chip

(Code Name: Golden Gate)

Preliminary Specification V0.9

ITE TECH. INC.

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Revision History

Section	Revision	Page
1	• Added a new feature, “SM Bus”.	1
3	• Chapter 3, Pin Configuration, was revised.	5
4	• Table 4-3, Miscellaneous Signals, was revised.	10
	• Table 4-5, IT8888G Pins Listed in Numeric Order, was revised.	11
	• Table4-6, Power-On-Strap Settings, was revised.	12

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1. Features

- **PCI Interface**
  - PCI Specification V. 2.1 compliant
  - Supports 32-bit PCI bus & up to 33 MHz PCI bus frequency
  - Supports PERR# & SERR# Error Reporting
  - Supports Delayed Transaction
  - Optional CLKRUN# interface support

- **Programmable PCI Address Decoders**
  - Supports either programmable positive decode or full subtractive decode of PCI cycles
  - Provides 6 positively decoded I/O blocks & 4 positively decoded memory blocks.
  - Optional support ROMCS# fast positive decoder

- **PC/PCI DMA Controller**
  - Comply with Intel Mobile PC/PCI DMA R2.2
  - Supports PPDREQ# and PPDGNT#
  - Provides software transparent capability

- **Distributed DMA Controller**
  - Comply with Distributed DMA R6.0
  - Supports 7 DDMA channels
  - Optional DDMA-Concurrent PCI bus

- **ISA Interface**
  - Supports full ISA compatible functions
  - Supports ISA at ¼ of PCI frequency
  - ISA Bus Master supported
  - Supports 4 ISA slots

- **SM Bus**
  - Comply with System Management Bus Specification R. 1.0
  - Supports single master mode
  - Interface to Serial E^2PROM

- **Serial IRQ**
  - Comply with Serialized IRQ Support for PCI system R6.0
  - Supports both continuous and quite modes
  - Auto detect Start Frame width and slot number
  - Encodes all ISA IRQs and IOCHCK#

- **Optional FLASH ROM Interface**
  - Supports up to 1 Mbytes ROM size
  - Positively fast decodes F-segments by power-on strapping

- **Versatile power-on strapping options**
- **Supports NOGO function**
- **Single 33 MHz Clock Input**
- **+3.3V PCI I/F with +5V tolerant I/O buffers**
- **+5V ISA I/F and core Power Supply**
- **Package: 160 TFBGA**

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2. General Description

The IT8888G is a PCI to ISA bridge single function device. The IT8888G serves as a bridge between the PCI bus and ISA bus. The IT8888G's 32-bit PCI bus interface is compliant with PCI Specification V2.1 and supports both PCI Bus Master & Slave. The PCI interface supports both programmable positive and full subtractive decoding schemes.

The IT8888G also integrates two enhanced DMA Slave controllers for achieving PCI DMA cycles: PC/PCI DMA Slave Controller & Distributed DMA Slave Controllers.

The IT8888G also implements the optional fast positive decode of F, E, D, C memory segments. This special feature can provide a direct connection to an FALSH boot ROM.

The NOGO function, which is also implemented in the IT8888G for enabling or disabling subtractive decode of PCI interface, could be a software controlled output pin from other host controlled devices. The Serial IRQ is also implemented in the device for sending and receiving ISA IRQs & IOCHCK#. The device includes an ISA interface which supports full ISA compatible functions.

The IT8888G is available in 160-pin TFBGA package.

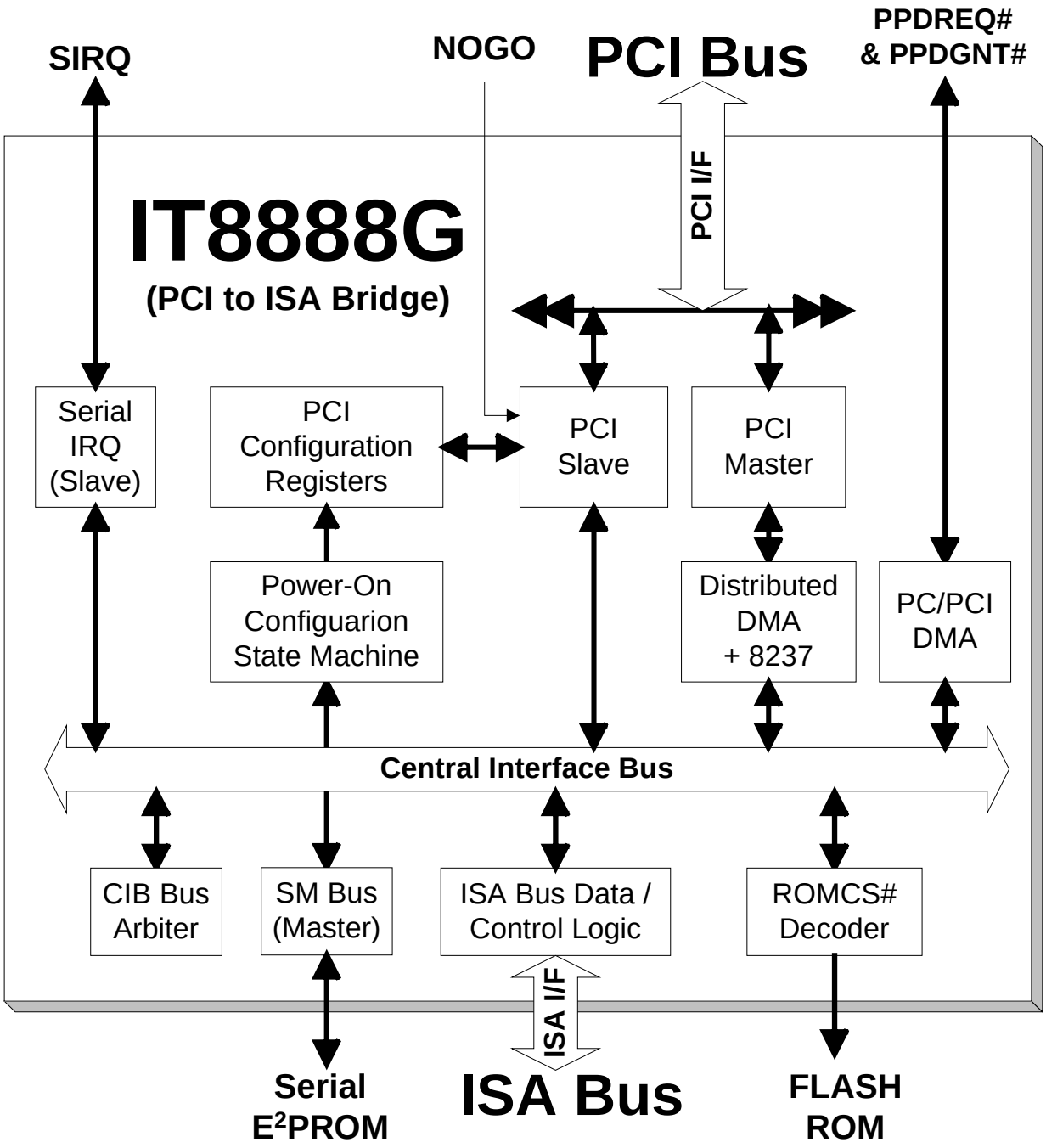
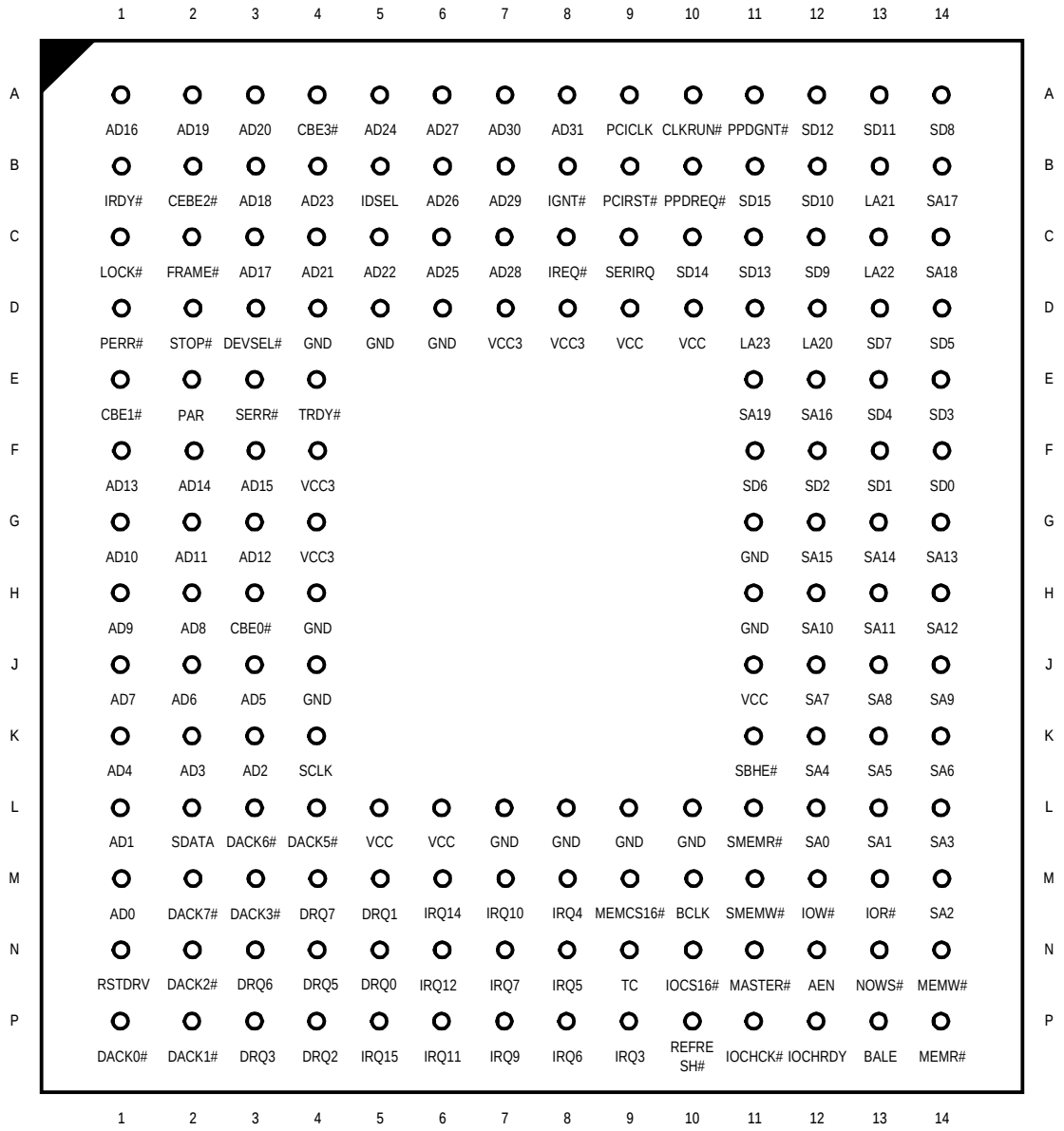


Figure 2-1. IC Block Diagram

3. Pin Configuration

Top View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AD16	AD19	AD20	CBE3#	AD24	AD27	AD30	AD31	PCICLK	CLKRUN#	PPDGNT#	SD12	SD11	SD8
B	IRDY#	CEBE2#	AD18	AD23	IDSEL	AD26	AD29	IGNT#	PCIRST#	PPDREQ#	SD15	SD10	LA21	SA17
C	LOCK#	FRAME#	AD17	AD21	AD22	AD25	AD28	IREQ#	SERIRQ	SD14	SD13	SD9	LA22	SA18
D	PERR#	STOP#	DEVSEL#	GND	GND	GND	VCC3	VCC3	VCC	VCC	LA23	LA20	SD7	SD5
E	CBE1#	PAR	SERR#	TRDY#							SA19	SA16	SD4	SD3
F	AD13	AD14	AD15	VCC3							SD6	SD2	SD1	SD0
G	AD10	AD11	AD12	VCC3							GND	SA15	SA14	SA13
H	AD9	AD8	CBE0#	GND							GND	SA10	SA11	SA12
J	AD7	AD6	AD5	GND							VCC	SA7	SA8	SA9
K	AD4	AD3	AD2	SCLK							SBHE#	SA4	SA5	SA6
L	AD1	SDATA	DACK6#	DACK5#	VCC	VCC	GND	GND	GND	GND	SMEMR#	SA0	SA1	SA3
M	AD0	DACK7#	DACK3#	DRQ7	DRQ1	IRQ14	IRQ10	IRQ4	MEMCS16#	BCLK	SMEMW#	IOW#	IOR#	SA2
N	RSTDRV	DACK2#	DRQ6	DRQ5	DRQ0	IRQ12	IRQ7	IRQ5	TC	IOCS16#	MASTER#	AEN	NOWS#	MEMW#
P	DACK0#	DACK1#	DRQ3	DRQ2	IRQ15	IRQ11	IRQ9	IRQ6	IRQ3	REFRESH#	IOCHCK#	IOCHRDY	BALE	MEMR#

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4. Pin Description

Table 4-1. PCI Bus Interface Signals

Pin #	Signal	I/O	Description	Level
M1,L1,K1~K3, J1~J3,H1,H2, G1~G3,F1~F3, C3~C7,B6,B7, B3,B4,A5~A8, A1~A3	AD[31:0]	I/O	***PCI Multiplexed Address / Data 31 - 0.*** 32-bit bi-directional address/data multiplexed lines. AD31 is the MSB and AD0 is the LSB. The direction of these pins are defined below: *PHASE* / *Bus Master* / *Target* Address Phase / Output / Input Read Data Phase / Input / Output Write Data Phase / Output / Input	3.3V
A4,B2,E1,H3	C/BE[3:0]#	I/O	***Command/Byte Enable 3 - 0 #.*** Multiplexed bus command and byte enables.	3.3V
D3	DEVSEL#	I/O	***Device Select #.*** When driven active low, the signal indicates the driving device has decoded its address as the target of the current access. This pin acts as an output pin when the IT8888G (including ISA slave) is the slave of PCI bus cycle transaction. Otherwise, it is an input pin.	3.3V
E4	TRDY#	I/O	***Target Ready #.*** This signal indicates that the target of the current data phase of the transaction is ready to be completed. This pin acts as an output pin when the IT8888G (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.	3.3V
B1	IRDY#	I/O	***Initiator Ready #.*** This signal indicates that the initiator is ready to complete the current data phase of the transaction. This pin acts as an output pin when the IT8888G is the bus master of the PCI bus. Otherwise, it is an input pin.	3.3V
C2	FRAME#	I/O	***FRAME #.*** This signal is driven by the initiator to indicate the beginning and duration of a PCI access.	3.3V
B5	IDSEL	I	***Initialization Device Select.*** This signal is used as a chip select during PCI Configuration read / write transactions.	3.3V
E2	PAR	I/O	***Parity*** This signal is used for the even parity check on both AD[31:0] & C/BE[3:0]# lines. The PAR input/output direction follows the AD[31:0] input/output direction.	3.3V
D1	PERR#	I/O	***Parity Error #.*** This signal is used for reporting data parity errors during all PCI transactions, except in a Special Cycle. PERR# is an output when it detects a parity error in receiving data as a PCI Target or in reading data as a PCI Master.	3.3V
E3	SERR#	I/OD	***System Error #.*** This signal is used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. (input for IC test only)	3.3V
C1	LOCK#	I	***Lock #.*** This signal indicates a Lock Cycle for an atomic operation that may require multiple transactions to complete.	3.3V
D2	STOP#	I/O	***Stop #.*** This signal indicates that the current target is requesting the initiator to stop the current transaction. This pin acts as an output pin when the IT8888G (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.	3.3V
C8	IREQ#	I/O	***PCI Bus Request #.*** This signal is asserted to request the host bridge to allow the IT8888G to become the PCI bus master. (DDMA)	3.3V

Pin #	Signal	I/O	Description	Level
			(input for IC test only)	
B8	**IGNT#**	I	***PCI Bus Grant #.*** This signal is asserted from the host bridge allowing the IT8888G to become the PCI bus master. (DDMA)	3.3V
B10	**PPDREQ#**	I/O	***PC/PCI DMA (PPDMA) Request #.*** This signal is used to encode the ISA DMA request information to the host bridge for PPDMA function. (input for IC test only)	3.3V
A11	**PPDGNT#**	I	***PC/PCI DMA (PPDMA) Grant #.*** This signal is asserted from the host bridge to send DACKn# information to IT8888G for PPDMA function.	3.3V
A9	**PCICLK**	I	***33 MHz PCI Clock.***	3.3V
B9	**PCIRST#**	I	***PCI Bus Reset #.*** PCIRST# is used to reset PCI bus devices.	3.3V

Table 4-2. ISA Bus Interface Signals

Pin #	Signal	I/O	Description	Level
B14,C14,E11,E12,G12~G14,H12~H14,J12~J14,K12~K14,L12~L14,M14	**SA[19:0]**	I/O	***ISA Address 19 - 0.*** SA[19:0] are outputs except during the ISA master cycles.	5V
B13,C13,D11,D12,	**LA[23:20]**	I/O	***ISA Latch Address 23 - 20.*** Latchable Address bus LA23 to LA20 are outputs except during the ISA master cycles.	5V
K11	**SBHE#**	I/O, P/U 50K	***System Byte High Enable #.*** This signal indicates that the high byte on the ISA data bus is valid. SBHE# is an output except during the ISA master cycles	5V
A12~A14,B11,B12,C10~C12,D13,D14,E13,E14,F11~F14	**SD[15:0]**	I/O, P/U 50K	***ISA Data 15 - 0.*** 16-bit bi-directional data lines. SD15 is the MSB.	5V
M13	**IOR#**	I/O, P/U 50K	***I/O Read #.*** Active low output asserted by the CPU or DMA controller to read data or status information from the ISA device. Acts as input when ISA master cycles.	5V
M12	**IOW#**	I/O, P/U 50K	***I/O Write #.*** Active low output asserted by the CPU or DMA controller to write data or control information to the ISA device. Acts as an input during ISA master cycles.	5V
N12	**AEN**	I/O, P/U 50K	***Address Enable.*** This signal is used to indicate DMA accesses. This signal is also used as power-on strapping select.	5V
P14	**MEMR#**	I/O, P/U 50K	***Memory Read #.*** This signal is an output signal for all cycles except when the ISA master controls the bus.	5V
N14	**MEMW#**	I/O, P/U 50K	***Memory Write #.*** This signal is an output signal for all cycles except when the ISA master controls the bus.	5V
N10	**IOCS16#**	I, P/U 50K	***16-bit I/O Access #.*** This signal indicates that the bus size of current ISA I/O slave is 16 bits.	5V
M9	**MEMCS16#**	I/O, P/U 50K	***16-bit Memory Access #.*** This signal indicates that the bus size of current ISA memory slave is 16 bits. During DMA/MASTER cycles, MCS16# is asserted low when memory target is on the PCI bus.	5V
N13	**NOWS#**	I, P/U 50K	***No Wait States #.*** This signal is asserted by the ISA slave in order to shorten the ISA cycle. The IT8888G samples NOWS# to escape standard wait states from the PCI when the ISA slaves have completed the transfer.	5V
P12	**IOCHRDY**	I/O, P/U 50K	***I/O Channel Ready.*** IOCHRDY is used by ISA slaves to insert wait states. During the ISA master cycles, IOCHRDY is asserted low by the IT8888G when the slave is on the PCI bus.	5V
N11	**MASTER#**	I, P/U 50K	***16-bit Master #.*** Indicates that a 16-bit ISA master takes control of the ISA bus.	5V
P11	**IOCHCK#**	I, P/U 50K	***I/O Channel Check #.*** ISA bus error indication	5V

Pin #	Signal	I/O	Description	Level
P10	REFRESH#	I/O, P/U 50K	***System Refresh Control #.*** Output to ISA bus when converting system timer ticks into a refresh cycle. Input from ISA master is used to refresh on-board and slot DRAM.	5V
M4,M5,N3~N5, P3,P4	DRQ[7~ 5, 3~0]	I, P/D 50K	***DMA Request 7, 6, 5, 3, 2, 1, 0.*** These active high input signals are used to indicate the DMA service request from DMA devices, or the ISA bus control request from the ISA master.	5V
L3,L4,M2,M3,N2,P1,P2	DACK[7~ 5, 3~0]#	I/O, P/U 50K	***DMA Acknowledge 7, 6, 5, 3, 2, 1, 0 #.*** Active low outputs to acknowledge the corresponding DMA requests. (input for IC test only)	5V
N9	TC	I/O, P/U 50K	***Terminal Count.*** This signal is asserted to indicate the end of a DMA transfer. This signal is also used as power-on strapping select.	5V
P5	IRQ15	I, P/U 50K	***Interrupt Request 15.*** This pin is the parallel interrupt request line 15.	5V
M6	IRQ14/ ROMCS#	I/O, P/U 50K	***Interrupt Request 14 /ROM Chip Select #*** The function selection of this pin is determined by ROM decoding related Configuration register settings. Please refer to section 5.14 Optional FLASH ROM Interface.	5V
M7,M8,N6~N8, P6~P9	IRQ[12~9, 7~3]	I, P/U 50K	***Interrupt Request 12, 11, 10, 9, 7, 6, 5, 4, 3.*** These pins are the parallel interrupt request lines.	5V
N1	RSTDRV	O	***ISA Reset.*** A high level on this output resets the ISA bus. This signal asynchronously terminates any activity and places the ISA device in the reset state.	5V
L11	SMEMR#	I/O, P/U 50K	***System Memory Read #.*** This signal is an output signal for access under 1MB; otherwise, tri-state. (input for IC test only)	5V
M11	SMEMW#	I/O, P/U 50K	***System Memory Write #.*** This signal is an output signal for access under 1MB; otherwise, tri-state. (input for IC test only)	5V
M10	BCLK	O	***Bus Clock*** ISA bus clock equals to ¼ of PCI clock.	5V
P13	BALE	I/O, P/U 50K	***Buffer Address Latch Enable*** ***This signal is also used as power-on strapping select.***	5V

Table 4-3. Miscellaneous Signals

Pin #	Signal	I/O	Description	Level
A10	NOGO/ CLKRUN#	I/O	***NOGO / Clock Run #*** The function selection of this pin is determined by Cfg_54h<20>. When acting as NOGO, it is an input from chipset to disable the subtractive decode of the IT8888G; when acting as CLKRUN#, it is an input/output for the IT8888G to request PCICLK to keep running.	5V
C9	SERIRQ	I/O	***Serial IRQ*** This is Serialized IRQ for encoding parallel IRQ lines to one pin.	5V
L2	SDATA	I/O, P/U 50K	***Serial Bus Data*** System Management Bus data for Serial E^2PROM.	5V
K4	SCLK	I/OD, P/U 50K	***Serial Bus Clock*** System Management Bus clock output for Serial E^2PROM. (input for IC test only)	5V

Table 4-4. Power Signals

Pin #	Signal	I/O	Description	Level
D7,D8,F4,G4,	**VCC3**	PWR	***PCI Interface Power Pins.*** Those are connected to 3.3V power supply.	3.3V
D9,D10,J11,L5, L6	**VCC**	PWR	***ISA Interface and chip core power pins.*** 5V power pins.	5V
D4~D6,G11,H4, H11,J4,L7~L10	**GND**	PWR	***Ground pins***	0 V

Table 4-5. IT8888G Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	AD16	C13	LA22	H1	AD9	M3	DACK3#
A2	AD19	C14	SA18	H2	AD8	M4	DRQ7
A3	AD20	D1	PERR#	H3	CBE0#	M5	DRQ1
A4	CBE3#	D2	STOP#	H4	GND	M6	IRQ14
A5	AD24	D3	DEVSEL#	H11	GND	M7	IRQ10
A6	AD27	D4	GND	H12	SA10	M8	IRQ4
A7	AD30	D5	GND	H13	SA11	M9	MEMCS16#
A8	AD31	D6	GND	H14	SA12	M10	BCLK
A9	PCICLK	D7	VCC3	J1	AD7	M11	SMEMW#
A10	CLKRUN#	D8	VCC3	J2	AD6	M12	IOW#
A11	PPDGNT#	D9	VCC	J3	AD5	M13	IOR#
A12	SD12	D10	VCC	J4	GND	M14	SA2
A13	SD11	D11	LA23	J11	VCC	N1	RSTDRV
A14	SD8	D12	LA20	J12	SA7	N2	DACK2#
B1	IRDY#	D13	SD7	J13	SA8	N3	DRQ6
B2	CBE2#	D14	SD5	J14	SA9	N4	DRQ5
B3	AD18	E1	CBE1#	K1	AD4	N5	DRQ0
B4	AD23	E2	PAR	K2	AD3	N6	IRQ12
B5	IDSEL	E3	SERR#	K3	AD2	N7	IRQ7
B6	AD26	E4	TRDY#	K4	SCLK	N8	IRQ5
B7	AD29	E11	SA19	K11	SBHE#	N9	TC
B8	IGNT#	E12	SA16	K12	SA4	N10	IOCS16#
B9	PCIRST#	E13	SD4	K13	SA5	N11	MASTER#
B10	PPDREQ#	E14	SD3	K14	SA6	N12	AEN
B11	SD15	F1	AD13	L1	AD1	N13	NOWS#
B12	SD10	F2	AD14	L2	SDATA	N14	MEMW#
B13	LA21	F3	AD15	L3	DACK6#	P1	DACK0#
B14	SA17	F4	VCC3	L4	DACK5#	P2	DACK1#
C1	LOCK#	F11	SD6	L5	VCC	P3	DRQ3
C2	FRAME#	F12	SD2	L6	VCC	P4	DRQ2
C3	AD17	F13	SD1	L7	GND	P5	IRQ15
C4	AD21	F14	SD0	L8	GND	P6	IRQ11
C5	AD22	G1	AD10	L9	GND	P7	IRQ9
C6	AD25	G2	AD11	L10	GND	P8	IRQ6
C7	AD28	G3	AD12	L11	SMEMR#	P9	IRQ3
C8	IREQ#	G4	VCC3	L12	SA0	P10	REFRESH#
C9	SERIRQ	G11	GND	L13	SA1	P11	IOCHCK#
C10	SD14	G12	SA15	L14	SA3	P12	IOCHRDY
C11	SD13	G13	SA14	M1	AD0	P13	BALE
C12	SD9	G14	SA13	M2	DACK7#	P14	MEMR#

Table 4-6. Power-On-Strap Settings

Signal	Pin #	Jumper	Description
AEN	**N12**	(P/Up)	Reserved for enabling chip test function when PCIRST#=0
		P/Down	IT8888G Normal Function
BALE	**P13**	(P/Up)	Fast DEVSEL# timing for F-segment BIOS (both 000FXXXXh and FFFFXXXXh). It will set Cfg_50h<3>
		P/Down	No response or Subtractive Decode for F-segment access
TC	**N9**	(P/Up)	Enable SM-bus Boot ROM Configuration. It will set Cfg_50h<4>, but will be auto-cleared when finishing download configure code.
		P/Down	Disable SM-bus Boot ROM Configuration

5. Functional Description

The IT8888G provides full ISA interface to hook up on PCI bus, so that the existing legacy ISA devices could be supported in new generation PC chipset architecture without ISA interface.
There are some sub-function blocks in the IT8888G as described below:

5.1 PCI Slave Interface

The IT8888G PCI Slave interface provides some positively decode space:

- IT8888G PCI configuration register spaces – positively decode w/ medium DEVSEL# speed on the Type0 PCI configuration cycle, the access space is described in 6.2 Access Configuration Registers on page 6-2.
- Six I/O positively decode spaces – defined in IT8888G Configuration Registers: Cfg_58h ~ Cfg_6Fh.
- Four Memory positively decode spaces – defined in IT8888G Configuration Registers: Cfg_70h ~ Cfg_7Fh.
- Optional I/O Port 80 Write Snooping.
- Optional F-segment BIOS claim w/ Fast DEVSEL# speed.
- ISA Palette decoding (ref: Cfg_50h<7:6>).
- DDMA registers spaces.
- PC/PCI DMA cycle space: I/O addresses of 0000h / 0004h / 00C0h / 00C4h.

The IT8888G supports PCI 2.1 Delayed Transaction feature which can be enabled / disabled by programming Cfg_50h<1>. The benefit of Delayed Transaction is that the PCI bus is still available and can be used by other PCI master, even when there is an ISA PIO cycle in progress behind IT8888G.
When Delayed Transaction is enabled, the IT8888G will retry the PCI-to-ISA cycle claimed by IT8888G and latch those address / command / byte-combination, and issues ISA cycle. When the ISA site is not finished, the PCI Slave interface of IT8888G will still retry any PCI cycle. Once the ISA cycle is finished, the PCI Slave interface will wait the same PCI cycle (same address / command / Byte-enable) and terminate it normally with TRDY# asserted. But before that, the other PCI cycle with different address or command or Byte-enable still will be retried.
If the original PCI bus masters after retried never issue the same cycle within the programmed DISCARD Timer, the IT8888G will discard that ISA transaction, so that the IT8888G is able to respond to other PCI transactions without locking its ISA bus interface. Please refer to the Cfg_54h<15:8> in 6.3.11, the Retry/Discard Timers of the Misc. Control Register on page 6-16 for the setting of Discard Timer. There is an option to report System Error via asserting SERR#.
The IT8888G also supports Exclusive access via LOCK# control. Please refer to PCI Specification Revision 2.1, for more detailed description.

5.2 PCI Master Interface

The IT8888G will issue PCI cycle for ISA bus master cycle and DDMA memory cycle if those accesses are forwarded to PCI bus. The Cfg_50h<23:12> define the decoding spaces for IT8888G to decide forwarding the access of ISA bus master or DDMA controller to PCI bus or not.
When the accessed space is forwarding to PCI bus, the IT8888G will assert IREQ# to PCI bus arbiter if the DACKn# source is DDMA. Once the IGNT# is asserted by PCI arbiter and the PCI bus is in idle state, the PCI Master I/F of IT8888G will issue non-burst PCI Memory Read/Write cycles or PCI I/O Read/Write cycles (if Cfg_50h<23>=1). In the mean time, the IOCHRDY will be de-asserted to insert wait-state until forwarding cycle is finished on PCI site.
When in PC/PCI DMA (PPDMA) cycle, the DACKn# is decoded from PPDGNT#, and the IT8888G will not issue IREQ#. As long as the PPDGNT# and MASTER# signal are asserted and there exist an ISA command issued by ISA master, then the PCI Master I/F of IT8888G will issue a PCI cycle for ISA master if the accessed space is located on PCI bus.
Whenever the PCI Master I/F of IT8888G is retried, it will release PCI bus ownership and re-arbiter and re-issue the same transaction. But if the same retry occurs too many times and exceeds the Retry Timer limitation, then the PCI Master I/F will stop trying and there is an option to report System Error via asserting SERR#. Please refer to Cfg_54h<7:0> in 6.3.11 Retry/Discard Timers, Misc. Control Register

on page 6-16 for more detailed Retry Timer setting.

5.3 PCI Parity

The IT8888G, like other standard PCI devices, can handle parity error and other errors. Whenever the IT8888G detects address parity error, it is able to assert SERR# if the SERR# reporting mechanism is enabled in PCI Command/Status register.
Also when IT8888G acts as a PCI slave, it will check the data parity of writing in data; when IT8888G acts as a PCI master, it will check the data parity of reading back data. Once it detects a data parity error, it can report data parity error and assert PERR# if the PERR# reporting mechanism is enabled in PCI Command/Status register.

5.4 Positively Decode Spaces

The six positively decode I/O spaces can be programmed to claim PCI I/O cycle with Fast / Medium / Slow / Subtractive DEVSEL# timing speed. In addition, the ISA I/O aliases can be set to support legacy ISA card with non-fully decoded (only decodes with XA9~0). In other words, when alias is enabled for one I/O space, then the addresses A15~A10 of the PCI access address will be ignored for the enabled I/O space. All I/O spaces are limited under 64KB I/O size. IT8888G only claims I/O access with PCI address A[31:16]=0000h. When programmed to subtractive decoding speed, IT8888G will claim PCI I/O access only when whole chip Subtractive decode function is enabled (Cfg_50h<0>).
The four positively decode Memory spaces can also be programmed to claim PCI Memory cycle with Fast / Medium / Slow / Subtractive DEVSEL# timing speed. The memory space is not limited, i.e., even above ISA 16MB size, if it is fall into IT8888G Memory positive decoding spaces, then it will be forwarded to ISA bus with address A31~A24 ignored. So users must carefully claim memory spaces, since the mechanism can support memory relocation. When programmed to subtractive decoding speed, IT8888G will claim PCI Memory access only when whole chip Subtractive decode function is enabled (Cfg_50h<0>), but the claimed space is restricted under memory space base/size setting, not limited to 16MB size.

5.5 Subtractive Decode

IT8888G supports subtractive decode. In general, the subtractive decode mechanism of PCI-to-PCI Bridge chip is to respond to all non-claimed space. But for IT8888G, avoiding ISA space wrapped, it only responses to the memory space under 16MB size (ISA only has 24-bit addressing ability) when processing subtractive decode, except when the access space is hit to one of four positively decode memory space with slowest DEVSEL# timing speed. And the IT8888G only responds to unclaimed PCI I/O space under 64KB.

5.6 PC/PCI DMA (PPDMA) Slave Controller

The IT8888G, following the " Mobile PC/PCI DMA Arbitration and Protocols MHPG Architecture Functional Architectures Specification" by Intel Corporation, Revision 2.2, builds a PC/PCI DMA (PPDMA) Slave which supports all 7 ISA DMA channels through a single PPDREQ# / PPDGNT# pair. It provides a very low cost, low pin count mechanism. Please check the waveform for more details.
This protocol works as the followings: the IT8888G encodes the DMA channel request information on the PPDREQ# line and decodes the PPDGNT#, which is output from PPDMA Host (in chipset), to assert the DACKn# of the granted DMA channel to ISA bus.
The PPDMA protocol supports Single DMA, Demand DMA, but not Block DMA, nor software request DMA transfers.
For PPDMA transfer, the PPDMA Host will separate Memory transaction portion from DMA operation, and issues PCI I/O transaction to PPDMA Slave with PPDGNT# asserted and special address listed below:

PCI I/O Address	R/W	IT8888G Operation
00h	R/W	Normal DMA operation without TC

PCI I/O Address	R/W	IT8888G Operation
04h	R/W	Normal DMA operation with TC
C0h	R	DMA Verify operation without TC
C4h	R	DMA Verify operation with TC

The IT8888G PPDMA slave controller can handle the PCI Retry while it was granted the bus, it continues to hold DACKn# active to ISA bus even when the PPDGNT# is removed. Also when the PCI Master I/F of IT8888G issues cycle for ISA Master and is retried, PPDMA slave would re-send the PPDREQ# to advise PPDMA Host to process Passive Release.

5.7 Distributed DMA (DDMA) Slave Controller

The IT8888G integrates two DMA controllers (8237) to build a 7-channel DDMA salve for DDMA function, which comply with Distributed DMA Specification R6.0.
There are seven DMA channels in IT8888G. Each channel maps to different ISA DMA channel, i.e. DMA channel 7~5, 3~0. Each channel can be treated as a separate DDMA salve, which has its own DDMA channel base address and can be enabled / disabled separately.
To achieve compatibility with ISA, the DDMA channel 7~5 are fixed at 16-bit transfer width; the DDMA channel 3~0 are fixed at 8-bit transfer width. Each channel supports 24 or 32 bits addressing. That is to say, with IT8888G, the system OS or drivers can perform DMA operation to/from anywhere in 4GB-memory space, and is free from the limit of ISA 16MB memory space. When not using the high page register, the system OS or drivers either write 00h or disable high page for dedicated channel.
In PC system, the DDMA Host is located in chipset, and it converts the address and data of legacy DMA accesses (including transferring base address, word counter register, mode / command / mask /… registers in I/O port 00h~1Fh, C0h~DFh and page registers in I/O port 8Xh~9Xh). This enables the IT8888G will receive PCI I/O cycles with the address = programming register offset plus pre-configured Base Address of dedicated DDMA slave channel. Please refer to 6.4 DDMA Slave Registers Description on page 6-25 for DDMA Slave Register mapping. For detailed register descriptions of legacy DMA controller, there are numerous manufactures' data books that describe the functionality.

5.8 Type-F DMA Timing

The IT8888G also supports Type F DMA timing. Each DMA channel can be programmed to operate in normal DMA timing or Type-F timing. For normal timing, the DDMA controller issuing I/O and Memory commands or the PPDMA module issuing the DMA I/O command meet the DMA operating timing defined in ISA Specification (IEEE P996 draft). Since the system memory bus is located behind ISA bus in legacy IBM PC/AT architecture, the timing is very loose (slow). But for current PC architecture, the system memory is located on Host bridge chip (or PCI North Bridge), thus DMA cycles can be operated faster to achieve better ISA DMA performance.

5.9 ISA Bus I/O Recovery Time

The recovery time of back to back ISA I/O cycles is 1.5 BCLK (ISA System bus clock). The IT8888G provides different I/O recovery time setting for 8-bit I/O cycles and 16-bit I/O cycles.
The configured 8-bit I/O recovery time is inserted after ISA I/F finishes the 8-bit I/O cycle, and the configured 16-bit I/O recovery time is inserted after ISA I/F finishes the 16-bit I/O cycle. No additional recovery time will be inserted due to byte conversion (PCI I/O cycle could be 8/16/24/32 bits, but ISA I/O is only 8/16 bits).

5.10 ISA Bus Arbiter

The IT8888G internal ISA arbiter will handle and exclude DDMA cycle, Refresh cycle and PIO cycle from PCI bus to optimize the ISA bus utilization.
To achieve PCI/ISA concurrency, there are some technologies to improve system performance: Delayed Transaction, Passive Release and the "DDMA-Concurrent" in the IT8888G design.
In legacy PC architecture, the CPU and PCI bus are held throughout the whole DMA operation even

when the DMA access space is onto ISA bus or when the forwarded PCI transaction requires just a few PCI clocks to complete. IT8888G provides one option: DDMA-Concurrent cycle when DDMA operation (Cfg_54h<31>). When enabled, the IT8888G will request PCI bus only when DDMA controller or ISA master issued a transaction to be forwarded to PCI bus, and the IT8888G will release PCI bus after it finished PCI bus cycle, even when the DDMA / ISA master still occupies ISA bus.
This is achieved by ISA arbiter, whenever DDMA occupy ISA bus, the PCI Slave will retry all PCI cycles belonging to IT8888G, so that the PCI bus can be used by other PCI transactions.
The ISA Bus Refresh timer requests ISA memory REFRESH operation every 15.36μs which is divided from PCI clocks by 512. The refresh module could be disabled by clearing Cfg_54h<26>.

5.11 SMB Boot ROM Configuration

In addition that the IT8888G configuration can be done by PCI Configuration cycles through system chipset, the IT8888G also offers an optional configuration method via the System Management Bus (SMB, similar to I^2C BUS) Boot ROM. As the current version of IT8888G only supports single master mode, users are prohibited to connect the IT8888G SMB interface to other system SMB bus. Only Serial E^2PROM can be connected, and the preset slave address is 1010000b.
The Serial E^2PROM Data is grouped by each five bytes into the 1^{st} byte, which serves as an index to indicate which PCI Configuration register is. The other 4 bytes are the 32-bits data will be written to the indexed register.

SMB ROM Data format in Serial E^2PROM is illustrated below:

ROM Address	ROM Data	IT8888G Operation
top		
5n	Index = AAh	Stop
5m+4	Data	Cfg_50h<31:24>
5m+3	Data	Cfg_50h<23:16>
5m+2	Data	Cfg_50h<15:8>
5m+1	Data	Cfg_50h<7:0>
5m	Index = 50h	Cfg_50h
6	Data	Cfg_XXh<7:0>
5	Index = XXh	Cfg_XXh
4	Data	Cfg_??h<31:24>
3	Data	Cfg_??h<23:16>
2	Data	Cfg_??h<15:8>
1	Data	Cfg_??h<7:0>
0	Index = ??h	Cfg_??h

Whether the chip will execute SMB Boot ROM Configuring Sequence or not is determined by one power-on-strap setting. Please refer to the Table 4-6 Power-On-Strap Settings on page 4-8. If SMB boot ROM Configuration is enabled, the IT8888G will then set the SMB_In_Progress status bit (Cfg_50h<4>) on page 6-12 and begin to issue the I^2C Sequential Read Operation. It writes to PCI Configuration Registers after it has finished reading every five bytes from SM ROM. If it reads an Index value as AA_{hex}, then it will stop I^2C Sequential Read Operation and clear the SMB_In_Progress status bit. The system BIOS can monitor the status bit to see if SMB is in progress before BIOS can decide to enable some computer system sub-functions.

Conversely, if SMB boot ROM Configuration is disabled in power-on-strap setting, the IT8888G will then clear the SMB_In_Progress status bit, and no I^2C Sequential Read Operation occurs.

For instance, if users intend to claim a Memory space of $00F3XXXX_h$ (64KB size) and one I/O space of $02AC_h$ ~ $02AD_h$ (2byte size) for a special ISA card (or users try to hook up the ISA device to PCI bus), a Serial E^2PROM can be programmed. The resulted data are listed on the next page:

Serial E^{2}PROM Address	Serial E^{2}PROM Data	IT8888G Configuration Register
top ~ B	XX_h	
A	**AA_h**	IT8888G SMB I/F Stop
9	$C1_h$	Cfg_64h<31:24> Medium DEVSEL#, 2Byte size
8	00_h	Cfg_64h<23:16> = reserved
7	02_h	Cfg_64h<15:0> = $02AC_h$
6	AC_h	
5	64_h	Index 64_h => Cfg_64h
4	$A2_h$	Cfg_7Ch<31:24> Slow Medium, 64KB size
3	00_h	Cfg_7Ch<23:0> = $00F3XXXX_h$
2	$F3_h$	
1	00_h	
0	$7C_h$	Index $7C_h$ => Cfg_7Ch

In the example above, the IT8888G SMB Configuration block will write the 32-bit data of $A200F300_h$ to Cfg_7Ch when it finishes reading byte 0~4 of Serial E^{2}PROM. It will also write the 32-bit data of $C10002AC_h$ to Cfg_64h when it finishes reading byte 5~9 of Serial E^{2}PROM. After it receives an AA_h in the ROM position of 5xN (i.e. address of 5_d, 10_d, 15_d, .. etc.), the SMB I/F stops fetching more data and clear the SMB_In_Progress status bit.

For detailed SMB Configuration operation, please refer to the "IT8888G SMB Configuration Programming Guide".

The SMB Boot Configuring mechanism is patent pending.

5.12 Serialized IRQ

The IT8888G builds a Serialized IRQ slave which complies with Serialized IRQ Support for PCI system R6.0.
The Serialized IRQ slave provides signal filtering and encoding logic for all ISA IRQ channels (IRQ [15:14, 12:9, 7:3] and IOCHCK#), which also supports both continuous and quite mode, and auto detect Start Frame width and slot number.

5.13 NOGO and CLKRUN#

The IT8888G also supports NOGO function, which is MUX-ed with the CLKRUN# signal (selected by Cfg_54h<20>).
The NOGO is an input and controlled by chipset to disable the subtractive decode mechanism of the IT8888G, since there is only one subtractive decode device present on PCI bus. For short term, system manufacturers may use GPIO of chipset to control the NOGO pin of the IT8888G to boot up system, but the IT8888G also provides a mechanism to turn on/off the subtractive decode. And it will not be affected by DMA operation, nor by Delayed transaction.
The IT8888G supports CLKRUN# function to reduce system power consumption when no PCI activity in progress. The CLKRUN# function follows the protocol defined in PCI Mobile Design Guide, Revision 1.0. But since the ISA system clock is divided from PCICLK, if some ISA cards still need ISA bus clock all the time, then the user should leave the Cfg_54<27> stay on default value of one. Thus the IT8888G will monitor system CLKRUN# signal and keep PCICLK running; otherwise, the IT8888G will only claim CLKRUN# when ISA Master / DMA requests service or for the DMA service duration, or when the Serialized IRQ module detects the status change on any ISA interrupt requests.

5.14 Optional FLASH ROM Interface

The IT8888G provides ROM decoding and write protect. The ROM chip select can be decoded by programming versatile Cfg_50h<31:24> settings through segments C to F under 1MB and the top 1MB of 4GB. The ROM decoding logic provides ROMCS# signal (which is shared with IRQ14 signal, selected by the internal logic, i.e., when the ROM decoding related Configuration register settings are enabled, the pin 54 will be ROMCS# output automatically; otherwise, it will be IRQ14 input). The PCI Slave I/F needs to claim PCI memory space either by configuring four positively decoding spaces or by setting IT8888G in the subtractive decode mode, except in the power-on-strap settings: F-segment setting (BALE).
If F-segment is set as positively decode, the IT8888G will only do fast DEVSEL# decoding speed and ROMCS# is generated automatically. Its space is F-segment of both 1MB top and 4GB top. Once the ROM is not on ISA interface, the IT8888G will disable F-segment fast decoding itself.

5.15 Testability

The IT8888G provides several test modes, which are aimed for chip testing, not for system testing.

Test Mode	PCIRST#	AEN	DRQ1	DRQ0
Normal Operation	1	X	X	X
	0	0	X	X
	0	1	0	0
Tri-State Test	0	1	0	1
NAND Chain Test	0	1	1	0
Reserved	0	1	1	1

Tri-State Test:
This test mode tri-states all outputs and bi-directional buffers, including the NAND chain outputs, BCLK and RSTDRV.

NAND Chain Test:
The IT8888G builds the NAND Chain test mode. This test mode tri-states all outputs and bi-directional buffers, except for BCLK and RSTDRV, and all the other output buffers are configured as inputs in NAND Chain test mode and are included in the NAND chain. The first input of the NAND chain is DACK2#. The NAND chain is routed counter-clockwise around the chip (e.g., DACK2#, DACK1#, DACK0#, DREQ7,…). The BCLK is an intermediate output, and the RSTDRV is the final output. PCIRST#, AEN, DRQ1, DRQ0, BCLK and RSTDRV pins are not included in the NAND chain. This testing method can be used to verify chip package connectivity, V_{IH}/V_{IL} DC characteristics.

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6. Register Description

6.1 Configuration Register Map

The IT8888GF PCI header configuration register set complies with Type 00h Configuration Space Header described in the PCI Specification R. 2.1.

Table 6-1. IT8888G Configuration Register Map

31 16	15 00	Index
Device ID (8888h)	Vendor ID (1283h)	00h
Status	Command	04h
Base Class Code (06h) / Sub-class code(01/80h)	Programming I/F (00h) / Revision ID (01h)	08h
Reserved (00h) / Header Type (00h)	Latency Timer (00h) / Cache Line Size (00h)	0Ch
Reserved		10h~2Bh
Subsystem Device ID (0000h)	Subsystem Vendor ID (0000h)	2Ch
Reserved		30~3Fh
DDMA Slave Channel_1 Register	DDMA Slave Channel_0 Register	40h
DDMA Slave Channel_3 Register	DDMA Slave Channel_2 Register	44h
DDMA Slave Channel_5 Register	DMA Type F Timing / PC/PCI DMA Control	48h
DDMA Slave Channel_7 Register	DDMA Slave Channel_6 Register	4Ch
ROMCS# / Master/DMA access	MTOP, I/O Recovery / Timing Control	50h
Misc. Control / Reserved	Discard Timer / Retry Timer	54h
Positively Decoded I/O_Space_0		58h
Positively Decoded I/O_Space_1		5Ch
Positively Decoded I/O_Space_2		60h
Positively Decoded I/O_Space_3		64h
Positively Decoded I/O_Space_4		68h
Positively Decoded I/O_Space_5		6Ch
Positively Decoded Memory_Space_0		70h
Positively Decoded Memory_Space_1		74h
Positively Decoded Memory_Space_2		78h
Positively Decoded Memory_Space_3		7Ch
Reserved		80h~FFh

6.2 Access Configuration Registers

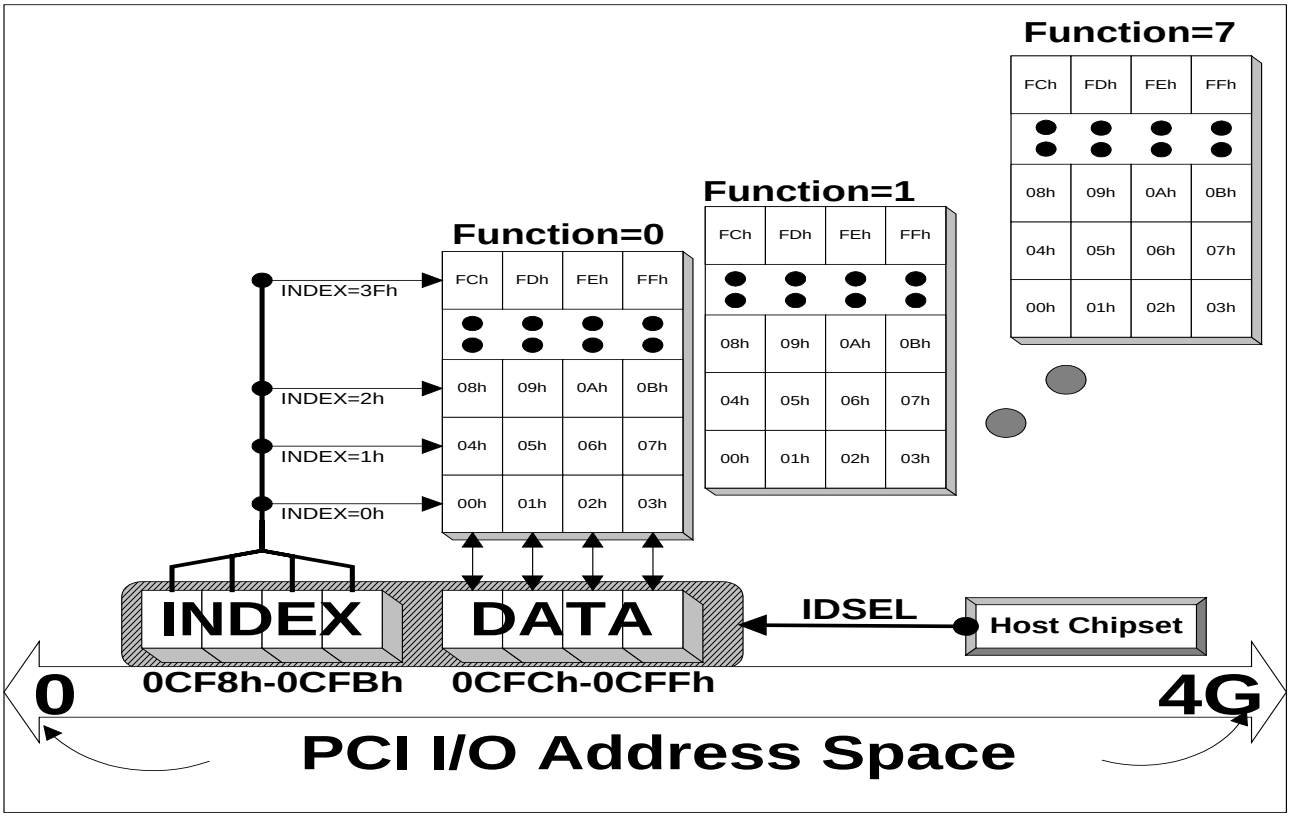
The IT8888G will respond to all PCI Bus Configuration cycles when the IDSEL input is asserted high. Address bits 1-0 of the Configuration cycle are both zeros and address bits 10-8 correspond to internal functions.
The Type0 configuration address format is as follows:

AD31-11	AD10-8	AD7-2	AD1-0	C/BE3-0#
Only one asserted to active IDSEL	Function Select, IT8888G only respond to Function = 000b	Register Select, to select one double-word register	Configuration Type, IT8888G only response to Type = 00b	Byte Select, to select one or more byte in selected double-word register

The configuration registers can be accessed as byte, word (16 bits) or Double-Word (32 bits) quantities or any byte combination. In all of these accesses, only byte enables are used, AD[1:0] is always 00b when accessing the configuration registers. All multi-byte fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the fields). Registers that are marked "**Reserved**" will be decoded and return zeros when read. All bits defined as "**Reserved**" within IT8888G's PCI Configuration Registers will be read as zero and will be unaffected by writes, unless specifically documented otherwise.
The software can use the PCI Configuration Mechanism One to read or write the IT8888G PCI configuration register space. The PCI Configuration Mechanism One utilizes two 32-bit I/O ports located at addresses 0CF8h and 0CFCh. These two ports are:

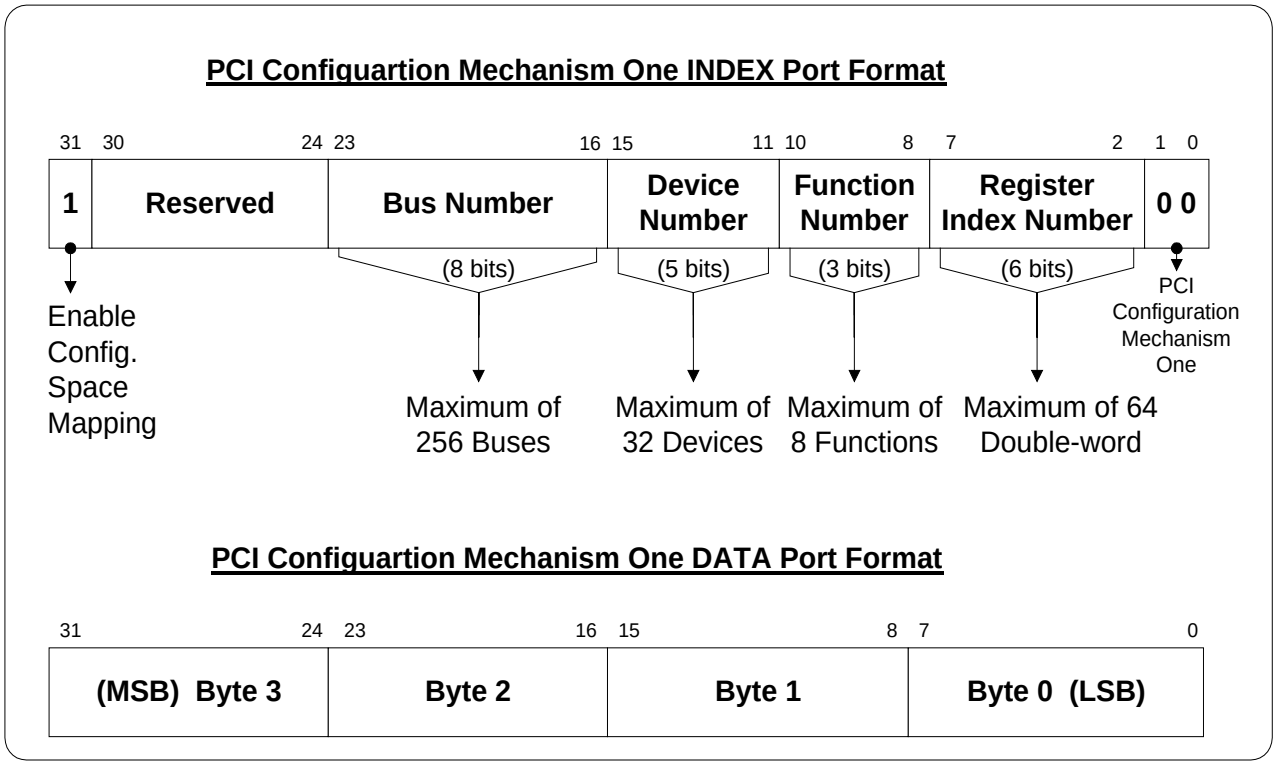
1. **INDEX Port:** 32-bit wide, occupying I/O address 0CF8h through 0CFBh.
2. **DATA Port:** 32-bit wide, occupying I/O address 0CFCh through 0CFFh.

Figure 6-1. PCI Configuration Register Structure



Accessing any PCI configuration register is a two-step process:
Step 1: Perform I/O writes of the bus number, physical device number, function number, and register index number to the PCI Configuration Mechanism One INDEX Port. (The motherboard chipset will decode the bus number, device number and then generate the IDSEL signal to select the device. The device then decodes the function number to select which bank of register to be accessed and decodes the register index number to select which double-word register will be accessed.)
Step 2: Perform an I/O read from or write to the PCI Configuration Mechanism One DATA Port. The PCI Configuration Mechanism One INDEX & Data Port format is illustrated below:

Figure 6-2. PCI Configuration Access Mechanism #1



6.3 Configuration Registers Description

Below is the register description format:

Index Value		Register Function	
register bits	r/w attribute	Register bits description	Default value

6.3.1 Device/Vendor ID Register

- **Vendor Identification (VID) Register**

  Address Offset: 00h - 01h Default Value: 1283h
  Access: Read-only Size: 16 bits
  The Vendor ID Register contains the vendor identification number for ITE. This 16-bit register combined with the Device ID Register uniquely identifies any PCI device. Writes to this register have no effect.

Cfg_00h		Device/Vendor ID Register	
<15:0>	RO	Vendor ID	1283h

- **Device Identification (DID) Register**

  Address Offset: 02h - 03h Default Value: 8888h
  Access: Read-only Size: 16 bits
  The Device ID Register contains the device identification number for IT8888G. This 16-bit register along with the Vendor ID Register uniquely identifies any PCI device. Writes to this register have no effect.

Cfg_00h		Device/Vendor ID Register	
<31:16>	RO	Device ID	8888h

6.3.2 Status / Command Register

- **Command (CMD) Register**

  Address Offset: 04h - 05h Default Value: 0007h
  Access: Read/Write Size: 16 bits
  The Command register provides coarse control over the IT8888G's ability to generate and respond to PCI cycles.

Cfg_04h		Status / Command Register	
<15:10>	RO	Reserved	all zero
<9>	RO	Fast back-to-back control. IT8888G will not perform FBTB access to the target on PCI bus.	0b
<8>	R/W	SERR# drives low enable. A value of 1 enables IT8888G to drive SERR#. A value of 0 disables SERR# signal.	0b
<7>	RO	AD bus stepping. IT8888G does not perform AD stepping.	0b
<6>	R/W	Parity error response. When the bit is 0, IT8888G will ignore any parity error, which is detected on PCI bus interface.	0b
<5:3>	RO	Reserved	000b
<2>	RO	Enable IT8888G to act as a master on primary interface.	1b
<1>	RO	Downstream memory transaction enabling.	1b
<0>	RO	Downstream I/O transaction enabling.	1b

- **Status (STS) Register**

  Address Offset: 06h - 07h Default Value: 0280h
  Access: Read Only, Write-1-to-Clear, SMB Load Size: 16 bits
  The status register is used to record status information for PCI bus related events. Reads to this register behave normally. Some bits with access attribute of W1C (Write-1-to Clear) means when writes to this register with a '1' to the corresponding bit location cause that bit to be reset.

Cfg_04h		Status / Command Register	
<31>	R/W1C	Set by IT8888G whenever it detects a parity error on PCI bus.	0b
<30>	R/W1C	Set by IT8888G whenever it asserts SERR#.	0b
<29>	R/W1C	Set by IT8888G whenever it, as a PCI bus master, terminates a transaction by signaling a Master Abort.	0b
<28>	R/W1C	Set by IT8888G whenever it, as a master, terminates a transaction by receiving a Target Abort.	0b
<27>	R/W1C	Set by IT8888G whenever it, as a target, terminates a transaction by signaling a Target Abort.	0b
<26:25>	R/L	Medium DEVSEL# timing for IT8888G as a target to respond to an access on PCI bus.	01b
<24>	R/W1C	Set by IT8888G when three conditions are met: 1) asserting PERR# itself or observing PERR# being asserted; 2) IT8888G acts as a bus master for the operation in which an error occurs; 3) Cfg_04h<6> is set.	0b
<23>	RO	Fast back-to-back capability (when IT8888G acts as a target).	1b
<22:16>	RO	Reserved	all zero

6.3.3 Class Code/ Revision ID Register

- **Revision Identification (RID) Register**

  Address Offset: 08h Default Value: 01h
  Access: Read Only Size: 8bits
  The Revision ID Register contains the device revision number for IT8888G device. These bits are read-only. Writing to this register has no effect.

- **Programming Interface (PIF) Register**

  Address Offset: 09h Default Value: 00h
  Access: Read Only Size: 8bits
  The Programming interface byte of the Class Code register indicates whether the device supports legacy and/or native mode like IDE interface.

- **Sub-Class Code (SCC) Register**

  Address Offset: 0Ah Default Value: 01h/80h
  Access: Read Only Size: 8bits
  This Register contains the sub-class code for IT8888G. This Sub-Class code is 01h, indicating it is an “ISA Bridge”. These bits are read-only and writes to this register have no effect.

- **Base Class Code (BCC) Register**

  Address Offset: 0Bh Default Value: 06h
  Access: Read Only Size: 8bits
  This Register contains the Base Class Code for IT8888G. This Base Class code is 06h, indicating it is a “Bridge Devices”. These bits are read-only and writes to this register have no effect.

Cfg_08h		Class Code/ Revision ID Register	
<31:24>	RO	Base-Class Code	06h
<23:16>	RO	Sub-Class Code. The default RO value depends on the value of Cfg_50h<0>. I.e. if Cfg_50h<0> is one (Subtractive Decode), then the Cfg_08h<23:16> is RO as 01h (as ISA bridge); otherwise, RO as 80h (as Other bridge device). The default value of Cfg_50h<0> is 0b.	80h (or 01h)
<15:8>	RO	Programming Interface	00h
<7:0>	RO	Revision ID	00h

6.3.4 Header Type/ Primary MLT/ Cache Line Size Register

- **Cache Line Size (CLS) Register**

  Address Offset: 0Ch Default Value: 00h
  Access: Read-only Size: 8bits
  This register specifies the system cache-line size in the unit of 32-bit words.

- **Master Latency Timer (MLT) Register**

  Address Offset: 0Dh Default Value: 00h
  Access: Read-only Size: 8bits
  This register specifies, in the unit of PCI bus clocks, the value of the 8 most significant bits among the 11-bit Latency Timer for this device when the internal DMA controller is used and the device is a bus master.

- **Header Type (HTR) Register**

  Address Offset: 0Eh Default Value: 00h
  Access: Read-only Size: 8bits
  This register identifies the header layout of the configuration space. These bits are read-only and writes to this register have no effect.

Cfg_0Ch		Header Type/ Primary MLT/ Cache Line Size Register	
<31:0>	RO	Reserved	00000000h

6.3.5 Subsystem Device/Vendor ID Register

- **Subsystem Vendor Identification (SVID) Register**

  Address Offset: 2Ch – 2Dh Default Value: 0000h
  Access: Read-only Size: 16bits
  This value is used to identify the vendor of the subsystem. Subsystem Vendor Ids can be obtained from the PCI-SIG and are used to identify the vendor of the add-in board or subsystem.

- **Subsystem Device Identification (SDID) Register**

  Address Offset: 2Eh – 2Fh Default Value: 0000h
  Access: Read-only Size: 16bits
  This value is used to identify a particular subsystem. This register along with SVID register is used to uniquely identify the add-in board or subsystem where the PCI device resides.

Cfg_2Ch		Subsystem Device/Vendor ID Register	
<31:16>	R/L	Subsystem Device ID	0000h
<15:0>	R/L	Subsystem Vendor ID	0000h

6.3.6 DDMA Slave Channel_1 Register / DDMA Slave Channel_0 Register

- **DDMA Slave Channel 0 Register**

  Address Offset: 40h – 41h Default Value: 0000h
  Access: Read/Write, Read-only Size: 16bits
  This register is used for DDMA Channel 0 base address assignment, data width status and enable control.

Cfg_40h		DDMA Slave Channel_1 Register / DDMA Slave Channel_0 Register	
<15:4>	R/W	DDMA Slave Channel_0 Base Address A[15:4]	000h
<3>	R/W	DDMA Slave Channel_0 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_0 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<2:1>	RO	DDMA Slave Channel_0 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	00b
<0>	R/W	DDMA Slave Channel_0 Enable. 0=Disabled, 1=Enabled.	0b

- **DDMA Slave Channel 1 Register**

  Address Offset: 42h – 43h Default Value: 0000h
  Access: Read/Write, Read-only Size: 16bits
  This register is used for DDMA Channel 1 base address assignment, data width status and enable control.

Cfg_40h		DDMA Slave Channel_1 Register / DDMA Slave Channel_0 Register	
<31:20>	R/W	DDMA Slave Channel_1 Base Address A[15:4]	000h
<19>	R/W	DDMA Slave Channel_1 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_1 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<18:17>	RO	DDMA Slave Channel_1 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	00b
<16>	R/W	DDMA Slave Channel_1 Enable. 0=Disabled, 1=Enabled.	0b

6.3.7 DDMA Slave Channel_3 Register / DDMA Slave Channel_2 Register

- **DDMA Slave Channel 2 Register**

  Address Offset: 44h – 45h Default Value: 0000h
  Access: Read/Write, Read-only Size: 16bits
  This register is used for DDMA Channel 2 base address assignment, data width status and enable control.

Cfg_44h		DDMA Slave Channel_3 Register / DDMA Slave Channel_2 Register	
<15:4>	R/W	DDMA Slave Channel_2 Base Address A[15:4]	000h
<3>	R/W	DDMA Slave Channel_2 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_2 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<2:1>	RO	DDMA Slave Channel_2 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	00b
<0>	R/W	DDMA Slave Channel_2 Enable. 0=Disabled, 1=Enabled.	0b

- **DDMA Slave Channel 3 Register**

  Address Offset: 46h – 47h Default Value: 0000h
  Access: Read/Write, Read-only Size: 16bits
  This register is used for DDMA Channel 3 base address assignment, data width status and enable control.

Cfg_44h		DDMA Slave Channel_3 Register / DDMA Slave Channel_2 Register	
<31:20>	R/W	DDMA Slave Channel_3 Base Address A[15:4]	000h
<19>	R/W	DDMA Slave Channel_3 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_3 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<18:17>	RO	DDMA Slave Channel_3 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	00b
<16>	R/W	DDMA Slave Channel_3 Enable. 0=Disabled, 1=Enabled.	0b

6.3.8 DDMA Slave Channel_5 Register / DMA Type-F Timing / PPD Register

- **PPD Register**

Address Offset: 48h Default Value: FFh
Access: Read/Write Size: 8bits
This register is used to enable the PC/PCI DMA engine and each channel.

Cfg_48h		DDMA Slave Channel_5 Register / DMA Type-F Timing / PPD Register	
<7:5>	R/W	PPD DREQ Enable bits for Channel_[7:5]. 0= Masked, 1= Enabled.	111b
<4>	R/W	PPD Global Enable bit. 0b: Disable PPDREQ#/PPDGNT# coding 1b: Enable PPDREQ#/PPDGNT# coding	1b
<3:0>	R/W	PPD DREQ Enable bits for Channel_[3:0]. 0=Masked, 1= Enabled.	1111b

- **DMA Type-F Timing**

Address Offset: 49h Default Value: 00h
Access: Read/Write Size: 8bits
This register is used to control DMA Type F timing which applies to both DDMA and PPD. The Type F DMA timing is not ISA compatible timing.

Cfg_48h		DDMA Slave Channel_5 Register / DMA Type-F Timing / PPD Register	
<15:8>	R/W	Type F DMA Timing Enable for each channel (apply to both DDMA and PPD, user should aware that, the Type F DMA Timing is not ISA compatible timing). 0= Disabled, 1=Enabled.	00h

- **DDMA Slave Channel 5 Register**

Address Offset: 4Ah – 4Bh Default Value: 0002h
Access: Read/Write, Read-only Size: 16bits
This register is used for DDMA Channel 5 base address assignment, data width status and enable control.

Cfg_48h		DDMA Slave Channel_5 Register / DMA Type-F Timing / PPD Register	
<31:20>	R/W	DDMA Slave Channel_5 Base Address A[15:4]	000h
<19>	R/W	DDMA Slave Channel_5 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_5 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<18:17>	RO	DDMA Slave Channel_5 Transfer Data width. 00=8 bits, 01=16 bits, 10=32 bits, 11=Reserved.	01b
<16>	R/W	DDMA Slave Channel_5 Enable. 0= Disabled, 1=Enabled.	0b

6.3.9 DDMA Slave Channel_7 Register / DDMA Slave Channel_6 Register

- **DDMA Slave Channel 6 Register**

Address Offset: 4Ch – 4Dh Default Value: 0002h
Access: Read/Write, Read-only Size: 16bits
This register is used for DDMA Channel 6 base address assignment, data width status and enable control.

Cfg_4Ch		DDMA Slave Channel_7 Register / DDMA Slave Channel_6 Register	
<15:4>	R/W	DDMA Slave Channel_6 Base Address A[15:4]	000h
<3>	R/W	DDMA Slave Channel_6 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_6 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<2:1>	RO	DDMA Slave Channel_6 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	01b
<0>	R/W	DDMA Slave Channel_6 Enable. 0=Disabled, 1=Enabled.	0b

- **DDMA Slave Channel 7 Register**

Address Offset: 4Eh – 4Fh Default Value: 0002h
Access: Read/Write, Read-only Size: 16bits
This register is used for DDMA Channel 7 base address assignment, data width status and enable control.

Cfg_4Ch		DDMA Slave Channel_7 Register / DDMA Slave Channel_6 Register	
<31:20>	R/W	DDMA Slave Channel_7 Base Address A[15:4]	000h
<19>	R/W	DDMA Slave Channel_7 Non-Legacy Extended addressing Enable. If disabled, then the Base Address A[31:24] register of Channel_7 will be always reset to 00h for memory access under 16MB. 0=Disabled, 1=Enabled.	0b
<18:17>	RO	DDMA Slave Channel_7 Transfer Data width. 00=8bits, 01=16bits, 10=32bits, 11=Reserved.	01b
<16>	R/W	DDMA Slave Channel_7 Enable. 0=Disabled, 1=Enabled.	0b

6.3.10 ROM / ISA Spaces and Timing Control

- **Timing Control Register**

Address Offset: 50h Default Value: 001XX000b
Access: Read/Write, Read-only Size: 8bits
This register is used for PCI Target I/F Response.

Cfg_50h		ISA Spaces and Timing Control	
<7:6>	R/W	**Palette Handling.** 00b: iWiR. Ignore write, ignore Read access. 01b: sWiR. Snoop write, ignore Read access 10b: Sw+R. Snoop write, positive decode read access 11b: +W+R. Positive decode write, positive decode read access	00b
<5>	R/W	I/O Port 00000080h Snoop Write (For POST code dump): 1b: Enable Snoop Write to Port 80h 0b: No response or do Subtractive decode for Port 80h	1b
<4>	RO	Reserved	--
<3>	R/W	F-Segment BIOS access (of both 000FXXXXh & FFFFXXXXh): 1b: Positive decode with Fast DEVSEL# timing for F-segment 0b: No response or do Subtractive decode for F-segment	Power-On Strap value of BALE

<2>	R/W	Reserved, must be written with 0. For compatible test only. Enable Processing Delayed Transaction in PC/PCI DMA cycle: 1b: Delayed Transaction is enabled in PPDMA cycle if Cfg_50<1> is also enabled 0b: Delayed Transaction is disabled in PPDMA cycle, response as non-Delayed Transaction.	0b
<1>	R/W	Delayed Transaction in PIO cycle: 1b: Delayed Transaction is enabled. 0b: Delayed Transaction is disabled.	0b
<0>	R/W	Non-Claimed PCI cycle until Subtractive DEVSEL# timing: 1b: Responses as a Subtractive decode agent 0b: Still No response (only positive decode pre-defined space)	0b

- **Memory Top / IO Recovery Register**

Address Offset: 51h Default Value: F0h
Access: Read/Write Size: 8bits

This register is used for system BIOS to set extended memory top in 16MB space (below memory hole) and ISA I/O recovery time between two different PCI I/O accesses (i.e. no additional recovery wait state will be inserted during byte conversion).

Cfg_50h		ISA Spaces and Timing Control	
<15:12>	R/W	TOP of Memory boundary (Up to Memory Hole) in 1MB ~ 16MB location through PCI bus when DMA or ISA Master access: 0000b: 1M, 0001b: 2M, 0010b: 3M, 0011b: 4M, 0100b: 5M, 0101b: 6M, 0110b: 7M, 0111b: 8M, 1000b: 9M, 1001b: 10M, 1010b: 11M, 1011b: 12M, 1100b: 13M, 1101b: 14M, 1110b: 15M, 1111b: 16M.	1111b
<11:10>	R/W	16-bit I/O Access Recovery Time 00b:3.5 BCLK, 01b:4.5 BCLK, 10b:5.5 BCLK, 11b: 7.5 BCLK	00b
<9:8>	R/W	8-bit I/O Access Recovery Time 00b:3.5 BCLK, 01b:5.5 BCLK, 10b:7.5 BCLK, 11b:11.5 BCLK	00b

- **ISA Space Register**

Address Offset: 52h Default Value: FFh
Access: Read/Write Size: 8bits

This register is used for IT8888G to decide whether to forward DDMA or ISA Master cycle to PCI bus.

Cfg_50h		ISA Spaces and Timing Control	
<23>	R/W	KBC Space (0060/2/4/6) location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<22>	R/W	Memory Space of 000EXXXXh location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<21>	R/W	Memory Space of 000D8000h~000DFFFFh location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<20>	R/W	Memory Space of 000D0000h~000D7FFFh location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b

Cfg_50h		ISA Spaces and Timing Control	
<19>	R/W	Memory Space of 000C8000h~000CFFFFh location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<18>	R/W	Memory Space of 000C0000h~000C7FFFh (VGA BIOS) location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<17>	R/W	Memory Space of 000A0000h~000BFFFFh (Video Buffer) location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b
<16>	R/W	Memory Space of 00080000h~0009FFFFh location when DMA or ISA Master access: 0b: @ ISA, Disable forwarding. 1b: @ PCI, then issue PCI master cycle.	1b

- **ROM Decoding Register**

Address Offset: 53h Default Value: 01h
Access: Read/Write Size: 8bits
This register is used to generate ROM chip select.

Cfg_50h		ISA Spaces and Timing Control	
<31 >	R/W	Enable ROMCS# from Memory space FFFEXXXXh (Top E-seg/4GB). 0b: Excludes FFFEXXXXh; 1b: Includes FFFEXXXXh	0b
<30 >	R/W	Enable ROMCS# from Memory space FFF80000h ~ FFFDFFFFh (Extended 384K of Top 4GB). 0b: Excludes; 1b: Includes	0b
<29 >	R/W	Enable ROMCS# from Memory space FFF00000h ~ FFF7FFFFh (1MB Extended 512K of Top 4GB). 0b: Excludes; 1b: Includes	0b
<28>	R/W	Enable ROMCS# from Memory space 000EXXXXh (E-seg/1MB) 0b: Excludes 000EXXXXh; 1b: Includes 000EXXXXh	0b
<27>	R/W	Enable ROMCS# from Memory space 000DXXXXh (D-seg/1MB) 0b: Excludes 000DXXXXh; 1b: Includes 000DXXXXh	0b
<26>	R/W	Enable ROMCS# from Memory space 000C8000h ~ 000CFFFFh 0b: Excludes 000C8000h ~ 000CFFFFh 1b: Includes 000C8000h ~ 000CFFFFh	0b
<25>	R/W	Enable ROMCS# from Memory space 000C0000h ~ 000C7FFFh 0b: Excludes 000C0000h ~ 000C7FFFh 1b: Includes 000C0000h ~ 000C7FFFh	0b
<24>	R/W	Flash ROM Write Protect (Mask ROMCS# and/or MEMW#) 0b: Enable Write to ROM; 1b: Write-Protect	1b

6.3.11 Retry/Discard Timers, Misc. Control Register

- **Retry Timer Control Register**

Address Offset: 54h Default Value: 3Fh
Access: Read/Write, Write-1-to-Clear Size: 8bits
This register is used for PCI Master I/F to count Retry control.

Cfg_54h		Retry/Discard Timers, Misc. Control Register	
<7>	R/W	Enable Retry overflow report to SERR#. 0=Disabled, 1=Enabled.	0b
<6>	R/W1C	Read 1 as the PCI Master interface can not complete its transaction	0b

Cfg_54h		Retry/Discard Timers, Misc. Control Register	
		within the time (overflow) defined in Cfg_54h<5:0>. Write 1 to clear.	
<5:0>	R/W	Retry Timer. PCI Master interface repeats retried transactions and if the retry counts exceed the Retry Timer value (x 8 times), then the PCI Master interface will give up more retry and set status bit (Cfg_54h<6>). 00h=not check retry; 01h=8 times; FFh=255*8 times.	3Fh

- **Discard Timer Control Register**

Address Offset: 55h Default Value: 3Fh
Access: Read/Write, Write-1-to-Clear Size: 8bits
This register is used for PCI Target I/F to count retried time for Discard control.

Cfg_54h		Retry/Discard Timers, Misc. Control Register	
<15>	R/W	Enable Discard overflow report to SERR#. 0=Disabled, 1=Enabled.	0b
<14>	R/W1C	Read 1 as the PCI Target interface can not receive the same retried transaction more than the time (overflow) defined in Cfg_54h<13:8>. Write 1 to clear.	0b
<13:8>	R/W	Discard Timer. If the PCI Master still doesn't repeat the same transaction when timer expired (Value x256 PCI clocks) for the PCI Target interface that issued the retry cycle, the PCI Target interface will then stop waiting and set status bit (Cfg_54h<14>). 00h=never expire; 01h=256T; FFh=255*256T.	3Fh

- **Misc. Control Register**

Address Offset: 56h – 57h Default Value: 8C00h
Access: Read/Write Size: 16bits
This register is used for PCI I/F Arbitration for DDMA/PPDMA and test and CLKRUN# function.

Cfg_54h		Retry/Discard Timers, Misc. Control Register	
<31>	R/W	Enable DDMA-Concurrent option 0: Disabled, Hold PCI bus through all DMA cycles 1: Enabled PCI & DMA / ISA-Master Accesses Concurrent.	1b
<30>	R/W	Enable Dummy PPDREQ# message for patching PC/PCI DMA undefined multiple DMA requests underrun/overrun. 0: Disabled, as PC/PCI DMA protocol not supports DMA devices multiple de-asserted simultaneously. 1: Enabled, IT8888G will issue a dummy PPDREQ# message (empty requests) to update the PPDREQ# decoding in core logic chipset.	0b
<29>	R/W	Enable Dummy FRAME# for some chipset arbitration patch when DDMA / ISA Master access with DDMA-Concurrent mode disabled. 0: Disabled, no Dummy FRAME#. 1: Enabled Dummy FRAME# for DDMA Verify and DDMA/ Master non-PCI access. (Available only when Cfg_54h<31>=0).	0b
<28>	R/W	SA[1:0] Toggling of ISA I/O cycles from the same one PCI I/O (due to multiple bytes). But when accessing the internal DDMA I/O ports, the SA[1:0] will be always increased for DMA device driver to program 32-bit Base_Address or 16-bit Word_Count registers): 0: Address Increased as ISA Memory mapped I/O cycles. 1: Address Fixed as the first ISA I/O for the successive I/O.	0b
<27>	R/W	Force PCI clock always running (whenever CLKRUN# sampled high, then drive low output for 2T): 1: Force PCICLK running. 0: Request PCI clock only for ISA master, DDMA and Interrupt.	1b
<26>	R/W	Enable ISA Bus Refresh Timer	1b

Cfg_54h		Retry/Discard Timers, Misc. Control Register	
		1: Enable Processing Refresh every 15.36μs. (PCI clock will be kept running by asserting CLKRUN#.) 0: Disable Refresh Timer.	
<25>	R/W	Reserved for IC test only. Test SMB interface	0b
<24>	R/W	Reserved for IC test only. Test Refresh Address Counter	0b
<23>	R/W	Enable ISA Bus Master to update Flash ROM (when Cfh_50h<24> = 0) 0: Disabled, only PIO (CPU + PCI Master) and DMA cycle can write into ROM with control timing for WE#-Controlled Write Operation. 1: Enabled, and the control timing is used for Flash ROM CE#-Controlled Write Operation	0b
<22>	R/W	Enable PCI Configure write operation to change the content of Subsystem Device/Vendor ID Register (Cfg_2Ch<31:0>). 0: Disabled, only SMB_ROM Configuring can update it. 1: Enabled. It is generally provided for optional device BIOS to change subsystem ID for its device.	0b
<21>	R/W	Mask IOCHCK# to report to SERIRQ coding 0: Unmasked, IOCHCK# status will be reflected in SERIRQ coding. 1: Masked, IOCHCK# will not be reflected in SERIRQ coding.	0b
<20>	R/W	Select the function of pin#138 to be NOGO or CLKRUN#: 0=NOGO, 1=CLKRUN#.	0b
<19>	R/W	Enable ISA IOCHCK# report (Cfg_54h<18>) to SERR#. 0=Disabled, 1=Enabled.	0b
<18>	R/W1C	Read 1 as the ISA IOCHCK# is asserted. This is the inverse state of the latched ISA IOCHCK# signal. Write 1 to clear.	0b
<17>	R/W	Enable checking PCI I/O Cycle Byte Lane Error (Cfg_54h<16>) and report to SERR#. 0=Disabled, 1=Enabled.	0b
<16>	R/W1C	Read 1 as the PCI I/O Cycle Byte Lane Error occurred. Write 1 to clear.	0b

6.3.12 Positively Decoded IO_Space_0 Register

Address Offset: 58h – 5Bh Default Value: 00000000h
Access: Read/Write Size: 32bits

This register is used for the configuration and the Positively Decoded I/O Space 0.

Cfg_58h		Positively Decoded IO_Space_0	
<31>	R/W	IO_Space_0 Enable: 1b: IT8888G will respond to IO_Space_0; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_0: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_0: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_0 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_0: A[15:0], with A[31:16]=0000h	0000h

6.3.13 Positively Decoded IO_Space_1 Register

Address Offset: 5Ch – 5Fh Default Value: 00000000h
Access: Read/Write Size: 32bits

This register used for configuration and the Positively Decoded I/O Space 1.

Cfg_5Ch		Positively Decoded IO_Space_1	
<31>	R/W	IO_Space_1 Enable: 1b: IT8888G will respond to IO_Space_1; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_1: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_1: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_1 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_1: A[15:0], with A[31:16]=0000h	0000h

6.3.14 Positively Decoded IO_Space_2 Register

Address Offset: 60h – 63h Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded I/O Space 2.

Cfg_60h		Positively Decoded IO_Space_2	
<31>	R/W	IO_Space_2 Enable: 1b: IT8888G will respond to IO_Space_2; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_2: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_2: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_2 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_2: A[15:0], with A[31:16]=0000h	0000h

6.3.15 Positively Decoded IO_Space_3 Register

Address Offset: 64h – 67h Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded I/O Space 3.

Cfg_64h		Positively Decoded IO_Space_3	
<31>	R/W	IO_Space_3 Enable: 1b: IT8888G will respond to IO_Space_3; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_3: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_3: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_3 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b

Cfg_64h		Positively Decoded IO_Space_3	
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_3: A[15:0], with A[31:16]=0000h	0000h

6.3.16 Positively Decoded IO_Space_4 Register

Address Offset: 68h – 6Bh Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuring and the Positively Decoded I/O Space 4.

Cfg_68h		Positively Decoded IO_Space_4	
<31>	R/W	IO_Space_4 Enable: 1b: IT8888G will respond to IO_Space_4; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_4: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_4: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_4 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_4: A[15:0], with A[31:16]=0000h	0000h

6.3.17 Positively Decoded IO_Space_5 Register

Address Offset: 6Ch – 6Fh Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded I/O Space 5.

Cfg_6Ch		Positively Decoded IO_Space_5	
<31>	R/W	IO_Space_5 Enable: 1b: IT8888G will respond to IO_Space_5; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for IO_Space_5: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28>	R/W	Alias Enable for IO_Space_5: 1b: Don't care A[15:10]; 0b: Fully decode	0b
<27>	RO	Reserved	0b
<26:24>	R/W	IO_Space_5 Size: 000b: 1 bytes 010b: 4 bytes 100b: 16 bytes 110b: 64 bytes 001b: 2 bytes 011b: 8 bytes 101b: 32 bytes 111b: 128 bytes	000b
<23:16>	RO	Reserved	00h
<15:0>	R/W	Base Address of IO_Space_5: A[15:0], with A[31:16]=0000h	0000h

6.3.18 Positively Decoded Memory_Space_0 Register

Address Offset: 70h – 73h Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded Memory Space 0.

Cfg_70h		Positively Decoded Memory_Space_0	
<31>	R/W	Memory_Space_0 Enable: 1b: IT8888G will respond to Memory_Space_0; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for Memory_Space_0: 00b: Subtractive speed 10b: Medium speed	00b

Cfg_70h		Positively Decoded Memory_Space_0	
		01b: Slow speed 11b: Fast speed	
<28:27>	RO	Reserved	00b
<26:24>	R/W	Memory_Space_0 Size: 000b: 16KB 010b: 64KB 100b: 256KB 110b: 1MB 001b: 32KB 011b: 128KB 101b: 512KB 111b: 2MB	000b
<23:16>	R/W	High Page Base Address of Memory_Space_0: A[31:24]. IT8888G will relocate the access within Memory_Space_0 to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.	00h
<15:0>	R/W	Low Base Address of Memory_Space_0: A[23:8]. Bits <15:6> are R/W as A[23:14]; Bits <5:0> are RO as 6'b000000.	0000h

6.3.19 Positively Decoded Memory_Space_1 Register

Address Offset: 74h – 77h Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded Memory Space 1.

Cfg_74h		Positively Decoded Memory_Space_1	
<31>	R/W	Memory_Space_1 Enable: 1b: IT8888G will respond to Memory_Space_1; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for Memory_Space_1: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28:27>	RO	Reserved	00b
<26:24>	R/W	Memory_Space_1 Size: 000b: 16KB 010b: 64KB 100b: 256KB 110b: 1MB 001b: 32KB 011b: 128KB 101b: 512KB 111b: 2MB	000b
<23:16>	R/W	High Page Base Address of Memory_Space_1: A[31:24]. IT8888G will relocate the access within Memory_Space_1 to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.	00h
<15:0>	R/W	Low Base Address of Memory_Space_1: A[23:8]. Bits <15:6> are R/W as A[23:14]; Bits <5:0> are RO as 6'b000000.	0000h

6.3.20 Positively Decoded Memory_Space_2 Register

Address Offset: 78h – 7Bh Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded Memory Space 2.

Cfg_78h		Positively Decoded Memory_Space_2	
<31>	R/W	Memory_Space_2 Enable: 1b: IT8888G will respond to Memory_Space_2; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for Memory_Space_2: 00b: Subtractive speed 10b:Medium speed 01b: Slow speed 11b: Fast speed	00b
<28:27>	RO	Reserved	00b
<26:24>	R/W	Memory_Space_2 Size: 000b: 16KB 010b: 64KB 100b: 256KB 110b: 1MB 001b: 32KB 011b: 128KB 101b: 512KB 111b: 2MB	000b
<23:16>	R/W	High Page Base Address of Memory_Space_2: A[31:24]. IT8888G will relocate the access within Memory_Space_2 to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.	00h
<15:0>	R/W	Low Base Address of Memory_Space_2: A[23:8].	0000h

Cfg_78h		Positively Decoded Memory_Space_2	
		Bits <15:6> are R/W as A[23:14]; Bits <5:0> are RO as 6'b000000.	

6.3.21 Positively Decoded Memory_Space_3 Register

Address Offset: 7Ch – 7Fh Default Value: 00000000h
Access: Read/Write Size: 32bits
This register is used for configuration and the Positively Decoded Memory Space 3.

Cfg_7Ch		Positively Decoded Memory_Space_3	
<31>	R/W	Memory_Space_3 Enable: 1b: IT8888G will respond to Memory_Space_3; 0b: No-response	0b
<30:29>	R/W	Decoding Speed for Memory_Space_3: 00b: Subtractive speed 10b: Medium speed 01b: Slow speed 11b: Fast speed	00b
<28:27>	RO	Reserved	00b
<26:24>	R/W	Memory_Space_3 Size: 000b: 16KB 010b: 64KB 100b: 256KB 110b: 1MB 001b: 32KB 011b: 128KB 101b: 512KB 111b: 2MB	000b
<23:16>	R/W	High Page Base Address of Memory_Space_3: A[31:24]. IT8888G will relocate the access within Memory_Space_3 to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.	00h
<15:0>	R/W	Low Base Address of Memory_Space_3: A[23:8]. Bits <15:6> are R/W as A[23:14]; Bits <5:0> are RO as 6'b000000.	0000h

6.3.22 Undefined Register

Address Offset: those not listed above Default Value: 00000000h
Access: Read Only Size: 32bits
These registers are reserved as read only.

Cfg_XXh (else)		All other configuration registers in IT8888G	
<31:0>	RO	Reserved	00000000h

6.4 DDMA Slave Registers Description

Only one register Base address is dedicated to each DDMA slave channel, and unique 16-byte register spaces are allocated for each DDMA Slave channel. Below is the DDMA slave register description:

DDMA Slave Address	R/W	Register Name	IT8888G Operation
Channel_N Base Address + 0h	W	Transfer Base Address[7:0]	Write to 8237_8 or 8237_16 Base address register of Channel_N
Channel_N Base Address + 0h	R	Current Transfer Address[7:0]	Read from 8237_8or 8237_16 Current address register of Channel_N
Channel_N Base Address + 1h	W	Transfer Base Address[15:8]	Write to 8237_8 or 8237_16 Base address register of Channel_N1
Channel_N Base Address + 1h	R	Current Transfer Address[15:8]	Read from 8237_8 or 8237_16 Current address register of Channel_N
Channel_N Base Address + 2h	W	Transfer Base Address[23:16]	Write to Low Page register of Channel_N
Channel_N Base Address + 2h	R	Current Transfer Address[23:16]	Read from Low Page register of Channel_N
Channel_N Base Address + 3h	W	Transfer Base Address[31:24]	Write to High Page register of Channel_N
Channel_N Base Address + 3h	R	Current Transfer Address[31:24]	Read from High Page register of Channel_N
Channel_N Base Address + 4h	W	Base Word Count[7:0]	Write to 8237_8 or 8237_16 Base Word Count register of Channel_N
Channel_N Base Address + 4h	R	Current Word Count[7:0]	Read from 8237_8 or 8237_16 Current Word Count register of Channel_N
Channel_N Base Address + 5h	W	Base Word Count[15:8]	Write to 8237_8 or 8237_16 Base Word Count register of Channel_N
Channel_N Base Address + 5h	R	Current Word Count[15:8]	Read from 8237_8 or 8237_16 Current Word Count register of Channel_N
Channel_N Base Address + 6h	W	Base Word Count[23:16]	No Operation
Channel_N Base Address + 6h	R	Current Word Count[23:16]	Read 00h
Channel_N Base Address + 7h	N/A	Reserved	No Operation

[1] DDMA Host should handle Byte-Flip-Flop pointer.

DDMA Slave Registers Description (continued)

DDMA Slave Address	R/W	Register Name	IT8888G Operation
Channel_N Base Address + 8h	W	Command	Write to 8237_8 or 8237_16 Command register
Channel_N Base Address + 8h	R	Status	Read from 8237_8or 8237_16 Status register and convert / duplicate data bits, depending on Channel_N information.
Channel_N Base Address + 9h	W	S/W DMA Request	Write to 8237_8 or 8237_16 Request register
Channel_N Base Address + 9h	R	Reserved	Read Data Undefined
Channel_N Base Address + Ah	N/A	Reserved	Ignore Write; Read Data Undefined
Channel_N Base Address + Bh	W	Mode	Write to 8237_8 or 8237_16 Mode register
Channel_N Base Address + Bh	R	Reserved	Read Data Undefined
Channel_N Base Address + Ch	N/A	Reserved	Ignore Write; Read Data Undefined
Channel_N Base Address + Dh	W	Master Clear	Write to 8237_8 or 8237_16 Master Clear register
Channel_N Base Address + Dh	R	Reserved	Read Data Undefined
Channel_N Base Address + Eh	N/A	Reserved	Ignore Write; Read Data Undefined
Channel_N Base Address + Fh	W	Multi-Channel Mask	Write to 8237_8 or 8237_16 Single Channel Mask register w/ shifting data bit<0> to bit<2> and converting Channel_N information to bit<1:0>
Channel_N Base Address + Fh	R	Multi-Channel Mask	Read from 8237_8or 8237_16 Single Channel Mask register and convert / duplicate data bits, depending on Channel_N information.

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7. Characteristics

Absolute Maximum Ratings*

Applied Voltage (V_{CC}) ..... -0.3V to 6.0V

Input Voltage (V_I) ..... -0.3V to V_{CC}+0.3V

Output Voltage (V_O) ..... -0.3V to V_{CC}+0.3V

Storage Temperature (T_{STG}) ..... -40°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in "Recommended Operating Conditions" is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7-1. Recommended Operating Conditions

Symbol	Parameter	Min.	Typical	Max.	Units
VCC3	Power Supply	3.0	3.3	3.6	V
VCC	Power Supply	4.75	5.0	5.25	V
V_{IN}	Input Voltage	0		VCC / VCC3	V
T_{OPT}	Operating Temperature	0	25	70	^{o}C

7.1 DC Electrical Characteristics

Table 7-2. General DC Characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Units
I_{IL}	Input Low Current	no P/D or P/U	-1		1	μA
I_{IH}	Input High Current	no P/D or P/U	-1		1	μA
I_{OZ}	Tri-state Leakage Current		-10		10	μA
I_{CC}	Operating Current	from VCC source				mA
I_{CC3}	Operating Current	from VCC3 source				mA
C_{IN}	Input Capacitance			3		ρF
C_{OUT}	Output Capacitance			3 to 6		ρF
C_{BID}	Bi-directional buffer Capacitance			3 to 6		ρF

Table 7-3. DC Electrical Characteristics

(TOPT=0oC~70oC, VCC3=3.0~3.6V, VCC=4.75~5.25V)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Units
V_{IL}	Input Low Voltage for 5V cell	TTL			0.8	V
V_{IL}	Input Low Voltage for 3.3V cell	CMOS			0.3*VCC3	V
V_{IL}	Schmitt Input Low Voltage	TTL		1.10		V
V_{IH}	Input High Voltage for 5V cell	TTL	2.2			V
V_{IH}	Input High Voltage for 3.3V cell	CMOS	0.7*VCC3			V
V_{IH}	Schmitt Input High Voltage	TTL		1.87		V
V_{OL}	Output Low Voltage for 5V cell				0.4	V
V_{OL}	Output Low Voltage for 3.3V cell				0.4	V
V_{OH}	Output High Voltage for 5V cell		3.5			V
V_{OH}	Output High Voltage for 3.3V cell		2.3			V

7.2 AC Characteristics

Table 7-4. AC Characteristics of PCI Interface Timing

(VCC=5.0V±5%, VCC3=3.3V±5%, Ta=0oC~70oC, CL=50 F2) unit: ns

Symbol	Parameter	Min.	Typical	Max.	Notes
t_{VALID_PCI}	Valid output delay time				
t_{SETUP_PCI}	Input setup time				
t_{HOLD_PCI}	Input hold time				
t_{ON_PCI}	Float to Active				
t_{OFF_PCI}	Active to Float				

Table 7-5. AC Characteristics of ISA Interface Timing (PIO Cycle)

(Measured in Design Simulation) unit: 1T=1 PCICLK period ≥ 30ns
In the following parameters, the LA[23:20] signals are replaced by SA[23:20] to simplify descriptions.

Symbol	Parameter	Typical	Notes
t_{BCLK}	BCLK frequency	≤ 8.25	MHz (=PCICLK/4)
t_{L_BCLK}	BCLK low period	≥ 2T	1T=1 PCICLK period
t_{H_BCLK}	BCLK high period	2T	
t_{H_BALE}	BALE high period in PIO mode	2T	
$t_{OS\_LA\_BALE}$	SA[23:2] valid to BALE de-asserted	≥ 4T	
$t_{OS\_LA\_M}$	SA[23:2] valid to MEMR#/MEMW# asserted	≥ 4T	16-bit memory access
		≥ 6T	8-bit memory access
$t_{OS\_LA\_IO}$	SA[23:2] valid to IOR#/IOW# asserted	≥ 6T	16-/8-bit I/O access
$t_{OS\_SA\_M}$	SA[1:0], SBHE# valid to MEMR#/MEMW# asserted	2T	16-bit memory access
		4T	8-bit memory access
$t_{OS\_SA\_IO}$	SA[1:0], SBHE# valid to IOR#/IOW# asserted	4T	16-/8-bit I/O access
t_{OH_A}	SA[23:0], SBHE# hold after command de-asserted	≥ 2T	all PIO access
t_{W_M}	MEMR#/MEMW# low width	8T	16-bit access w/o NOWS#
		18T	8-bit access w/o NOWS#
		≥ 4T	16-bit access w/ NOWS#
		≥ 6T	8-bit access w/ NOWS#
t_{W_IO}	IOR#/IOW# low width	6T	16-bit access
		18T	8-bit access w/o NOWS#
		≥ 6T	8-bit access w/ NOWS#
t_{OS_SD}	SD[15:0] valid to MEMW#/IOW# asserted	0T	16-bit memory write
		2T	else
t_{OH_SD}	SD[15:0] hold/float after MEMW#/IOW# de-asserted	2T	all PIO write access
t_{OH_CMD}	command hold from IOCHRDY	≥ 4T	all PIO write access

[2] All the pads loading are based on 50ρF for Typical simulated values.

Table 7-6. AC Characteristics of ISA Interface Timing (DMA Cycle)

(Measured in Design Simulation) unit: 1T=1 PCICLK period ≥ 30ns
In the following parameters, the LA[23:20] signals are replaced by SA[23:20] to simplify descriptions.

Symbol	Parameter	Typical	Notes
DDMA Mode			
$t_{DD\_AEN\_DACK}$	AEN asserted to DACKn# asserted	0T	DACK[7:5]#
		4T	DACK[3:0]#
$t_{DD\_DACK\_AEN}$	DACKn# de-asserted to AEN de-asserted	0T	DACK[7:5]#
		4T	DACK[3:0]#
$t_{DD\_DACK\_IOR}$	DACKn# asserted to IOR# asserted	6T	
$t_{DD\_DACK\_IOW}$	DACKn# asserted to IOW# asserted	14T	
$t_{DD\_DACK\_M}$	DACKn# asserted to MEMR#/MEMW# asserted	14T	Memory space on ISA
$t_{DD\_PAGE\_M}$	Page Address valid to MEMR#/MEMW# asserted	14T	SA[23:17/16]
$t_{DD\_SA\_M}$	Base Address valid to MEMR#/MEMW# asserted	10T	SA[16/15:0]
$t_{DD\_M\_SA}$	Address hold after MEMR#/MEMW# de-asserted	4T	SA[23:0]
$t_{DD\_W\_R}$	IOR#/MEMR# hold after MEMW#/IOW# de-asserted	2T	
$t_{DD\_OS\_SD}$	SD[15:0] setup to IOW# de-asserted	8T	Memory space on PCI
$t_{DD\_OH\_SD}$	SD[15:0] hold/float after MEMW#/IOW# de-asserted	4T	
$t_{DD\_W\_IOR}$	IOR# width	≥ 26T	Memory space on PCI
		30T	Memory space on ISA
$t_{DD\_W\_IOW}$	IOW# width	≥ 16T	Memory space on PCI
		24T	Memory space on ISA
$t_{DD\_W\_MEMR}$	MEMR# width	26T	Memory space on ISA
$t_{DD\_W\_MEMW}$	MEMW# width	20T	Memory space on ISA
$t_{DD\_OS\_TC}$	TC valid to IOR#/IOW# de-asserted	22/28T	
$t_{DD\_OH\_TC}$	TC hold after IOR#/IOW# de-asserted	4/6T	

Table 7-6 AC Characteristics of ISA Interface Timing (DMA Cycle) (continued)

(Measured in Design Simulation) unit: 1T=1 PCICLK period ≥ 30ns

Symbol	Parameter	Typical	Notes
PC/PCI DMA Mode			
$t_{PP\_SU\_IOR}$	PPDMA I/O cycle start to IOR# asserted	≥ 7T	
$t_{PP\_SU\_IOW}$	PPDMA I/O cycle start to IOW# asserted	≥ 13/9T	Normal/Type-F DMA
$t_{PP\_HD\_IOR}$	IOR# de-asserted to PPDMA I/O cycle end	6T	DACKn#/AEN hold until PPDGNT# de-asserted
$t_{PP\_HD\_IOW}$	IOW# de-asserted to PPDMA I/O cycle end	8T	
$t_{PP\_OS\_SD}$	SD[15:0] setup to IOW# asserted (falling edge)	8/4T	Normal/Type-F DMA
$t_{PP\_OH\_SD}$	SD[15:0] hold/float after IOW# de-asserted	8T	
$t_{PP\_W\_IOR}$	IOR# width	26/6T	Normal/Type-F DMA
$t_{PP\_W\_IOW}$	IOW# width	18/6T	Normal/Type-F DMA
$t_{PP\_OSR\_TC}$	TC valid to IOR # de-asserted	28/8T	Normal/Type-F DMA
$t_{PP\_OSW\_TC}$	TC valid to IOW# de-asserted	26/10T	Normal/Type-F DMA
$t_{PP\_OH\_TC}$	TC hold after IOR#/IOW# de-asserted	4/6T	

Table 7-7. AC Characteristics of SMB Interface Timing

(refer to Figure 7-23, Measured in Design Simulation) unit: s

Symbol	Parameter	Typical	Notes
t_{SCLK}	SCLK frequency	≤ 86.8	KHz (= PCICLK/384)
t_{L_SCLK}	SCLK low period	5.76	μs (= 192 PCI clocks)
t_{H_SCLK}	SCLK high period	5.76	μs
t_{SU_STA}	Start condition setup time	5.76	μs
t_{HD_STA}	Start condition hold time	5.76	μs
t_{SU_STOP}	Stop condition setup time	5.76	μs
t_{OS_SDATA}	SDATA output setup time	2.38	μs (= 96 PCI clocks)
t_{OH_SDATA}	SDATA output hold time	2.38	μs
t_{IS_SDATA}	SDATA input setup time	-2.3	μs
t_{IH_SDATA}	SDATA input hold time	-2.3	μs

7.3 Waveforms

In the following waveforms, the LA[23:20] signals symbol are replaced by SA[23:20] to simplify drawings.

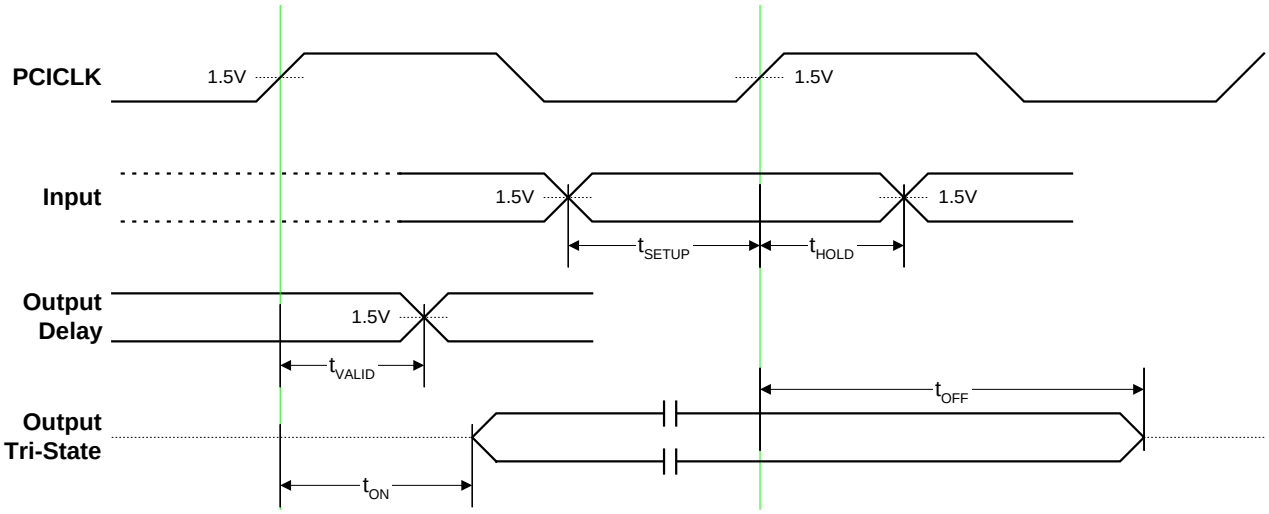


Figure 7-1. PCI Bus Interface Timing

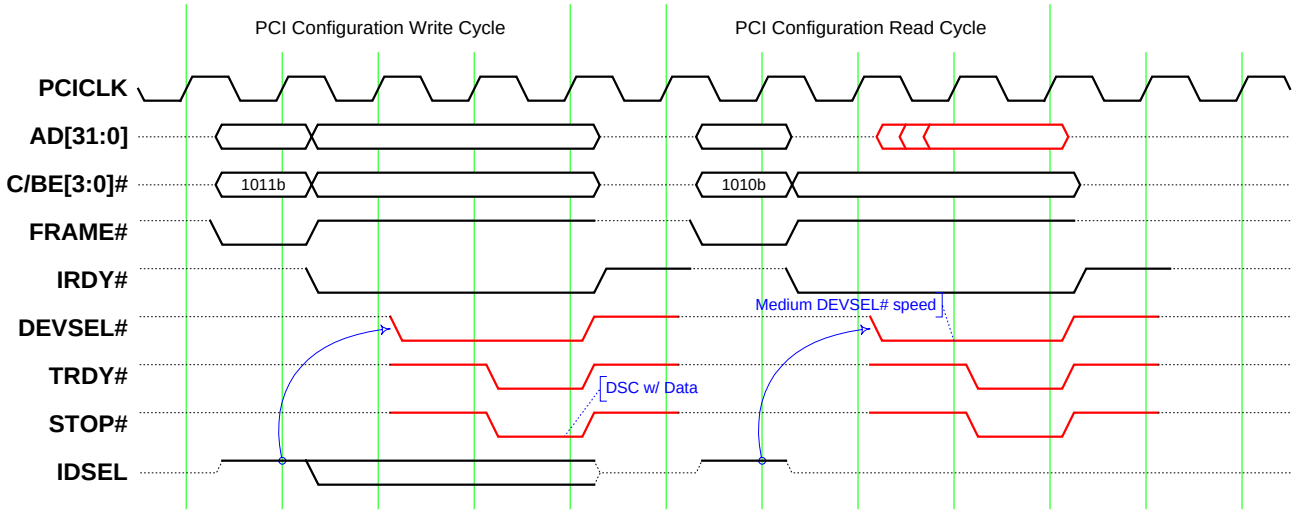


Figure 7-2. PCI Configuration Write / Read Cycle

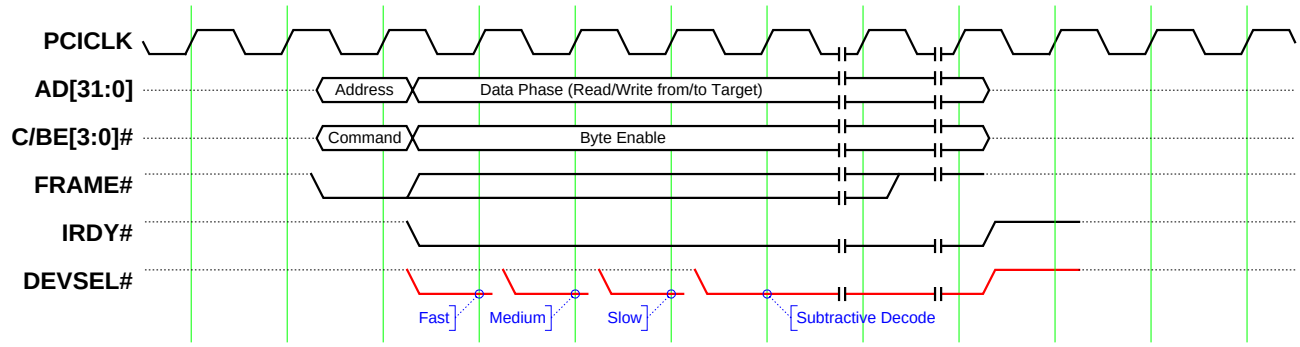


Figure 7-3. DEVSEL# Decoding Speed

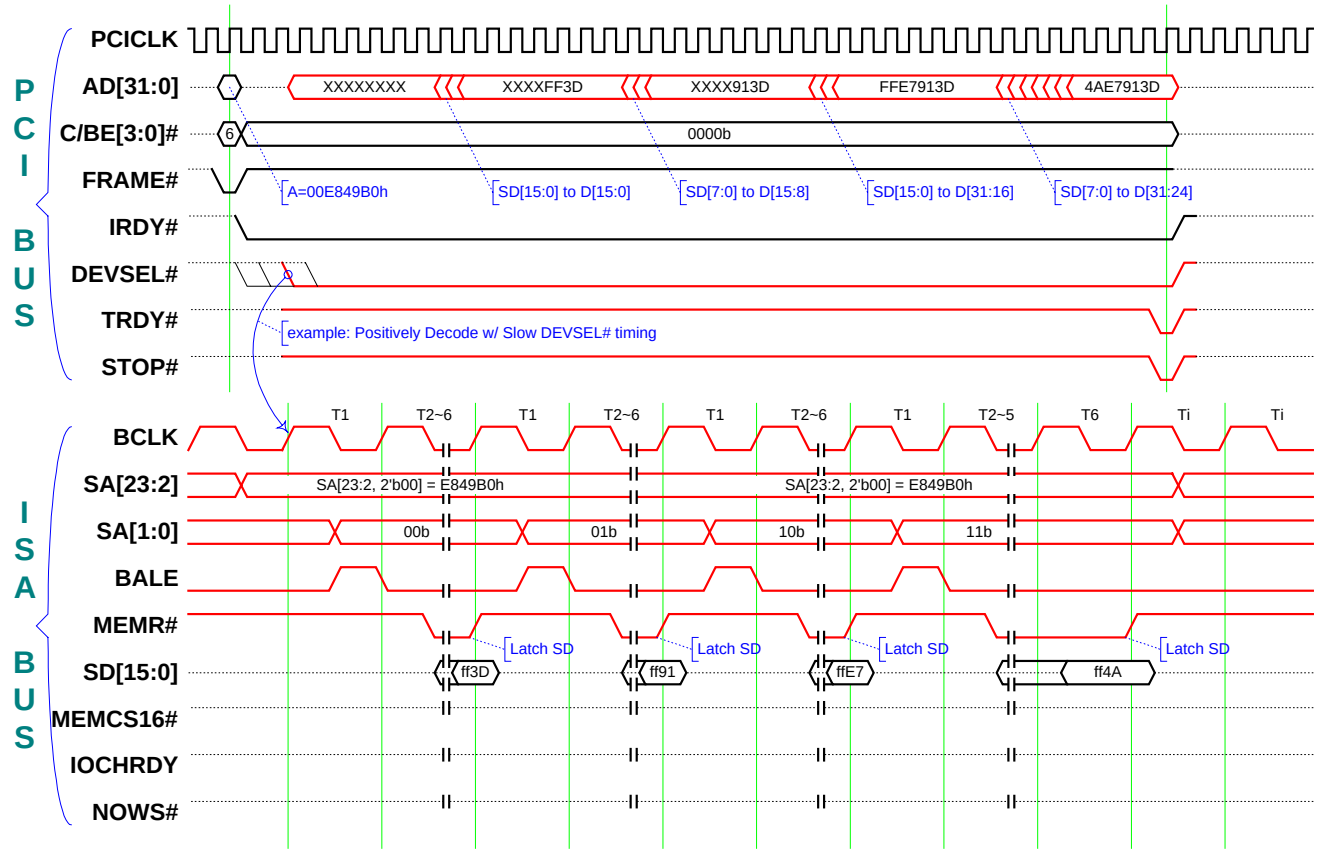


Figure 7-4. PCI Memory Read from ISA Device when Delayed Transaction is disabled

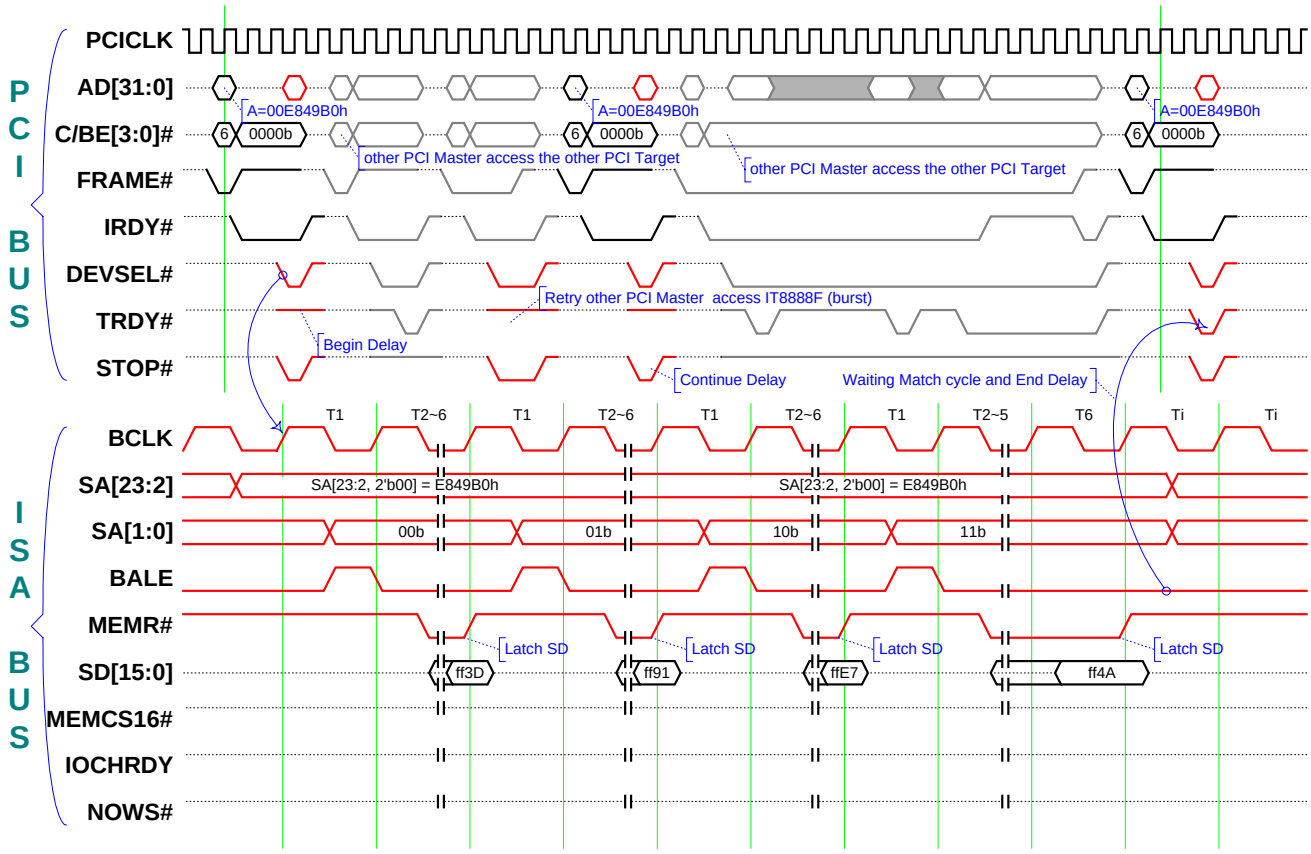


Figure 7-5. PCI Memory Read from ISA Device when Delayed Transaction is enabled

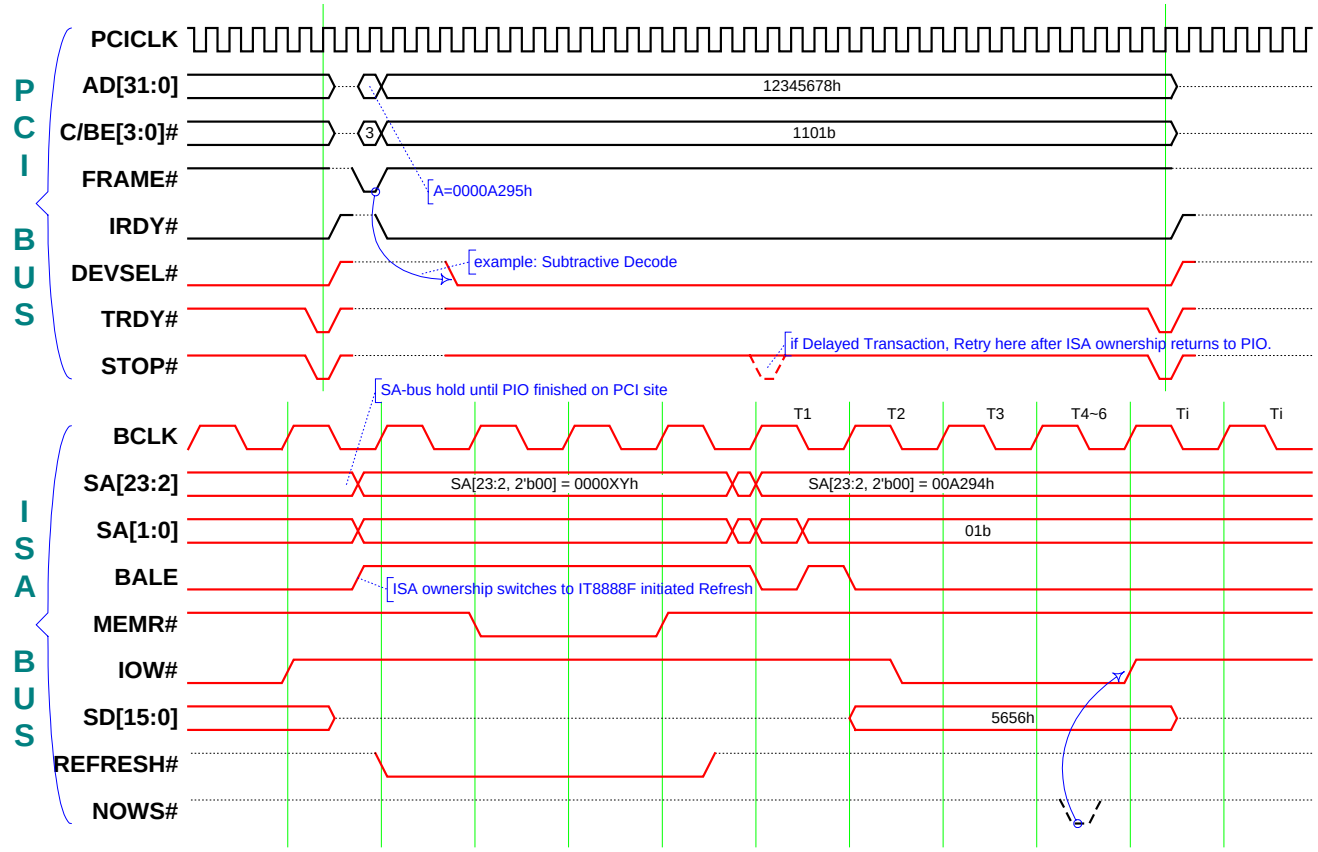


Figure 7-6. IT8888G Initiated Refresh Cycle

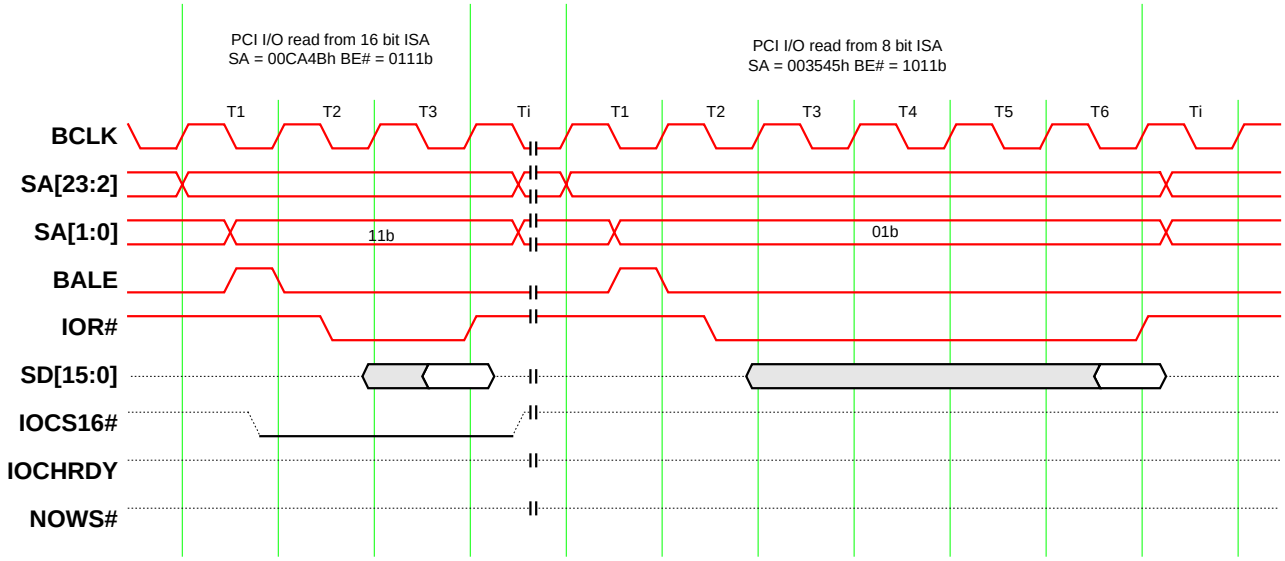


Figure 7-7 PCI I/O Read from ISA device

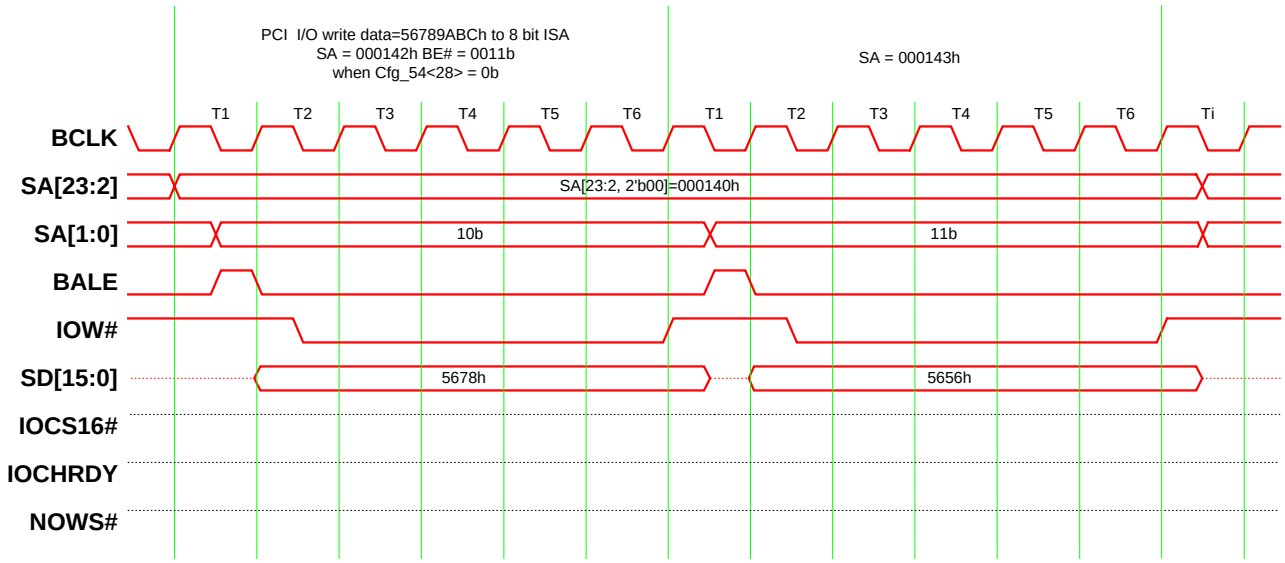


Figure 7-8 PCI I/O Write to 8-bit ISA Device when Cfg_54<28>=0b

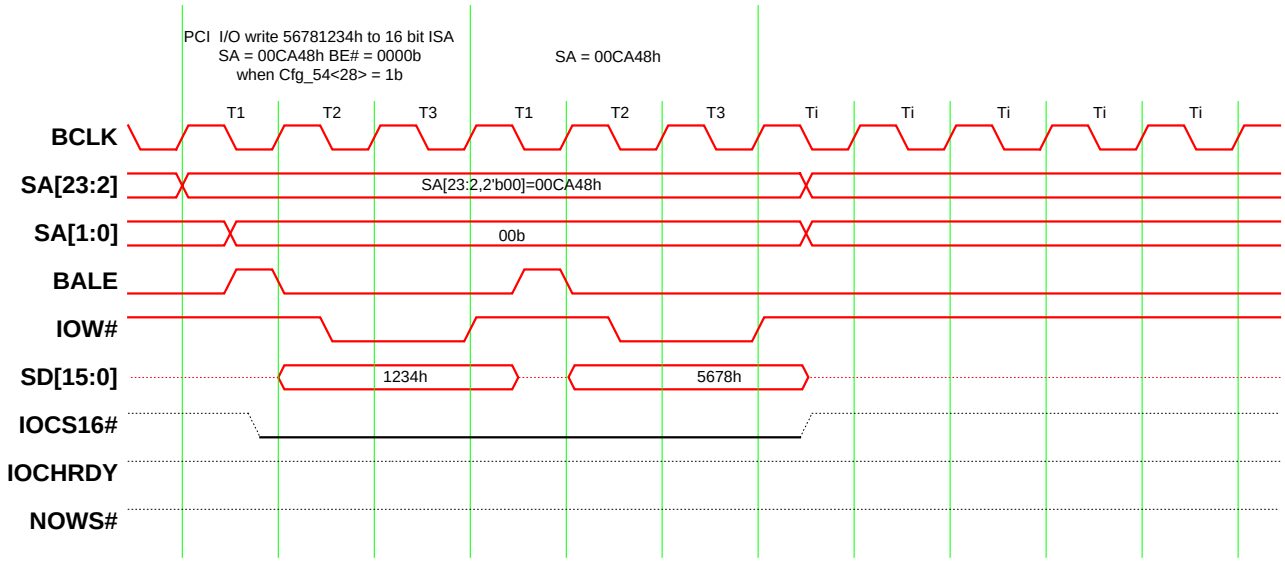


Figure 7-9. PCI I/O Write to 16-bit ISA Device when Cfg_54<28>=1b

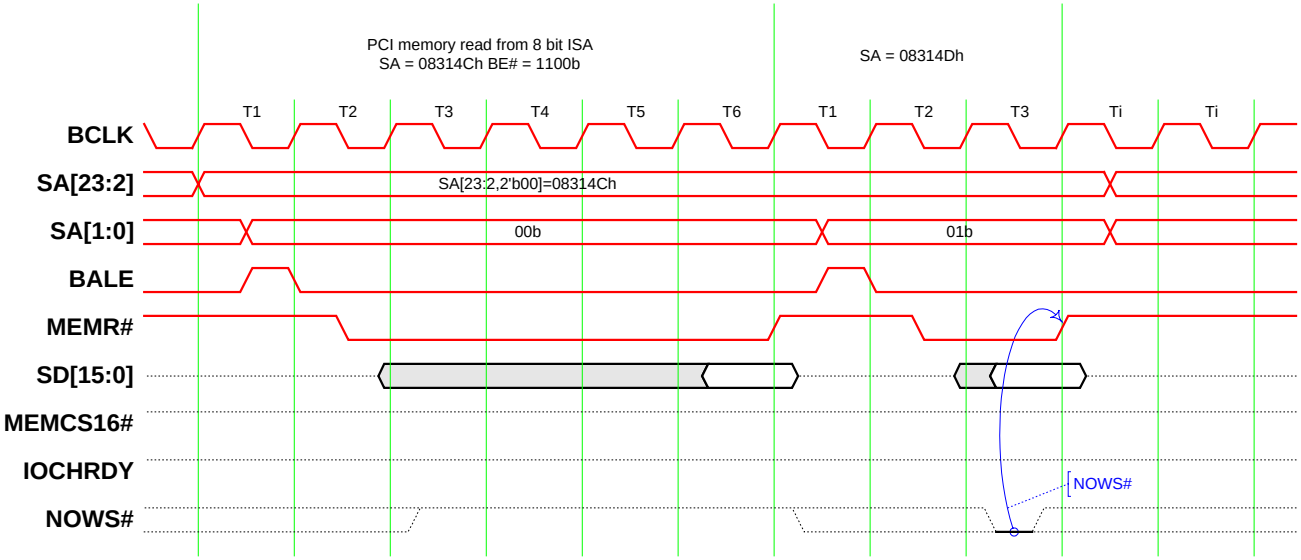


Figure 7-10. PCI Memory Read from 8-bit ISA Device

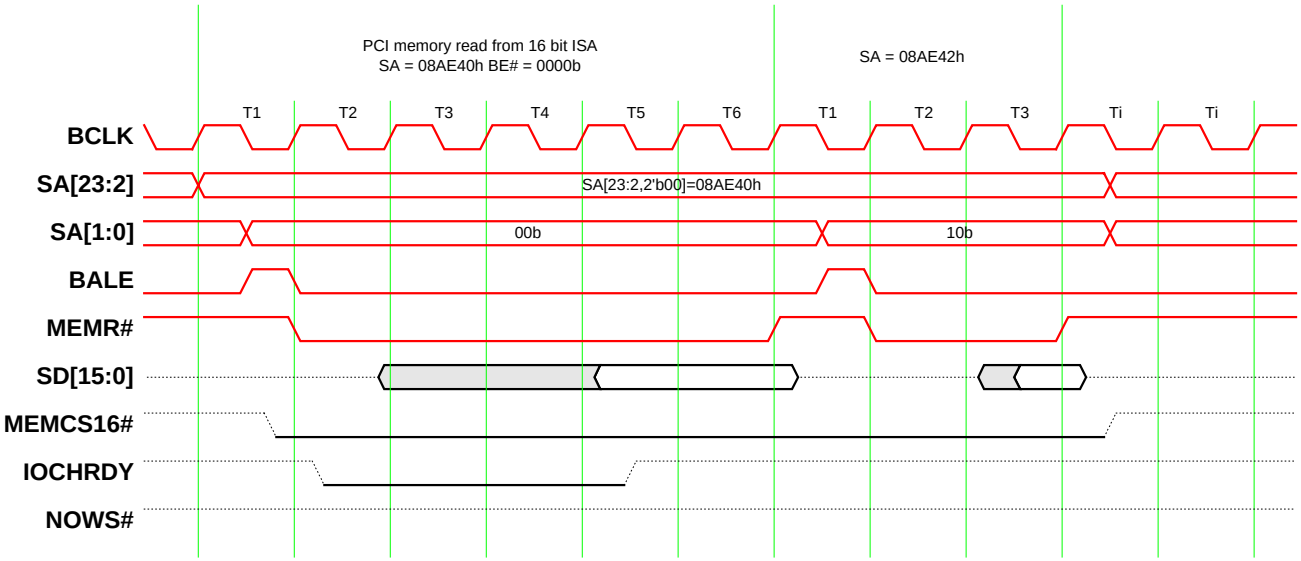


Figure 7-11. PCI Memory Read from 16-bit ISA Device

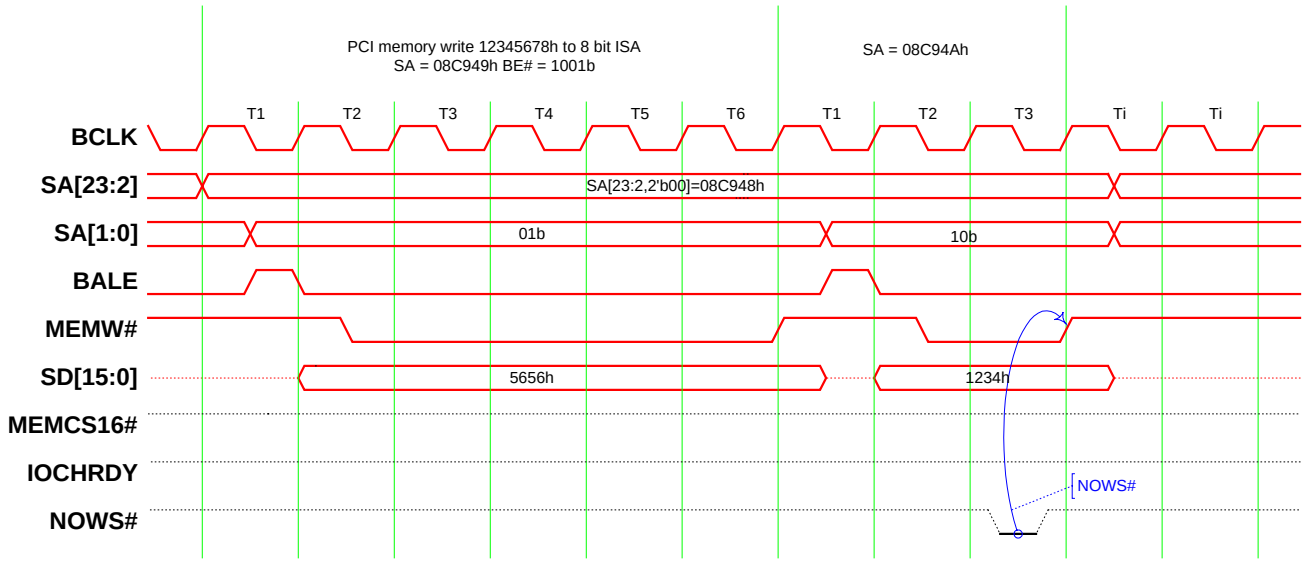


Figure 7-12. PCI Memory Write to 8-bit ISA Device

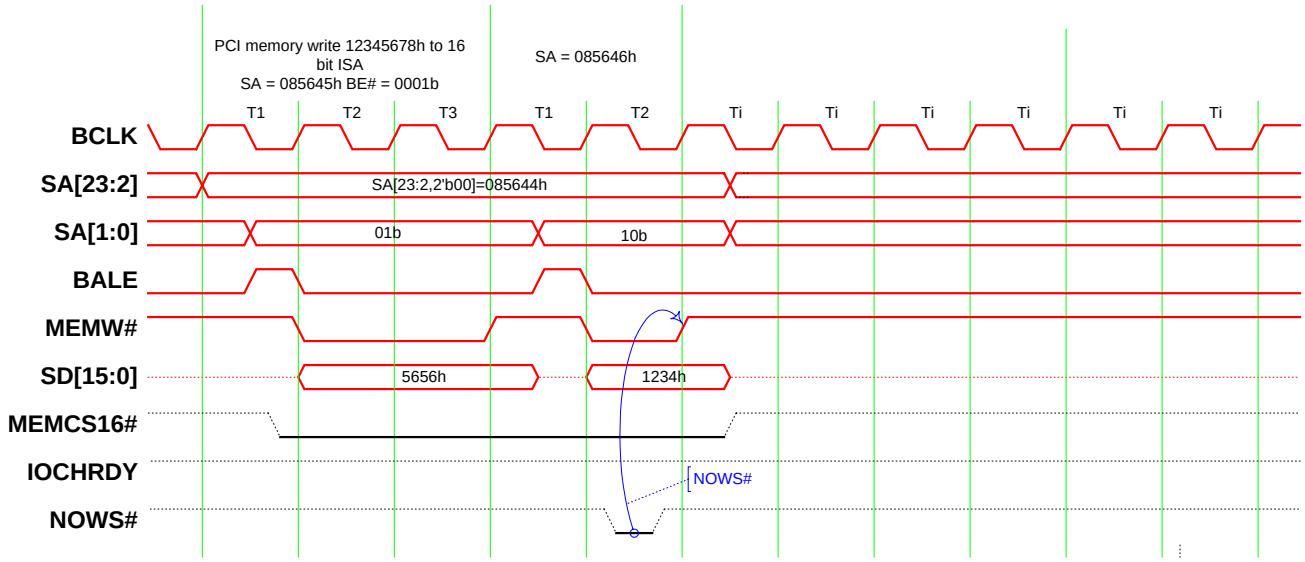


Figure 7-13. PCI Memory Write to 16-bit ISA Device

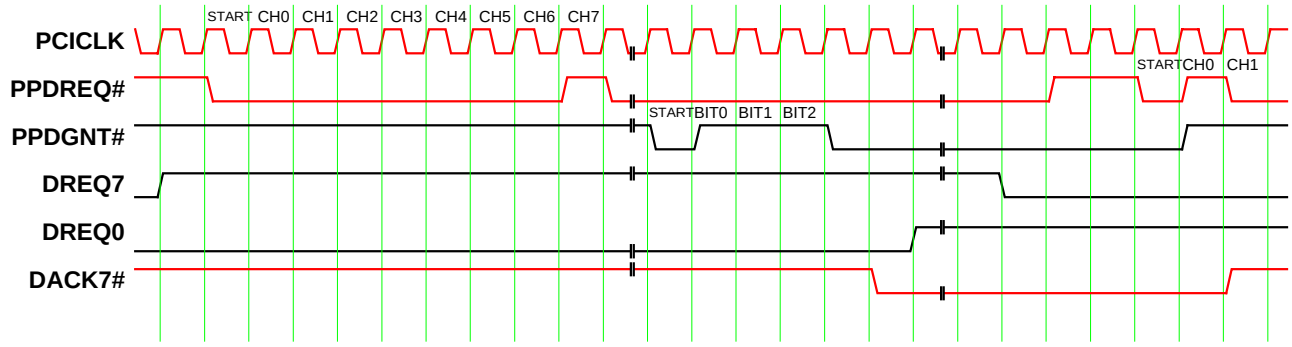


Figure 7-14. DREQn/DACKn# Coding in PC/PCI DMA Function

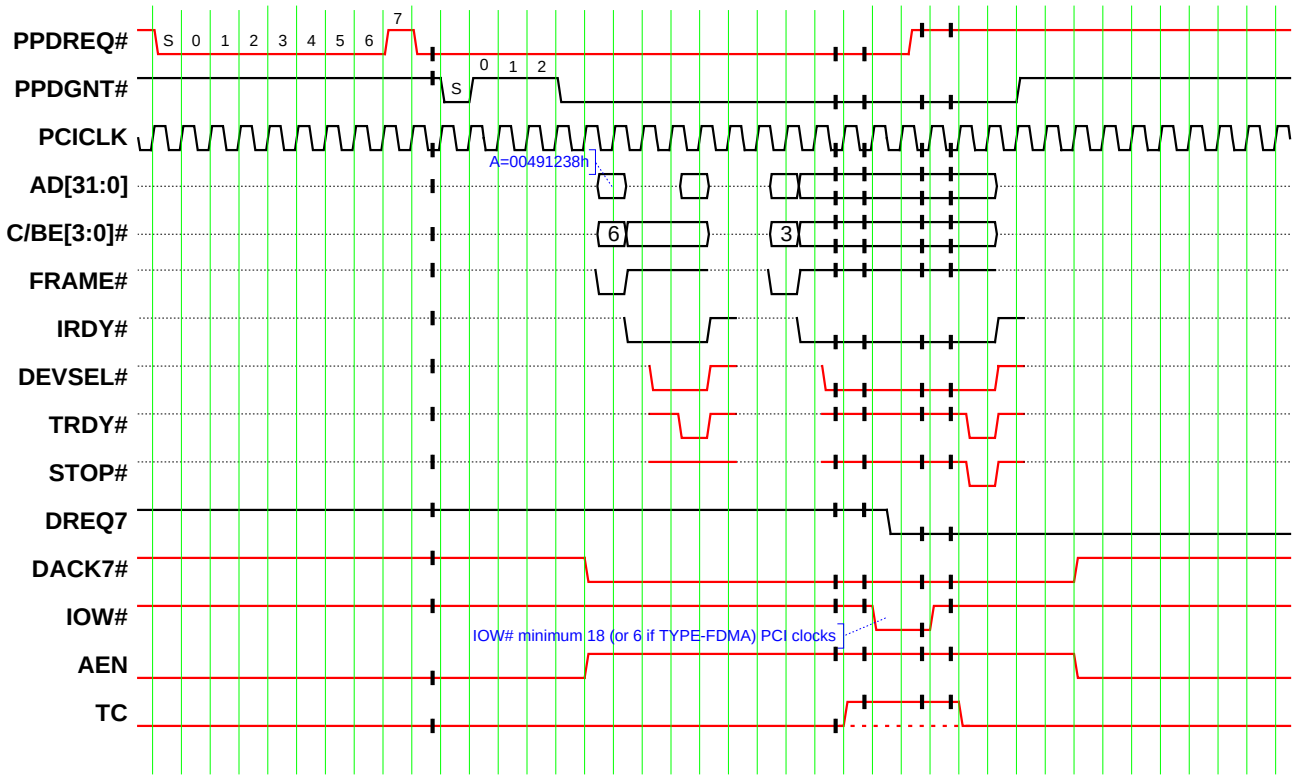


Figure 7-15. DMA Read Operation in PC/PCI DMA (Memory Access to PCI with TC)

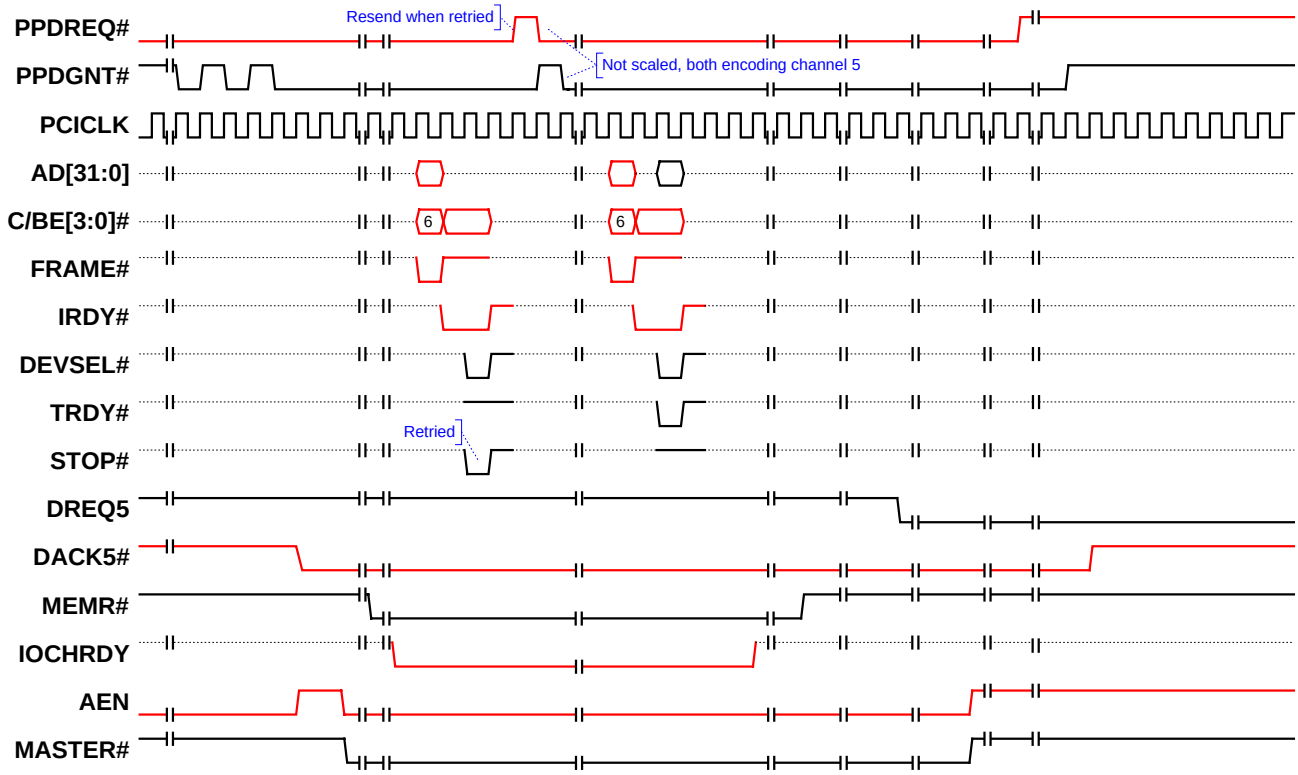


Figure 7-16. ISA Master Memory Read from PCI in PC/PCI DMA (Retried and Normal Termination)

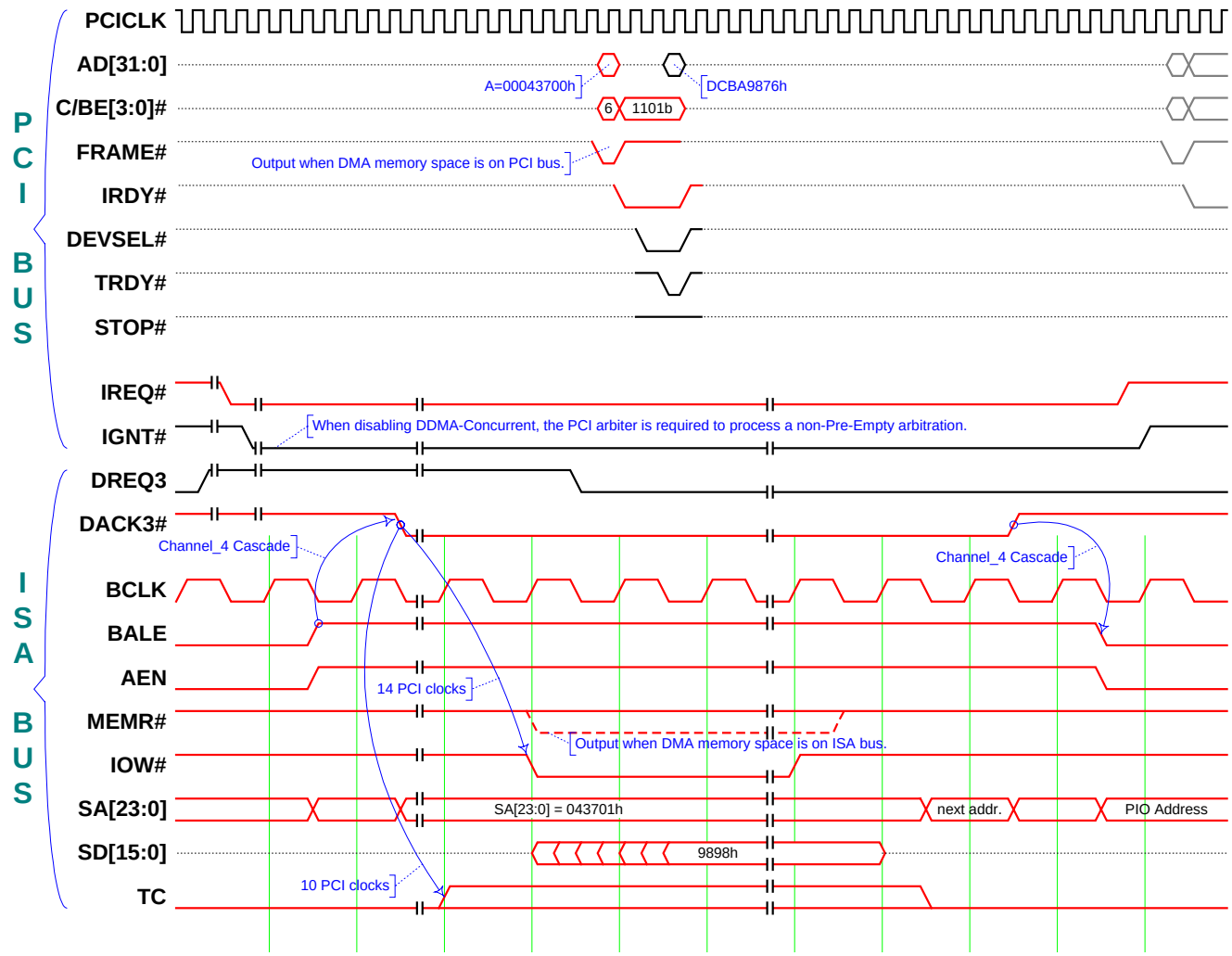


Figure 7-17. DMA Read Operation in DDMA (Memory Access to PCI when DDMA-Concurrent is disabled.)

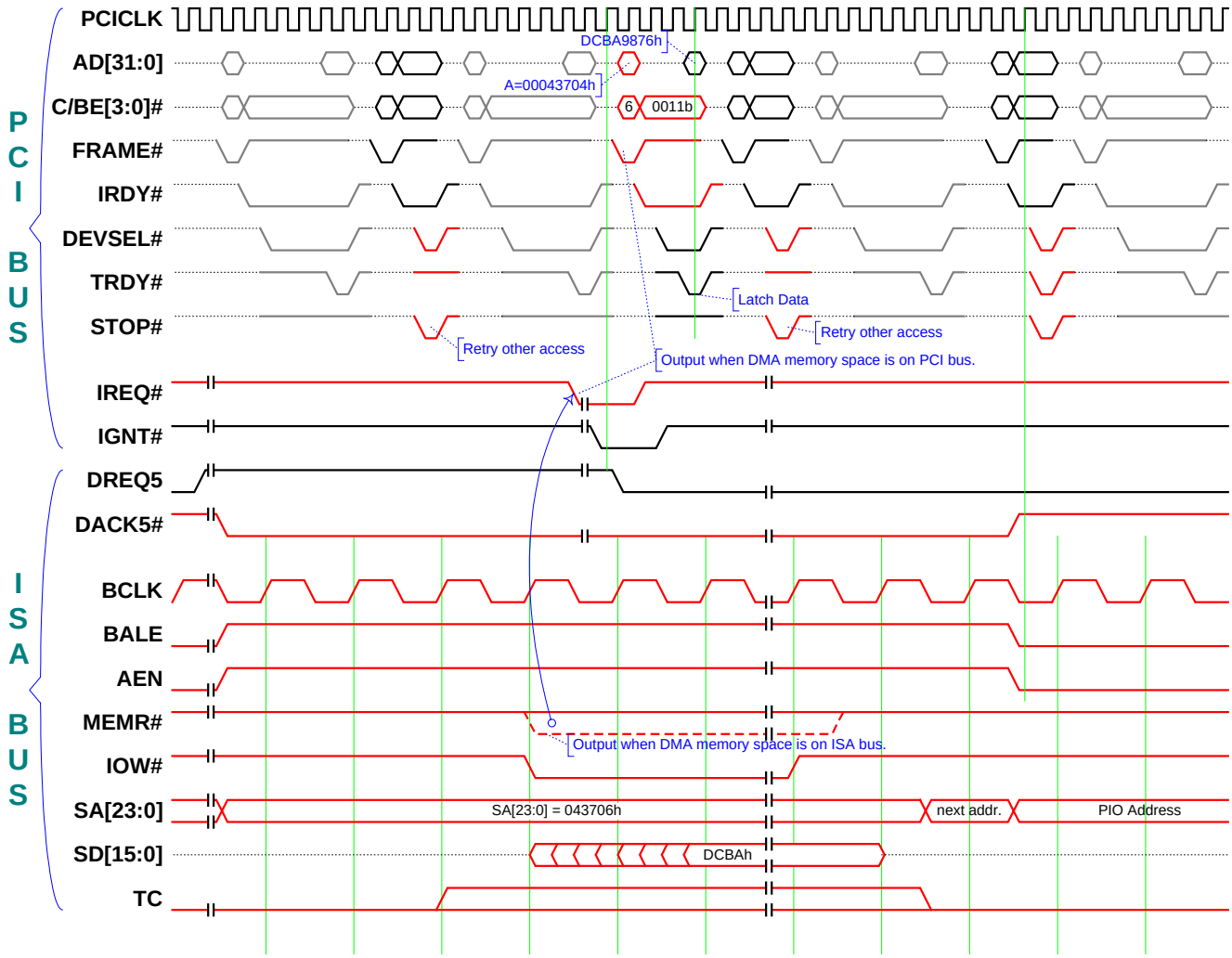


Figure 7-18. DMA Read Operation in DDMA (Memory Access to PCI when both Delayed-Transaction and DDMA-Concurrent are enabled.)

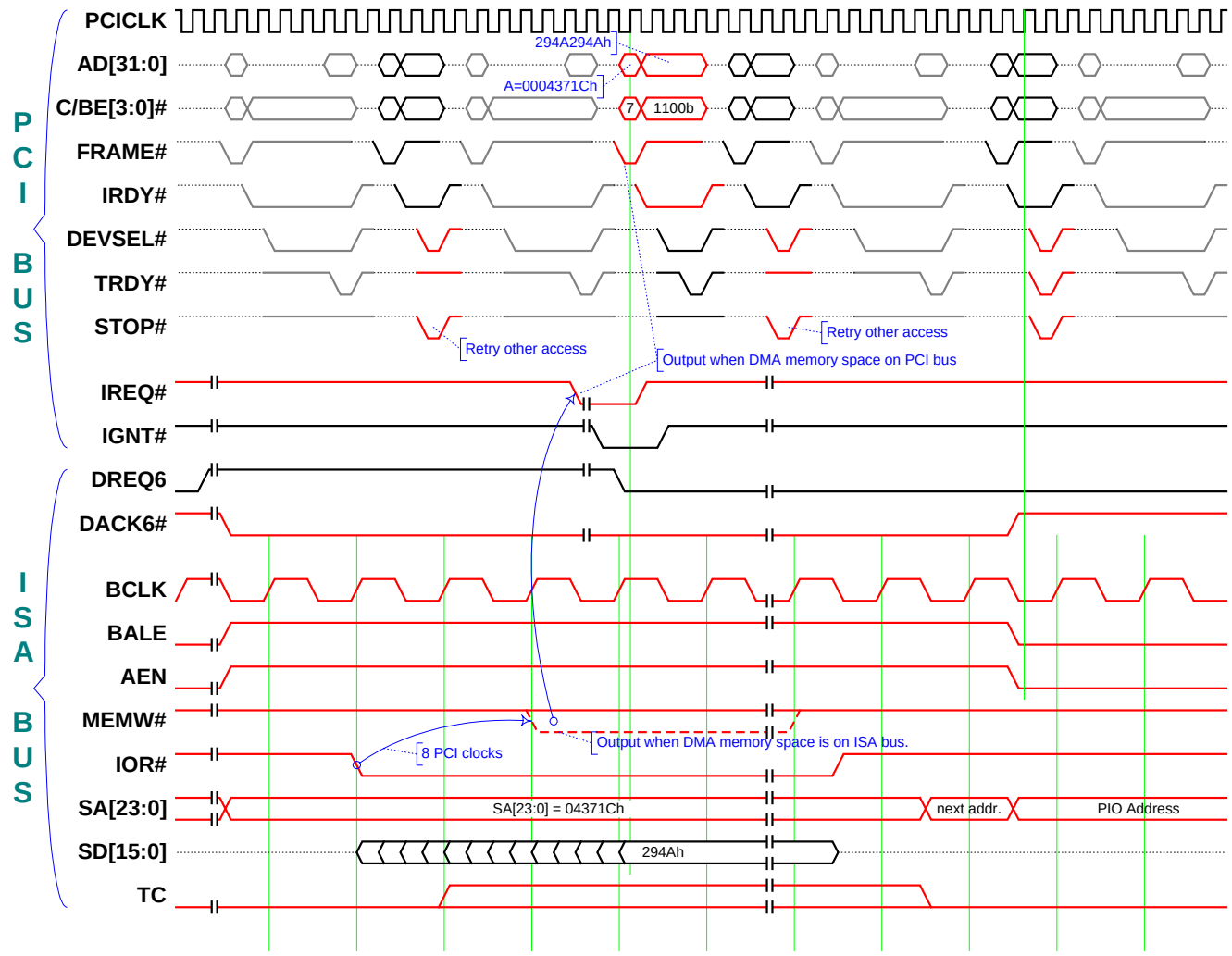


Figure 7-19. DMA Write Operation in DDMA (Memory Access to PCI when both Delayed-Transaction and DDMA-Concurrent are enabled.)

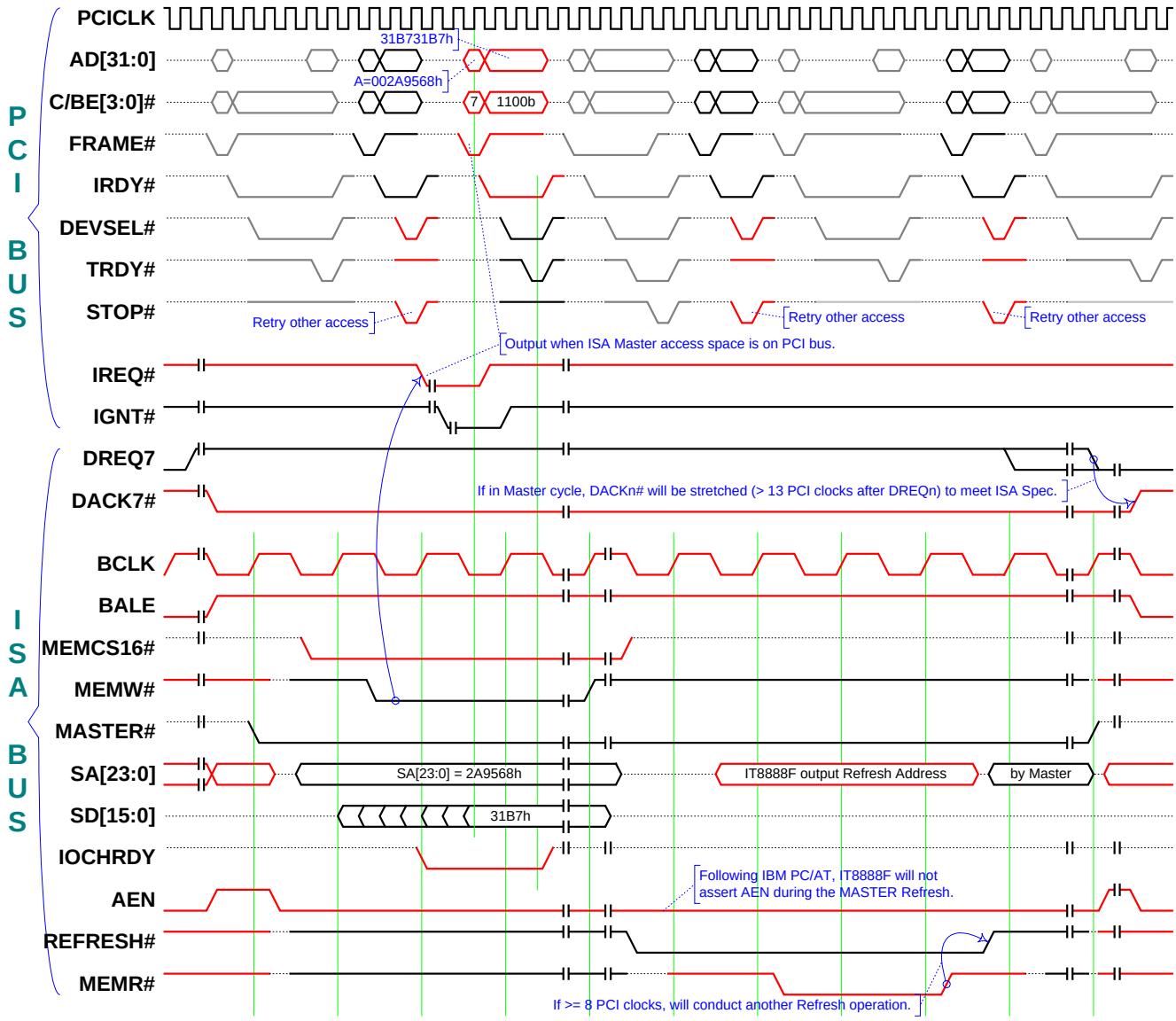


Figure 7-20. ISA Master Write and Master-Initiated-Refresh Operation in DDMA (Memory Access to PCI when both Delayed-Transaction and DDMA-Concurrent are enabled.)

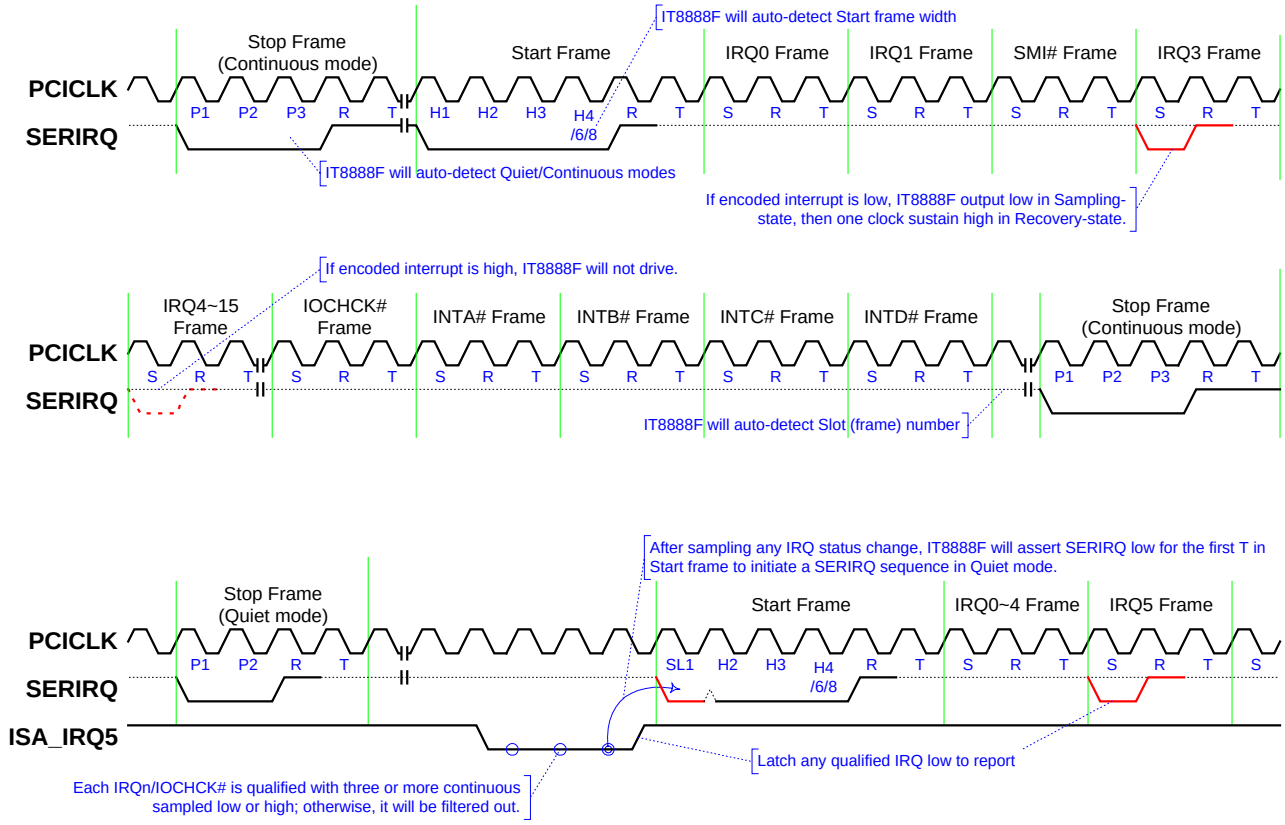


Figure 7-21. Serialized IRQ Coding

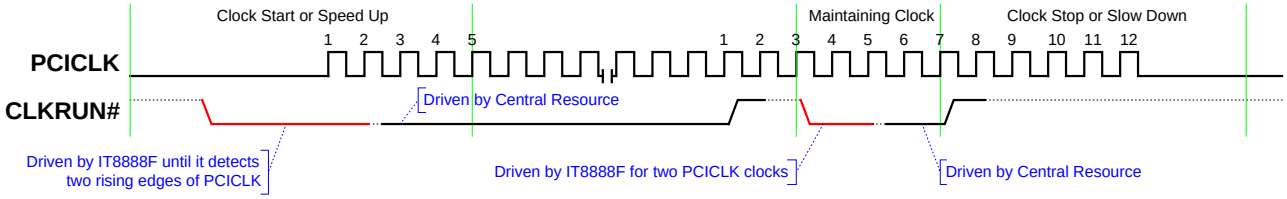


Figure 7-22 CLKRUN# Operation

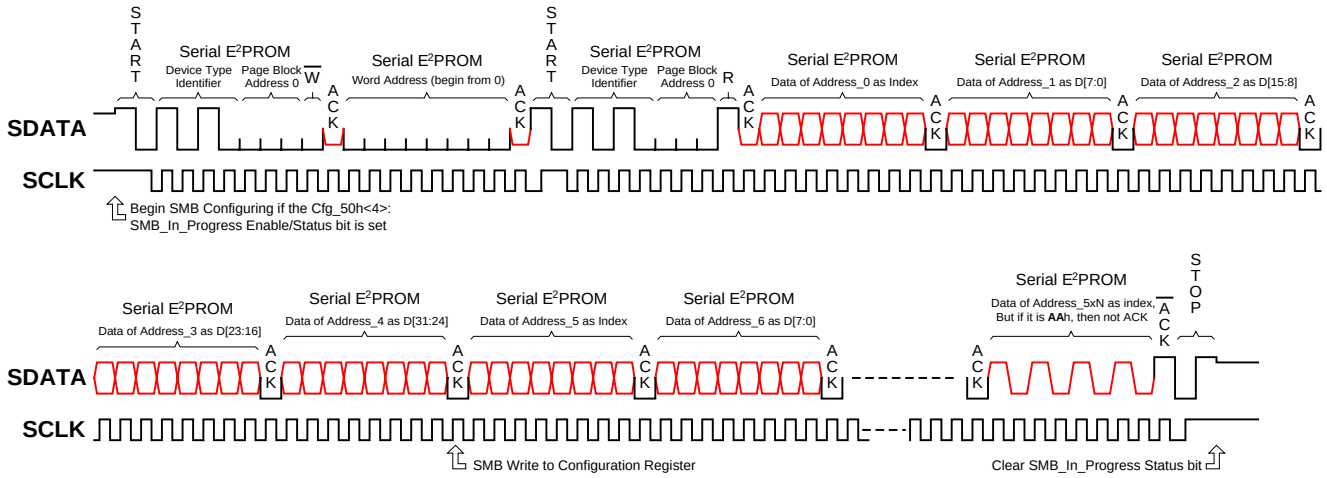


Figure 7-23. SMB Serial E²PROM Configuration Programming

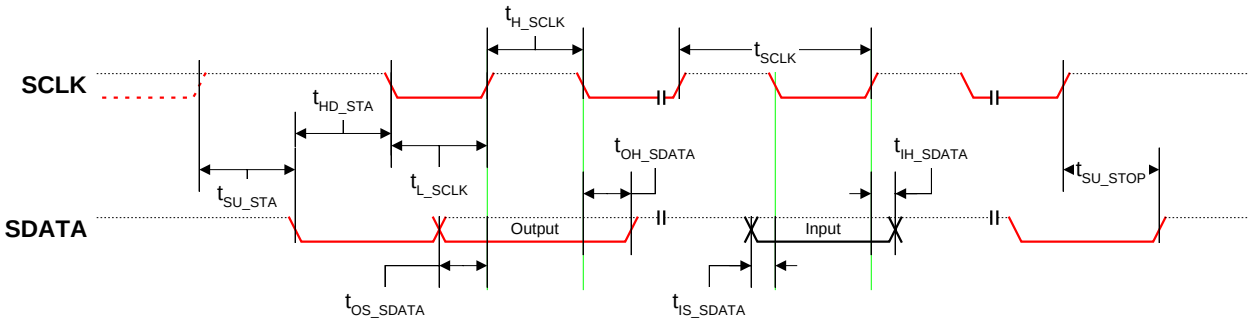
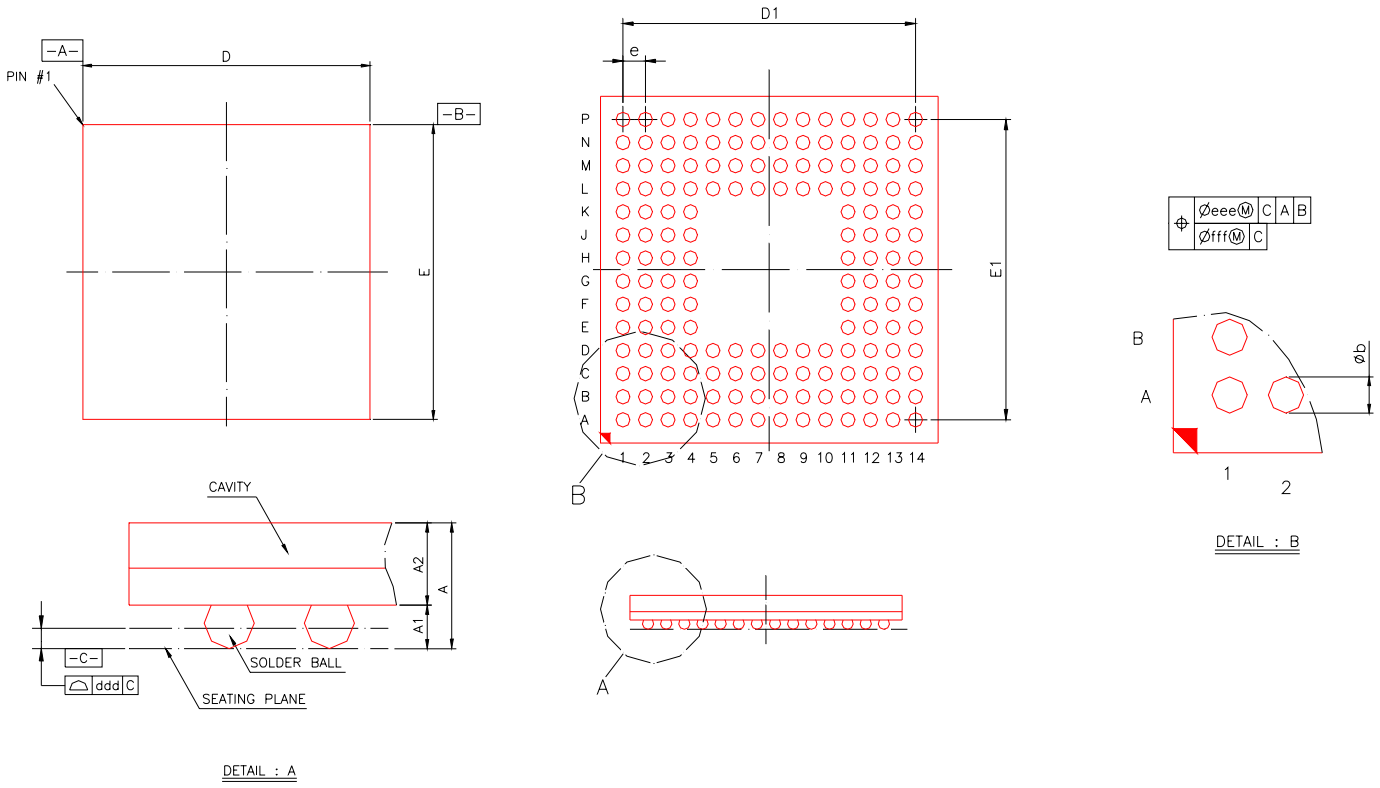


Figure 7-24 SMB Serial E²PROM Interface Timing

8. Package Information

TFBGA 160(12*12) Outline Dimensions **unit: inches/mm**



Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	--	--	1.40	--	--	0.055
A_1	0.25	0.30	0.35	0.010	0.012	0.014
A_2	0.80	0.89	0.98	0.031	0.035	0.039
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	10.40 BSC			0.409 BSC		
E1	10.40 BSC			0.409 BSC		
e	0.80 BSC			0.031 BSC		
b	0.35	0.40	0.45	0.014	0.016	0.018
ddd	0.2			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	14/14			14/14		

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.
2. REFERANCE DOCUMENT: JEDEC MO-205
3. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

DI-TFBGA160(12*12)v0

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9. Ordering Information

Part No.	Package
IT8888G	160 TFBGA

ITE also provides lead-free component. Please mark " -L " at the end of the Part No. when the parts ordered are lead-free.