CMM5104

Radiation Hardened, High Reliability, CMOS/SOS 4096 Word by 1-Bit LSI Static RAM

November 1995

Features

- **Radiation Hardened to 10K RAD (Si)**
- **SEP Effective LET No Upsets: >100 MEV-cm^2/mg**
- **Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/ Bit-Day (Typ)**
- **Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s**
- **Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse**
- **Latch-Up Free Under Any Conditions**
- **Fully Static Operation**
- **Single Power Supply 4.5V to 6.5V**
- **All Inputs and Outputs TTL Compatible**
- **Three-State Outputs**
- **Industry Standard 18 Pin Configuration**
- **Fast Access Time tAVQV = 200ns**
- **Low Standby and Operating Power**

Description

The CMM5104 is a high reliability 4096 word by 1-bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable.

CMOS/SOS technology permits operation in radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single event upset caused by cosmic rays or heavy ions.

TTL compatibility on all input and output terminals permits easy system integration. The data out signal has the same polarity as the input data. A separate data input and a separate Three-state output are used.

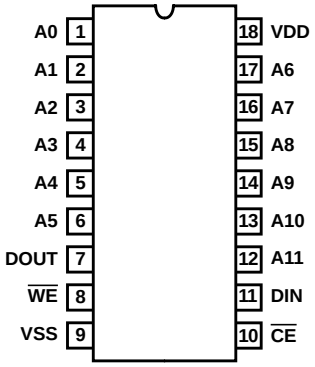
The CMM5104 is supplied in 18 lead dual-in-line sidebrazed ceramic package (D suffix). The part is also available in a 24 lead flatpack ceramic package (K suffix).

Ordering Information

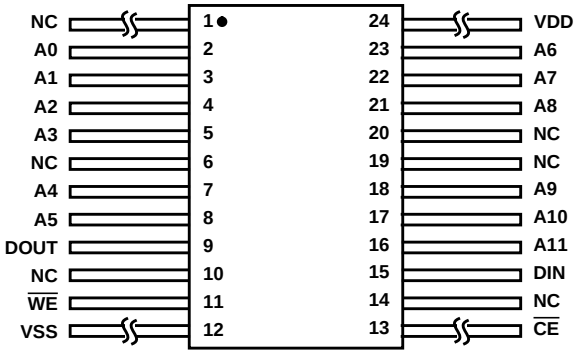
PART NUMBER	TEMP RANGE	PACKAGE
CMM5104K3	-55^{o}C to +125^{o}C	Class B, 24 Lead Ceramic Flatpack (Not Rad Verified)
CMM5104D3	-55^{o}C to +125^{o}C	Class B, 18 Lead SBDIP (Not Rad Verified)
CMM5104K1DZ	-55^{o}C to +125^{o}C	Class S, 24 Lead Ceramic Flatpack (Rad Verified)
CMM5104D1DZ	-55^{o}C to +125^{o}C	Class S, 18 Lead SBDIP (Rad Verified)
CMM5104D/Sample	25^{o}C	18 Lead SBDIP
CMM5104K/Proto	-55^{o}C to +125^{o}C	24 Lead Ceramic Flatpack

Pinouts

18 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835, CDIP2-T18
TOP VIEW

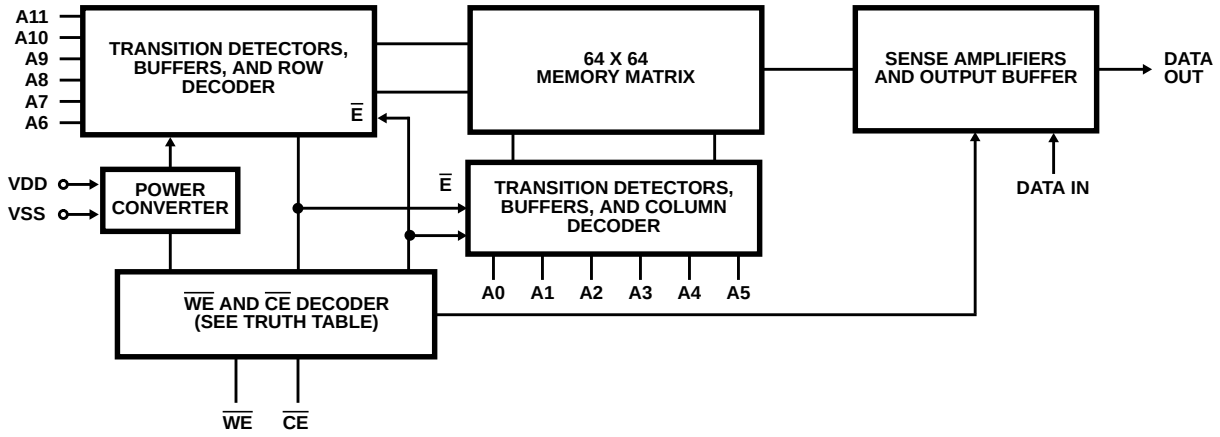


24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835, CDFP4-F24
TOP VIEW



Spec Number **518736**
File Number **3406.1**

Functional Diagram



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT
H	X	Not Selected	High Z
L	L	Write	High Z
L	H	Read	Data Out

Absolute Maximum Ratings

Supply Voltage (VDD),
All voltage values referenced to VSS terminal . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5 to VDD +0.5V
Input Current, Any One Input . . . . . ±10mA
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C
Typical Derating Factor. . . . . 3.0mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	78°C/W	18°C/W
Ceramic Flatpack Package	80°C/W	20°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 0.64W
Ceramic Flatpack Package 0.63W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . . 12.8mW/°C
Ceramic Flatpack Package . . . . . 12.5mW/°C
Gate Count . . . . . 5400 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +6.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VDD/2 to VDD
Data Retention Supply Voltage 2.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Quiescent Device Current	IDD	VIN = 0V or VDD, VDD = 5.25V	-	0.1	-	1.0	mA
Operating Device Current (Note 2)	IOPER	Cycle Time = 1µs, VDD = 5.25V	-	4.5	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs, VDD = 5.25V	-	0.1	-	1.0	mA
Output Low Drive (Sink) Current	IOL	VOUT = 0.4V, VDD = 4.75V	4.0	-	2.5	-	mA
Output High Drive (Source) Current	IOH	VOUT = VDD - 0.4V, VDD = 4.75V	-3	-	-2	-	mA
Input Low Voltage (Note 3)	VIL	VDD = 4.75V	-	0.8	-	0.8	V
Input High Voltage (Note 3)	VIH	VDD = 4.75V	VDD/2	-	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD, VDD = 5.25V	-	±2	-	±10	µA
Three-State Output Leakage Current	IOZ	Applied Voltage = 0V or VDD, VDD = 5.25V	-	±5	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR	VDD = VDR	-	40	-	400	µA

NOTES:

1. VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified.
2. Operating current measured using 1MHz cycle and CL = 50pF.
3. Measured using 1MHz cycle.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

PARAMETER	SYMBOL	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
READ CYCLE TIMES						
Read Cycle	tAVAV	200	-	250	-	ns
Access from Address	tAVQV	-	200	-	250	ns
Access from $\overline{CE}$	tELQV	-	220	-	280	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	200	-	250	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1) **(Continued)**

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Write Pulse Width (Note 2)	tWLWH	125	-	145	-	ns
Address Set Up to Beginning of Write	tAVWL	0	-	0	-	ns
Address Set Up to End of Write	tAVWH	160	-	205	-	ns
Address Hold Time	tWHAV	40	-	45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	160	-	205	-	ns
$\overline{CE}$ Pulse Width (Note 1)	tELEH	180	-	220	-	ns
Data to Write Set Up Time	tDVWH	100	-	120	-	ns
Data Hold From Write	tWHDX	5	-	10	-	ns

NOTES:

1. VDD = 4.75V.
2. $\overline{CE}$ and $\overline{WE}$ must overlap at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Output Voltage Low Level	VOL	-	0.1	-	0.1	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.1	-	V
Input Capacitance (Note 2)	CIN	-	5	-	5	pF
Output Capacitance (Note 2)	COUT	-	7	-	7	pF
Output Hold From Address	tAVQZ	-	80	-	100	ns
Output Hold From $\overline{CE}$	tEHQZ	-	80	-	100	ns

NOTE:

1. Parameters in this table are not directly 100% tested, but are characterized at initial design and after design or processing changes affecting these parameters.
2. Capacitance measurements are made with no bias applied.

TABLE 4. POST 10K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VDD = 5.25V	-	1.0	mA
Operating Device Current (Note 1)	IOPER	Cycle Time = 1µs, VDD = 5.25V	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs, VDD = 5.25V	-	1.0	mA
Output Low Drive Current (Sink)	IOL	VOUT = 0.4V, VDD = 4.75V	2.5	-	mA
Output High Drive Current (Source)	IOH	VOUT = VDD - 0.4V, VDD = 4.75V	2.0	-	mA
Input Low Voltage (Note 2)	VIL	VDD = 4.75V	-	0.8	V
Input High Voltage (Note 2)	VIH	VDD = 4.75V	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD, VDD = 5.25V	-	±10	µA
Three-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD, VDD = 5.25V	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2.5	V
Data Retention Quiescent Current	IDDDR	VDD = VDR	-	400	µA

TABLE 4. POST 10K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C MIN	LIMITS POST RADIATION +25°C MAX	UNITS
Read Cycle	tAVAV	VDD = 4.75V	250	-	ns
Access from Address	tAVQV	VDD = 4.75V	-	250	ns
Access from $\overline{CE}$	tELQV	VDD = 4.75V	-	280	ns
Write Cycle	tAVAV	VDD = 4.75V	250	-	ns
Write Pulse Width (Note 3)	tWLWH	VDD = 4.75V	145	-	ns
Address Set Up to Beginning of Write	tAVWL	VDD = 4.75V	0	-	ns
Address Set Up to End of Write	tAVWH	VDD = 4.75V	205	-	ns
Address Hold Time	tWHAV	VDD = 4.75V	45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	VDD = 4.75V	205	-	ns
$\overline{CE}$ Pulse Width (Note 3)	tELEH	VDD = 4.75V	220		ns
Data to Write Set Up Time	tDVWH	VDD = 4.75V	120	-	ns
Data Hold From Write	tWHDX	VDD = 4.75V	10	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Measured using 1MHz cycle.
3. Operating current measured using 1MHz cycle and CL = 50pF.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IOL	-15% of 0 hr. value
Output High Drive Current (Source)	IOH	-15% of 0 hr. value
Three-State Output Leakage Current	IOZ	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-IRZ SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9
Group E, Subgroup 2		Samples/5005	1, 7, 9	N/A

Intersil - 3Z Product Flow

Radiation Verification (Each Wafer) Method 1019, 10K RADS (Si) Total Dose 2 Samples/Wafer, 0 Reject (3Z Product Flow continues below)

Intersil Space Level Product Flow -3 (Without Radiation Verification)

100% Internal Visual Inspection, Method 2010, Condition B or Alternate Condition B

100% Internal Visual Inspection, Method 2010, Condition B or Alternate Condition B

100% Temperature Cycle, Method 1010, Condition C

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% Fine/Gross Leak, Method 1014

100% Initial Electrical Test, +25^{o}C

Optional High Temperature Stress, 48 Hours at +125^{o}C (This is a Intersil option)

Optional Interim Electrical Test. (Only if the high temperature Stress was performed at Intersil' option.) 10% PDA

100% Static Burn-In, Method 1015, Condition A or B, 160 hours minimum, +125^{o}C minimum (or equivalent time/temperature per Method 1015)

100% Interim Electrical Test, 5% PDA, 3% PDA functional (Note 1)

100% Final Electrical Tests

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Data Package Generation (Note 3)

NOTES:

1. Failures from subgroups 1 and 7 are used for calculating PDA. The maximum allowable PDA is 5%.
2. Alternate Group A testing as allowed by MIL-STD-883, Method 5005 may be performed.
3. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Intersil Space Level Product Flow -IDZ

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer), 2 Samples/Wafer, 0 Rejects

Sample - Die Shear Monitor, Method 2019 or 2027

Sample - Wire Bond Monitor, Method 2011

100% Nondestructive Bond Pull, Method 2023

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% Serialization

100% Initial Test

Optional High Temperature Stress Test, 48 Hours at +125^{o}C (This is a Intersil option)

Optional Interim Electrical Test (T0) (Only if the high temperature stress test was performed.) 10% PDA (Note 1)

100% Static Burn-In 1, Condition A or B, 24 hours minimum, +125^{o}C minimum (or equivalent time/temperature), Method 1015

100% Interim Electrical Test (T1) and Deltas (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 Hours Minimum, +125^{o}C minimum, (or equivalent time/temperature), Method 1015

100% Interim Electrical Test (T2) and Delta (T0-T2) (Note 2 and 3)

100% Dynamic Burn-In, Condition D, 240 hours at 125^{o}C (or equivalent time/temperature), Method 1015

100% Interim Electrical Test (T3). 5% PDA All failures, Deltas (T0-T3) (Note 3)

100% Final Test, Method 5004

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 4)

100% External Inspection, Method 2009

Sample - Group A, Method 5005 (Note 5)

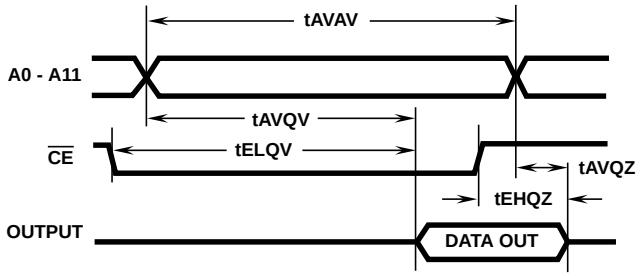
100% Data Package Generation (Note 6)

NOTES:

1. If the optional 48-hour Stress Test is not utilized, then the initial test is used for T0 reference when calculating deltas.
2. Failures from Interim Electrical Tests T1 and T2 are combined for determining PDA.
3. Failures from subgroups 1, 7, and deltas are used for calculating PDA. The maximum allowable PDA is 5% with no more than 3% from subgroup 7.
4. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004. Per Method 5004.
5. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
6. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, RAD Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

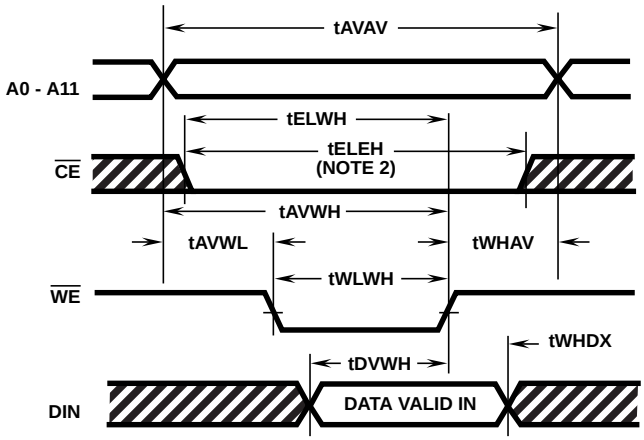
Timing Waveforms

READ CYCLE



NOTE: Timing measurement is referenced to VDD/2.

WRITE CYCLE



NOTES:

1. Timing measurement is referenced to VDD/2.
2. $\overline{CE}$ and $\overline{WE}$ must overlap for at least TWLWH minimum value, tDVWH minimum value must occur during this overlap.

Typical Performance Curves

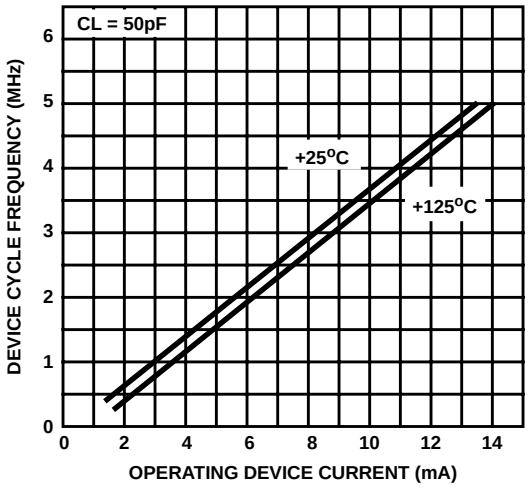


FIGURE 1. TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF CYCLE FREQUENCY

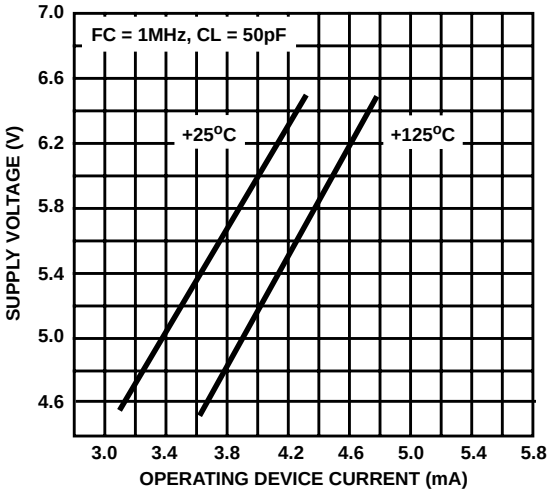


FIGURE 2. TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF SUPPLY VOLTAGE

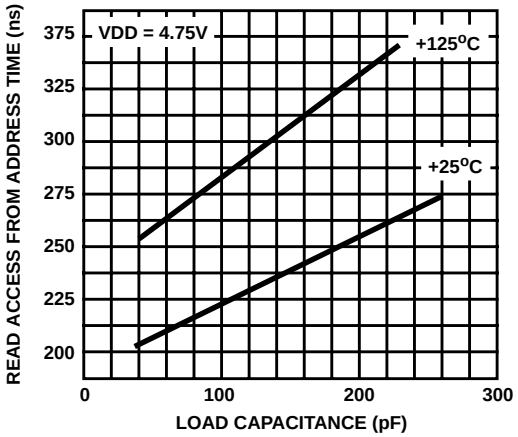
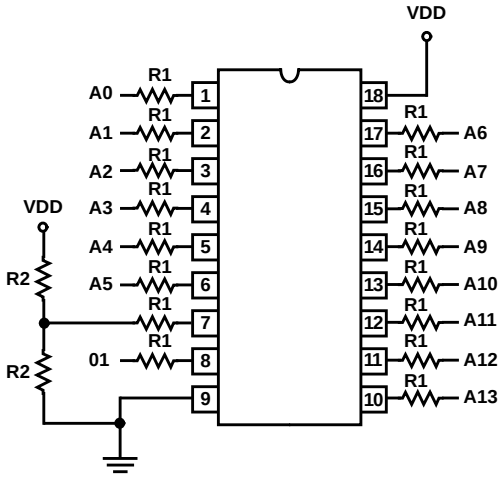


FIGURE 3. READ ACCESS FROM ADDRESS TIME (tAVQV) AS A FUNCTION OF LOAD CAPACITANCE (TIME MEASUREMENTS MADE AT 50% VDD POINT)

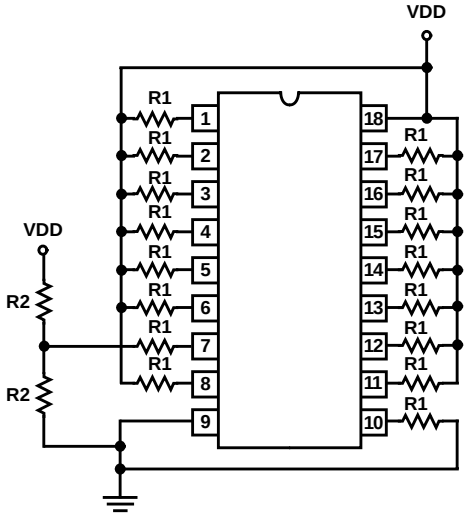
Burn-In Circuits



DYNAMIC CONFIGURATION

NOTES:

R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kW ± 5%
VDD = 5.5V (Min)
VIN = 0V, VDD
Frequency: A0 = 100kHz ± 5%; A1 = A0/2 . . . . A13 = A12/2
01 = 200kHz ± 5%, 0.6µs Low, 4.4µs High
Ceramic DIP biasing shown.

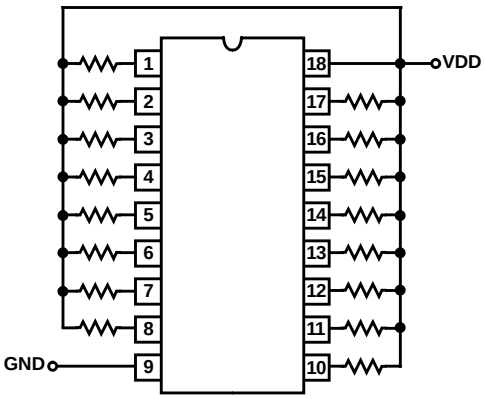


STATIC CONFIGURATION

NOTES:

R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kΩ ± 5%
VDD = 5.5V (Min)
Static Burn-In 1 memory array pre-initialized with all Highs at VDD, VIN = VDD
Static Burn-In 2 memory array pre-initialized with all Lows at VSS, VIN = VSS
Ceramic DIP biasing shown.

Irradiation Circuit



NOTES:

VDD = +5V, +5%
GND = 0V
All Resistors are 47kΩ ± 5%

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