PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC *PMC-Sierra, Inc.*

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

PM4318

OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE

TECHNICAL OVERVIEW

PRELIMINARY

ISSUE 1: APRIL 2001

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

REVISION HISTORY

Issue No.	Issue Date	Details of Change
Issue 1	Dec 2000	Document created
Issue 2	Apr 2001	Updated application drawings. Added monitor mode section.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654　　　　*ISSUE 2*

PMC-Sierra, Inc.

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

CONTENTS

LIST OF FIGURES

1   OCTLIU DEVICE OVERVIEW

The PM4318 OCTLIU is an octal T1/E1/J1 line interface unit that is ideal for use in long haul and short haul T1, J1 and E1 systems. It is available in a 288-pin 23mm x 23mm BGA package and implemented using low power 1.8/3.3V CMOS technology with 3.3V tolerant inputs. The OCTLIU is a versatile and feature rich device that provides enhanced diagnostics, standards compliance and a scaleable solution to meet the demands of high-density communication equipment.
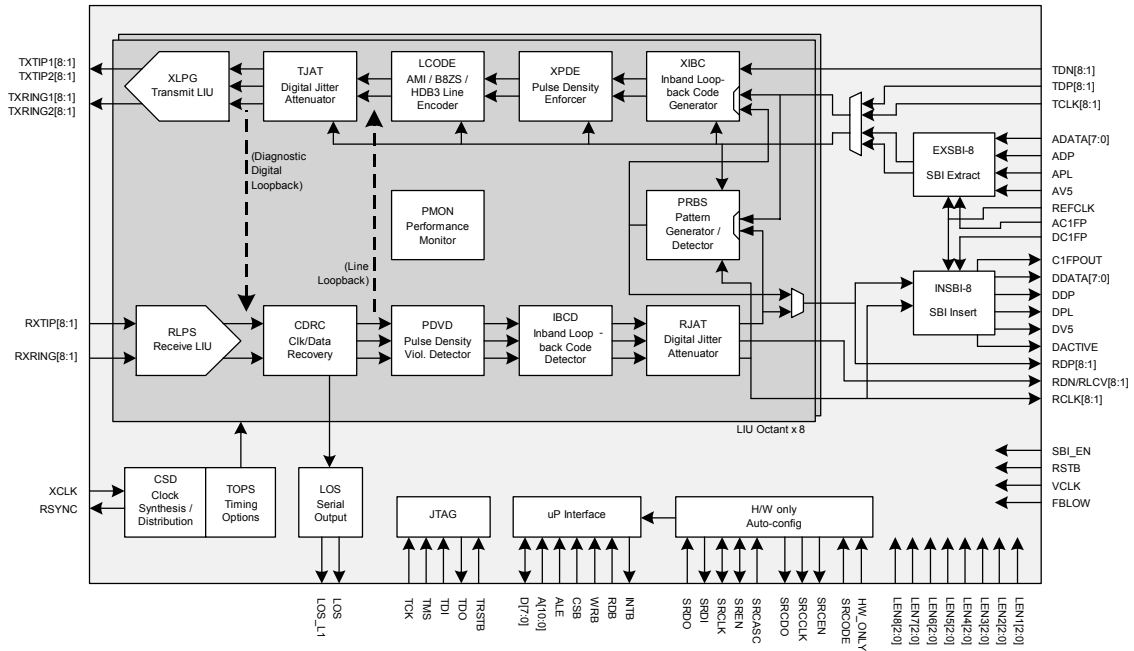
This document will answer the following questions:

- What are the competitive and system-level advantages of using the OCTLIU?

- Why is the OCTLIU ideal for high-density applications?

- What PMC-Sierra products and other components interwork with the OCTLIU?

A block diagram of the OCTLIU is shown in Figure 1.

This document provides an overview of the OCTLIU. A complete description of this device is contained in PMC-2001578, *OCTLIU Datasheet.* In the event that there are contradictions between this document and the datasheet, the datasheet takes precedence.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

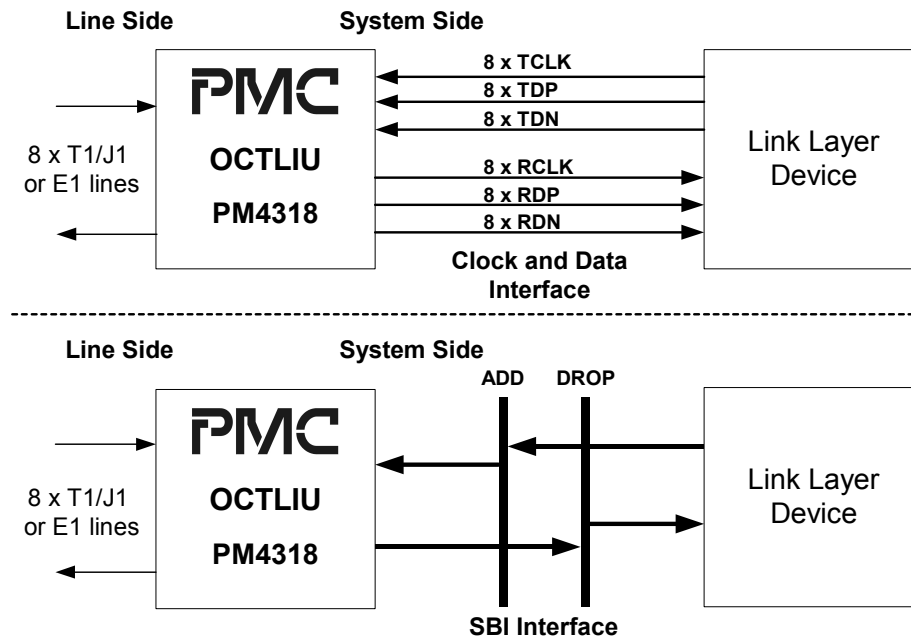## Figure 1 – Block Diagram

1.1 System interface

The OCTLIU supports two system interface configurations, which are selectable on a per-device basis:

- Clock and Data Interface

- Scaleable Bandwidth Interconnect (SBI)

Figure 2 provides a block level illustration of the system interface configurations, which are further described in the sections 1.1.1 and 1.1.2.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

Figure 2 – System Interface Configurations

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

1.1.1 Clock and Data Interface Mode

When configured in the Clock and Data Interface Mode, the OCTLIU provides eight serial system links, which consist of clock, positive data and negative data signals. Each link is independently configurable in both receive and transmit directions to support either single-rail or dual-rail data. The links can also be configured to sample or update on the falling or rising edge of the clock. When in single-rail mode, the transmit negative data pins (TDN) are ignored and the receive negative data pins (RDN) may be optionally used to signal error conditions on the individual lines.

1.1.2 Scaleable Bandwidth Interconnect (SBI)

The Scaleable Bandwidth Interconnect (SBI) bus interface optimizes system interconnectivity, enabling high-density applications with minimal intercircuit wiring.

The SBI bus is an 8-bit, 19.44 MHz time-division multiplexed bus designed to efficiently and seamlessly interconnect several multiport Layer 1 devices, such as the OCTLIU, to multiple high density Layer 2 devices such as the PM4332 TE32 and PM73122 AAL1gator-32. Including control signals, the SBI bus utilizes a total of 27-pins on the OCTLIU. The maximum number of devices sharing the bus is limited only by the need to meet AC timing requirements. A single SBI bus is capable of transferring both synchronous and asynchronous data up to OC-3 rates, using the SONET/SDH Virtual Tributary (VT) structure to carry T1 and E1 links (up to 84 T1 or 63 E1 links in total.)

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

2 KEY FEATURES OF THE OCTLIU

The OCTLIU offers many distinct advantages to system designers, which reduce board costs and simplify system design:

- Flexibility

- Density

- Enhanced diagnostics

- Jitter management

- Redundancy Support

- Standards Compliance

2.1 Flexibility

The OCTLIU provides a variety of customizable features, allowing designers to tailor the device to meet the specific needs of any T1/J1/E1 long haul or short haul application. With a few software or firmware changes the OCTLIU can be configured for use in any communication market, worldwide. This promotes design reuse and lowers engineering costs, since existing designs can be easily reconfigured for use in new markets.

The OCTLIU provides a digitally programmable line build out (LBO) and an optionally programmable pulse shape that extends up to 5 transmitted bit periods. This provides the ability to modify the transmitted pulse for use in custom applications.

The operation mode is selectable on a per device basis, providing 1.544Mbps or 2.058Mbps operation for T1/J1 or E1 interfaces respectively. Encoding and decoding of B8ZS, HDB3 and AMI line codes are supported.

The OCTLIU provides a flexible and configurable System Interface. Depending on the application, the OCTLIU may be configured in one of two System Interface modes:

- Clock and Data Interface

- Scaleable Bandwidth Interconnect (SBI)

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

The clock and data interface provides eight independently configurable serial links to layer 2 devices at DS1 or E1 line rates while the SBI bus supports multi-device operation up to OC-3 capacity, enabling high-density applications. Further details of these interfaces can be found in sections 1.1.1 and 1.1.2.

The OCTLIU may be controlled, configured and monitored via an 8-bit microprocessor or an SPI-compatible interface, offering access to all internal registers. The use of a microprocessor enables enhanced monitoring and diagnostic functionality while the use of an SPI-compatible PROM or 'hardware-only' mode reduces overall cost and complexity.

In 'hardware-only' mode, a single SPI-compatible serial PROM can be used to configure multiple OCTLIUs simultaneously by connecting the OCTLIUs in a cascade.

An input pin to the OCTLIU, "SRCODE," provides a means to execute the PROM configuration instructions conditionally. Two different configuration sequences can thus be stored in a single PROM (for DS1 or E1 operation, for example) and the SRCODE input is used to select which one will be applied. Different OCTLIU devices in a cascade can have their SRCODE inputs set to different values for maximum flexibility.

The OCTLIU also supplies a recovered clock signal for use in loop-timed system configurations with other devices. The signal is composed of a recovered and de-jittered line rate clock of a selected line interface, providing a 1.544 MHz or 2.048 MHz reference clock. In addition, the signal may optionally be synchronously divided to create an 8kHz reference clock. The source of the recovered clock is configurable to be any one of the eight line interfaces.

2.2   Density

The OCTLIU integrates eight line interface circuits with both long haul and short haul capability into a single chip. It is implemented using low power 1.8/3.3V CMOS technology with 3.3V tolerant inputs and packaged in a high-density 288-pin 23mm x 23mm SBGA package.

When using the clock and data system interface, the OCTLIU seamlessly interconnects to octal framers, SARs, packet processors and line concentrators (M13.) This is a cost-effective two-chip solution for eight port T1/J1 and E1 line cards.

The Scaleable Bandwidth Interconnect (SBI) bus interface optimizes system interconnectivity, enabling higher-density applications. It supports up to an OC-3 capacity of data or an equivalent of 84 T1 or 63 E1 links. The maximum number

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

of devices sharing the bus is limited only by the need to meet AC timing requirements.

Consider a fully utilized SBI bus interface carrying 84 T1 links. A single-rail clock and data interface would require 4 x 84 or 336 wires to support this capacity. Use of the SBI bus interface results in a reduction of 309 interconnecting wires, lowering system costs and power. There is no other system interface available that can offer this level of density, using such minimal circuit interconnection.

The SBI bus interface is a standard feature on many devices in the PMC-Sierra product portfolio. The OCTLIU is able to leverage this existing technology by pairing with high-density counterparts such as the PM5366 TEMAP-84, PM4332 TE32 and PM73122 AAL1gator-32 to create next-generation high-density solutions.

2.3   Enhanced Diagnostics

Carrier-grade access products require the ability to support diagnostic testing. This allows the service provider to conduct line testing and verification during service installation and enables ongoing line quality monitoring. The OCTLIU offers extensive control, test and monitoring functionality.

2.3.1 Error Detection and Insertion

The following errors are detected on each line interface:

- Line Code Violations (LCVs)

- B8ZS/HDB3 line code signatures

- Excessive zeroes violations (defined by HDB3, B8ZS and AMI)

- Loss of Signal (LOS)

- Violations of the ANSI T1.403 12.5% pulse density rule

These errors, either singly or in combination, can selectively generate interrupts to the microprocessor.

For enhanced error analysis, bipolar violations defined by B8ZS, HDB3 or AMI line codes may be inserted into the transmitted data stream. An all-ones transmission is supported to provision Alarm Indication Signaling (AIS). This allows validation of the far-end receive interface by monitoring for proper error detection. Transmission error insertion is enabled via microprocessor control.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

The OCTLIU optionally provides bipolar violation transparent operation for both the transmit and receive interfaces. This feature can be set on a line by line basis by configuring the receive and/or transmit interface to dual-rail (bipolar) mode. When in bipolar violation transparent operation, the OCTLIU allows bipolar violations to pass through the device uncorrected. This enables system-level testing by propagating errors through the OCTLIU to other devices.

Performance monitoring features of the OCTLIU are enabled via microprocessor access to internal counters that accumulate line code violations for each individual line.

The OCTLIU offers reduced error diagnostic capabilities in the hardware only mode. Loss of Signal (LOS) error detection is supported for each line interface via the LOS and LOS_L1 pins. LCV and excessive zero error conditions can also be detected on each line interface by monitoring the RLCV pins when the clock and data interface is used in single-rail mode.
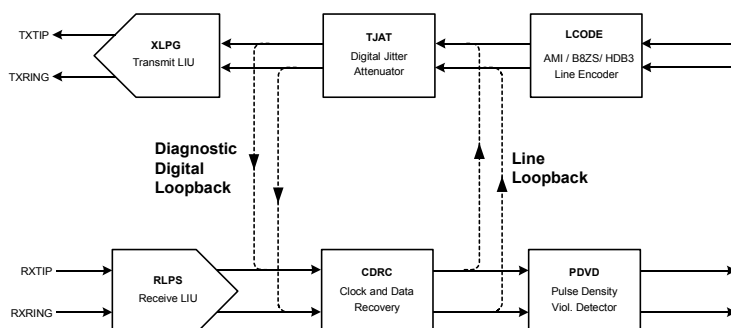
2.3.2 Loopback Testing

The OCTLIU provides two loopback modes to aid in network and system diagnostics:

- Line Loopback

- Diagnostic Digital Loopback

A graphical representation of the loopback modes is illustrated in Figure 3. For a system-level view of loopback operation, refer to the OCTLIU Block Diagram in Figure 1.

Figure 3 – Loopback Modes

Line loopback allows for line quality monitoring and the testing of far-end equipment. Line loopback may be initiated or halted at any time via microprocessor control or upon the detection of an inband loopback code sequence (when present for 5.1 seconds.) The activate and deactivate loopback

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

codes recognized by the OCTLIU are programmable and may range between 3 to 8 bits in length. Each of these codes may selectively be configured to generate an interrupt. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303.

The OCTLIU can also generate a stream of inband loopback code to place far-end devices in loopback mode. The stream of generated data is unframed and consists of a continuous repetition of a user-specified code. The contents of the code and its length are programmable from 3 to 8 bits.   This mechanism further enhances the OCTLIUs diagnostic capabilities.

Diagnostic Digital Loopback enables testing of the system data path through the LIU. It can be initiated at any time via microprocessor control.

2.3.3 PRBS Pattern Generator/Detector

The OCTLIU provides Pseudo Random Binary Sequence (PRBS) generation and detection without the need for additional circuitry. Each line interface on the OCTLIU includes a 32-bit fully programmable PRBS generator and detector as recommended in ITU-T O.151. The pseudo-random sequence is user selectable from $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$ and may be inserted into or detected from a T1 or E1 stream in either the receive or transmit directions.

When used in conjunction with a PRBS capable framer, the OCTLIU provides the ability to isolate errors between the line interface and framer. More importantly, the OCTLIU alone facilitates PRBS testing of unframed data sequences, extending the use of this feature to any application.

2.3.4 JTAG

The OCTLIU supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.

2.4   Jitter Management

The OCTLIU provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter.

Jitter attenuation is provided on both the receive and transmit interfaces using a digital phase locked loop (PLL) and FIFO buffer. The OCTLIU exhibits negligible jitter gain for jitter frequencies below 5.7Hz (7.6Hz for E1), more correctly called wander, and attenuates jitter at frequencies above 5.7 Hz (7.6 Hz for E1) by 20dB per decade.

PMC-Sierra, Inc.

The OCTLIU can accommodate up to 61UI peak to peak of input jitter at jitter frequencies above 5.7Hz (7.6Hz for E1). For jitter frequencies below 5.7Hz (7.6Hz for E1) the tolerance increases 20dB per decade. Figure 4 illustrates the jitter characteristics of the transmit and receive Jitter Attenuation (JAT) blocks.

Figure 4 – JAT Jitter Tolerance
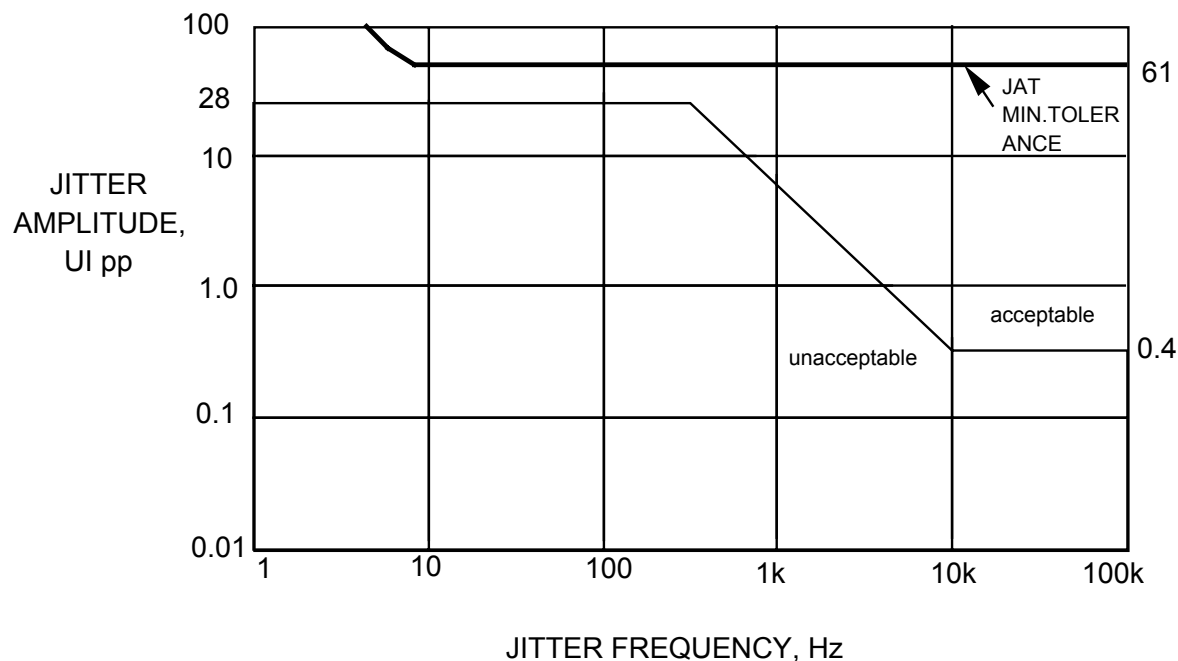
In the absence of input jitter, the output jitter is less than 0.025 UI peak to peak, complying with AT&T TR 62411.

2.5   Redundancy Support

OCTLIU offers built-in circuit protection, and redundancy support for use in applications requiring uninterrupted connectivity.

2.5.1 Monitor Mode

In short-haul applications, the RLPS Equalizer can be programmed in to a monitoring mode. In this mode the receiver is configured to recover signals attenuated by 20dB of inserted resistive (flat) loss. A "Monitor Mode" RLPS Equalizer RAM table is provided in the datasheet.   Any octant can be configured in this mode of operation. This feature is complaint with G.772 non-intrusive protected monitoring points and can be used to provide redundant signal recovery in network equipment.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

PM4318 OCTLIU

ISSUE 2

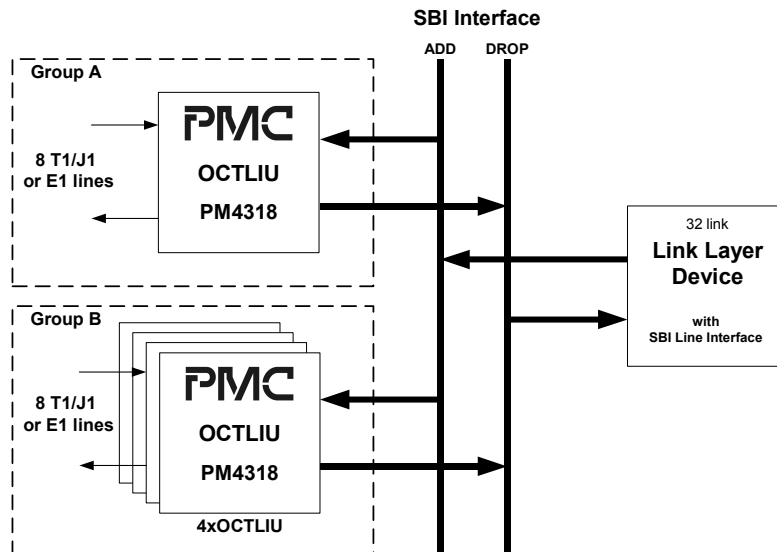*OCTAL T1/E1/J1 LINE INTERFACE DEVICE*

2.5.2 Line Redundancy

OCTLIU can be used to support a working and redundant physical link using a single framing device.

When using the SBI interface, the OCTLIU provides designers with the ability to map physical links to virtual tributaries within the SONET/SDH structure of the bus. This can be performed during system initialization or at any time via microprocessor control. This capability allows designers to 'connect' any line interface of the OCTLIU to any port of a Link Layer device. Line interfaces that are not mapped to a VT are tristated and do not affect the SBI bus. This allows designers to overprovision line interface devices without bus contention issues, provided that no active links are mapped to the same VT. To switch between links, the original link must be unmapped or 'disconnected' before a new link is activated in its place. Thus, in order to provide redundancy, a designer needs only to overprovision the line interface devices and not the link layer device. It is important to note, however, that this form of line switching is not a hitless transition since the link is inactive during the cross-over.

Figure 5 illustrates five OCTLIUs connected to a single SBI bus, sharing a single 32-link, Link Layer Device. For illustration purposes only, the OCTLIUs have been separated into two groups. Group A consists of a single OCTLIU, providing eight redundant links. Group B consists of four OCTLIUs which provide a total of 32 links, coinciding with the maximum number of links that the Link Layer device can support at any given time. If a physical line were broken on any of the active links in Group A, it could be swapped out with any of the links provided in Group B. In practice, *any* of the available line interfaces can be cross-connected with *any* of the link layer ports, provided that no two links are mapped to the same port. The SBI interface, in effect, acts as a low cost analog cross-connect for T1/J1 and E1 interfaces.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC *PMC-Sierra, Inc.*

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

Figure 5 – Redundancy Support

This architecture provides an efficient and cost-effective way to implement physical line protection in short haul or long haul applications. A system designer can overprovision line interface devices to provide redundancy without the need to overprovision framers or other Layer 2 devices.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

2.6   Standards Compliance

The OCTLIU complies to numerous standards and recommendations covered by ANSI, ETSI, ITU-T, AT&T, Bellcore and others. Adherence to these standards results in carrier-grade performance and worldwide interoperability. Please refer to the OCTLIU Data Sheet (PMC-2001578) for a complete listing of applicable standards.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

3   APPLICATION EXAMPLES

The OCTLIU enables the design of low power, high density, long haul and short haul communication systems for use in any market, worldwide.

The OCTLIU mates seamlessly with the PM4388 TOCTL and PM6388 EOCTL using a clock and data interface as shown in Figure 6 .This provides a simple and cost-effective solution to frame eight long haul or short haul T1 or E1 signals using only two chips.

Figure 6 – T1/E1 Framer/Transceiver

Figure 7 – DSLAMs and Wireless Equipment
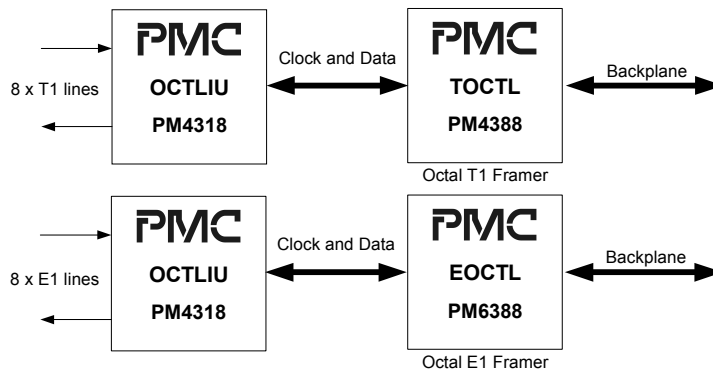
This above configuration can be used in conjunction with the PM7340 IMA-8 to support Inverse Multiplexing for ATM for use in DSLAMs and 3G Wireless Infrastructure Equipment. This is shown in Figure 7.
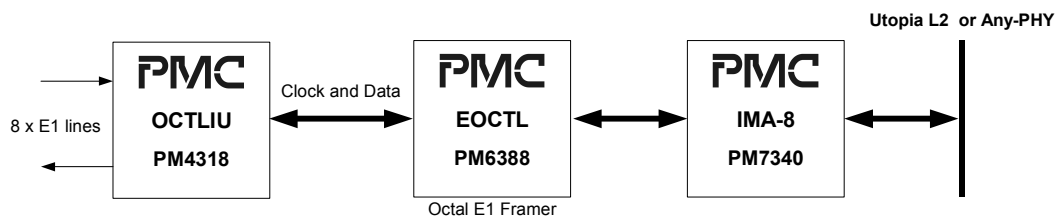
The SBI bus optimizes system interconnection in high-density applications as illustrated in Figure 8. The four OCTLIUs support up to 32 physical T1 or E1 lines, which are all multiplexed onto a single SBI bus operating at 19.44 MHz. The PM4332 TE32 directly interfaces with the OCTLIU via the SBI bus, providing framing for all 32 of the incoming signals.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC *PMC-Sierra, Inc.*

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

## Figure 8 – High Density T1/E1 Framer/Transceiver
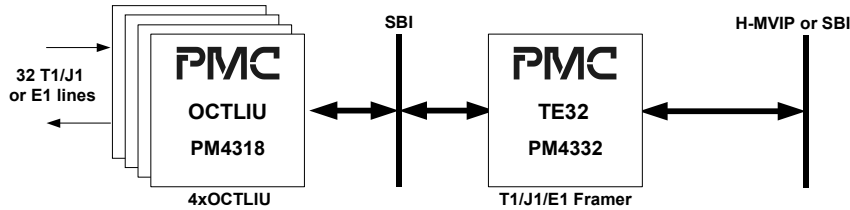
The above configuration can be scaled up to OC-3 capacity. Eleven OCTLIU's and three TE-32's are required to support 84 T1 links. Eight OCTLIU's and two TE-32's are required to support 63 E1 links. Figure 9 illustrates the use of the OCTLIU, TE-32 and PM7384 FREEDM-84 in an IP Edge Router Line card.

Figure 9 – High-Density IP Edge Router Line Card
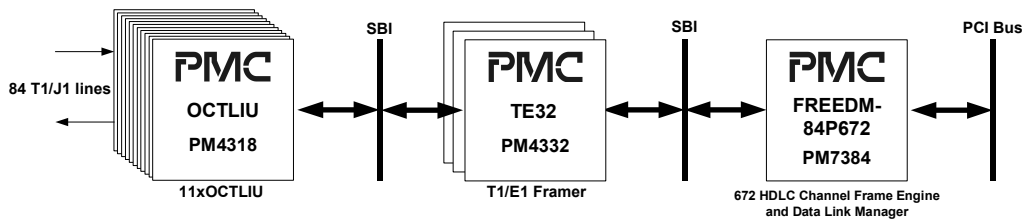
The OCTLIU, in unison with the PM4332 TE32 and PM73122 AAL1gator-32, supports structured AAL1, necessary for voice-switching applications. This is shown in Figure 10.

Figure 10 – Voice Switching Application
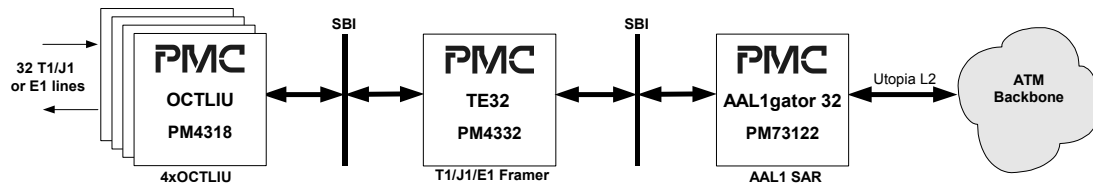
The TE32 may be removed from the above application, resulting in unstructured AAL1 capability that is used in leased line circuit emulation applications. This is illustrated in Figure 11.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

Figure 11 – Leased Line Circuit Emulation
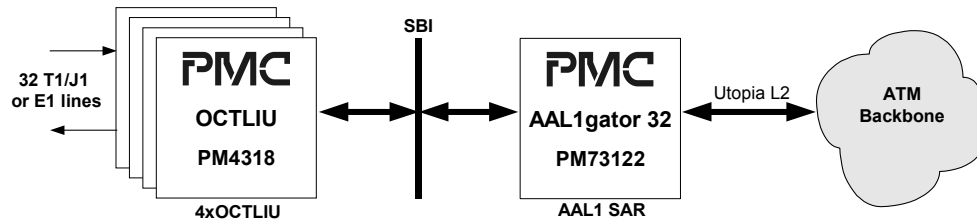
The OCTLIU is ideal for Metro Optical Access Equipment when used in conjunction with the PM5366 TEMAP-84. The TEMAP-84 integrates VT/TU mapping and multiplexing for 84 T1 or 63 E1 channels. In this application, T1 and E1 datastreams are bit asynchronously mapped to VT1.5's and VT2's respectively. This is illustrated in Figure 12.

Figure 12 – Metro Optical Access Equipment
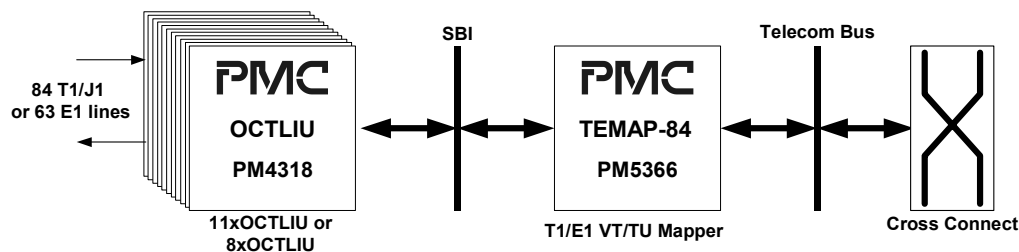
It is important to note that buffering may be required to minimize loading on the SBI bus in high-density configurations. In order to accommodate the space and architectural requirements of high-density designs, the SBI bus may be distributed across a backplane. Care must be taken to ensure that signal integrity is maintained.

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

NOTES

PRELIMINARY

TECHNICAL OVERVIEW

PMC- 2001654

PMC-Sierra, Inc.

ISSUE 2

PM4318 OCTLIU

OCTAL T1/E1/J1 LINE INTERFACE DEVICE

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
                                          (604) 415-4533
Web Site: http://www.pmc-sierra.com