TENTATIVE TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

PSEUDO SRAM AND NAND E^{2}PROM MEMORY MIXED MULTI-CHIP PACKAGE

DESCRIPTION

The TH50VPN5640EBSB is a mixed multi-chip package containing a 32-Mbit(33,554,432)bit pseudo static RAM and a 64-Mbit(69,206,016)bit NAND E^{2}PROM organized as 528bytes x 16pages x 1024blocks.

The power supply for the TH50VPN5640EBSB can range from 2.7 V to 3.1 V The TH50VPN5640EBSB is available in a 69-pin BGA package making it suitable for a variety of applications.

FEATURES

- Power supply voltage
  V_{CCs} = 2.7 V~3.1 V
  V_{CCn} = 2.7 V~3.1 V
- Pseudo SRAM page read operation mode
  Page read operation by 4 words
- Current consumption
  Operating: 30 mA maximum(CMOS level)
  Standby: 70 μA maximum(Pseudo SRAM CMOS level)
  Standby: 100 μA maximum(NAND E^{2}PROM)
- NAND E^{2}PROM Organization
  Memory cell allay 528 × 16K × 8
  Register 528 × 8
  Page size 528 bytes
  Block size (8K + 256) bytes
- NAND E^{2}PROM memory modes
  Read, Reset, Auto Page Program
  Auto Block Erase, Status Read
- NAND E^{2}PROM Mode control
  Serial input/output
  Command control
- Program/Erase Cycles 2.5E5 cycle (with ECC)
- Package
  P-FBGA69-1209-0.80A3:0.31 g (typ.)

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A	NC									NC
B	NC									NC
C	NC		A7	$\overline{LB}$	CLE	$\overline{WE}$ /WE#n	A8	A11		
D		A3	A6	$\overline{UB}$	CE#n	CE2S	A19	A12	A15	
E		A2	A5	A18	ALE	A20	A9	A13	NC	
F	NC	A1	A4	A17			A10	A14	V_{CCn}	NC
G	NC	A0	V_{SS}	DQ1			DQ6	NC	A16	NC
H		WP#n	$\overline{OE}$ /RE#n	DQ9	DQ3	DQ4	DQ13	DQ15	RY/$\overline{BY}$	
J		$\overline{CE1S}$	DQ0	DQ10	V_{CCqn}	VCCs	DQ12	DQ7	V_{SS}	
K			DQ8	DQ2	DQ11	NC	DQ5	DQ14		
L	NC									NC
M	NC									NC

PIN NAMES

A0~A20	Address Inputs
A0 , A1	Page Address Inputs for Pseudo SRAM
DQ0~DQ15	Data Inputs/Outputs
$\overline{CE1S}$, CE2S	Chip Enable Inputs for Pseudo SRAM
CE#n	Chip Enable Input for NAND E^{2}PROM
$\overline{OE}$ / RE#n	Output Enable Input for Pseudo SRAM Read enable Input for NAND E^{2}PROM
$\overline{WE}$ /WE#n	Write Enable Input for Pseudo SRAM Write Enable Input for NAND E^{2}PROM
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input for Pseudo SRAM
RY/$\overline{BY}$	Ready/Busy Output
WP#n	Write Protect/Program Acceleration Input
CLE	Command Latch Enable
ALE	Address Latch Enable
V_{CCs}	Power Supply for Pseudo SRAM
V_{CCn}, Vccqn	Power Supply for NAND E^{2}PROM
V_{SS}	Ground
NC	Not Connected

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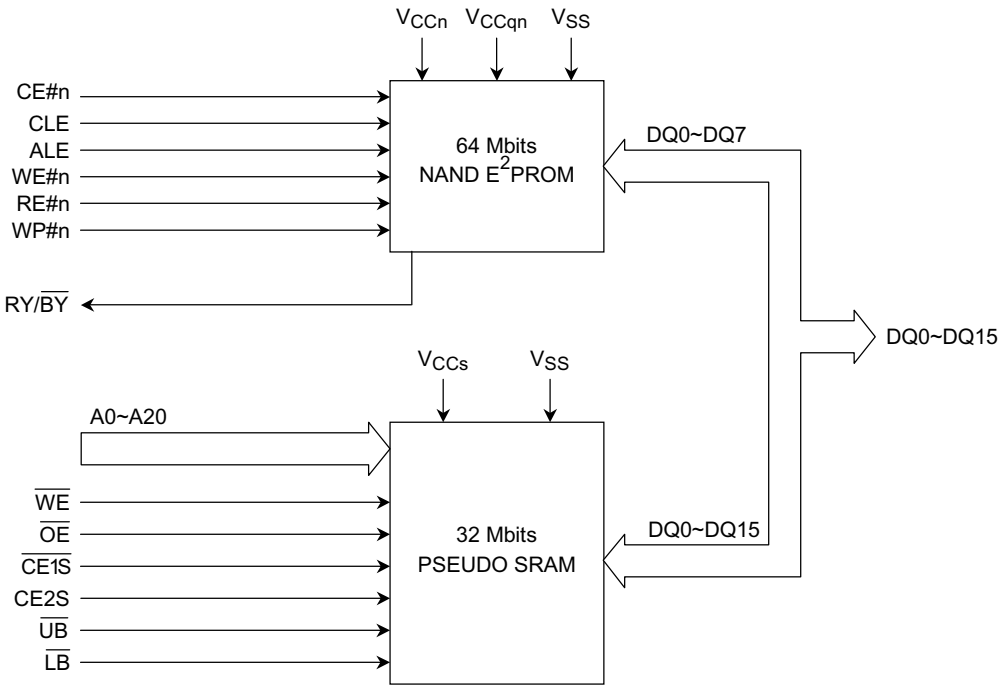
BLOCK DIAGRAM



MODE SELECTION

OPERATION	$\overline{CE1S}$	CE2S	$\overline{OE}$ RE#n	$\overline{WE}$ WE#n	$\overline{UB}$	$\overline{LB}$	CLE	ALE	CE#n	WP#n	DQ0~DQ7	DQ8~DQ15	Add
E^2PROM Serial Data Output	H	*	L	H	*	*	L	L	L	*	D_{OUT}	Hi-Z	*
	*	L											
E^2PROM Output Disable	H	*	H	H	*	*	L	L	L	*	Hi-Z	Hi-Z	*
	*	L											
E^2PROM Standby	H	*	*	H	*	*	L	L	H	*	S	S	S
	*	L											
E^2PROM Command Input	H	*	H	↑	*	*	H	L	L	*	COMAND-IN	Hi-Z	*
	*	L											
E^2PROM Data Input	H	*	H	↑	*	*	L	L	L	*	D_{IN}	Hi-Z	*
	*	L											
E^2PROM Address Input	H	*	H	↑	*	*	L	H	L	*	A_{IN}	Hi-Z	*
	*	L											
E^2PROM During Programming	H	*	H	H	*	*	*	*	*	H	N	Hi-Z	*
	*	L											
E^2PROM During Erasing	H	*	H	H	*	*	*	*	*	H	N	Hi-Z	*
	*	L											
E^2PROMProgram, Erase Inhibit	H	*	H	H	*	*	*	*	*	L	N	Hi-Z	*
	*	L											
Pseudo SRAM READ	L	H	L	H	L	L	L	L	H	*	D_{OUT}	D_{OUT}	**
	L	H	L	H	H	L	L	L	H	*	D_{OUT}	Hi-Z	**
	L	H	L	H	L	H	L	L	H	*	Hi-Z	D_{OUT}	**
Pseudo SRAM WRITE	L	H	H	L	L	L	L	L	H	*	D_{IN}	D_{IN}	**
	L	H	H	L	H	L	L	L	H	*	D_{IN}	Hi-Z	**
	L	H	H	L	L	H	L	L	H	*	Hi-Z	D_{IN}	**
Pseudo SRAM Output Disable	L	H	H	H	*	*	*	*	H	*	Hi-Z	Hi-Z	**
	L	H	L	H	H	H	*	*	H	*	Hi-Z	Hi-Z	**
Pseudo SRAM Standby	H	H	*	*	*	*	*	*	*	*	N	N	*
Pseudo SRAM DeepPower-down Standby	H	L	*	*	*	*	*	*	*	*	N	N	*

Notes:*: Don't Care

**: At $\overline{CE1S}$ falling edge, all address(A2 to A20) are valid "IN". Page address signals(A0 and A1) must be V_{IH} or V_{IL}, during entire cycle.

D_{IN}: Data IN

A_{IN}: Address In

D_{OUT}: Data Out

Hi-Z: High impedance

COMAND-IN: Command Input

N: Depends on E^2PROM memory operation mode

S: Depends on Pseudo SRAM operation Mode

Does not apply when CE#n = $\overline{CE1S}$ = V_{IL} and CE2S = V_{IH} at the same time.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{CC}	V_{CCs}/V_{CCn} Supply Voltage	−0.3~3.6	V
V_{IN}	Input Voltage	−0.3~3.6	V
V_{DQ}	Input/Output Voltage	−0.5~V_{CC} + 0.3 (≤ 3.6)	V
T_{opr}	Operating Temperature	−25~85	°C
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10 s)	260	°C
I_{short}	Output Short Circuit Current	100	mA
T_{stg}	Storage Temperature	−55~125	°C

RECOMMENDED DC OPERATING CONDITIONS (Ta = –25°~85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
$V_{CCs}/V_{CCn}, V_{CCqn,}$	Power Supply Voltage	2.7	—	3.1	V
V_{IH}	Input High-Level Voltage	2.2	—	V_{CC} + 0.3	
V_{IL}	Input Low-Level Voltage	−0.3	—	0.4	
V_{DH}	Data Retention Voltage for Pseudo SRAM	2.5	—	3.0	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	—	—	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	—	—	20	pF

Note: These parameters are sampled periodically and are not tested for every device.

DC CHARACTERISTICS (Ta = –25°~85°C, V_{CCs}/V_{CCn} = 2.7 V~3.1 V)

SYMBOL	PARAMETER	CONDITION		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{CC}		—	—	±10	μA
I_{SOH}	Pseudo SRAM Output High Current	V_{OH} = 2.0 V		–0.5	—	—	mA
I_{SOL}	Pseudo SRAM Output Low Current	V_{OL} = 0.4 V		1.0	—	—	mA
I_{FOH}	E^2PROM Output High Current (TTL)	V_{OH} = 2.4 V		–0.4	—	—	mA
I_{FOL}	E^2PROM Output Low Current	V_{OL} = 0.4 V		2.1	—	—	mA
I_{FOL} (RY/$\overline{BY}$)	E^2PROM Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V		—	8	—	mA
I_{LO}	Output Leakage Current	V_{OUT} = 0 .4V~V_{CC}, $\overline{OE}$ = V_{IH}		—	—	±10	μA
I_{CCO1}	E^2PROM Operating Current (Serial Read)	CE#n= V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 50ns		—	10	30	mA
I_{CCO2}	E^2PROM Operating Current (Command Input)	t_{cycle} = 50 ns		—	10	30	mA
I_{CCO3}	E^2PROM Operating Current (Data Input)	t_{cycle} = 50 ns		—	10	30	mA
I_{CCO4}	E^2PROM Operating Current (Address Input)	t_{cycle} = 50 ns		—	10	30	mA
I_{CCO5}	E^2PROM Programming Current	—		—	10	30	mA
I_{CCO6}	E^2PROM Erasing Current	—		—	10	30	mA
I_{CCO7}	Pseudo SRAM Operating Current	CE2S = V_{IH}, $\overline{CE1S}$ = Cycling, I_{OUT} = 0 mA,	t_{RC} = Min	—	—	40	mA
			t_{RC} = 1us	—	—	5	mA
I_{CCO8}	Pseudo SRAM Page Access Operating Current	CE2S = V_{IH} , $\overline{CE1S}$ = V_{IL} , Page add. cycling, I_{OUT}= 0 mA	t_{RC} = Min	—	—	25	mA
I_{CCS1}	E^2PROM Standby Current(TTL)	CE#n= V_{IH}		—	—	1	mA
I_{CCS2}	E^2PROM Standby Current(MOS)	CE#n= V_{CCn}– 0.2 V		—	—	100	μA
I_{CCS3}	Pseudo SRAM Standby Current (TTL)	$\overline{CE1S}$ = V_{IH}, CE2S = V_{IH}		—	—	3	mA
I_{CCS4}	Pseudo SRAM Standby Current(MOS)	$\overline{CE1S}$ = V_{CCs} – 0.2 V, CE2S = V_{CCS} – 0.2 V		—	—	70	μA
I_{CCS5}	Pseudo SRAM Deep Power-down Standby Current	CE2S = 0.2 V		—	—	5	μA

AC CHARACTERISTICS AND OPERATING CONDITIONS(Pseudo SRAM)

(Ta = –25°C~85°C, V_{DD} = 2.7~3.1 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read or Write Cycle Time	100	—	ns
t_{CE}	$\overline{CE1S}$ Pulse Width	85	10000	ns
t_P	Pre-charge Time	15	—	ns
t_{CEA}	$\overline{CE1S}$ Access Time	—	85	ns
t_{OEA}	$\overline{OE}$ Access Time	—	85	ns
t_{OEP}	$\overline{OE}$ Pulse Width	85	10000	ns
t_{BEA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	25	ns
t_{APH}	Address(A0 and A1) Hold Time	85	—	ns
t_{ASC}	Address Set-up Time	–15	—	ns
t_{AHC}	Address Hold Time	70	—	ns
t_{ASO}, t_{ASW}	Address Set-up Time	0	—	ns
t_{AHO}, t_{AHW}	Address Hold Time	70	—	ns
t_{WHC}	$\overline{WE}$ Hold Time	0	—	ns
t_{RCS}	Read Command Set-up Time	10	—	ns
t_{RCH}	Read Command Hold Time	10	—	ns
t_{WP}	$\overline{WE}$ Pulse Width	85	10000	ns
t_{WCH}	$\overline{CE1S}$ to End of Write	85	—	ns
t_{CWL}	Write Command to $\overline{CE1S}$ Lead Time	85	—	ns
t_{WBH}	$\overline{LB}$, $\overline{UB}$ to End of Write	50	—	ns
t_{BWL}	Write Command to $\overline{LB}$, $\overline{UB}$ Lead Time	85	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DSW}	Data Set-up Time from $\overline{WE}$	30	—	ns
t_{DSC}	Data Set-up Time from $\overline{CE1S}$	30	—	ns
t_{DSB}	Data Set-up Time from $\overline{LB}$, $\overline{UB}$	30	—	ns
t_{DHW}	Data Hold Time from $\overline{WE}$	0	—	ns
t_{DHC}	Data Hold Time from $\overline{CE1S}$	0	—	ns
t_{DHB}	Data Hold Time from $\overline{LB}$, $\overline{UB}$	0	—	ns
t_{CLZ}	$\overline{CE1S}$ Low to Output Active	10	—	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	—	ns
t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Low to Output Active	0	—	ns
t_{WLZ}	$\overline{WE}$ Low to Output Active	0	—	ns
t_{CHZ}	$\overline{CE1S}$ High to Output High-Z	—	20	ns
t_{OHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{BHZ}	$\overline{LB}$, $\overline{UB}$ High to Output High-Z	—	20	ns
t_{WHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{PC}	Page Mode Cycle Time	25	—	ns
t_{AA}	Page Mode Address Acess Time	—	25	ns
t_{AOH}	Page Mode Output Data Hold Time	10	—	ns
t_{CS}	CE2S Set-up Time	0	—	ns
t_{CH}	CE2S Hold Time	200	—	µs
t_{DPD}	CE2S Pulse Width(Deep Power Down)	10	—	ms
t_{CHC}	CE2S Hold from $\overline{CE1S}$ (Power On)	0	—	ns
t_{CHP}	CE2S Hold from Power On	30	—	µs

AC TEST CONDITIONS（Pseudo SRAM）

PARAMETER	CONDITION
Input Pulse Level	V_{CCS}- 0.2V, 0.2 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	$V_{CCS} \times 0.5$
Timing Measurement Reference Level (output)	$V_{CCS} \times 0.5$
Output Load	C_L (30 pF) + 1 TTL Gate

AC TEST CONDITIONS（NAND E^2PROM）

PARAMETER	CONDITION
Input Pulse Level	0.4 V, 2.4 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	$V_{CCn} \times 0.5$
Timing Measurement Reference Level (output)	$V_{CCn} \times 0.5$
Output Load	C_L (30 pF) + 1 TTL Gate

AC CHARACTERISTICS AND OPERATING CONDITIONS(NAND E²PROM)

(Ta = –25°C~85°C, V_{DD} = 2.7~3.1 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	CE#n Setup Time	0	—	ns	
t_{CH}	CE#n Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	30	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	WE#n High Hold Time	20	—	ns	
t_{WW}	$\overline{WP}$ High to WE#n Low	100	—	ns	
t_{RR}	Ready to RE#n Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	40	—	ns	
t_{RC}	Read Cycle Time	60	—	ns	
t_{REA}	RE#n Access Time (Serial Data Access)	—	40	ns	
t_{CEA}	CE#n Access Time (Serial Data Access)	—	45	ns	
t_{REAID}	RE#n Access Time (ID Read)	—	40	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	RE#n High to Output High Impedance	—	30	ns	
t_{CHZ}	CE#n High to Output High Impedance	—	20	ns	
t_{REH}	RE#n High Hold Time	20	—	ns	
t_{IR}	Output-High-impedance-to- RE#n Rising Edge	0	—	ns	
t_{RSTO}	RE#n Access Time (Status Read)	—	40	ns	
t_{CSTO}	CE#n Access Time (Status Read)	—	50	ns	
t_{RHW}	RE#n High to WE#n Low	0	—	ns	
t_{WHC}	WE#n High to CE#n Low	30	—	ns	
t_{WHR}	WE#n High to RE#n Low	30	—	ns	
t_{AR1}	ALE Low to RE#n Low (ID Read)	100	—	ns	
t_{CR}	CE#n Low to RE#n Low (ID Read)	100	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	25	µs	
t_{WB}	WE#n High to Busy	—	200	ns	
t_{AR2}	ALE Low to RE#n Low (Read Cycle)	50	—	ns	
t_{RST}	Device Reset Time (Read/Program/Erase)	—	6/10/500	µs	

Note: (1) CE#n High to Ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin. (Refer to Application Note (20) toward the end of this document.)

(2) Sequential Read is terminated when t_{CEH} is greater than or equal to 100 ns. If the RE#n to CE#n delay is less than 30 ns, RY/$\overline{BY}$ signal stays Ready

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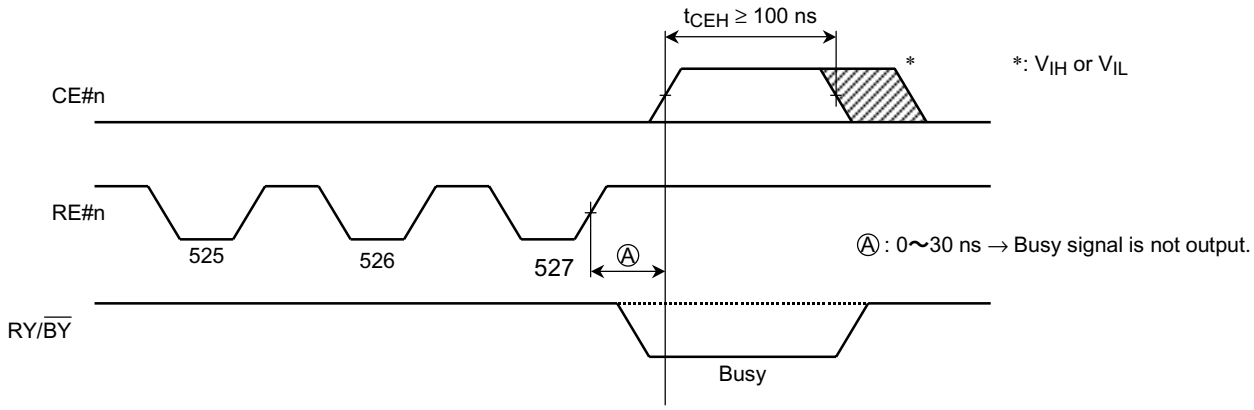


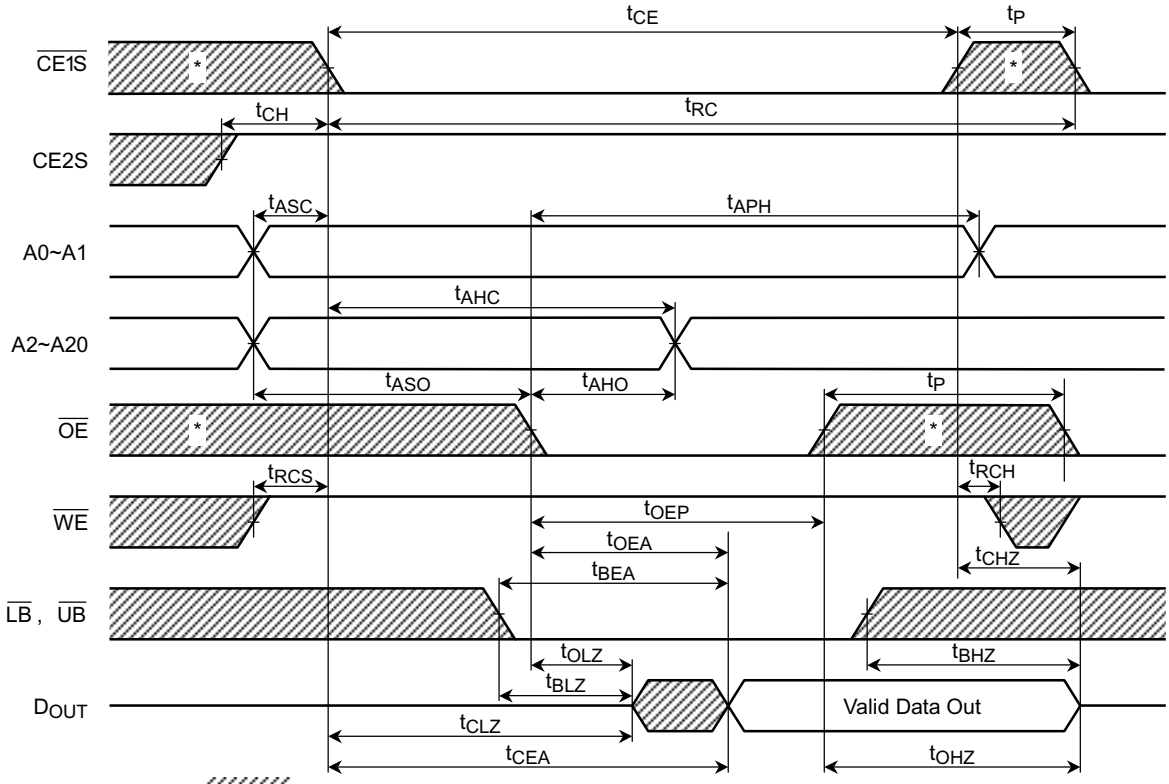
PROGRAMMING AND ERASING CHARACTERISTICS (Ta = -25° to 85, V_{CC} = 2.7 V to 3.1V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	200	1000	μs	
N	Number of Programming Cycles on Same Page	—	—	10		(1)
t_{BERASE}	Block Erasing Time	—	3	5	ms	

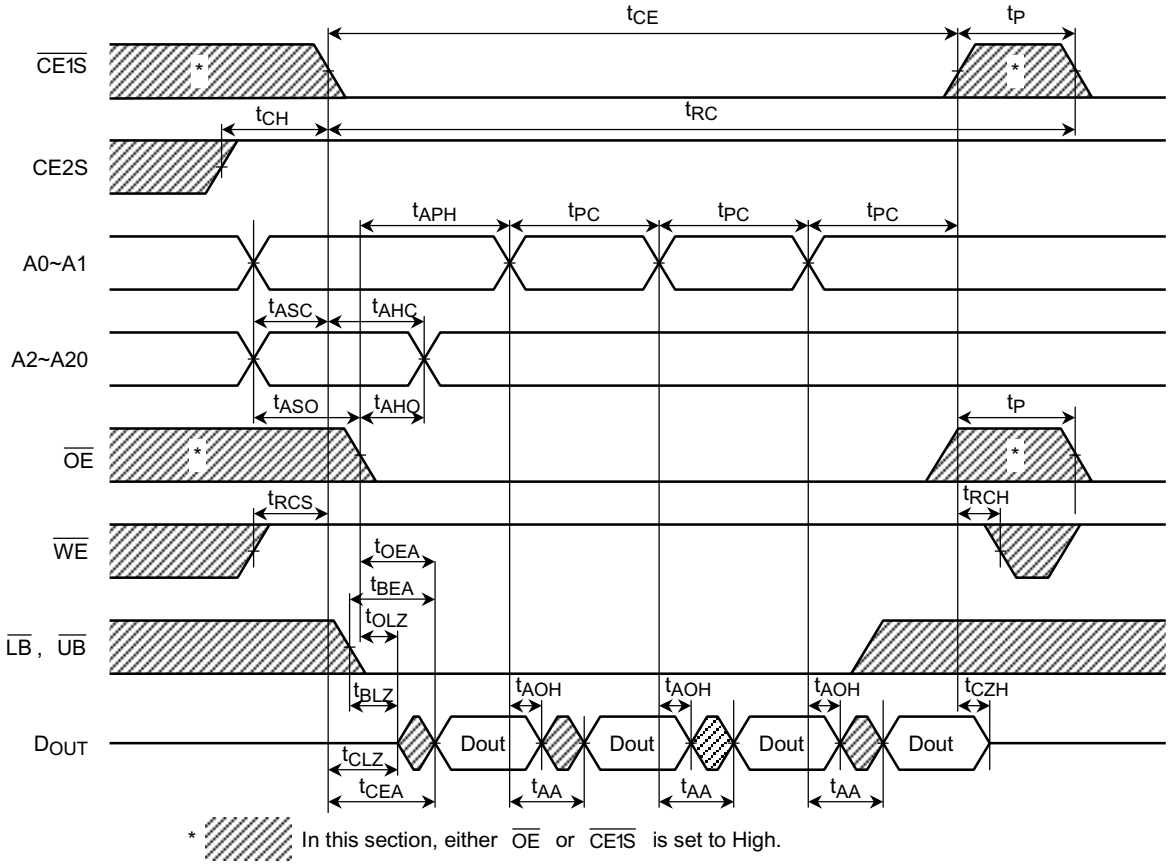
(1): Refer to Application Note (23) toward the end of this document.

TIMING DIAGRAMS

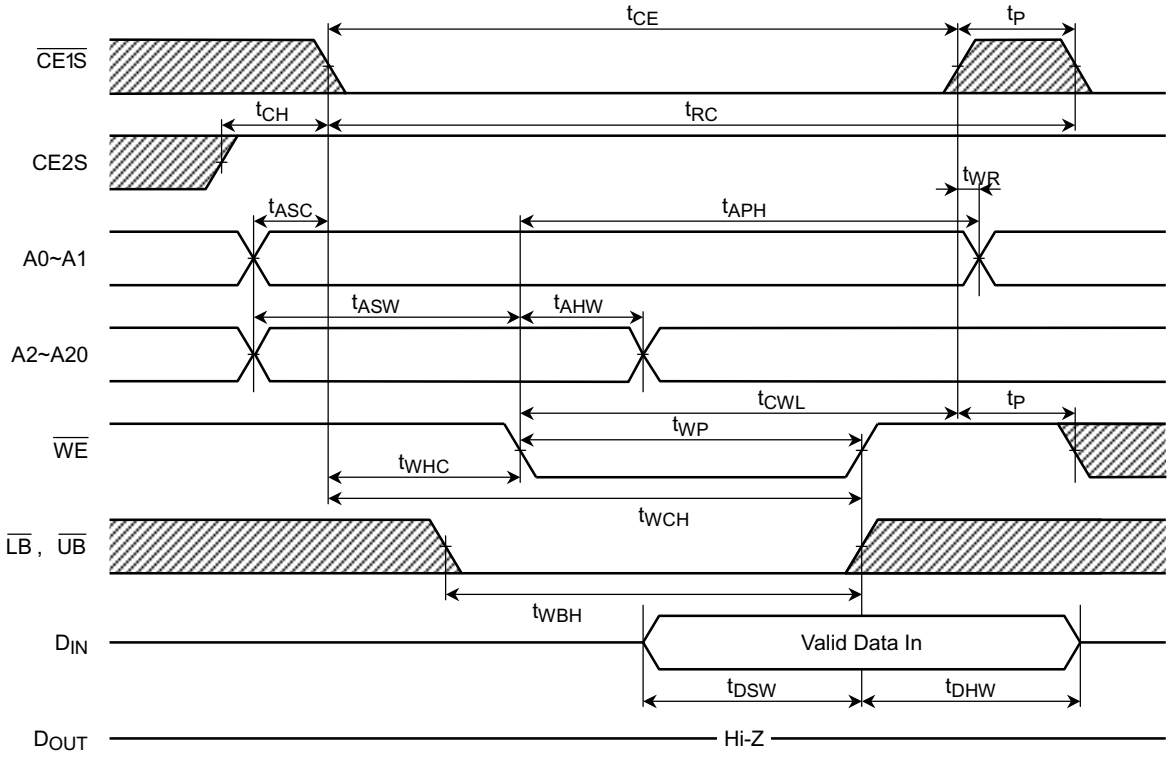
PSEUDO SRAM READ TIMING



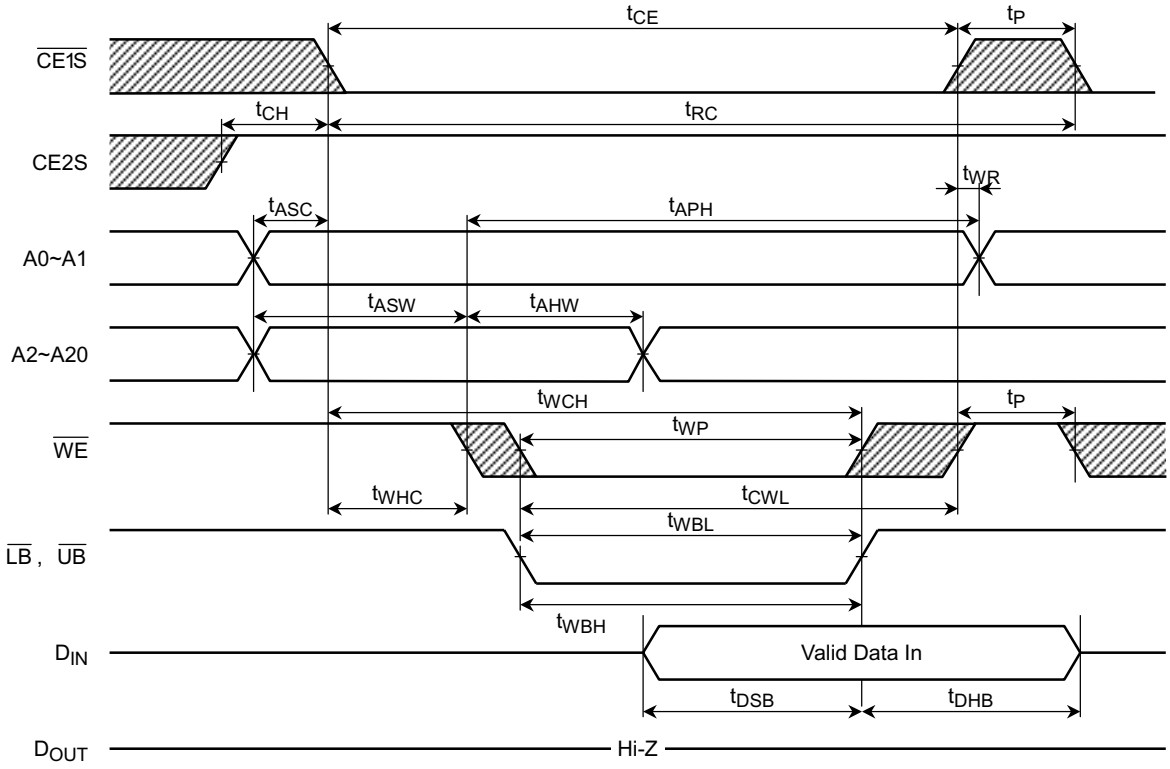
PSEUDO SRAM PAGE TIMING (4 words access)



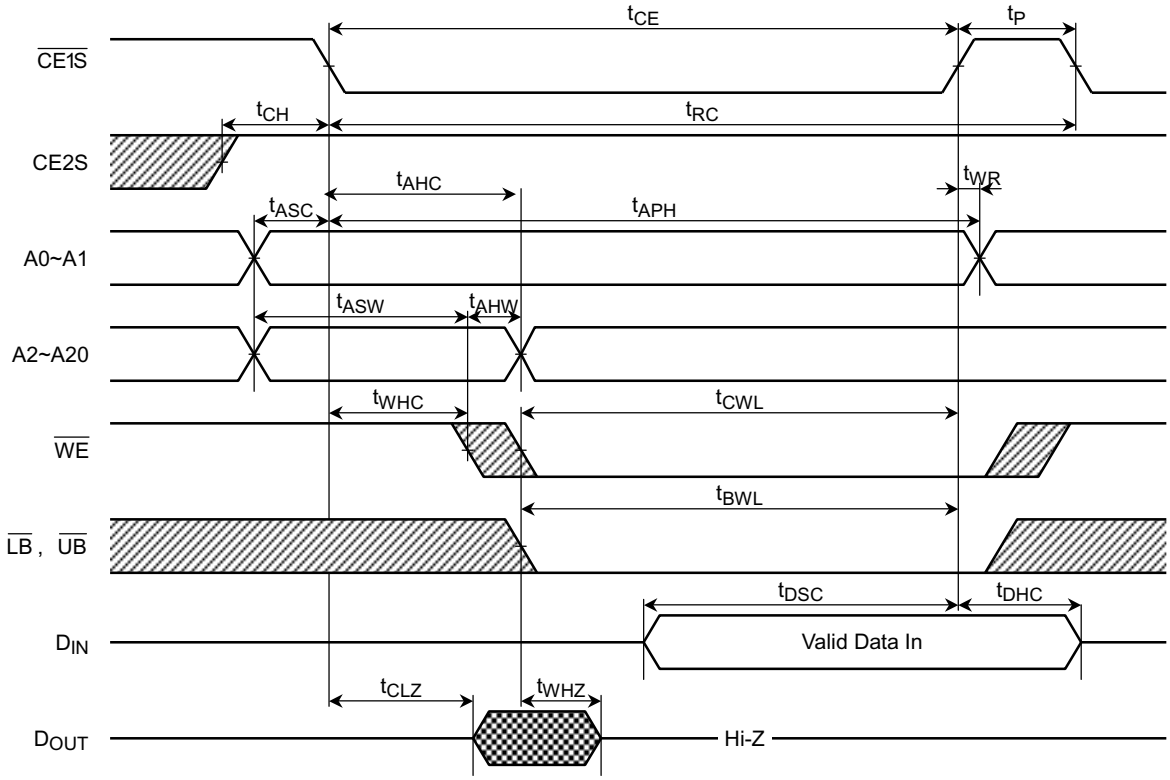
PSEUDO SRAM WRITE TIMING ($\overline{WE}$ Control Write)



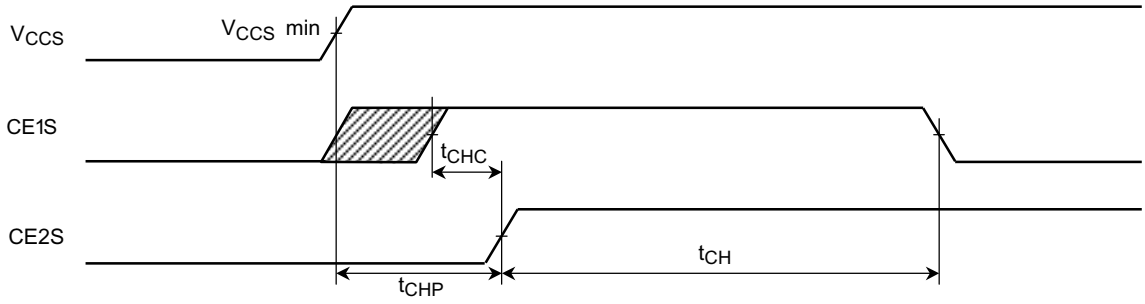
PSEUDO SRAM WRITE TIMING ($\overline{LB}$ / $\overline{UB}$ Control Write)



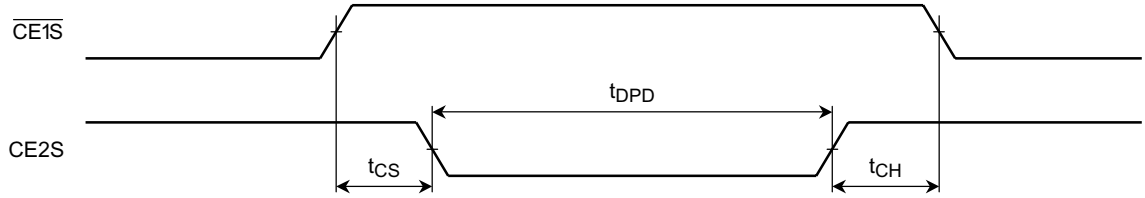
PSEUDO SRAM WRITE TIMING ($\overline{CE1S}$ Control Write)



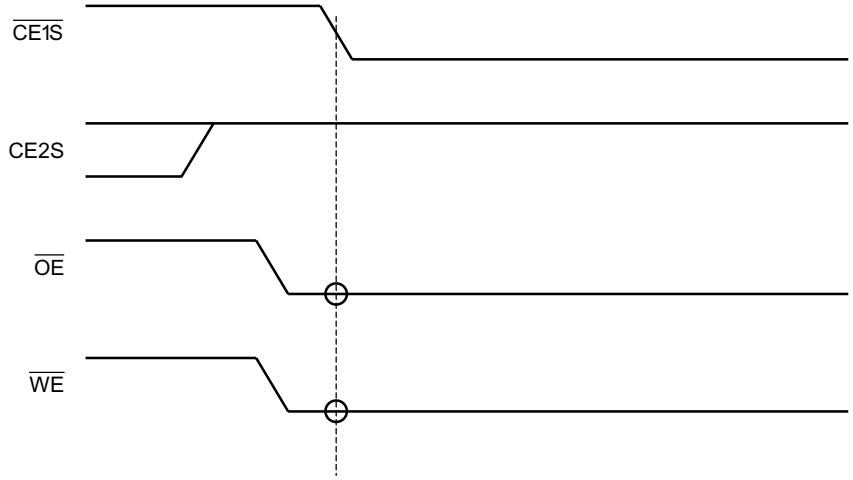
POWER ON TIMING



PSEUDO SRAM DEEP POWER-DOWN TIMING



PSEUDO SRAM PROHIBITION TIMING



The timing shown above is prohibited.
If both $\overline{OE}$ and $\overline{WE}$ go Low coincident with or before falling edge of $\overline{CE1S}$, a malfunction may occur since devices go into test modes for internal use.

APPLICATION NOTES AND COMMENTS

Note:

(1) Stresses greater than listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are reference to GND.

(3) I_{CCO} depends on the cycle time.

(4) I_{CCO} depends on output loading. Specified values are defined with the output open condition.

(5) After power-up, an initial pause of 200 μs with CE2S high is required with the output open condition.

(6) AC measurements are assumed t_T = 5 ns.

(7) Parameters t_{CHZ}, t_{OHZ}, t_{BHZ} and t_{WHZ} define the time at which the output goes the open condition and are not output voltage reference levels.

(8) During write cycles, input data is latched on the earliest of $\overline{WE}$, $\overline{LB}$/$\overline{UB}$ or $\overline{CE1S}$ rising edge. Therefore, input data must be valid during the set-up time (t_{DSC}, t_{DSB} or t_{DSW}) and hold time(t_{DHC}, t_{DHB} or t_{DHW}).

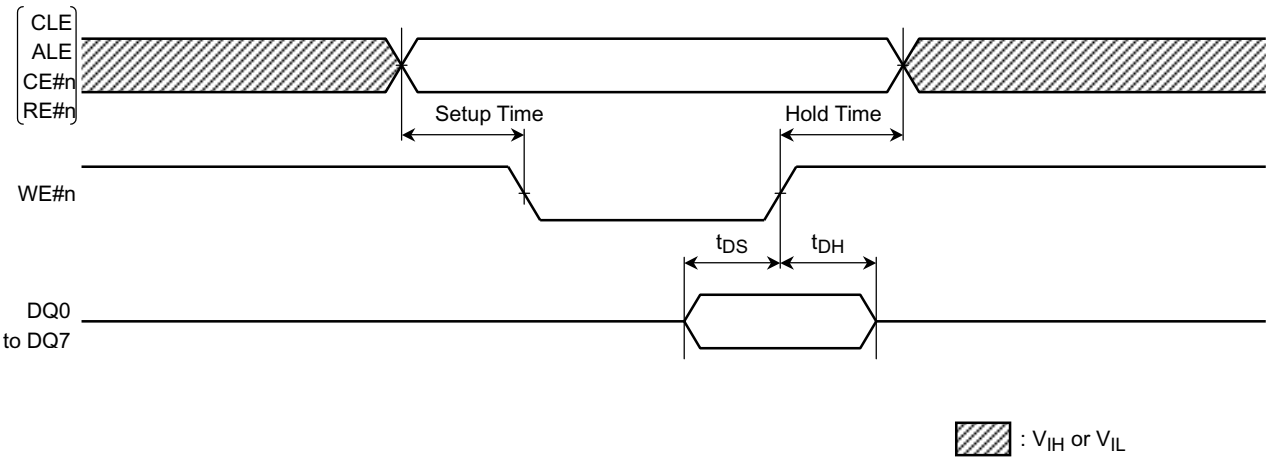
(9) Address(A2 to A20) inputs are latched on the falling edge of $\overline{CE1S}$. Therefore, addresses(A2 to A20) input must be valid during the set-up time (t_{ASC}) and hold time(t_{AHC}).

(10) Data cannot be retained at deep power-down stand-by mode

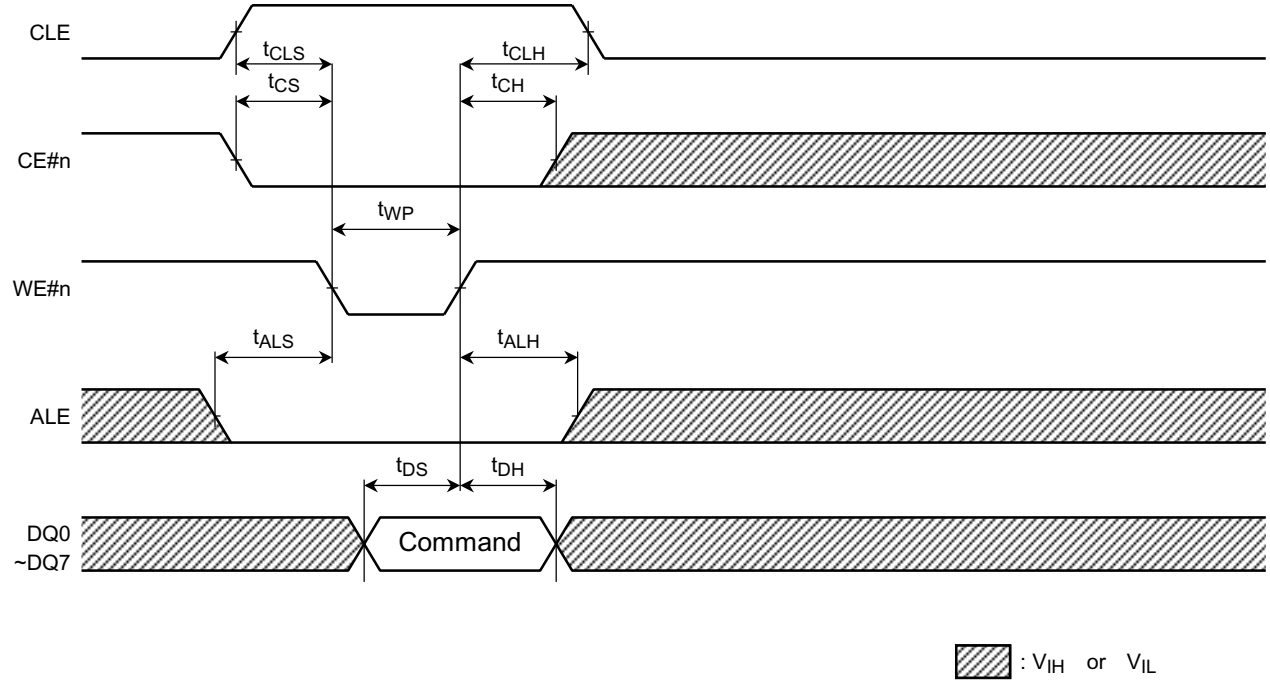
(11) If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.

(12) During the output state of DQ signals, input signals of reverse polarity must not be applied.

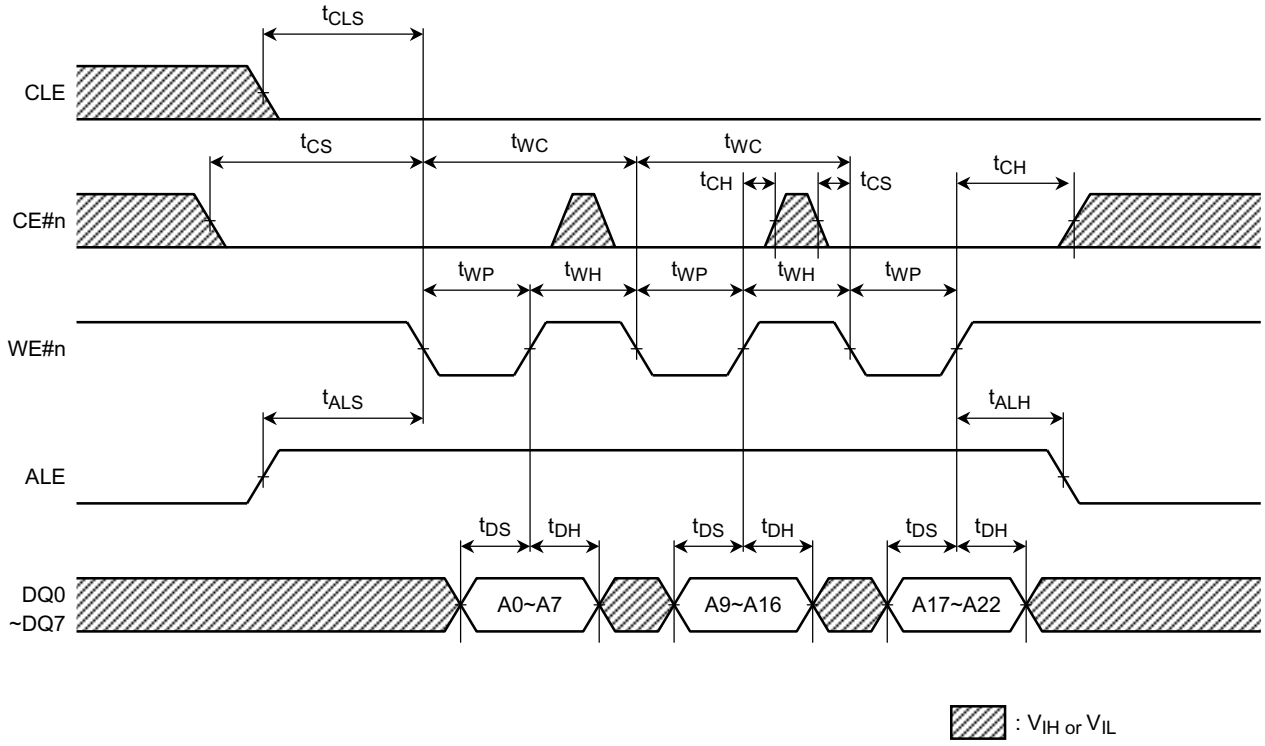
Latch Timing Diagram for Command/Address/Data



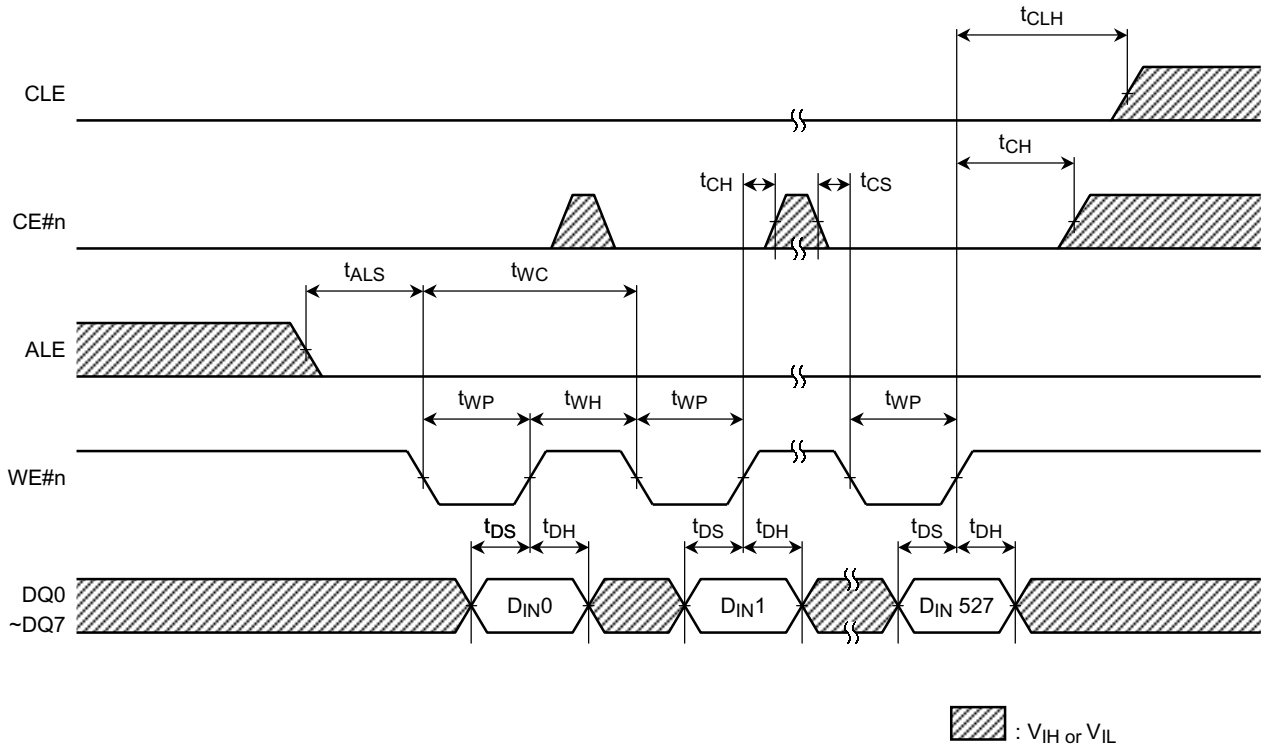
Command Input Cycle Timing Diagram



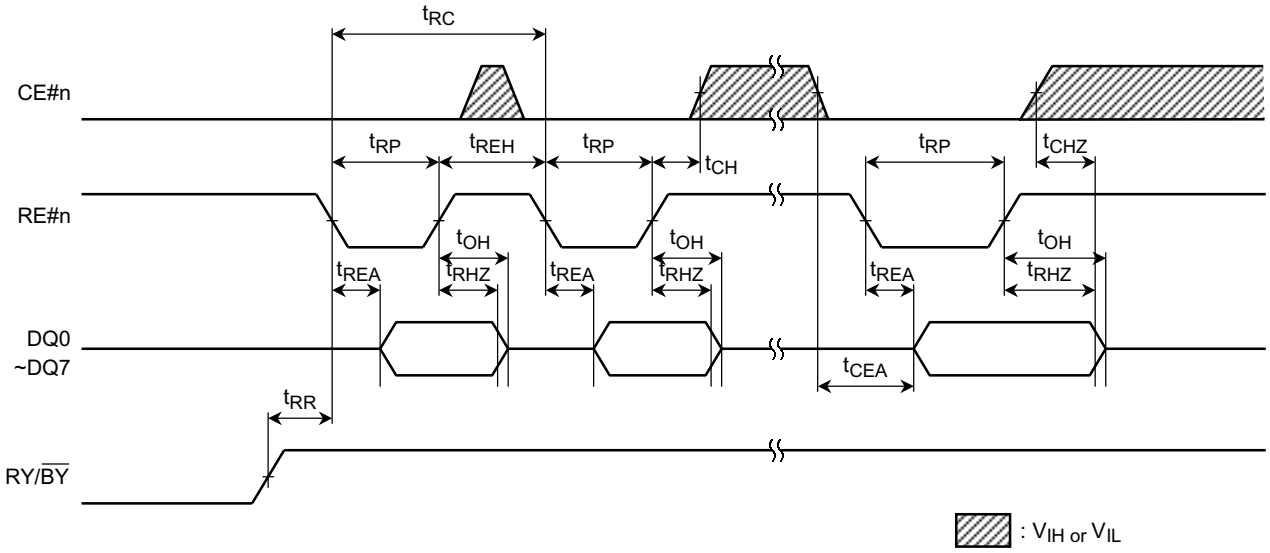
Address Input Cycle Timing Diagram



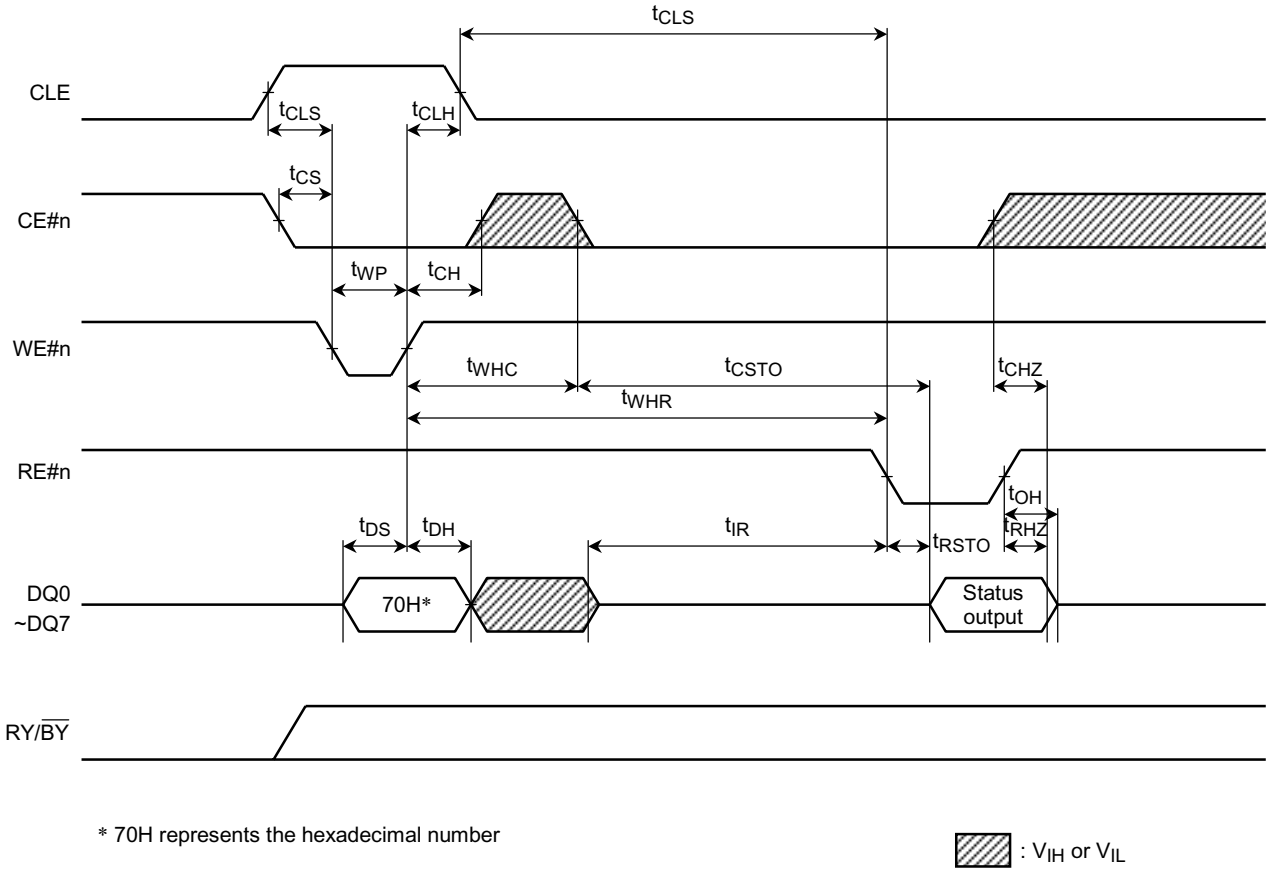
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



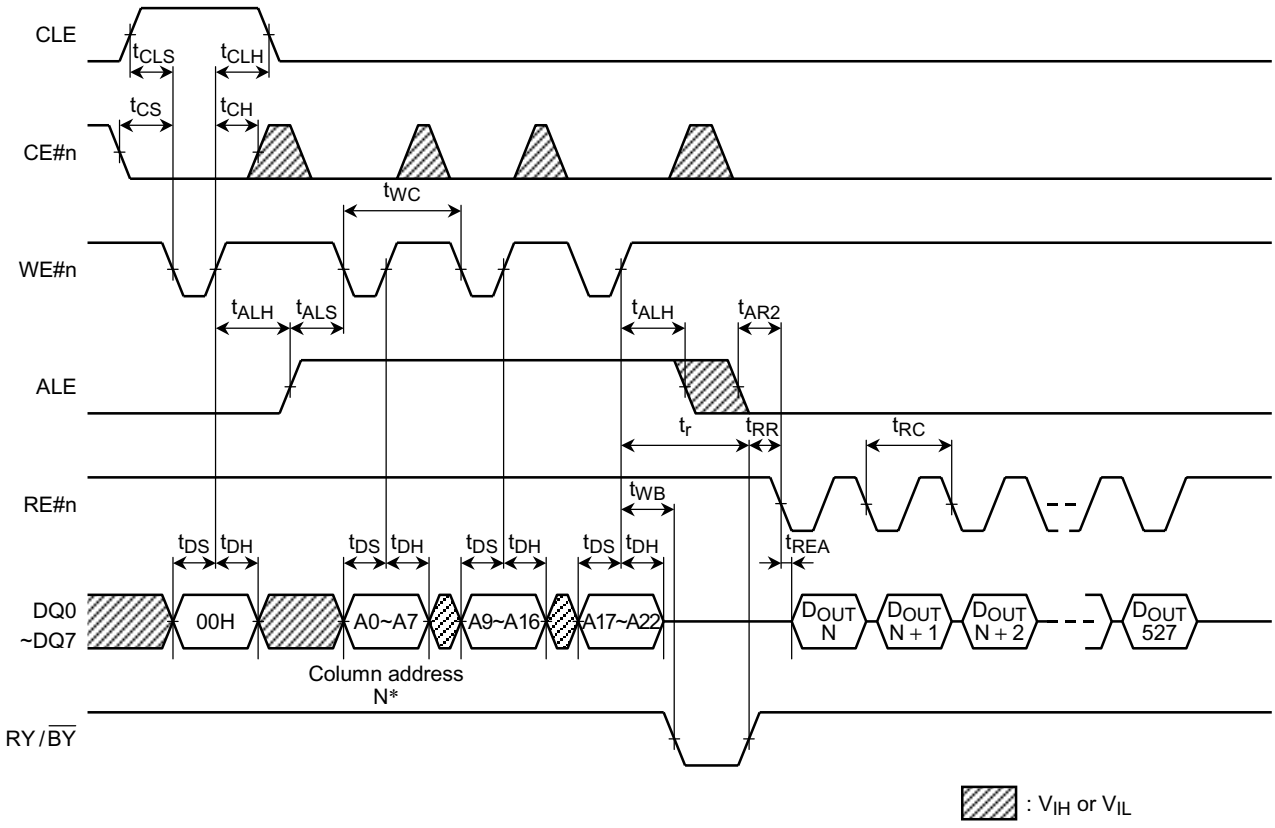
Status Read Cycle Timing Diagram



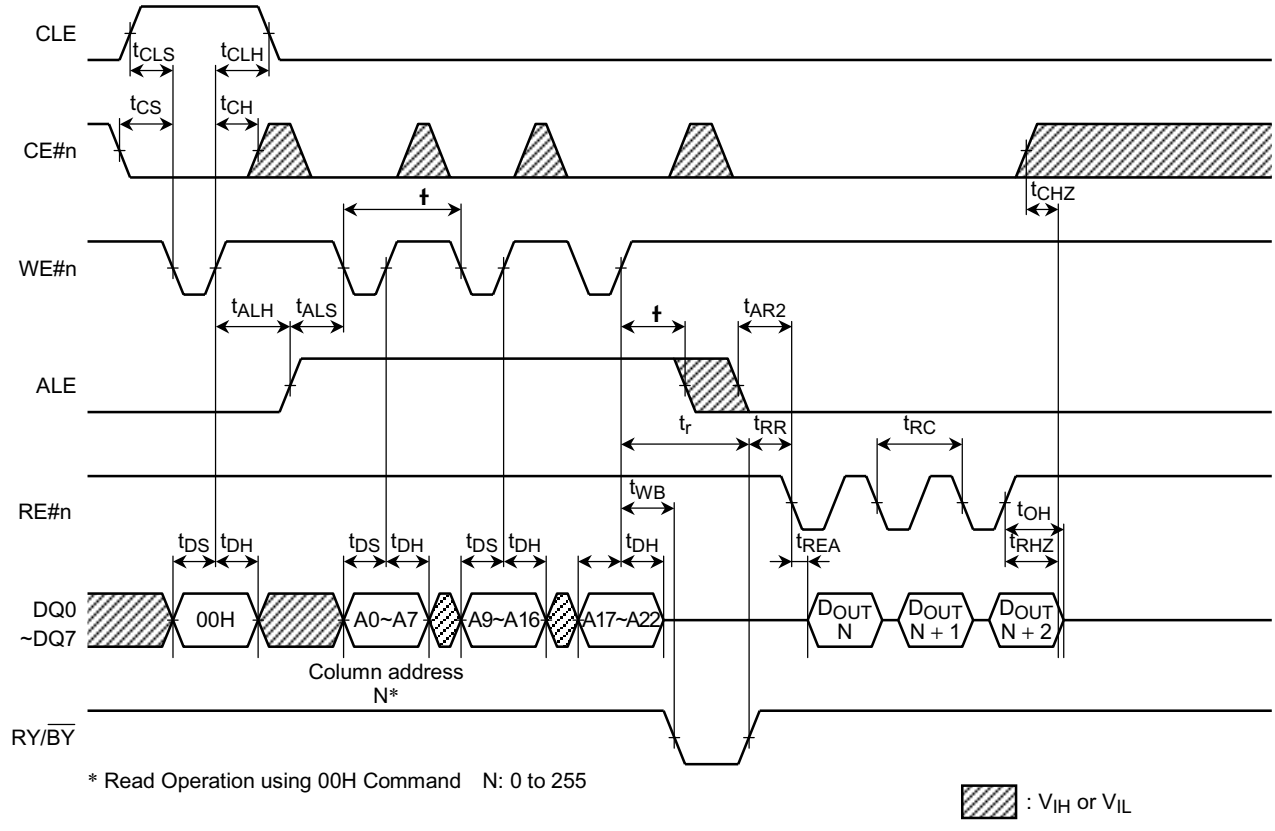
* 70H represents the hexadecimal number

: V_{IH} or V_{IL}

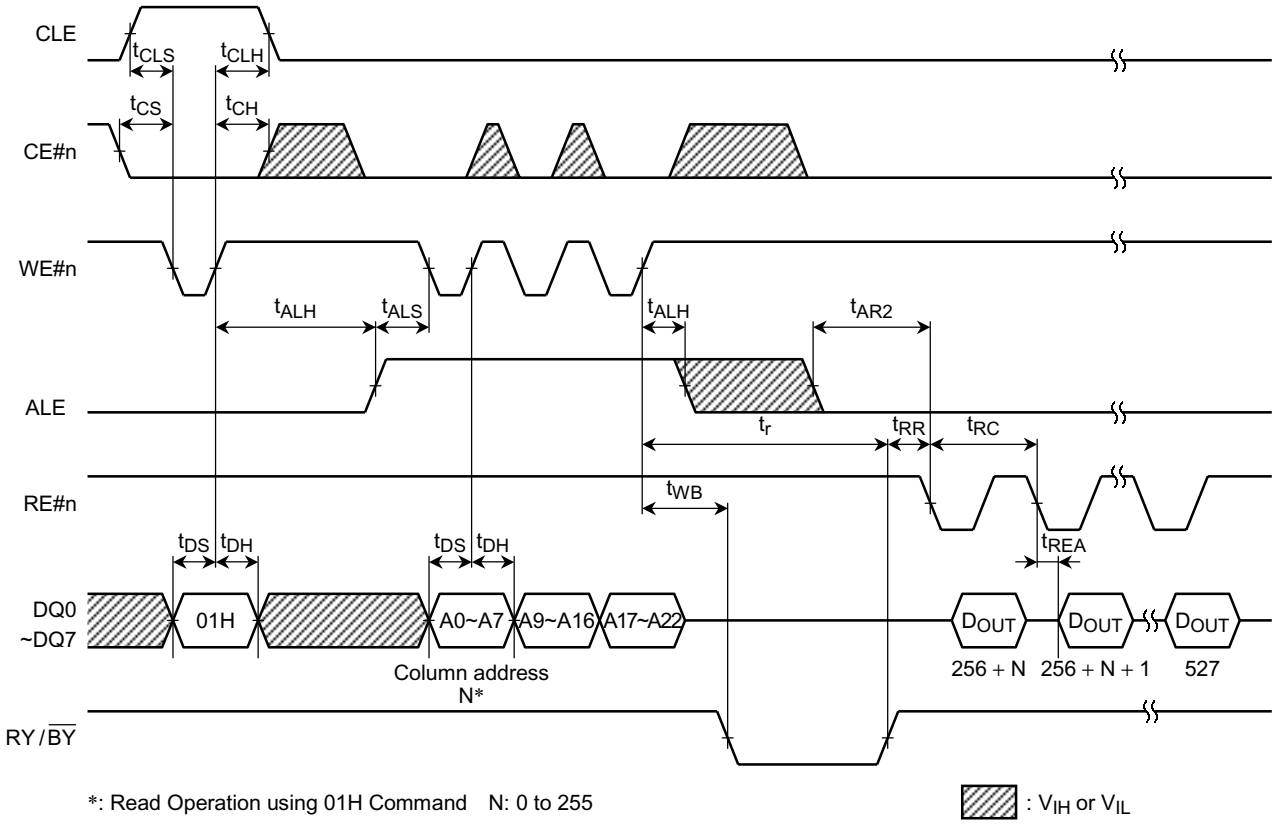
Read Cycle (1) Timing Diagram



Read Cycle (1) Timing Diagram: When Interrupted by CE#n



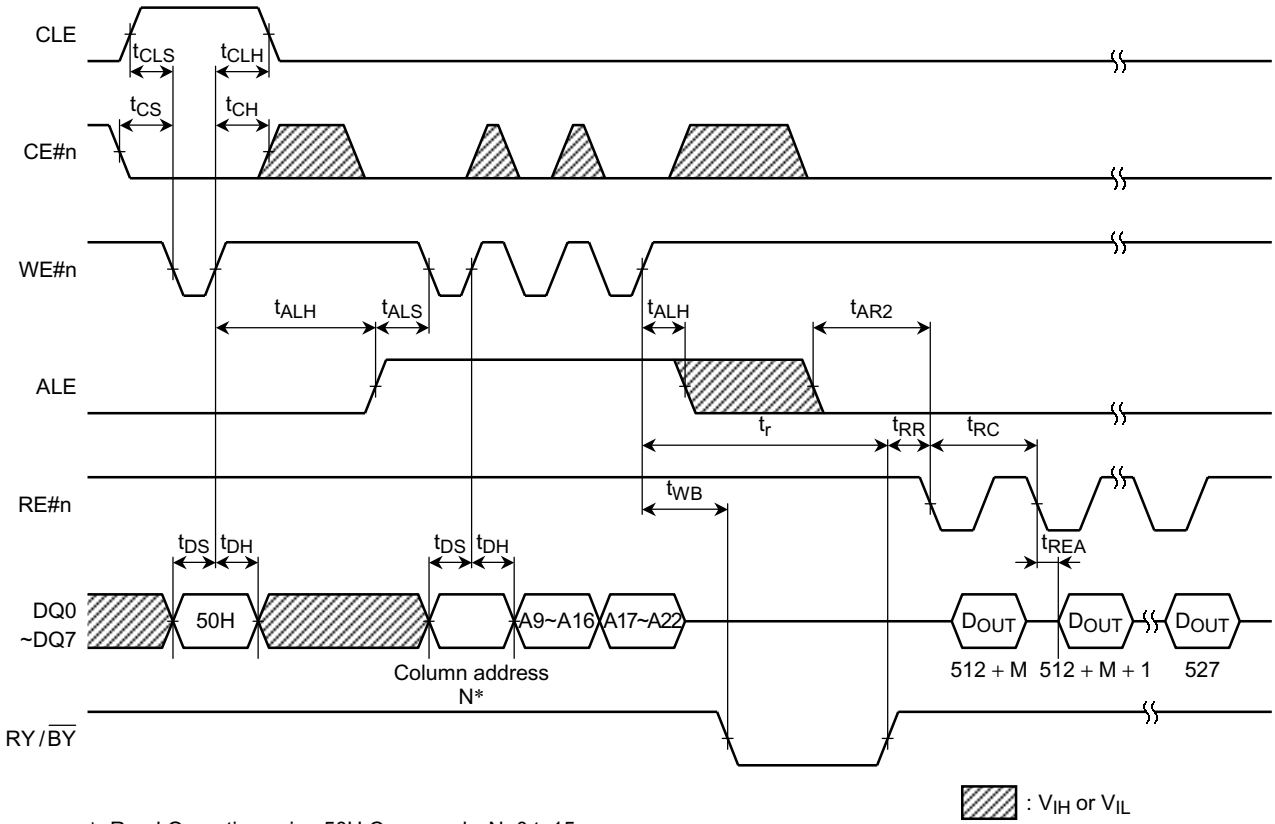
Read Cycle (2) Timing Diagram



*: Read Operation using 01H Command N: 0 to 255

: V_{IH} or V_{IL}

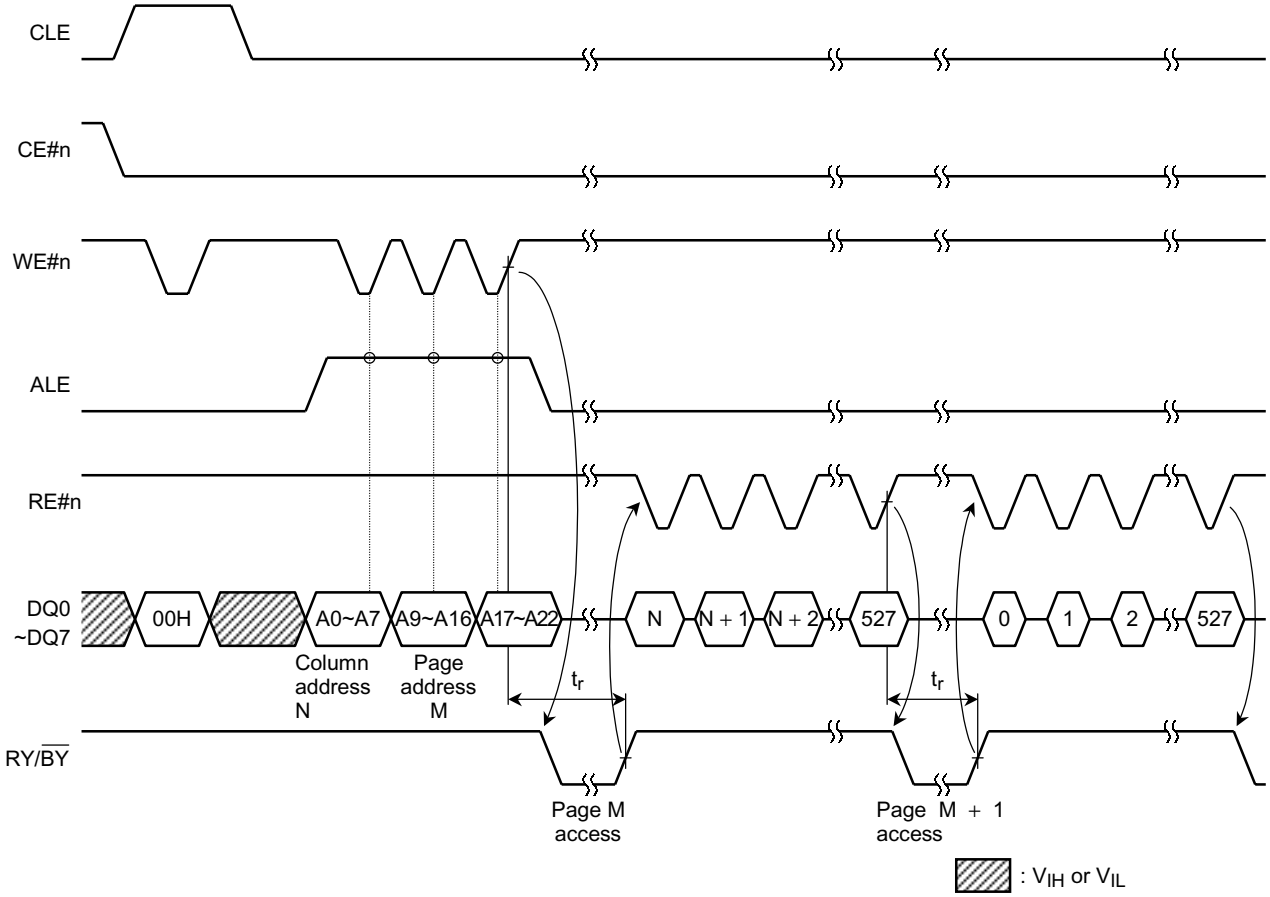
Read Cycle (3) Timing Diagram



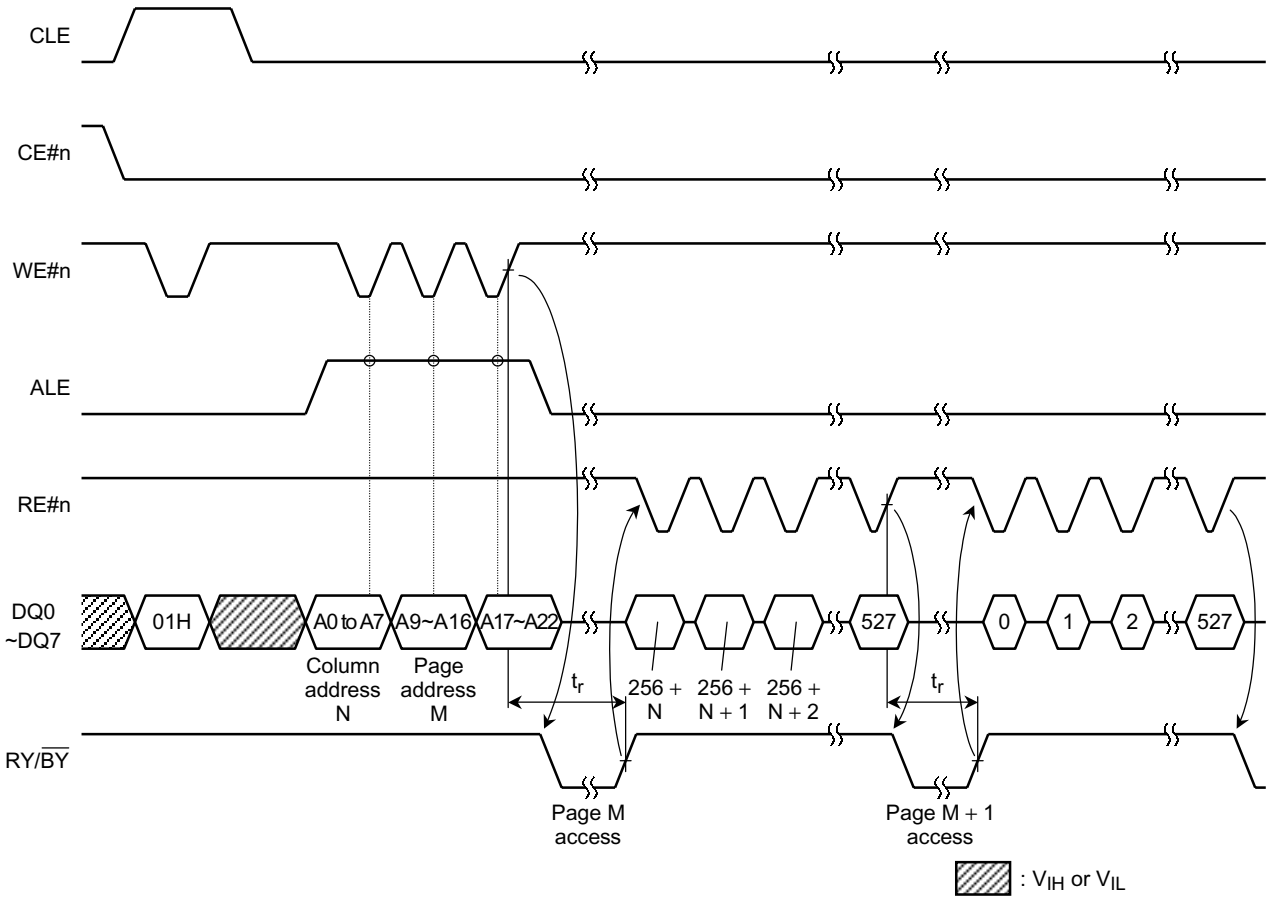
: V_{IH} or V_{IL}

*: Read Operation using 50H Command N: 0 to15

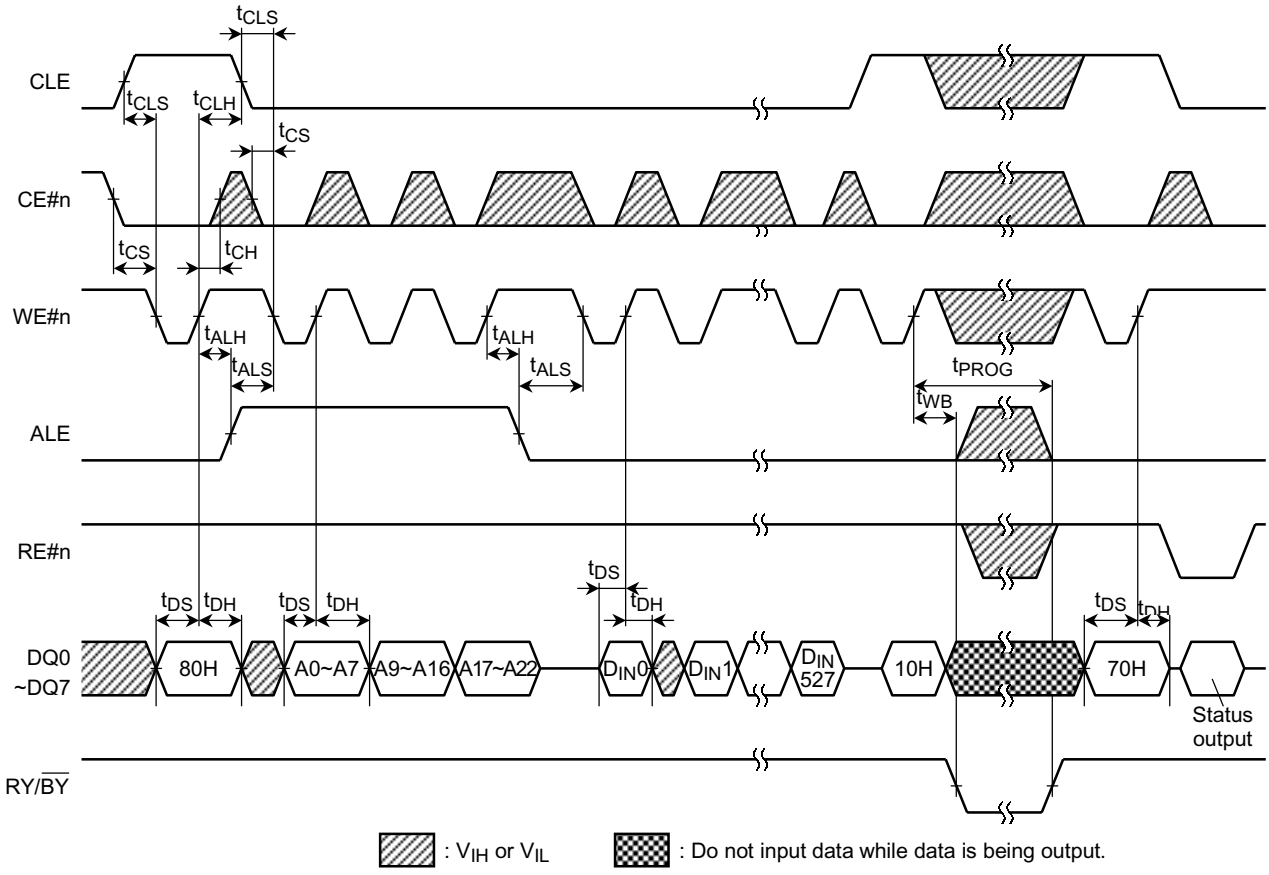
Sequential Read (1) Timing Diagram



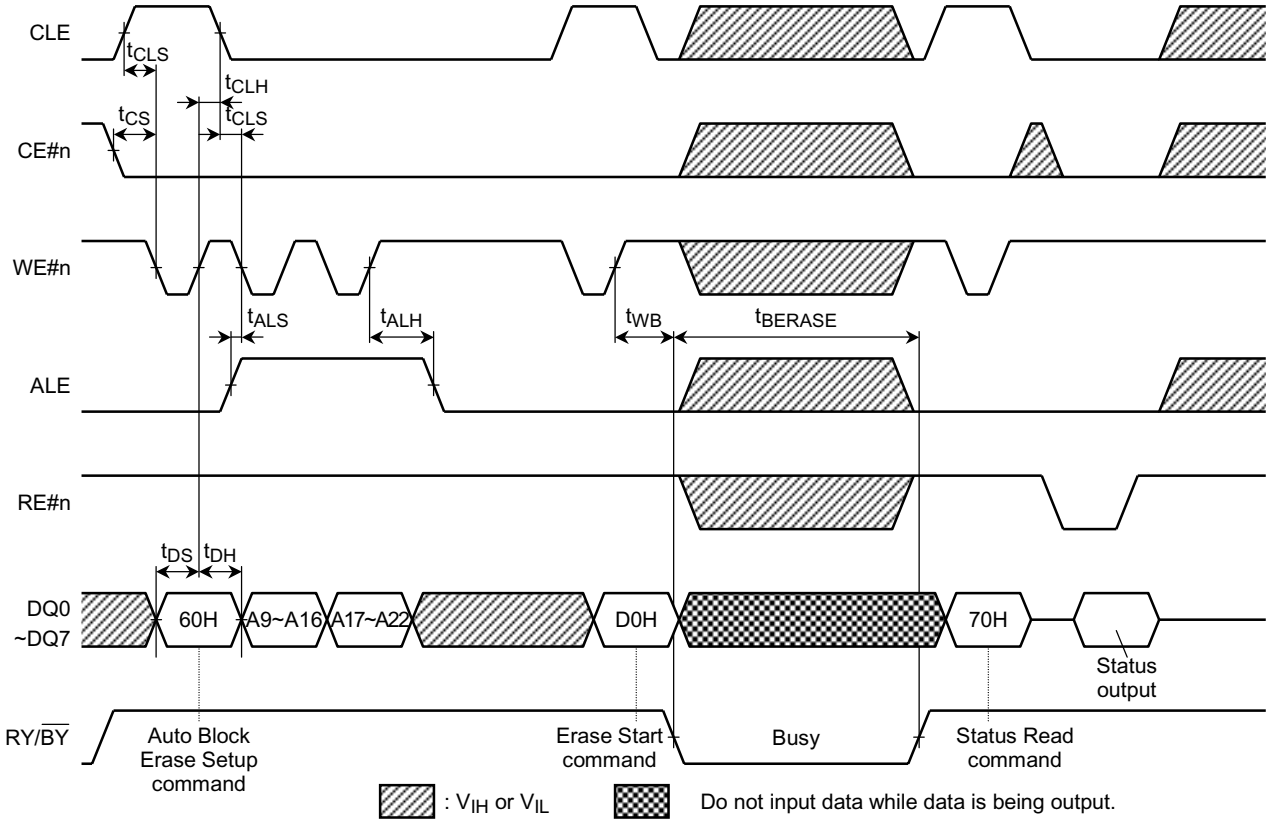
Sequential Read (2) Timing Diagram



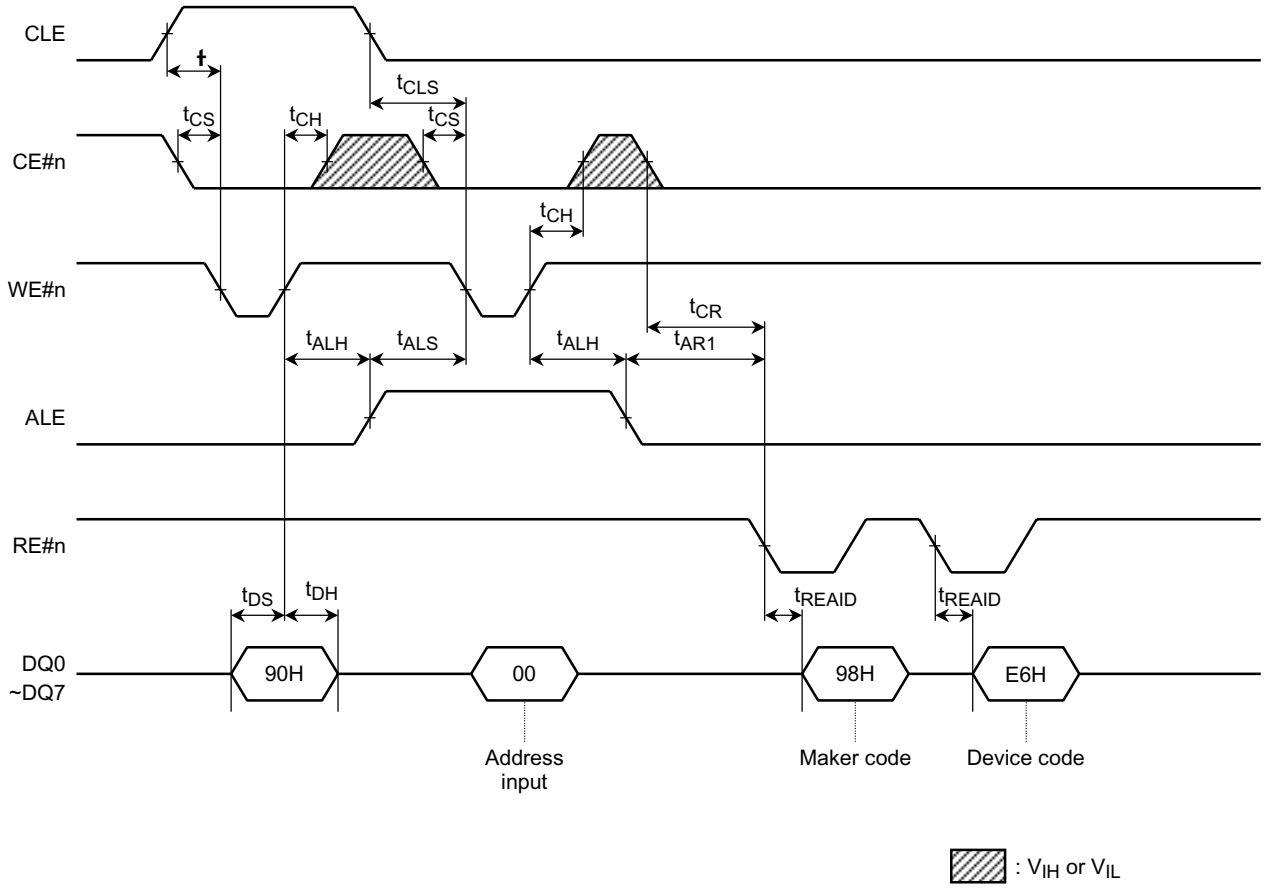
Auto-Program Operation Timing Diagram



Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



NAND PIN FUNCTIONS

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the DQ port on the rising edge of the WE#n signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of WE#n if ALE is High.

Input data is latched if ALE is Low.

Chip Enable: CE#n

The device goes into a low-power Standby mode when CE#n goes High during a wait state. The CE#n signal is ignored when device is in Busy state (R/B= L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the CE#n input goes High..

Write Enable: WE#n

The WE#n signal is used to control the acquisition of data from the DQ port.

Read Enable: RE#n

The RE#n signal controls serial data output. Data is available t_{REA} after the falling edge of RE#n.

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

DQ Port: DQ0 to 7

The DQ0 to 7 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: WP#n

The WP#n signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WP#n is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $\overline{RY/BY}$

The $\overline{RY/BY}$ output signal is used to indicate the operating condition of the device. The $\overline{RY/BY}$ signal is in Busy state ($\overline{RY/BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($\overline{RY/BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

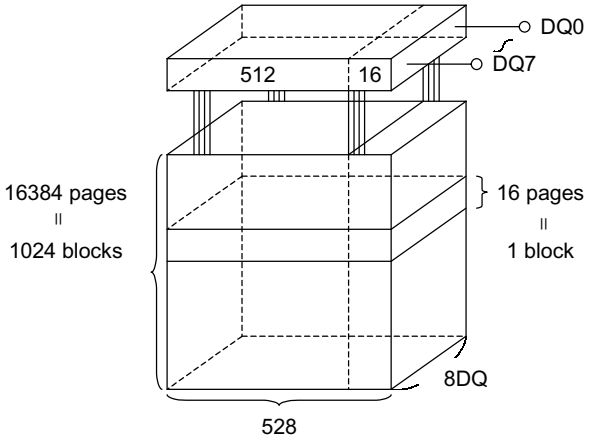


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 16 pages = (8K + 256) bytes
Capacity = 528 bytes × 16 pages × 1024 blocks

An address is read in via the DQ port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	*L	*L	A22	A21	A20	A19	A18	A17

A0~A7: Column address
A9~A22: Page address
(A13~A22: Block address
A9~A12: NAND address in block)

A8 is automatically set to Low or High by a 00H command or a 01H command.

*: DQ6 and DQ7 must be set to Low in the third cycle .

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, CE#n, WE#n, RE#n, WP#n and signals, as shown in Table 2.

Table 2. Logic table

	CLE	ALE	CE#n	WE#n	RE#n	WP#n
Command Input	H	L	L	⎍	H	*
Data Input	L	L	L	⎍	H	*
Address Input	L	H	L	⎍	H	*
Serial Data Output	L	L	L	H	⎌	*
During Read (Busy)	*	*	L	H	H	*
	*	*	H	*	*	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	○
Auto Program	10	—	
Auto Block Erase	60	D0	
Status Read	70	—	○
ID Read	90	—	

HEX data bit assignment
(Example)

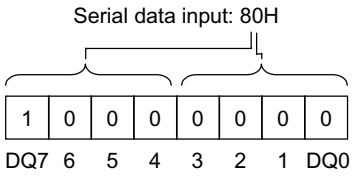


Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

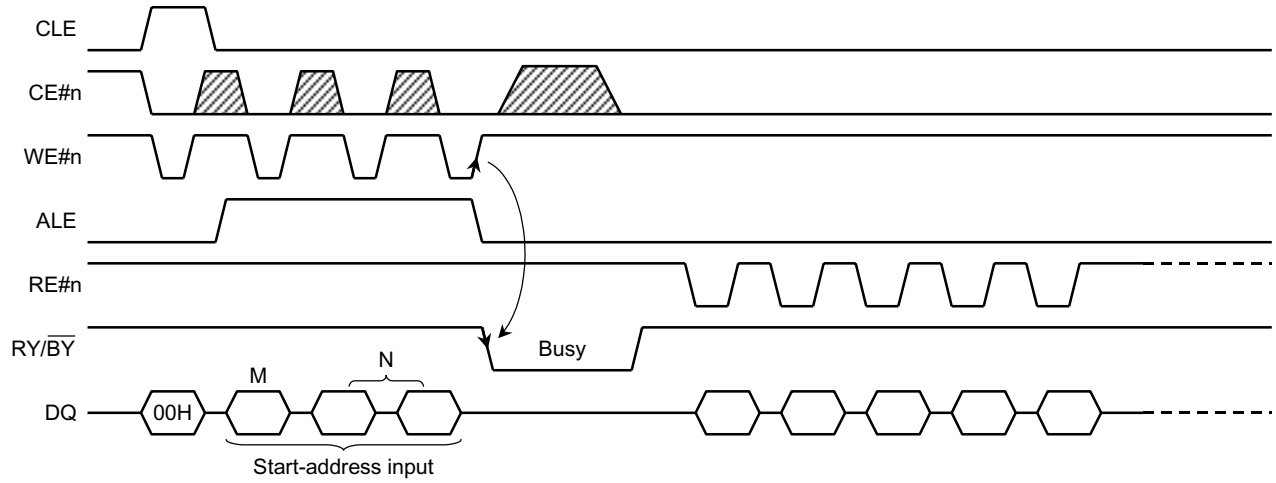
	CLE	ALE	CE#n	WE#n	RE#n	DQ0~DQ7	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL}

NAND DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.



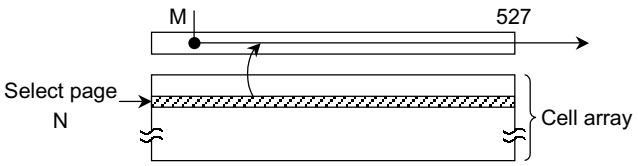
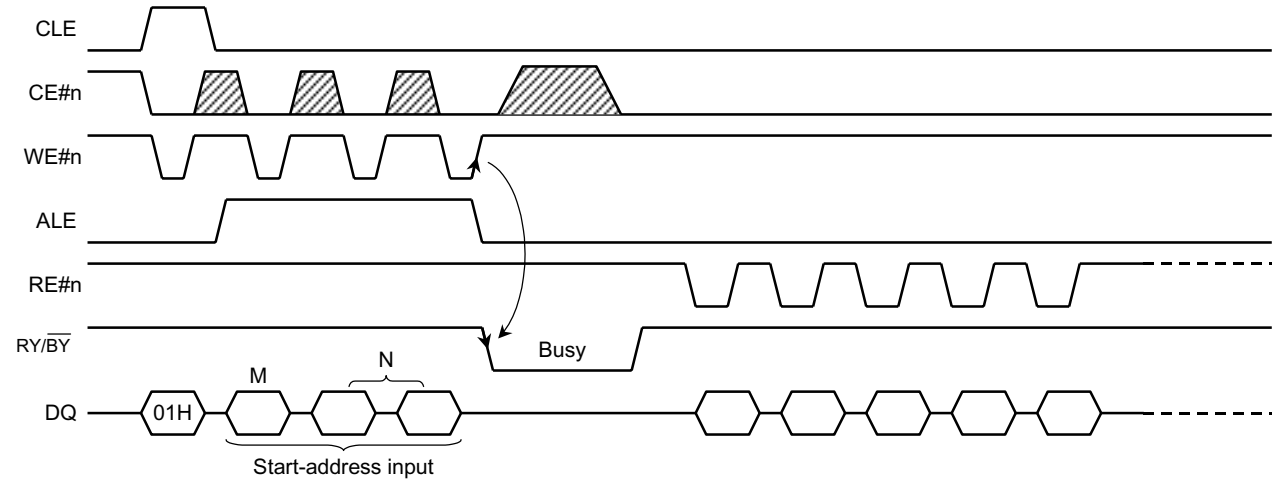


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of WE#n in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the RE#n clock from the start pointer designated in the address input cycle.

Read Mode (2)



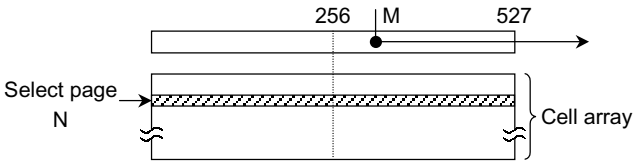


Figure 4. Read mode (2) operation

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

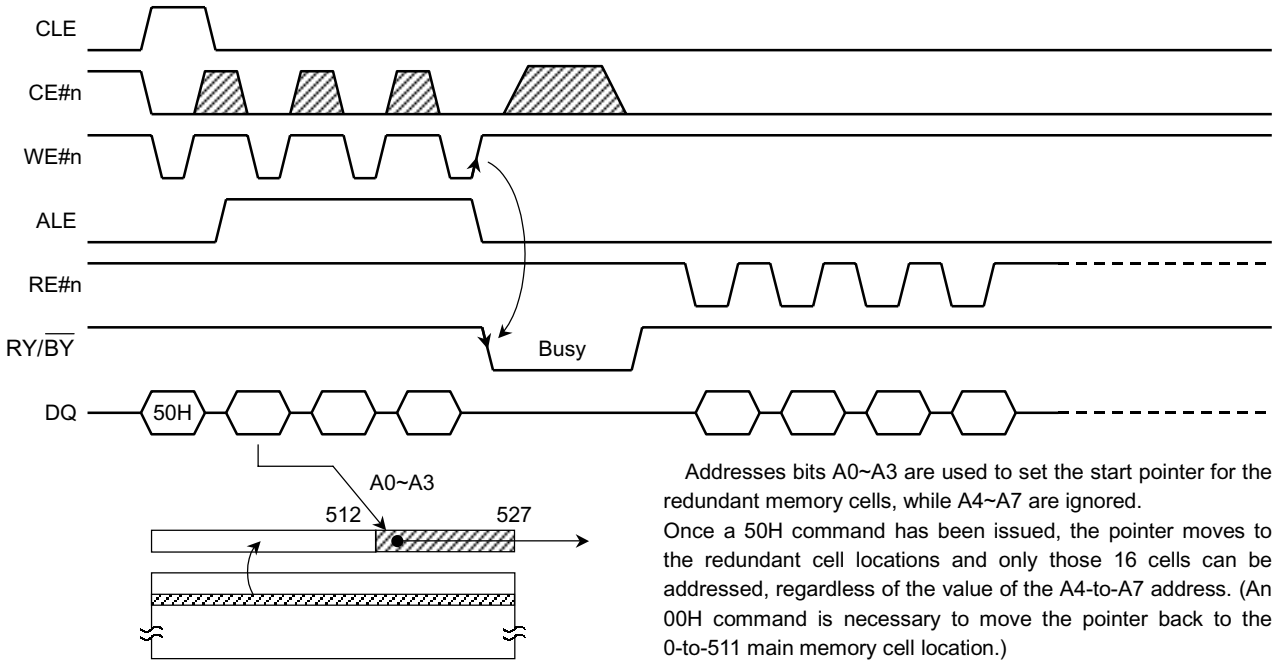


Figure 5. Read mode (3) operation

Addresses bits A0~A3 are used to set the start pointer for the redundant memory cells, while A4~A7 are ignored.
Once a 50H command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address. (An 00H command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the DQ port on the RE#n clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
DQ0	Pass/Fail	Pass: 0	Fail: 1
DQ1	Not Used	0	
DQ2	Not Used	0	
DQ3	Not Used	0	
DQ4	Not Used	0	
DQ5	Not Used	0	
DQ6	Ready/Busy	Ready: 1	Busy: 0
DQ7	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on DQ0 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

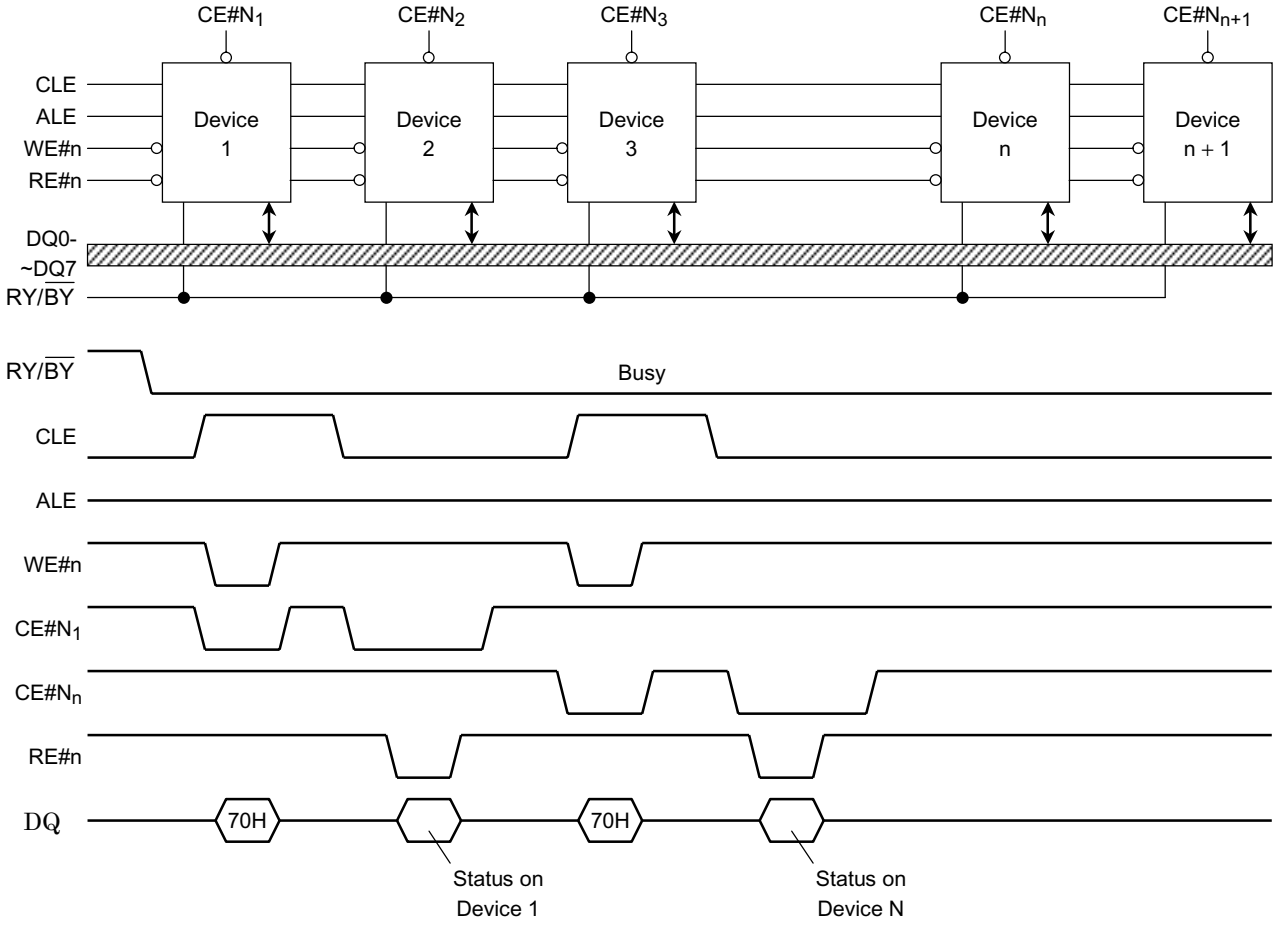


Figure 6. Status Read timing application example

System Design Note: If the RY/$\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

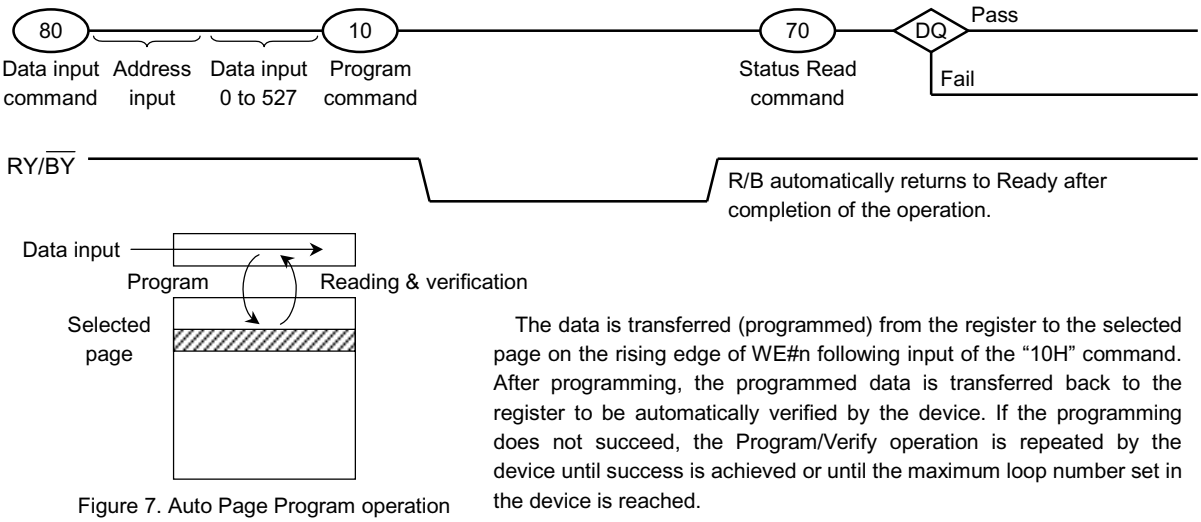
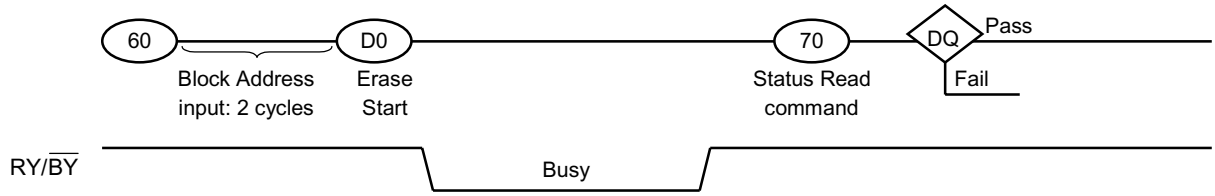


Figure 7. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of WE#n following input of the "10H" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE#n after the Erase Start command "D0H" which follows the Erase Setup command "60H". This two-cycle process for Erase operations acts as an ertra layer of protection from aceidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



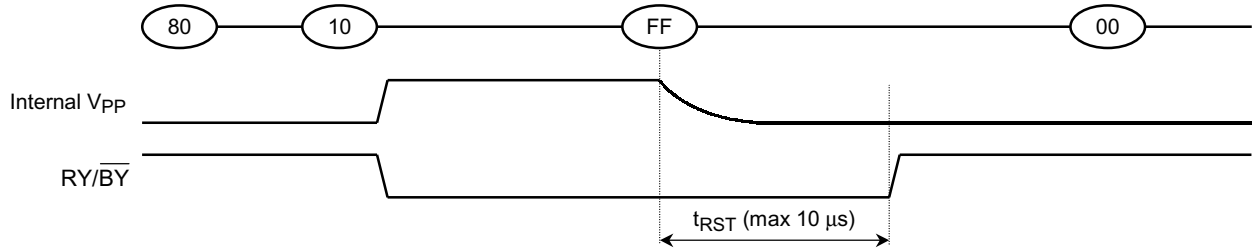
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFH" Reset command input during the various device operations is as follows:

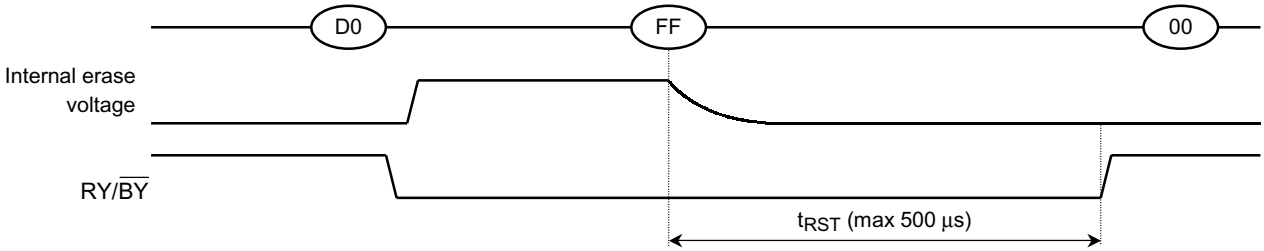
When a Reset (FFH) command is input during programming

Figure 8.



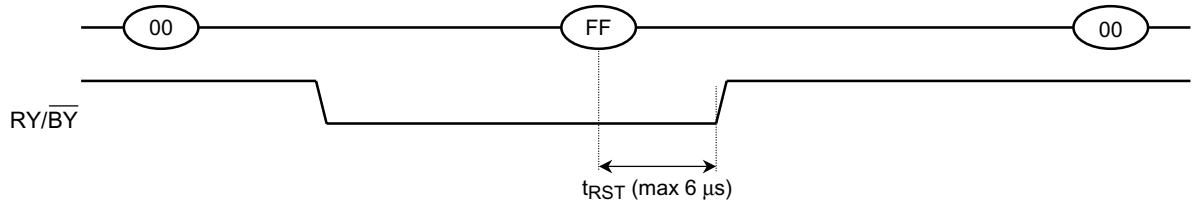
When a Reset (FFH) command is input during erasing

Figure 9.



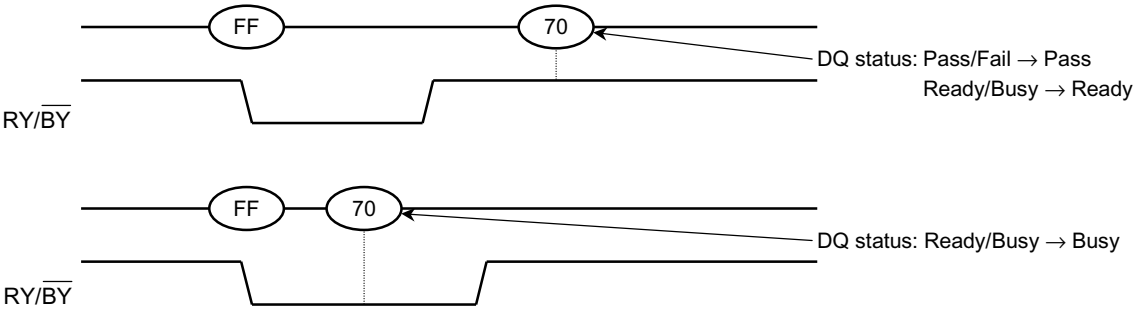
When a Reset (FFH) command is input during Read operation

Figure 10.



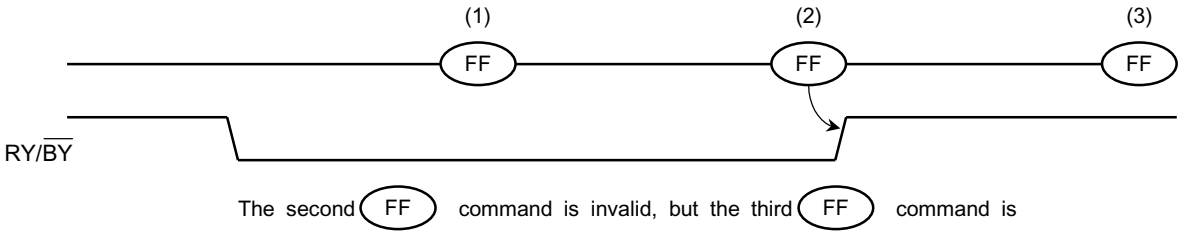
When a Status Read command (70H) is input after a Reset

Figure 11.



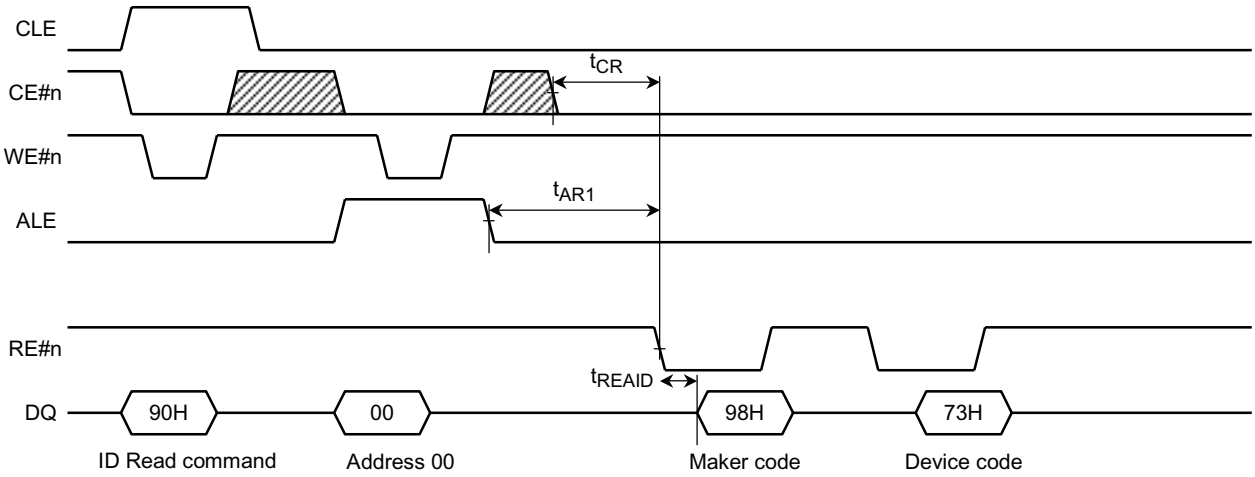
When two or more Reset commands are input in succession

Figure 12.



ID Read

The TH50VPN5640EBSB contains ID codes which identify the device type and the manufacturer.
The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAID}, t_{CR} and t_{AR1} refer to the AC Characteristics.

Figure 13. ID Read timing

Table 6. ID Codes read out by ID read command 90H

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	1	1	1	0	0	1	1	0	E6H

APPLICATION NOTES AND COMMENTS

(13) Power-on/off sequence:

The WP#n signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The WP#n signal may be negated any time after the V_{CC} reaches 2.5 V and CE#n signal is kept high in power up sequence.

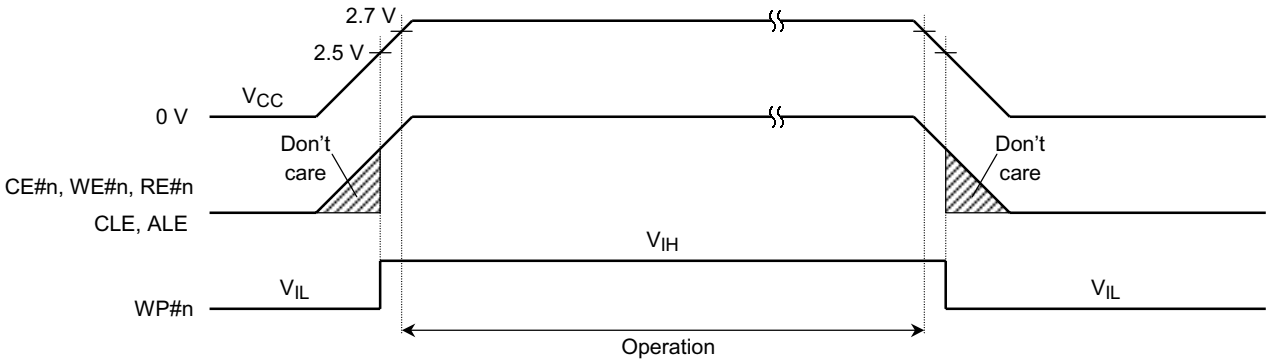
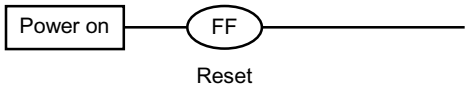


Figure 15. Power-on/off Sequence

In order to operate this device stably, after V_{CC} becomes 2.5 V, it recommends starting access after about 200 μs.

(14)Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.



Figure

(15) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

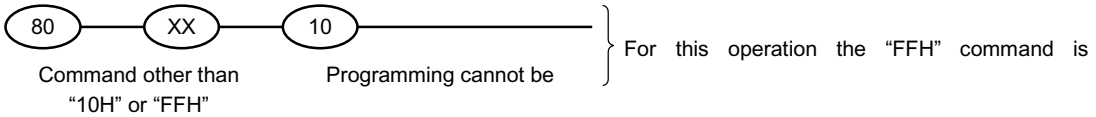
(16) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(17) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Program Execution command "10H" or the Reset command "FFH".

If a command other than "10H" or "FFH" is input, the Program operation is not performed.



(18) Status Read during a Read operation

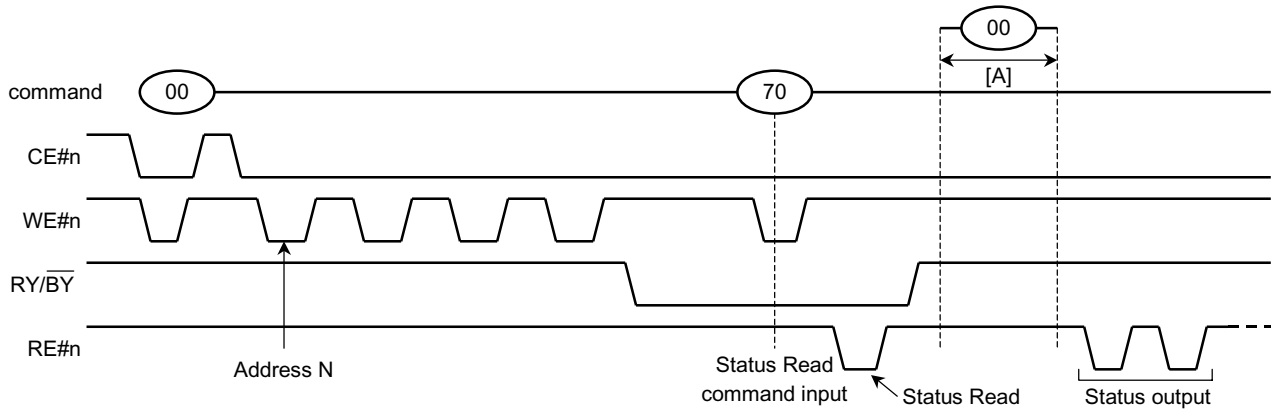


Figure 18.

The device status can be read out by inputting the Status Read command "70H" in Read mode.

Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(19) Pointer control for “00H”, “01H” and “50H”

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 8. Pointer Destination

Read Mode	Command	Pointer
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527

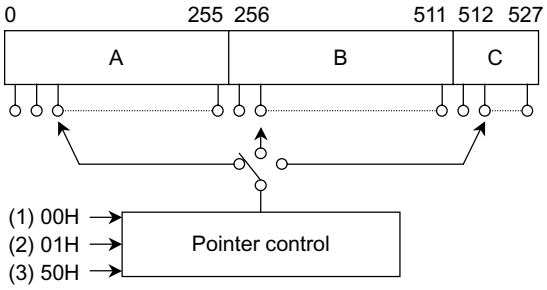
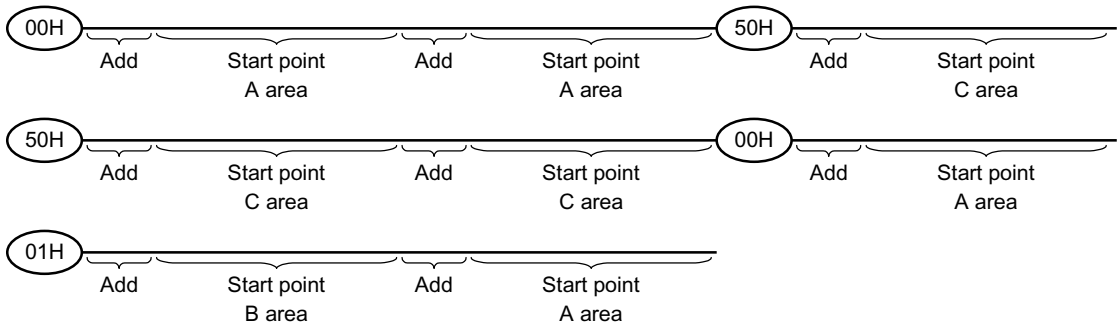


Figure 19. Pointer control

The pointer is set to region A by the “00H” command, to region B by the “01H” command, and to region C by the “50H” command.

(Example)

The “00H” command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50H command.

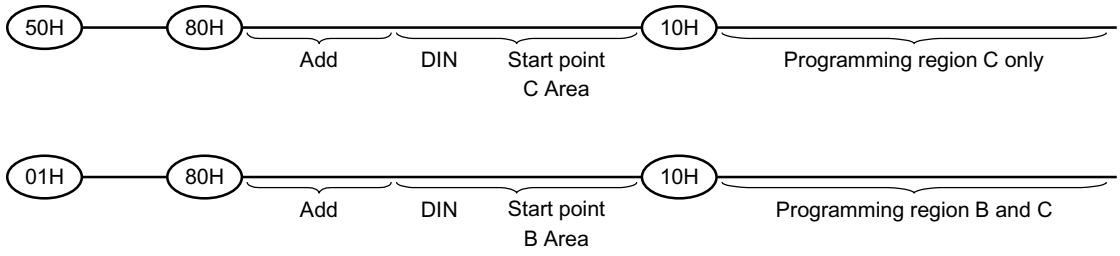


Figure 20. Example of How to Set the Pointer

(20) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.

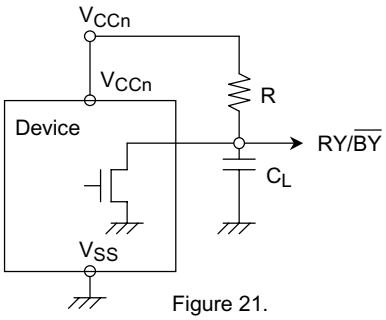
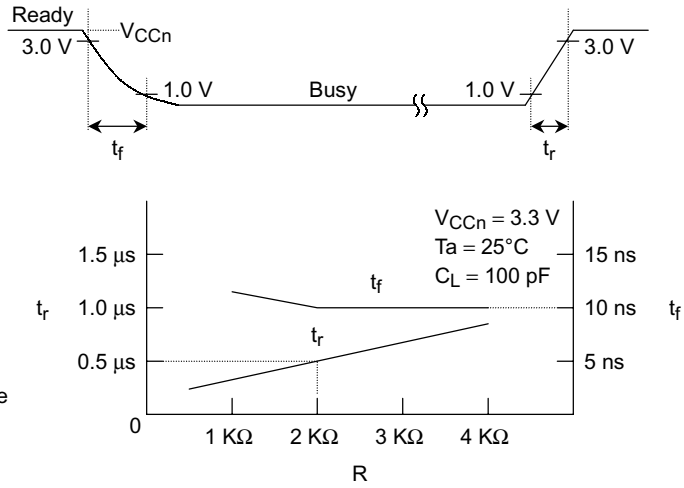


Figure 21.

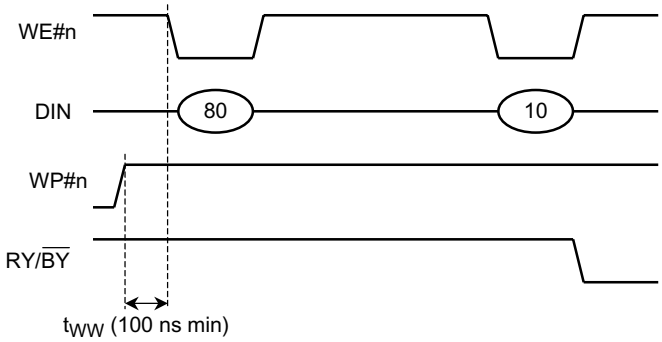
This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.



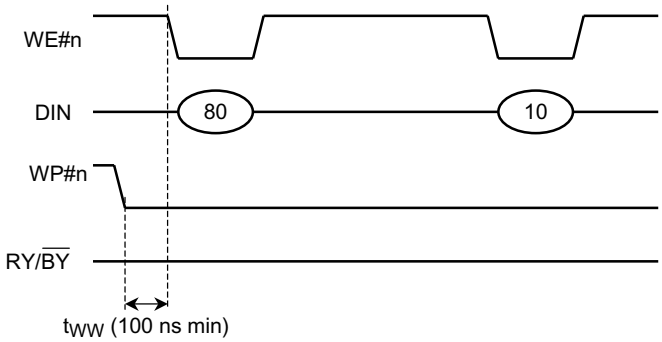
(21) Note regarding the WP#n signal

The Erase and Program operations are automatically reset when WP#n goes Low. The operations are enabled and disabled as follows:

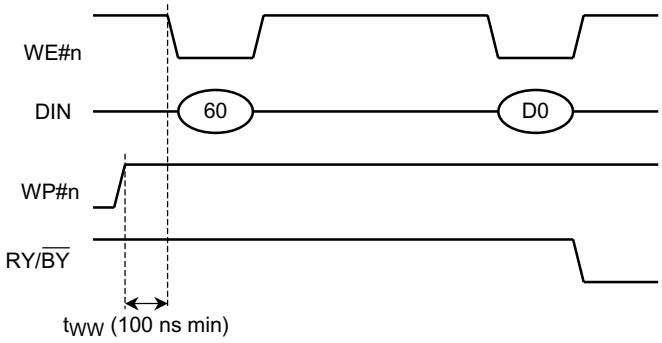
Enable Programming



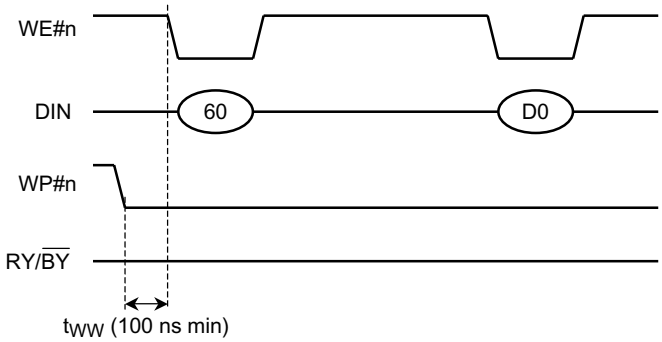
Disable Programming



Enable Erasing



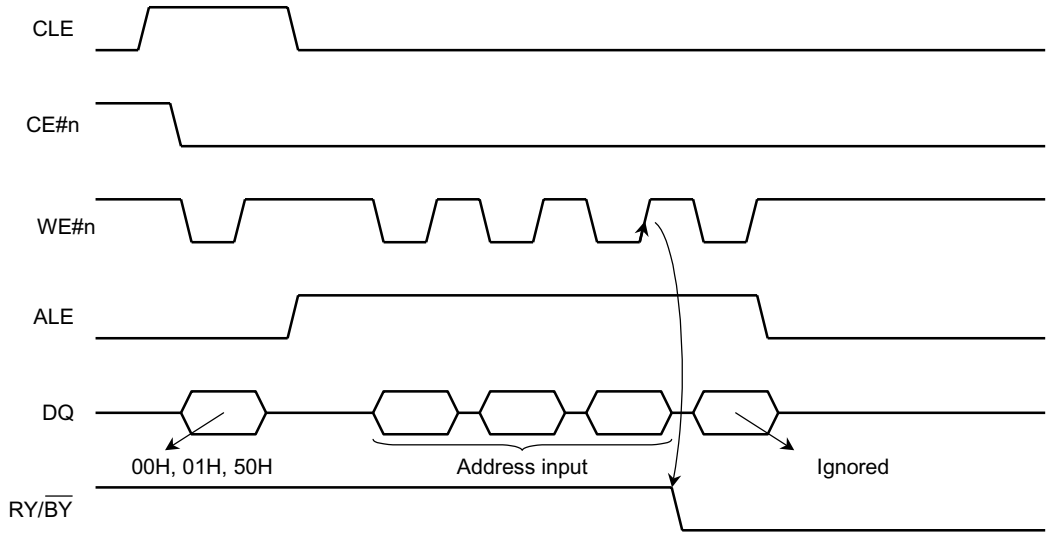
Disable Erasing



(22) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when WE#n goes High in the third cycle.

Figure 22.

Program operation

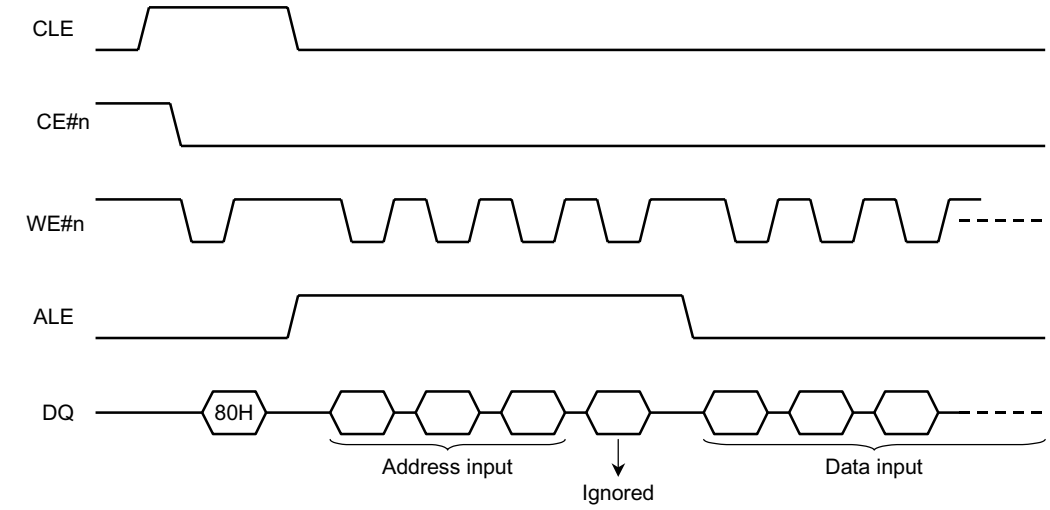


Figure 23.

(23) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as follows:

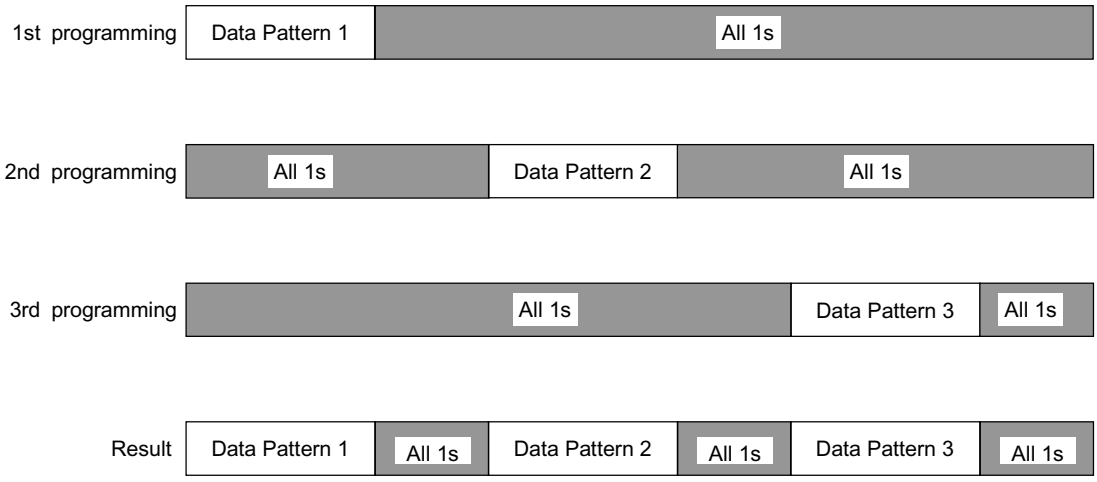


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1"
(i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all "1").

(24) Note regarding the RE#n signal

RE#n The internal column address counter is incremented synchronously with the RE#n clock in Read mode. Therefore, once the device has been set to Read mode by a "00H", "01H" or "50H" command, the internal column address counter is incremented by the RE#n clock independently of the address input timing, If the RE#n clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 25.)

Hence the RE#n clock input must start after the address input.

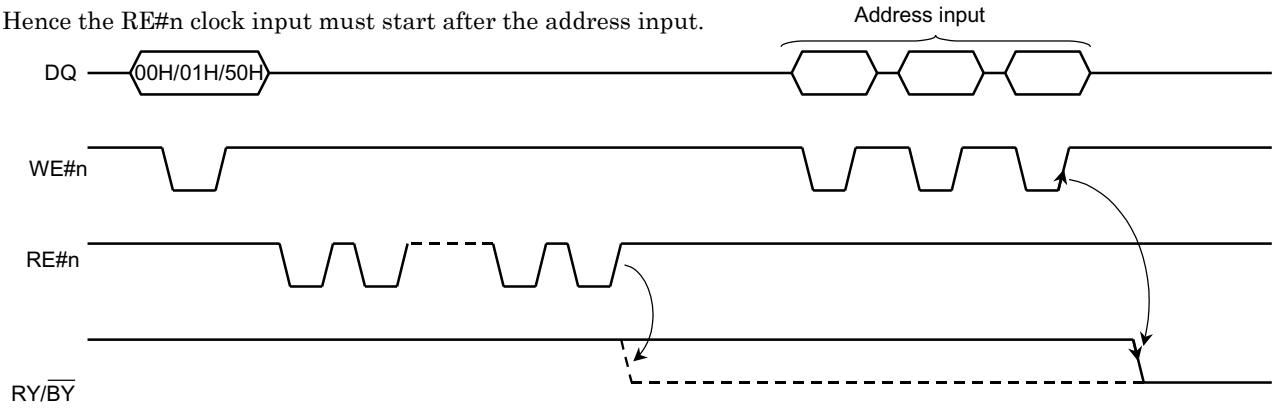


Figure 25.

(25) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

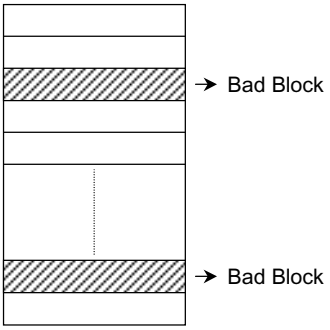


Figure 26.

At the time of shipment, all data bytes in a Valid Block are FFH. For Bad Block, all bytes are not in the FFH state. Please don't perform erase operation to Bad Block.

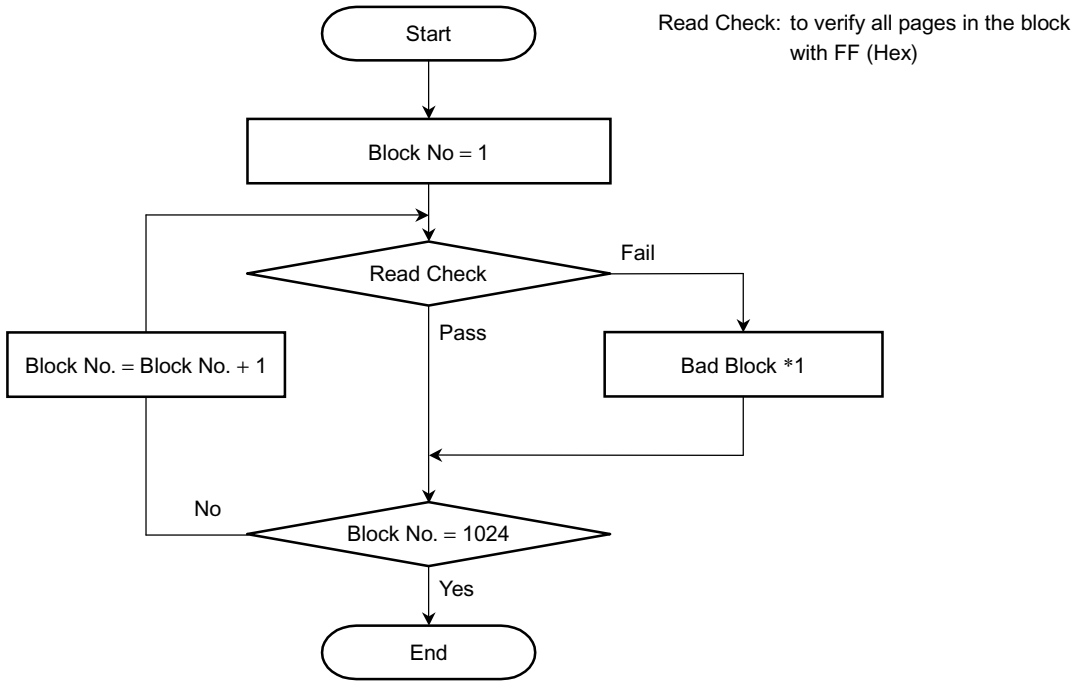
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1014	—	1024	Block

Bad Block Test Flow



*1: No erase operation is allowed to detected bad blocks

Figure 27

(26) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	(1) Block Verify after Program → Retry
		(2) ECC

- ECC: Error Correction Code
- Block Replacement

Program

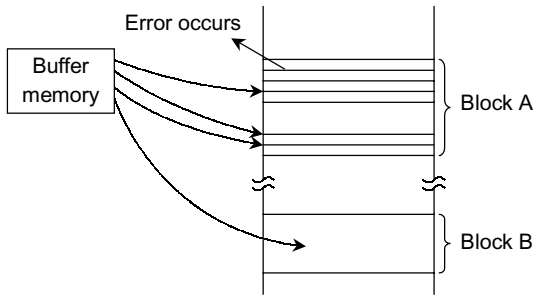


Figure 28.

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

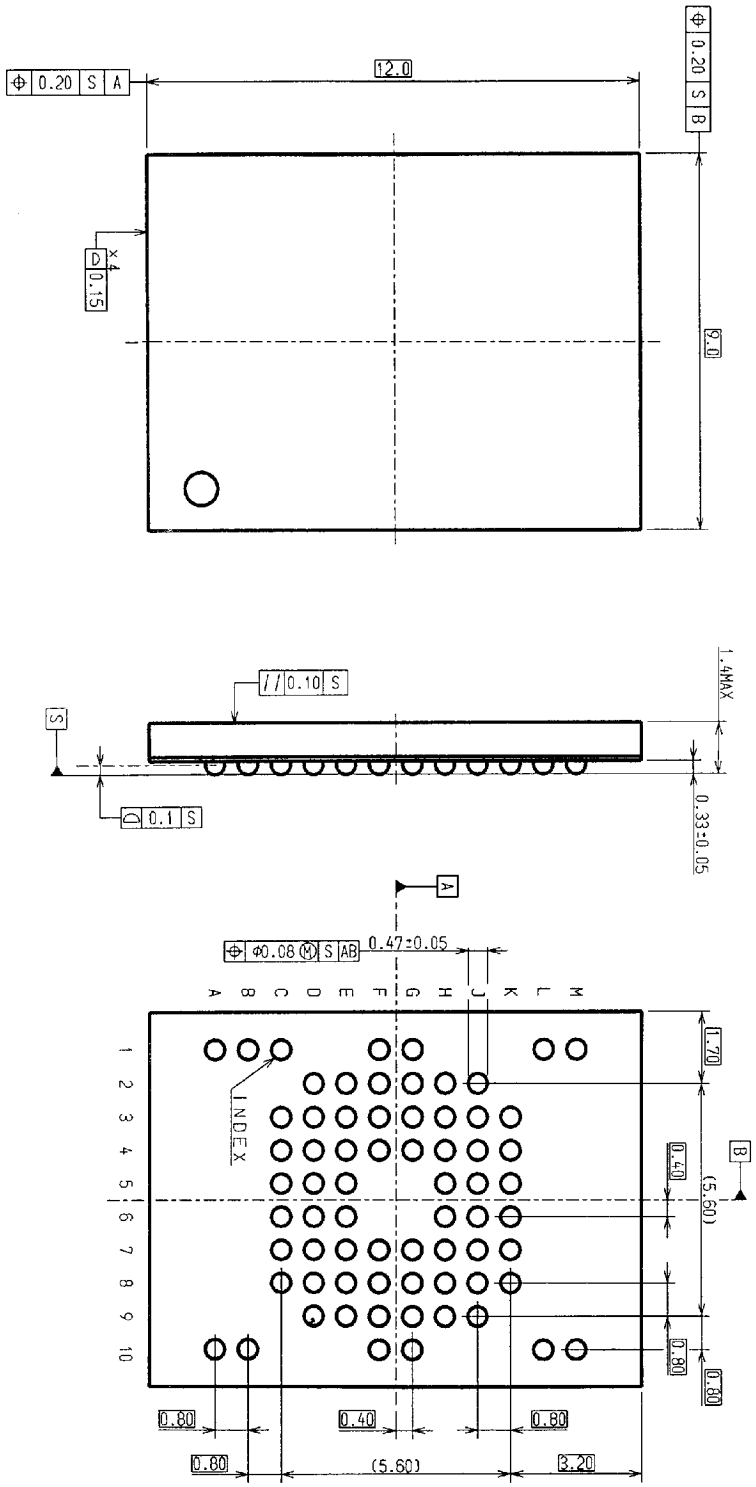
Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

PACKAGE DIMENSIONS

Unit: mm

P-FBGA69-1209-0.80A3



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