ML2517

Preliminary

Analog-Storage Single-chip Record/Playback LSI with 4M Bit-Cell Flash Memory

■ General Description

Thanks to a newly developed Analog Multi-Level Storage technology, the ML2517 stores non-compressed analog source signals directly into an on-chip 4M Bit-Cell Flash memory. The result is superb sound quality without the noise and distortions introduced through coding and decoding, and an impressive long-time record/playback capability of up to 17 minutes. The ML2517 is fully controllable by an external MCU via the industry standard SPI (Serial Peripheral Interface).

In addition, the no backup requirement and the low operating voltage (2.7 to 3.3 V) make the ML2517 an ideal choice for compact, handy and portable terminals. The ML2517 is a true single-chip solution for a record/playback subsystem practical for use with today's size-critical electronic products.

■ Features

- **On-chip non-volatile 4M bit-cell Flash memory**

  Program/Erase Cycles : 10,000 cycles
  Data Retention : 10 years

- **MCU Interface**

  Serial Peripheral Interface (SPI; Mode 0 and Mode 1)

- **Record/Playback Time Length (With the int. Osc. or ext. clock at 8.192 MHz)**

  ap. 640 sec (At fsam = 6.4 KHz)
  ap. 723 sec (At fsam = 5.3 KHz)
  ap. 1,024 sec (At fsam = 4.0 KHz)

- **Selectable Sampling Frequencies**

  4.0 KHz, 5.3 KHz, 6.4 KHz (guaranteed)
  4.0 KHz, 5.3 KHz, 6.4 KHz, 8.0KHz (target)

- **Dual record/play mode**

  1. Sequential record/play mode
  2. Random access record/play mode

- **Dual mode storage of analog and/or digital data**

  Digital storage size is variable from 2Kbit to 4Mbit.
  2Kbit data write time : ap. 406 msec (using **WRDT1** command)
  4Kbit data write time : ap. 531 msec (using **WRDT2** command)
  2Kbit data read time : ap. 380 msec

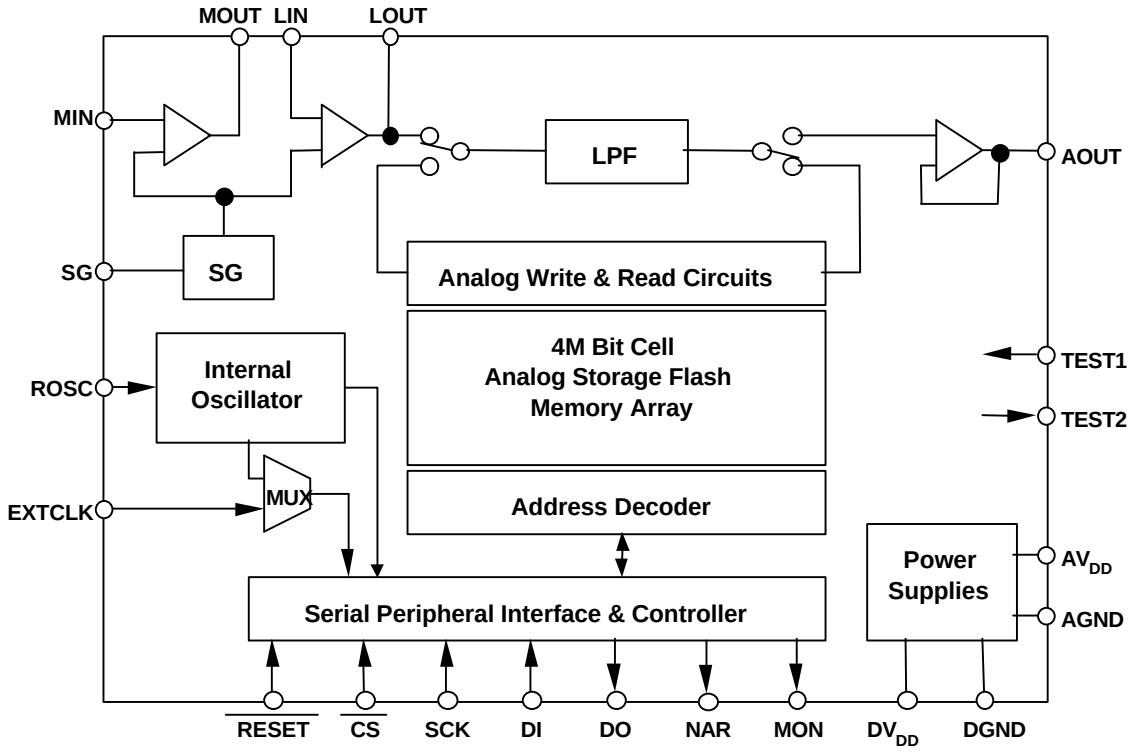
- **Built-in microphone amplifier**
- **Built-in LPF / Smoothing Filter (LPF attenuation – 40dB/oct)**

  Cutoff frequency scales with oscillator and sampling frequency
- **Built-in Oscillation Circuit, No oscillator required**

  Optional external clock input (Clock Frequency 1.0 MHz to 8.192 MHz)
- **Power Supply : 2.7 to 3.3 V**
- **Package : 32-pin Plastic SOP (SOP32-P-525-1.27K)**
- **Operating Temperature : –10°C to +70°C (guaranteed)**

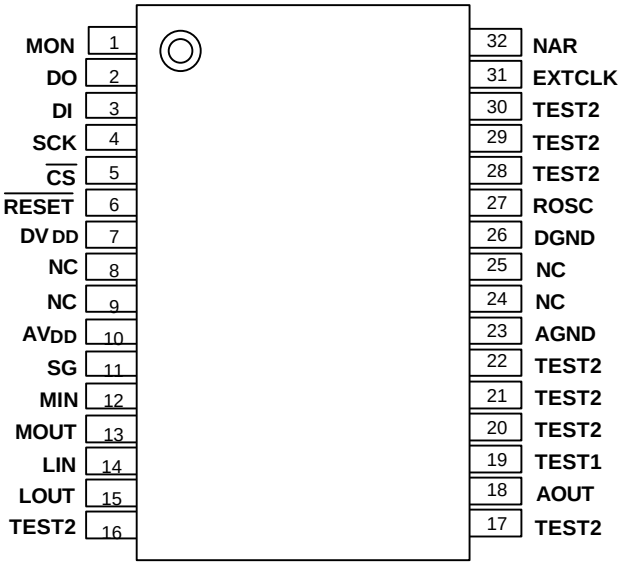
  : –40°C to +85°C (target)

■ BLOCK DIAGRAM



■ PIN COFIGURATION (TOP VIEW)

32-pin Plastic SOP
(SOP32-P-525-1.27-K)



NC : No connection. (Keep NC pins open.)

■ PIN DESCRIPTION

Pin	Symbol	Type	Description
6	**$\overline{\text{RESET}}$**	**I**	RESET input pin, resets the serial interface circuit only. A low level input to this pin initializes the serial interface. A low pulse after each power-on reset is required.
5	**$\overline{\text{CS}}$**	**I**	Chip select pin. A low level input enables data input/output through the serial interface.
4	**SCK**	**I**	Shift clock input pin for the DI and the DO pins.
3	**DI**	**I**	Serial input pin for command data.
2	**DO**	**O**	Serial output pin for status data.
32	**NAR**	**O**	Outputs a high level when the next address input is acceptable during the Random Access Mode.
1	**MON**	**O**	Outputs a high level during recording/playback operations, erase operations, and digital data read/write operations.
31	**EXTCLK**	**I**	External clock input pin. Allowable clock frequency range is 1.0 MHz to 8.192 MHz. When an external clock is not used and an internal oscillation clock in used, connect this pin to the DGND.
27	**ROSC**	**I**	Insert a 33kΩ resistor (±1% tolerance) between this pin and the DGND pins. Also, in external clock input case's, insert a resistor. The frequency of the internal oscillation circuit is determined by this resistor.
11	**SG**	**O**	Analog reference voltage (Signal Ground Voltage) output pin. Insert a capacitor no larger than 3300 pF between this pin and the AGND pin.
18	**AOUT**	**O**	Analog waveform output. Connect to an amplifier to drive an external speaker.
15	**LOUT**	**O**	Output pin from the internal OP AMP (operational amplifier).
14	**LIN**	**I**	Inverting input pin for the internal OP AMP . Non-inverting input pin is internally connected to SG voltage.
13	**MOUT**	**O**	Output pin from the internal OP AMP .
12	**MIN**	**I**	Inverting input pin for the internal OP AMP . Non-inverting input pin is internally connected to SG voltage.
19	**TEST1**	**I**	Pin for testing the ML2517, must be connected to DGND.
16,17,20, 21,22,28 29,30	**TEST2**	**O**	Pins for testing the ML2517, must be left unconnected.
7	**DV_{DD}**	**-**	Digital power supply pins. Insert a 0.1 μF or larger by-pass capacitor between these pins and the DGND pins
26	**DGND**	**-**	Digital Ground pins.
10	**AV_{DD}**	**-**	Analog power supply pin. Insert a 0.1 μF or larger by-pass capacitor between this pin and the AGND pin.
23	**AGND**	**-**	Analog Ground pin.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +5.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	-	–55 to +150	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0V	2.7 to 3.3	V
Operating Temperature	T_{OP}	-	–10 to +70	°C
External Clock Frequency *1	f_{EXTCLK}	-	1.0 to 8.192	MHz
Connection Register for ROSC pin	R_{ROSC}	-	33 ± 1%	KΩ

*1: Applicable only with external clock

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD} = AV_{DD} = 2.7 V to 3.3 V, DGND = AGND = 0 V, Ta = –10 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
high Input Voltage *1	V_{IH}	DGND=AGND=0V	0.8×V_{DD}	-	-	V
low Input Voltage *1	V_{IL}	-	-	-	0.2×V_{DD}	V
high Output Voltage *2	V_{OH}	I_{OH}=-400µA	V_{DD}-0.3	-	-	V
low Output Voltage *2	V_{OL}	I_{OL}=2mA	-	-	0.45	V
high Input Current *1	I_{IH}	V_{IH}=V_{DD}	-	-	10	µA
low Input Current *1	I_{IL}	V_{IL}=0V	-10	-	-	µA
Operating Current Consumption 1	IDD1	In Recording Operation	-	30	45	mA
Operating Current Consumption 2	IDD2	In Playback Operation	-	20	30	mA
Operating Current Consumption 3	IDD3	In Ready for command	-	5	10	mA
Power down Current Consumption	IDDS	-	-	-	10	µA

*1: Applicable to logic input pins (DI, SCK, $\overline{CS}$, $\overline{RESET}$ and EXTCLK) except ROSC and TEST1 pins.

*2: Applicable to logic output pins (DO, NAR and MON) except TEST2 pin.

Analog Characteristics

$DV_{DD} = AV_{DD} = 2.7V \sim 3.3V$, DGND = AGND = 0V, Ta = -10 ~ +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
OP Amp. Input Impedance *1	R_{INA}	-	1	-	-	MΩ
OP. Amp. Open Loop Gain *2	G_{OP}	f_{IN} = 0 ~ 4 KHz	40	-	-	dB
OP. Amp. Load Resistance *3	R_{OUTA}	-	200	-	-	KΩ
AOUT Load Resistance *4	R_{AOUT}	-	50	-	-	KΩ

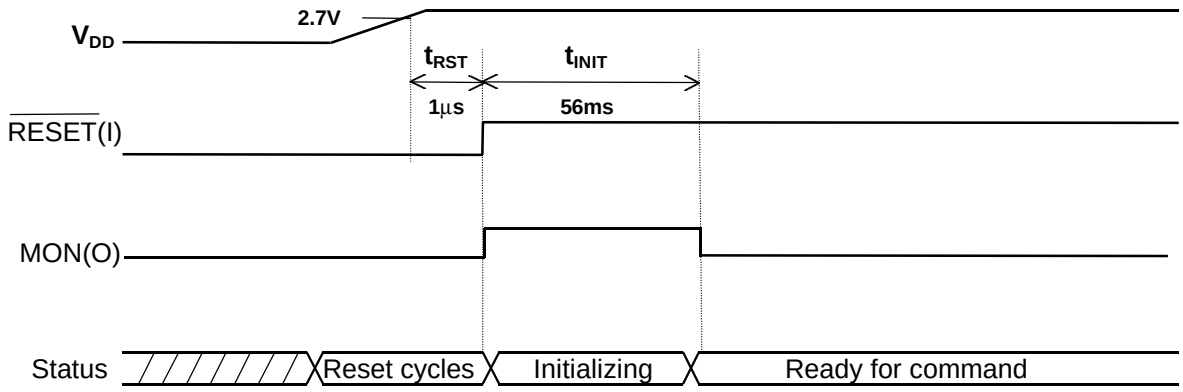
*1: Applicable to MIN and LIN pin.
*2: Applicable to MIN, MOUT, LIN and LOUT pins.
*3: Applicable to MOUT and LOUT pin.
*4: Applicable to AOUT pin.

■ TIMING DIAGRAM

Operational Timing at Power-On

To initialize the internal serial interface circuit of ML2517 after power-on, you must input a low pulse to the **RESET** pin with the timing shown below. The ML2517 enters the initializing cycles by inputting a high level to the **RESET** pin. During the initializing cycles, the ML2517 outputs a high level to the **MON** pin. After the **MON** pin is brought to L level, the ML2517 enters the standby state (Ready status) with the timing shown bellow. In this state the ML2517 accepts command input, for example, ***REC*** or ***PLAY*** command.

Timing for inputting $\overline{\text{RESET}}$ pulse at Power-on



Timing for Power Up and Power Down Operations

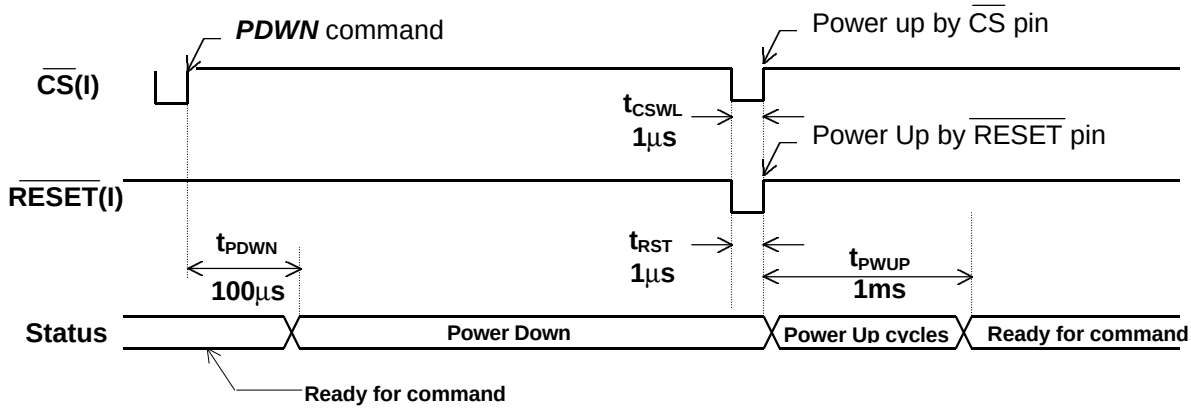
ML2517 stops its oscillation circuit to shift to the power-down state either by the ***PDWN*** command or by receiving a low level on the $\overline{\text{RESET}}$ pin. In the power-down state the ML2517 is in a low power consumption mode.

Two options are available to power up the ML2517 again after power down by the ***PDWN*** command:

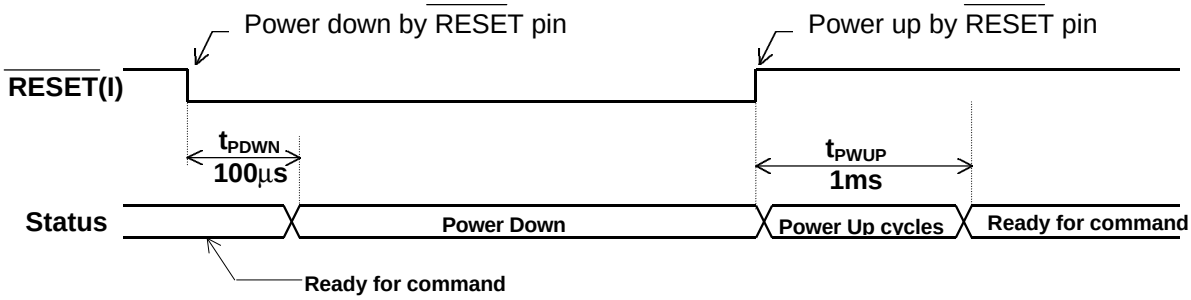
1. Input a low pulse to the $\overline{\text{RESET}}$ pin, or
2. Input a low level to the $\overline{\text{CS}}$ pin.

The following charts show timings for the power up and power down operations.

Timing for power-down operation by using the *PDWN* command



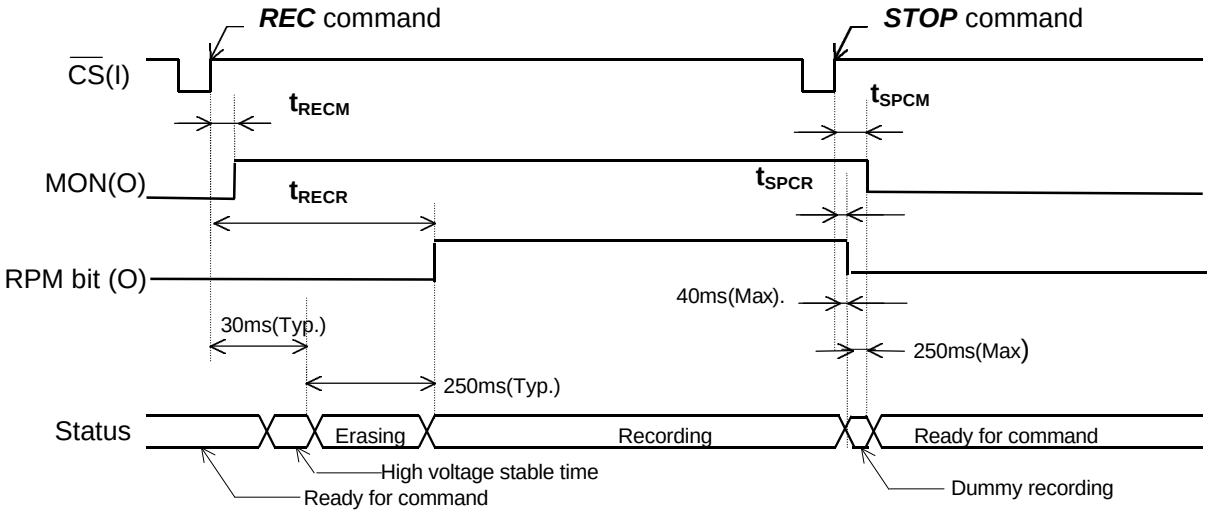
Timing for Power-down operation with the RESET pin



Timing for Record/Playback Operation

1. Timing for Recording Operation

The following chart shows timing for a recording operation at 6.4 KHz sampling frequency. It is assumed that the Start and Stop Addresses are set by the ***STADR*** and ***SPADR*** commands prior to the REC command input.

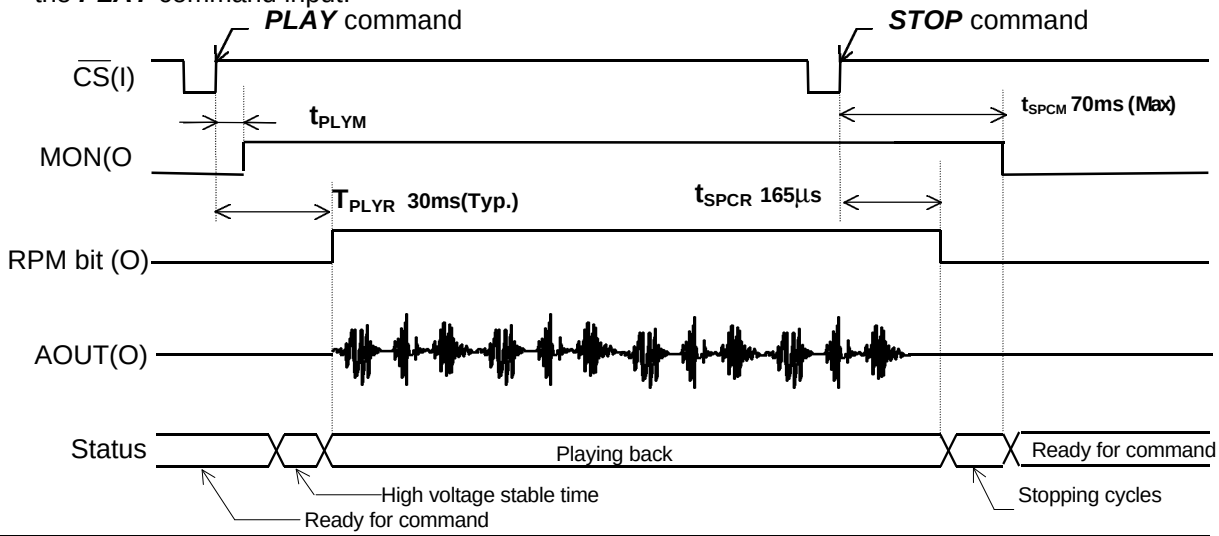


(Note 1) It takes about 280 ms (Typ.) for the ML2517 to start actual recording after the ***REC*** command input, as the ML2517 first erases 1 sector before it can start recording.

(Note 2) When recording is stopped by the ***STOP*** command, the ML2517 continues to record until the last address of the current page is reached. This "lag" recording time is the ***STOP*** command of about 40 ms (Max.). Afterwards, dummy recording is taken place up to the end of the following sector (max. 2 sectors). This dummy recording takes about 250 ms (Max).

2. Timing for Playback Operation

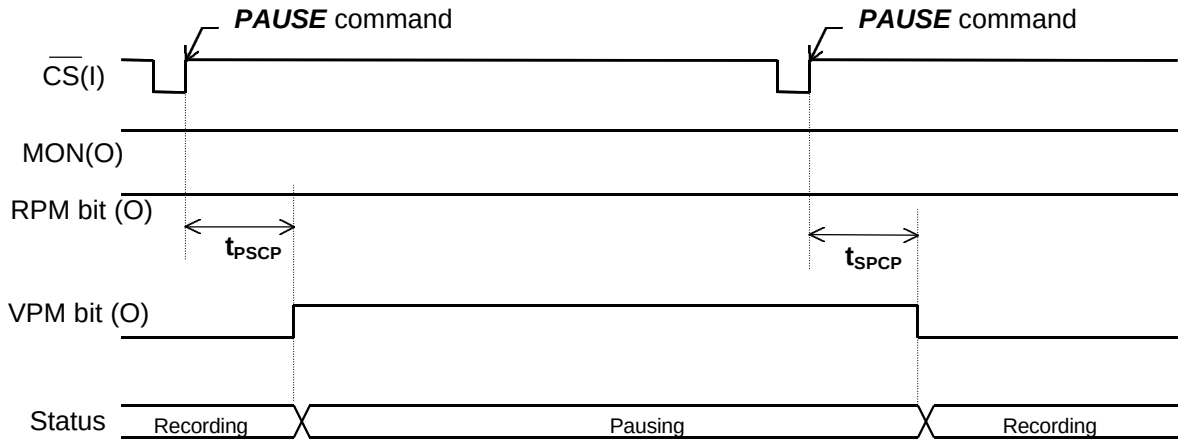
The following chart shows timing for playback operation at 6.4 kHz sampling frequency. It is assumed that the Start and Stop Addresses are set by the ***STADR*** and ***SPADR*** commands prior to the ***PLAY*** command input.

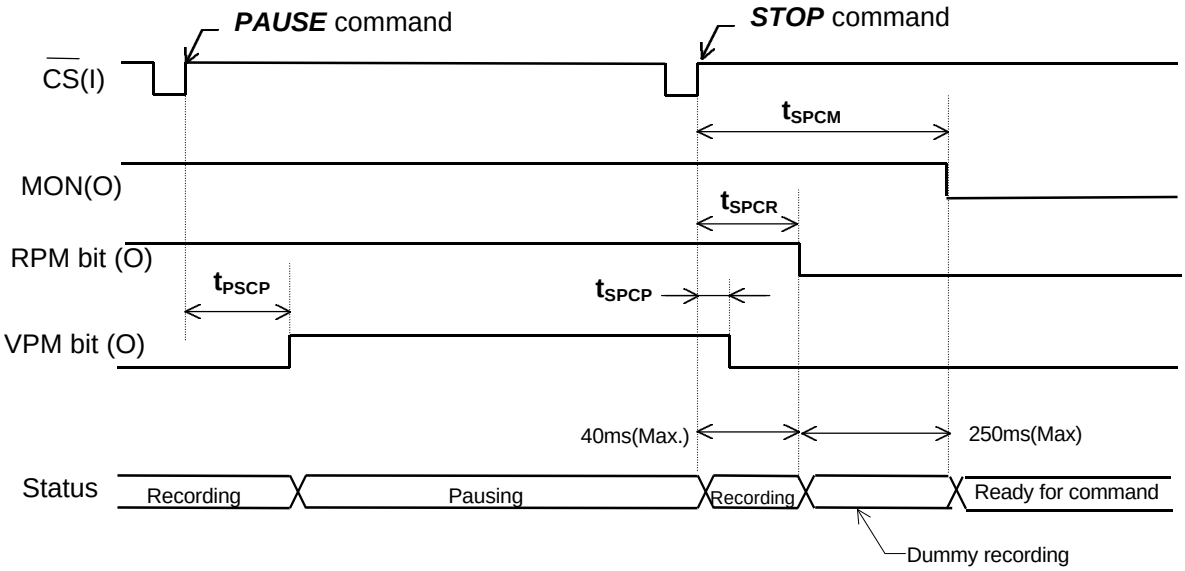


(Note) It takes about 70 ms (Max.) for the ML2517 to stop playback as Stopping cycles after ***STOP*** command input.

3. Timing for Pausing Operation by the *PAUSE* Command

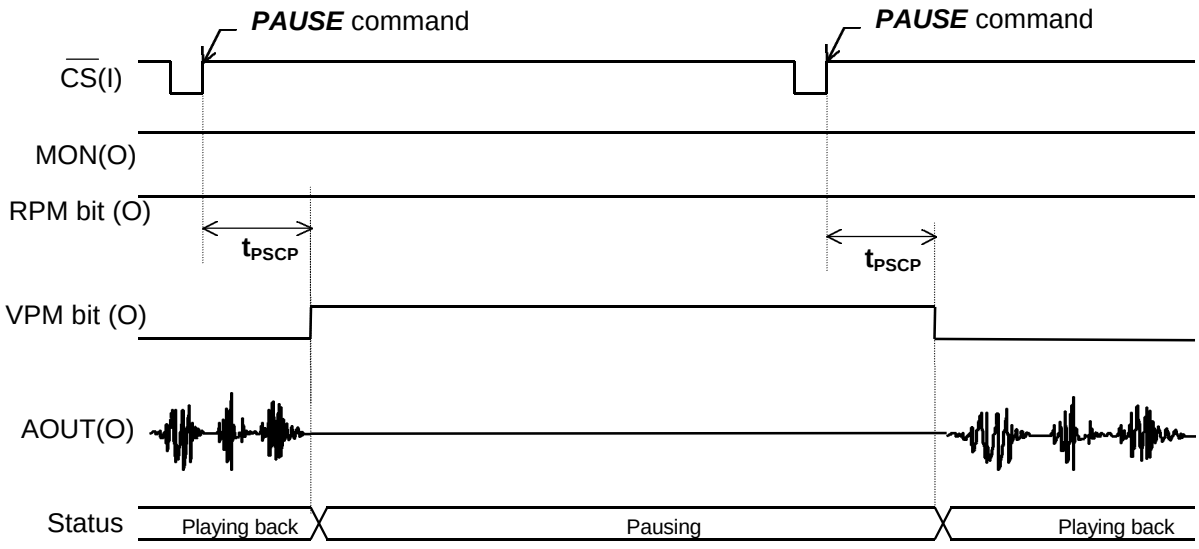
The following charts show timings for pausing recording operation by using the ***PAUSE*** command at 6.4 kHz sampling frequency.

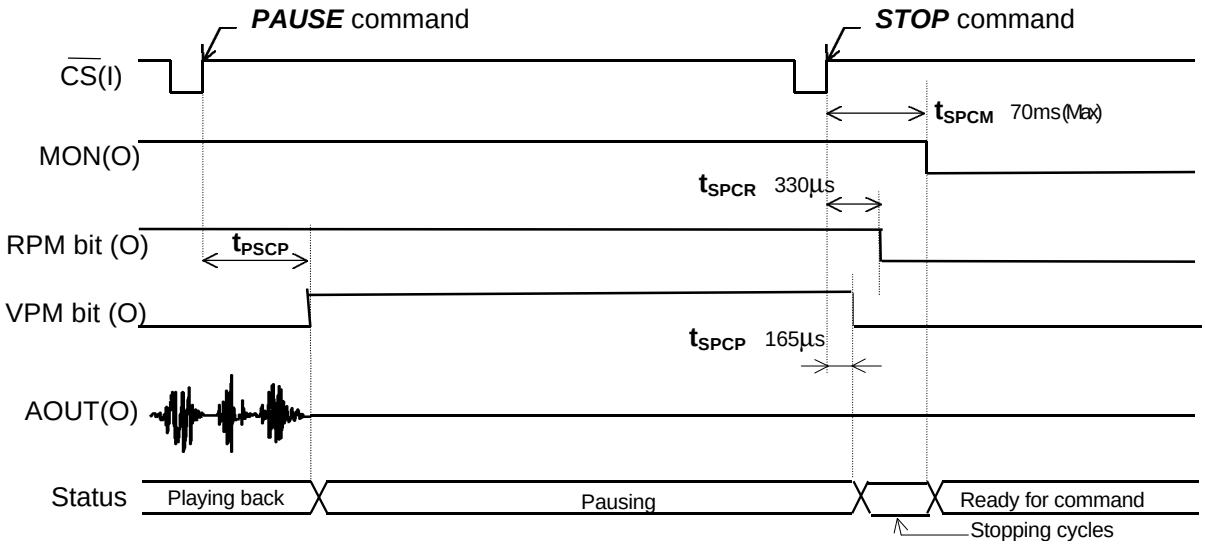




(NOTE) If the ***STOP*** command is input while recording is suspended by the ***PAUSE*** command, the ML2517 resumes recording and keeps on recording until the last address of the current page is reached. This "lag" recording time is about 40 ms (Max.). Afterwards, dummy recording is taken place up to the end of the following sector (max. 2 sectors). This dummy recording takes about 250 ms (Max).

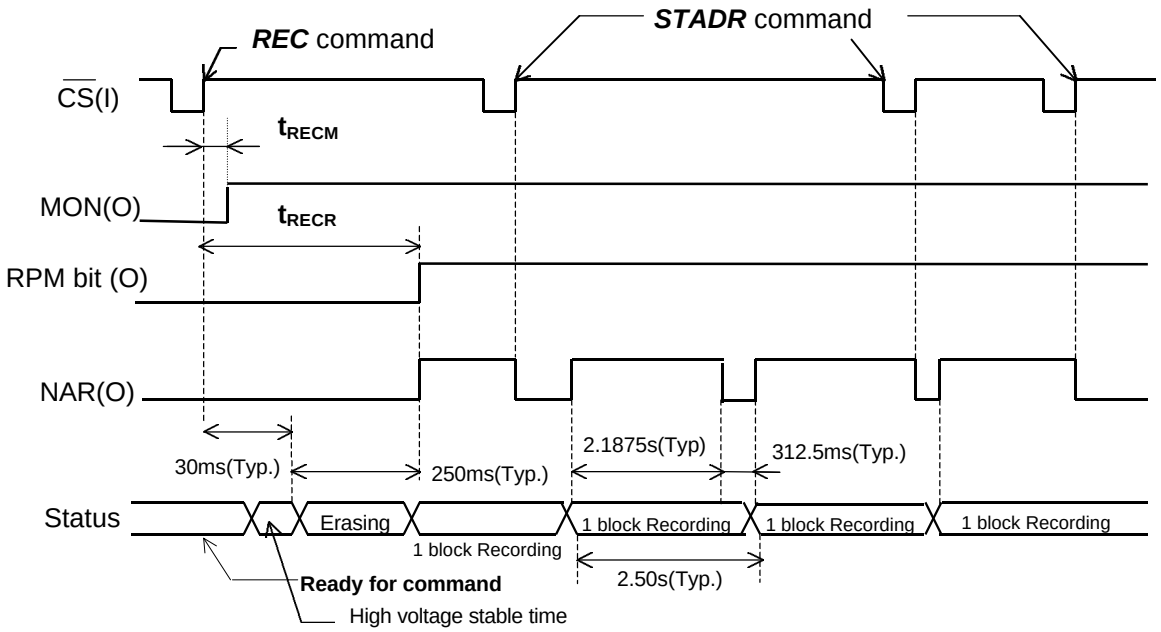
The following charts show timings for pausing playback by using the PAUSE command at 6.4 kHz sampling frequency.





4. Address specification timing in the Random Access Mode

In Random Access Mode, the record/playback addresses are set by a master MCU. The following timing diagram shows the address specification timing for a recording operation (sampling frequency = 6.4 KHz, block size = 8 sectors) This timing diagram is also Applicable to Playback operations and Erase operations as well.



The following are explanations of the **NAR** (Next Address Request) signal status in each operation.

NAR is activated only in Random Access Mode. **NAR** is fixed at a low level in Sequential Mode.

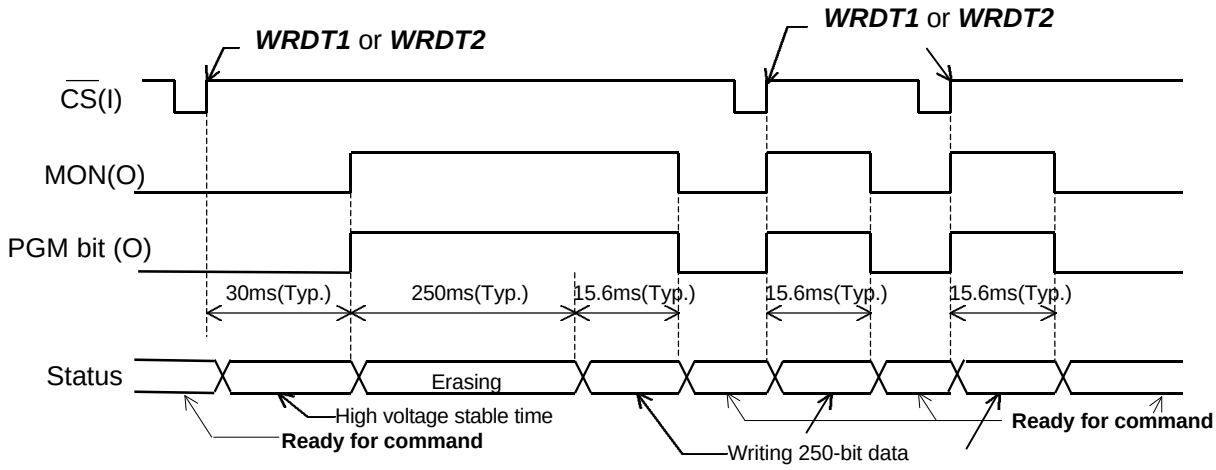
In Random Access Mode, the **NAR** signal goes high when another address request is acceptable after a ***REC***, ***PLAY*** or ***ERASE*** command is sent to the ML2517 , and then goes high again when another address request is acceptable. Successively when the next address is set by a ***STADR*** command, the **NAR** signal goes low again.

The sequence described above is repeated until the stop address specified by the ***SPADR*** command is reached or a ***STOP*** command is received.

If a ***SPADR*** command is not received during the **NAR** signal maintains a high level, the ML2517 starts recording and playback from the following block. The time maintaining a high level on the **NAR** signal indicates that the ML2517 is recording or playback for the number of sectors per 1 block minus 1 sector.

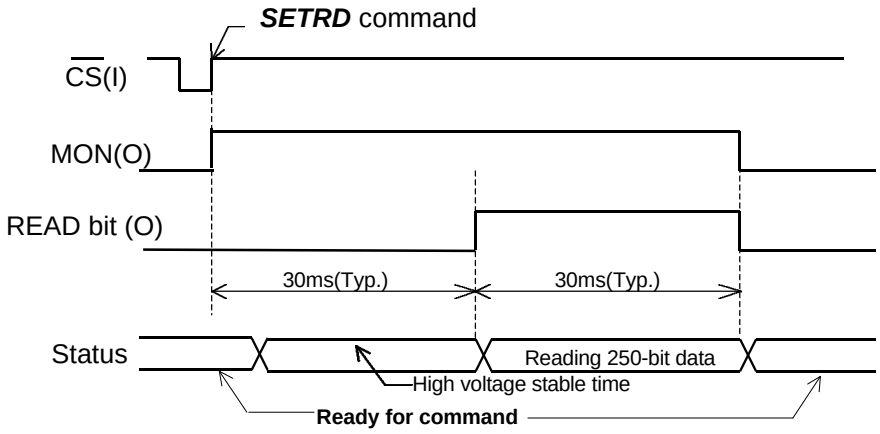
5. Digital data write timing

The digital data write timing diagram is shown below. It is assumed that the Start Addresses is set by the ***STADR*** command prior to the ***WRDT1*** command or ***WRDT2*** command input.



6. Digital data read timing

The timing diagram of a digital data read operation invoked by the ***SETRD*** command diagram is shown below. It is assumed that the Start Addresses is set by the ***STADR*** command prior to the ***SETRD*** command input.

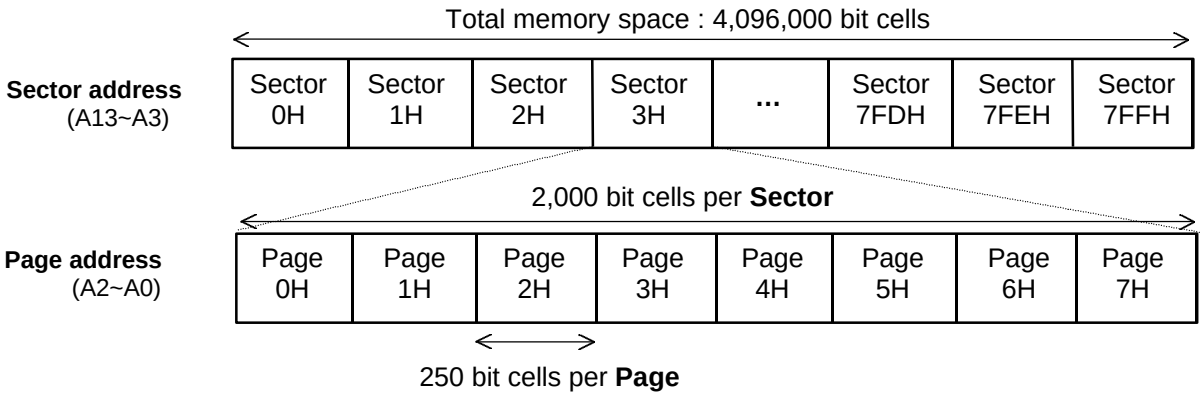


After issuing the ***SETRD*** command, the **MON** signal goes high while reading the 250-bits of data. The master MCU can know the data ready timing by the **MON** signal going low again.

■ Flash Memory Configuration

The ML2517 is equipped with 4Mbit cells (4,096,000 cells). The memory space is classified into 2,048 **sector**s, 2,000 bit cells each. Each sector is divided into 8 **page**s, 250 bit cells each. (See below)

Address bits A13 ~ A3 define the sector addresses, A2~A0 define the page addresses.



Flash Memory addressing

The **Page** is the minimum addressable unit of the ML2517's built in memory management. For some operations, the **Sector** is the minimum addressable unit.

For most operations, the start address must be specified in **Sector** units. (In Random Access Mode described later, the **Block**: multiple sectors are the minimum addressable unit)

On the other hand, the stop address of most operations can be specified in **Page** units.

In this case, the remaining bit cells of the last sector are not usable, unless the sector is erased and re-recorded. More detailed discussion will be made in the following sections.

■ FUNCTIONAL DESCRIPTION

There are two Record/Playback modes provided by the ML2517 as follows.

1. **Sequential Mode**
2. **Random Access Mode**

1. Sequential Mode

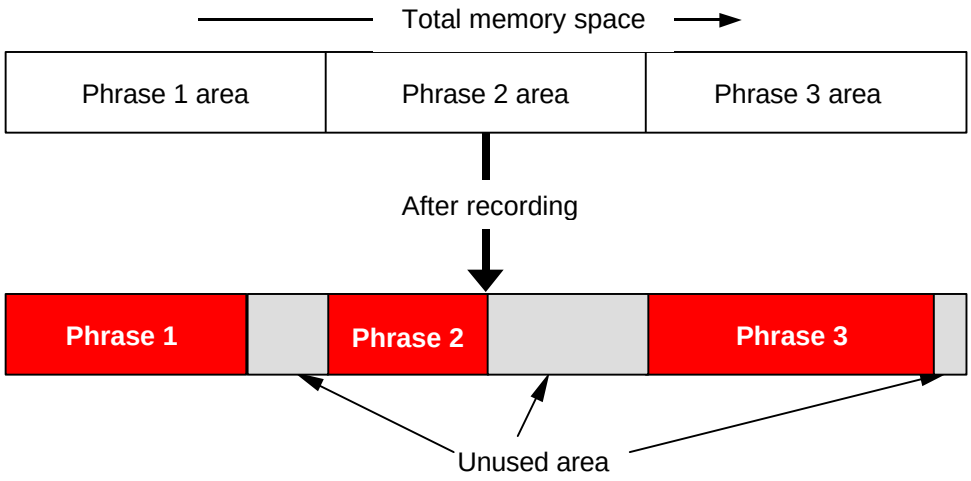
In the Sequential Mode, the ML2517 records or plays back the input signal into or from the flash cells between the specified start-address and stop-address. The stop-address must be larger than start-address.

Using the Sequential Mode, record/playback operation is realized with a simple control procedure.

The start-address in the recording mode can be specified by **Sector** address units (ap. 312.5 msec unit : at 6.4KHz sampling).

The stop-address in the recording mode can be specified by **Page** address units (ap. 39 msec unit : at 6.4KHz sampling). The playback start/stop-addresses can be specified by Page address units.

The following chart shows a sample of memory usage in the Sequential Mode.



Using this method the start and stop addresses of each phrase are stored in the built-in flash memory, this allows the information for the recording area addresses to be retained automatically when the power supply is off.

Flash memory addressing in Sequential Mode

In Sequential Mode, the recording start address is specified in **Sector** units (A13~A3).

The recording stop address and playback start/stop addresses can be specified in **Page** units (A13~A0).

The following table shows the minimum controllable time unit for each sampling frequency.

Addressing	Unit	Unit time for each sampling rate		
		6.4KHz	5.3KHz	4.0KHz
Record start address	A13~A3	312.5msec	377.35msec	500msec
Record stop address Playback start/stop address	A13~A0	39.06msec	46.88msec	62.5msec

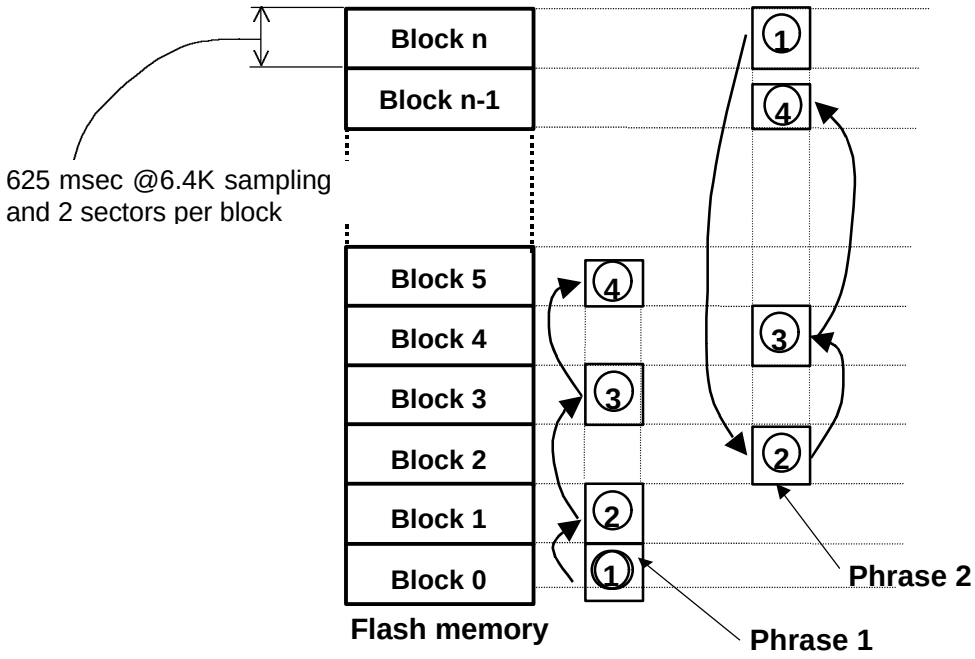
2. Random Access Mode

The Random Access Mode uses the memory in **Block** units and can specify the recording **Blocks** in random order. This mode is suitable to record and playback phases of a variable length of voice (or sound) without wasting memory.

Usually with a voice messaging system (such as two way pager, voice memo system etc.), different length messages are recorded, erased and re-recorded. The Random Access Mode is provided for such kinds of applications.

The start-address is specified by **Block** units, and is specified before recording into a new **Block**. Four different **Block** sizes can be selected.

Recording can start at any specified **Block**. Recording can continue, hopping to any specified **Block**s in random order, until the memory is filled.



By providing a **TOC** (Table of Contents) in the flash memory, recorded data information can be kept even when the power supply is off.

Recorded analog data is inherently retained through power cycles due to the non volatile flash memory technology. The host MCU can reserve some blocks to use as a **TOC.** These blocks can be used by the host MCU as data sectors to retain this sector allocation information through power cycles.

Flash memory addressing in Random Access Mode

In Random Access Mode , the record start address is specified by **Sector** address units (A13**~**A3). The record stop address is specified by **Page** address units (A13**~**A0). The playback start/stop-addresses are specified by **Page** address units. The next record/playback addresses are specified by **Block** address units after the ML2517 starts recording or playback.

Each **Block** is several numbers of continuous **Sector**s. The number of sectors in one Block is defined by the ***MODE*** command, one of four **Block** size is selectable (2 **Sector**s~16 **Sector**s / **Block**)

For more details, refer to the ***MODE*** command description.

The following table shows the minimum controllable time unit for each sampling frequency.

Addressing	Sectors/Block	Addressing range	Minimum controllable time unit		
			6.4KHz	5.3KHz	4.0KHz
Record start address	——	A13~A3	312.5msec	377.35msec	500msec
Recording start address (Block unit)	2 Sectors	A13~A4	625msec	750msec	1.0sec
	4 Sectors	A13~A5	1.25sec	1.5sec	2.0sec
	8 Sectors	A13~A6	2.5sec	3.0sec	4.0sec
	16 Sectors	A13~A7	5.0sec	6.0sec	8.0sec
Record stop address Playback start/stop address		A13~A0	39.06msec	46.88msec	62.5msec

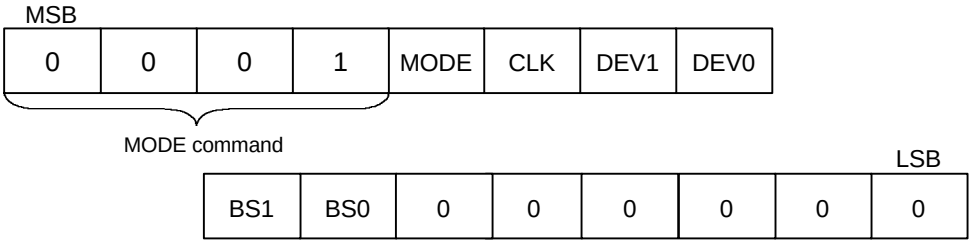
■ Control commands

ML2517 is controlled by receiving the following commands from a master MCU through a **SPI** serial communication link. This is a synchronous protocol, so 4 or 8 bit MCUs can send these commands in groups of whatever bit width is most convenient. 16, 32, or 64 bit MCUs can create 4, 8, …, bit width commands with the CS signal (bits shifted into the ML2517 when CS is false are ignored).

1. *MODE* command (1H)

The ***MODE*** command and the succeeding 12-bits of data specify the record/playback mode, clock mode, external clock dividing rate, and the block size for the Random Access Mode.

The latter half of the succeeding 12-bit data (last 6 bits) must be “0” because these bits are used for internal circuit testing.



MODE	Record/playback mode
0	Sequential Mode
1	Random Access Mode

CLK	Clock mode
0	Internal clock
1	External clock

DEV1	**DEV0**	External clock divide ration
0	0	No divide
0	1	1/2
1	0	1/4
1	1	1/8

BS1	**BS0**	Block size
0	0	2 sectors
0	1	4 sectors
1	0	8 sectors
1	1	16 sectors

After power-on reset, all data bits are initialized to “0”.

Please note that the reset pulse input to the $\overline{\text{RESET}}$ pin never changes these mode data bits, all data bits keep the previous status.

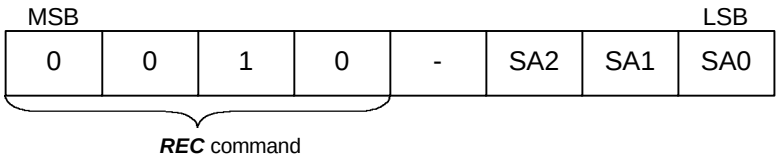
When using the external clock mode, divided clock frequency must be 1.024MHz.

2. *REC* command (2H)

The ***REC*** command and the succeeding 4-bit data initiate recording. This command can be used with either the Sequential Mode or the Random Access Mode. Recording starts at the specified start-address and continues to the specified stop-address or terminates if a ***STOP*** command is received.

The succeeding 4-bit data is to define a sampling frequency, as shown in the table below. When the sampling frequency is not defined with this command, recording is made at the last defined sampling frequency.

When reset and powered up, recording is set at 6.4 kHz the default sampling frequency.



SA2	SA1	SA0	Sampling frequency
0	0	0	4.0KHz
0	0	1	5.3KHz
0	1	0	6.4KHz (default)
0	1	1	**Do not use this value** * Note 1
1	0	0	1.0KHz
1	0	1	2.0KHz
1	1	0	2.67KHz
1	1	1	3.2KHz

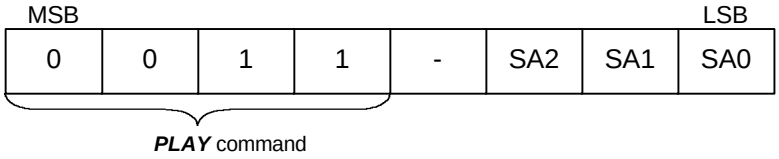
Note 1: The proper operation is not guaranteed by setting this value

3. *PLAY* command (3H)

The ***PLAY*** command and the succeeding 4-bits of data initiate playback. This command can be used with either the Sequential Mode or the Random Access Mode. Playback starts at the specified start-address and continues to the specified stop-address or terminates after a ***STOP*** command is received.

The succeeding 4-bits of data are to define a sampling frequency, same as with the ***REC*** command. When the sampling frequency is not defined with this command, playback is made at the last defined sampling frequency.

When reset and powered up, playback is set at 6.4 kHz the default sampling frequency.

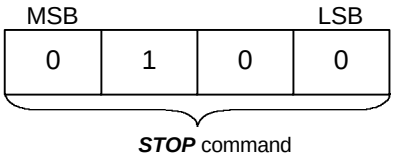


SA2	SA1	SA0	Sampling frequency
0	0	0	4.0KHz
0	0	1	5.3KHz
0	1	0	6.4KHz (default)
0	1	1	**Do not use this value** * Note 1
1	0	0	1.0KHz
1	0	1	2.0KHz
1	1	0	2.67KHz
1	1	1	3.2KHz

Note 1: The proper operation is not guaranteed by setting this value

4. *STOP* command (4H)

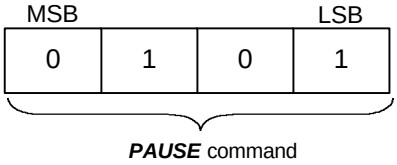
Record or playback stops after a ***STOP*** command is received. This command can be used either with the Sequential Mode or the Random Access Mode. Any data following this command is disregarded.



5. *PAUSE* command (5H)

The host MCU can temporarily suspend record or playback by the ***PAUSE*** command. This command can be used with either the Sequential Mode or the Random Access Mode. Any data following this command is disregarded.

Re-issuing this command resumes the suspended operation. If the ***STOP*** command is issued while pausing, the pause state is also stopped.

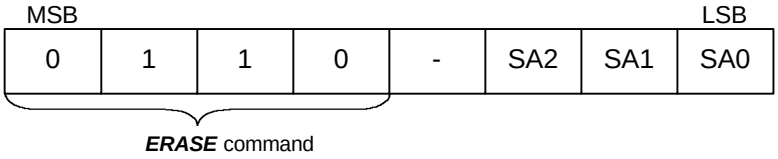


6. *ERASE* command (6H)

The ***ERASE*** command and the succeeding 4-bits of data, erase the recorded data in the specified address area. This command can be used with either the Sequential Mode or the Random Access Mode. "*Erase the recorded data*" means storing silent data.

The succeeding 4-bits of data define a sampling frequency, same as with the ***REC*** command. When the sampling frequency is not defined with this command, it is set to the last defined sampling frequency.

When reset and powered up, erase is set at 6.4 kHz the default sampling frequency.



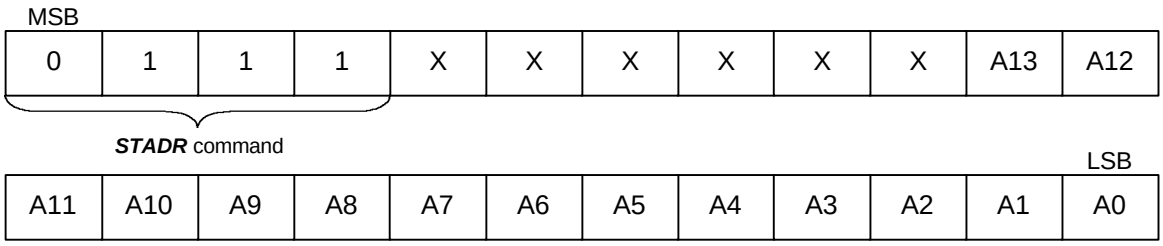
SA2	SA1	SA0	Sampling frequency
0	0	0	4.0KHz
0	0	1	5.3KHz
0	1	0	6.4KHz (default)
0	1	1	**Do not use this value** * Note 1
1	0	0	1.0KHz
1	0	1	2.0KHz
1	1	0	2.67KHz
1	1	1	3.2KHz

Note 1: The proper operation is not guaranteed by setting this value

7. *STADR* command (7H)

The ***STADR*** command and the succeeding 14-bits of data specify the start-address for record or playback operations of the Sequential Mode or the Random Access Mode. This command is also used to specify the start-address for digital read or write operations.

The ***STADR*** command should be issued before ***REC***, ***PLAY***, ***ERASE***, ***WRDT1***, ***WRDT2*** and ***SETRD*** commands. When this command is not issued prior to the commands described above, the operation starts at the last defined start-address. After resetting or power-on, the start-address is set to the memory's starting address by default.



In the Sequential Mode, A0 through A2 for Page addresses are ignored because the record start address is specified by Sector address units. In addition , the playback start-address is specified by Page address units and all address data is valid.

In the Random Access Mode ,A0 through A2 for Page addresses are ignored because the record start address is specified by Sector address units. In addition , the playback start-address is specified by Page address units and all address data is valid. The next record/playback addresses are specified by Block address units after the ML2517 starts recording or playback. And the following addresses are ignored depending on the block size.

Block size	Ignored bits
2 sector / block	A0 ~ A3
4 sectors / block	A0 ~ A4
8 sectors / block	A0 ~ A5
16 sectors / block	A0 ~ A6

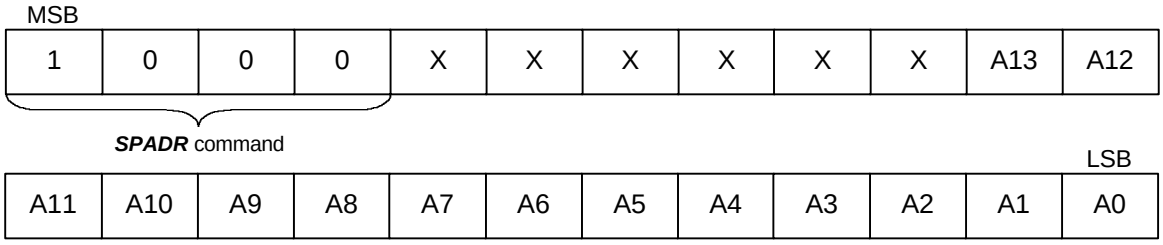
In the ***WRDT1*** command, A0 ~ A2 are ignored.

In the ***WRDT2*** command, A0 ~ A3 are ignored.

8. *SPADR* command (8H)

The ***SPADR*** command and the succeeding 14-bits of data specify the stop-address for record or playback operations of the Sequential Mode or the Random Access Mode.

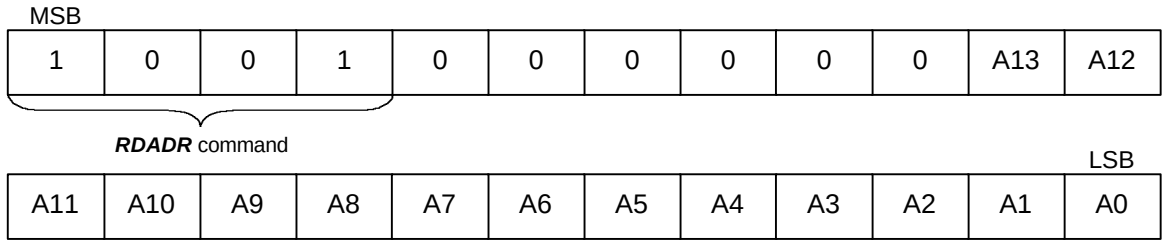
The ***SPADR*** command should be issued before the ***REC***, ***PLAY*** and ***ERASE*** commands. If this command is not issued prior to the commands described above, the operation starts at the last defined stop-address. After resetting or power-on, the stop-address is set to the memory's last (highest) address by default.



9. RDADR command (9H)

The ***RDADR*** command is used to read the contents of the current memory address counter. This command can be used with either the Sequential Mode or the Random Access Mode.

When the ML2517 receives this command and the following the 6-bits of dummy “0” bits, 14 bits of memory address counter contents appear sequentially at the DO pin synchronized with the SCK clock falling edge (read the data at the rising edge).



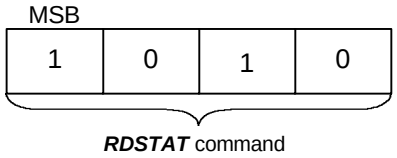
This command is provided to allow the master MCU to know the current memory counter address. This can be important for flexible control of the memory usage.

The ***RDADR*** command can be used during record, playback, and erase operations or the pausing state of each of these operations. Please note that the address specified by ***STADR*** command or ***SPADR*** command is returned if the ***RDARD*** is executed right after the ***STADR*** command or ***SPADR*** command execution.

10. *RDSTAT* command (AH)

This command requests the ML2517 to read the internal status register through the serial interface. Each bit of the internal status register is assigned as below.

When the ***RDSTAT*** command is executed, 3 bits of dummy data are sent from the DO pin synchronized with the SCK clock input. Successively, 9 bits of the internal status register contents are sent through the DO pin sequentially, MSB first.



LSB

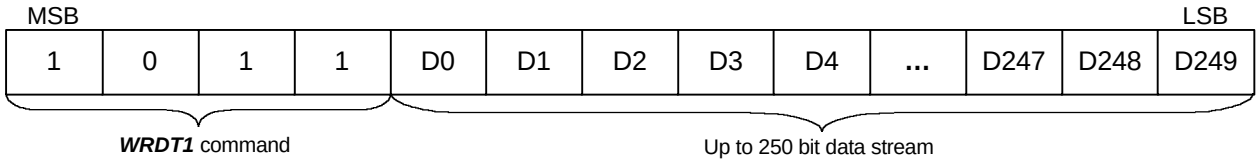
0	0	0	O8	O7	O6	O5	O4	O3	O2	O1	O0

Output bit	Symbol	Status
O8	**MON**	This bit is a “1” during the following operations; - Record, Playback, Erase operations - Digital data read, digital data write operations This bit stays at a “1” not only during the operation cycles described above but also any memory management cycles. This bit shows the same status as the MON pin.
O7	**REC**	This bit is a “1” during Record operations.
O6	**PLAY**	This bit is a “1” during Playback operations.
O5	**ERASE**	This bit is a “1” during Erase operations.
O4	**PAUSE**	This bit is a “1” during Pause operations.
O3	**FULL**	This bit goes to a “1” synchronized with the MON pin going low after the Record, Playback, or Erase operation reaches the last address of the memory. And operations automatically stop.
O2	**NAR**	This bit shows the same information as the NAR pin. During the Random Access Mode, this bit is a “1” when the next address input can be accepted.
O1	**PGM**	This bit is a “1” during digital data write operations.
O0	**READ**	This bit is a “1” during digital data read operations.

11. *WRDT1* command (BH)

The ***WRDT1*** command erases the 2,000 bits (cells) of the specified **Sector** and or writes the digital data of up to 250 bits per **Page** unit. The starting address is specified by the ***STADR*** command in **Sector** address units. The **Page** address bits (A0~A2) are forced to be "0".

The ***WRDT1*** command is followed by up to 250 bits of data (D0 ~ D249.) The number of bits of the data stream can be less than 250. The data stream can be terminated even though the number of bits has not reached 250 by setting the **CS** pin to a high level. The data stream bits are stored into each flash bit cell in order starting from the specified start address.



The ***WRDT1*** command can used repeatedly. The first ***WRDT1*** command erases the whole **Sectors** bit cells. After every ***WRDT1*** command execution, the address counter is incremented to indicate the next **Page**. The second and latter ***WRDT1*** commands do not perform the erase operation and simply write the bit cells by 250 bit cell units (one **Page**.) Repeating the ***WRDT1*** command 8 times rewrites all the bit cells of the specified **Sector**.

The 250 bit stream of data for each ***WRDT1*** command is stored in an internal buffer register. After the data transfer is finished, buffered data is physically programmed into flash memory cells. The physical programming operation starts synchronized with the rising edge of the **CS** input signal of the ML2517. At the same time, the ML2517 sets the **MON** pin to high and keeps it high until the programming operation is completed.

When the **MON** pin is high, the ML2517 is busy programming the flash cells. The master MCU must be programmed to wait until the **MON** pin goes low before sending the next ***WRDT1*** command.

Note that the ***WRDT1*** command should be repeated continuously for correct page address updating. If the ***WRDT1*** command repetition is interrupted by another command or reset-input, the address counter is initialized and the next ***WRDT1*** command erases the whole **Sector** contents and starts programming from the beginning of the **Sector**.

This repetition of the ***WRDT1*** command should be terminated by a dummy command such as ***STOP***. After ***WRDT1*** command execution the internal high voltage generation circuit remains active. Current consumption is higher in this condition. The dummy command will lower the power by turning off the high voltage generator used for writing.

To write into another **Sector** address, another ***STADR*** command is needed prior to ***WRDT1*** command execution. Even after the 8 times repetition of ***WRDT1*** command, the **Sector** address is not updated to the next **Sector** automatically.

Note 1 Even when the length of the data stream is less than 250 bits, the flash cell programming is performed for all of the 250 bit cells. The remaining bits are regarded as "0" and "0" is programmed into all remaining bit cells.

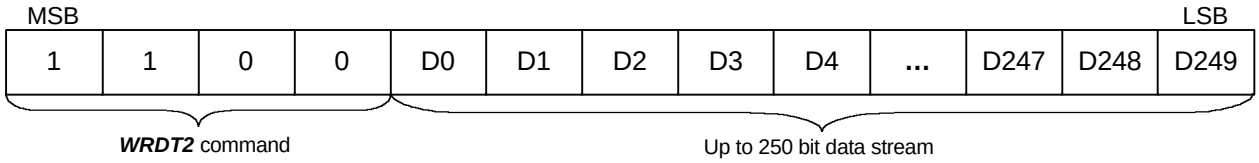
Note 2 ***WRDT1*** command can not be executed during the record, playback, or erase operations.

12. *WRDT2* command (CH)

The ***WRDT2*** command is almost the same as the ***WRDT1*** command. The difference is the ***WRDT2*** command works on two **Sector**s and the ***WRDT1*** command works on a single **Sector**. The programming time is much shorter using this command than the ***WRDT1*** command when writing multiple continuous **Sectors**.

The ***WRDT2*** commands erase the 4,000 bits (cells) of the specified two **Sector**s and writes the digital data in 250 bit (**Page**) units. The starting address is specified by the ***STADR*** command in two **Sector** address units (even address). The LSB of the **Sector** address (A3) and the **Page** address bits (A0~A2) are forced to be "0".

The ***WRDT2*** command is followed by up to 250 bits of data stream (D0 ~ D249.) The number of bits of the data stream can be less than 250. The data stream can be terminated even though number of bits does not reach to 250 by setting the **CS** pin high. The data stream bits are stored into each flash bit cell in order starting from the specified start address.



The ***WRDT2*** command is used repeatedly. The first ***WRDT2*** command erases the all of the two **Sectors** bit cells. After every ***WRDT2*** command, the address counter indicates the next **Page** (Please note that the **Page** address is updated crossing the **Sector** boundary between low and high **Sector**s). The second and latter ***WRDT2*** command do not perform the erase operation and simply write into the bit cells by 250 bit cell units (one **Page**). Repeating the ***WRDT2*** command 16 times, rewrites the all the bit cells of the specified two **Sector**s.

The 250 data stream bits of each ***WRDT2*** command are stored in an internal buffer register. After the data transfer is finished, buffered data is physically programmed into the flash memory cells. The physical programming operation starts synchronized with the rising edge of the **CS** input signal of the ML2517. At the same time, the ML2517 sets the **MON** pin high and keeps it high until the programming operation is completed.

When **MON** pin is high, the ML2517 is busy programming the flash cells. The master MCU must be programmed to wait until **MON** pin goes low before sending the next ***WRDT2*** command.

Note that the ***WRDT2*** command should be repeated continuously for correct page address updating. If the ***WRDT2*** command repetition is interrupted by another command or reset-input, the address counter is initialized and the next ***WRDT2*** command will erase the two **Sector**s contents and start programming from the beginning of the even (first) **Sector**.

The repetition of ***WRDT2*** command should be terminated by a dummy command such as ***STOP***. After the ***WRDT2*** command execution, the internal high voltage generation circuit remains active. Current consumption is higher. Power consumption can be reduced with a dummy command.

To write into another **Sector**, another ***STADR*** command is needed prior to the ***WRDT2*** command execution. Even after the 16 times repetition of ***WRDT2*** commands, the **Sector** address is not updated to the next even **Sector** automatically.

Note 1 Even when the length of the data stream is less than 250 bits, the flash cell programming is performed for all 250 cells. The remaining bits are regarded as "0" and "0" is programmed into the remaining cells.

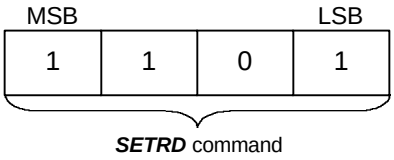
Note 2 The ***WRDT2*** command can not be used during record, playback, or erase operations.

13. *SETRD* command (DH)

The ***SETRD*** command retrieves 250 bits of digital data from the flash memory starting at the specified address and stores the data into an internal register. The start-address should be specified by the ***STADR*** command prior to the ***SETRD*** command. The start-address is specified in **Page** address units.

The **MON** pin output goes high during the digital data read operation, and goes low again after the operation is finished. The ML2517 is then ready for an ***RDDT*** command.

No data bits are required following this command. If there are any data bits, they are ignored.

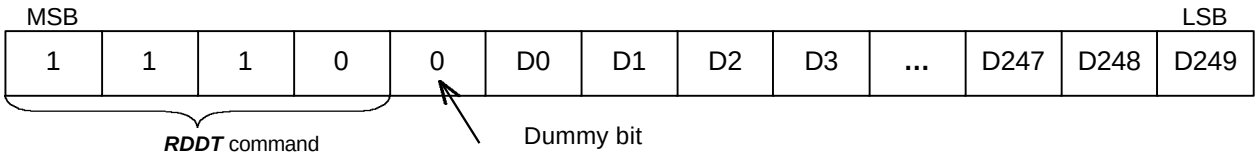


14. *RDDT* command (EH)

The ***RDDT*** command reads out the data that has been provided by the ***SETRD*** command in the internal buffer register. Up to 250 bits data can be sent out through **DO** pin synchronized with the **SCK** clock input.

Note that one dummy "0" data bit follows the RDDT command preceding the data stream.

The data transfer can be terminated even before all bits (250 bits) are transferred by setting the $\overline{\textbf{CS}}$ pin high.

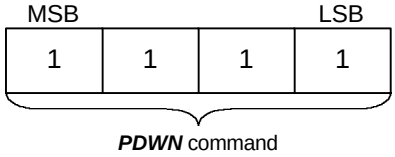


15. *PDWN* command (FH)

The ***PDWN*** command stops the all of ML2517 operations and sets the low power consumption mode (Power-down mode.)

If there are any data bits following the ***PDWN*** command, they are ignored.

By reset input or $\overline{\textbf{CS}}$ pin input going low, the ML2517 resumes from the power-down mode.



■ Serial Peripheral Interface (SPI)

The ML2517 communicates with the external MCU through the industry standard Serial Peripheral Interface (**SPI**). The ML2517 discriminates of Mode0 or Mode1 automatically from a level on the **SCK** pin at the falling edge of the $\overline{\textbf{CS}}$ pin. Mode0 is selected when a level on the **SCK** pin is "LOW" at the falling edge of the **CS** pin. The data signal applied to the **DI** pin is captured at the rising edge of the **SCK** signal. Mode1 is selected when a level on the **SCK** pin is "HIGH" at the falling edge of the $\overline{\textbf{CS}}$ pin. The data signal applied to the **DI** pin is captured at the falling edge of the **SCK** signal.

The following charts show timing for Mode 0.

1. Timing for Write Command Data

The following charts show timings for writing command data.

(1) The data transfer starts by changing the $\overline{\textbf{CS}}$ pin to the low level. The low input to the $\overline{\textbf{CS}}$ pin informs the ML2517 that the data transfer procedure is starting. The **SCK** level must also be low.

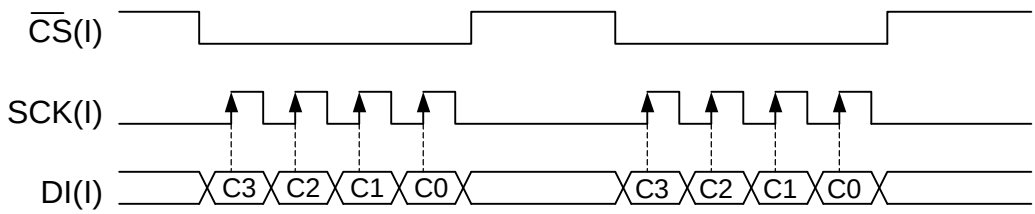
(2) After the $\overline{\textbf{CS}}$ pin goes low, the ML2517 is ready for data transfer. The command bits and data bits are applied to **DI** pin synchronized with the **SCK** signal, starting with the MSB in serial order. The data signal applied to the **DI** pin is captured at the rising edge of the **SCK** signal.

(3) After the last bit is fetched, the **SCK** signal should go low and stay low. The $\overline{\textbf{CS}}$ signal should be set high. Returning the $\overline{\textbf{CS}}$ pin high indicates that the data transfer is ended. Then the ML2517 starts command execution.

Note: ***RDADR***, ***RDSTAT***, ***WRDT*** and ***RDDT*** commands start execution immediately after the 4th bit of the command is fetched even before the **CS** pin goes high.

Note: If the $\overline{\textbf{CS}}$ pin is set high at times other than after the 4th, 8th, 16th , or 24th bit is fetched, the command input is disregarded.

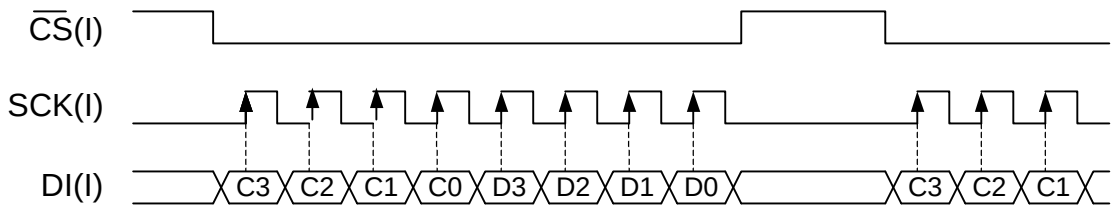
- **4-bit command format**



[Applicable commands]

REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN

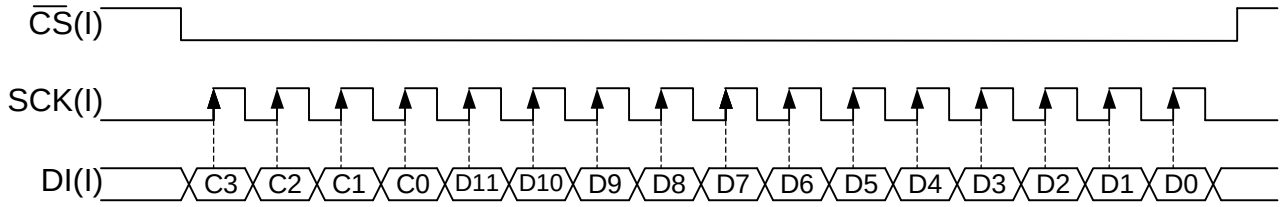
- **8-bit command format**



[Applicable command]

MODE,REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN

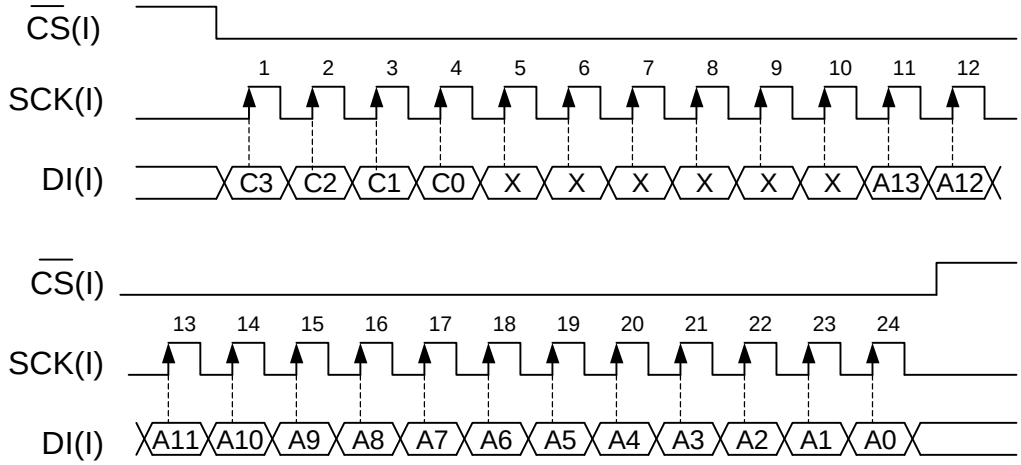
- **16-bit command format**



[Applicable command]

MODE,REC,PLAY,STOP,PAUSE,ERASE,SETRD,PDWN

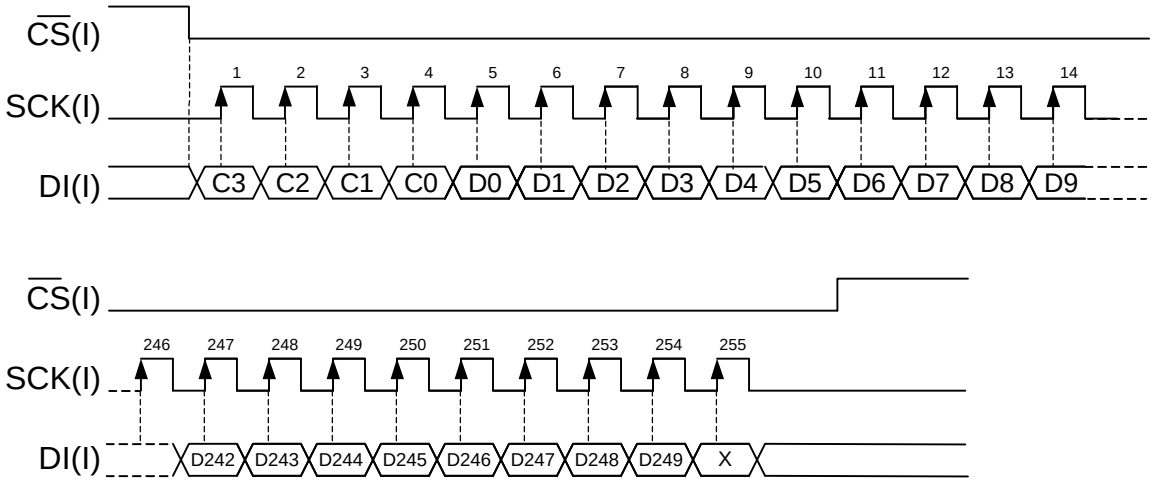
- **24-bit command format**



[Applicable command]

STADR, SPADR,MODE,REC,PLAY,STOP,PAUSE,ERASE,SETRD,PDWN

- **Digital data write timing (*WRDT* command)**



2. Timing for Data Read Commands

The timing for the ***RDSTAT***, ***RDADR*** and ***RDDT*** commands is shown below.

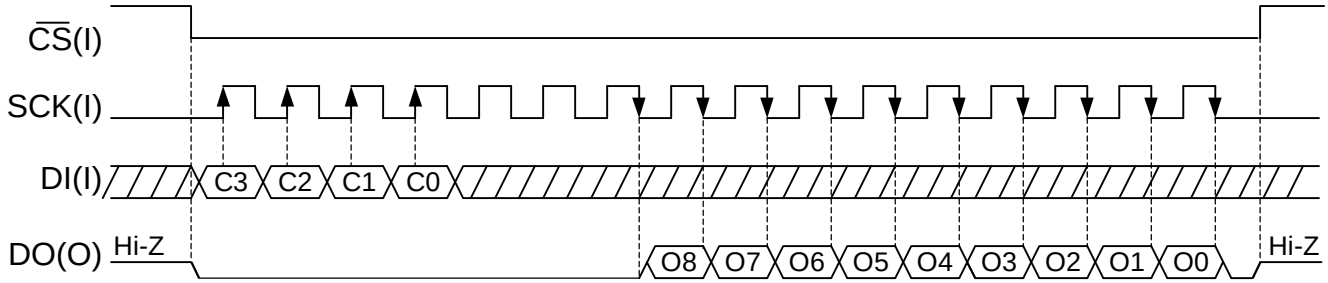
In the same manner as the write command timing, command bits start after the $\overline{\textbf{CS}}$ pin is set low and the data is fetched at the rising edge of the **CLK** signal.

For each command, a different delay time is inserted between the 4th bit of the command (**C0**) and the 1st bit of data (**O8**, **A13**, or **D0**) to allow for data setting. Please refer to the timing diagram for the delay cycles of each command.

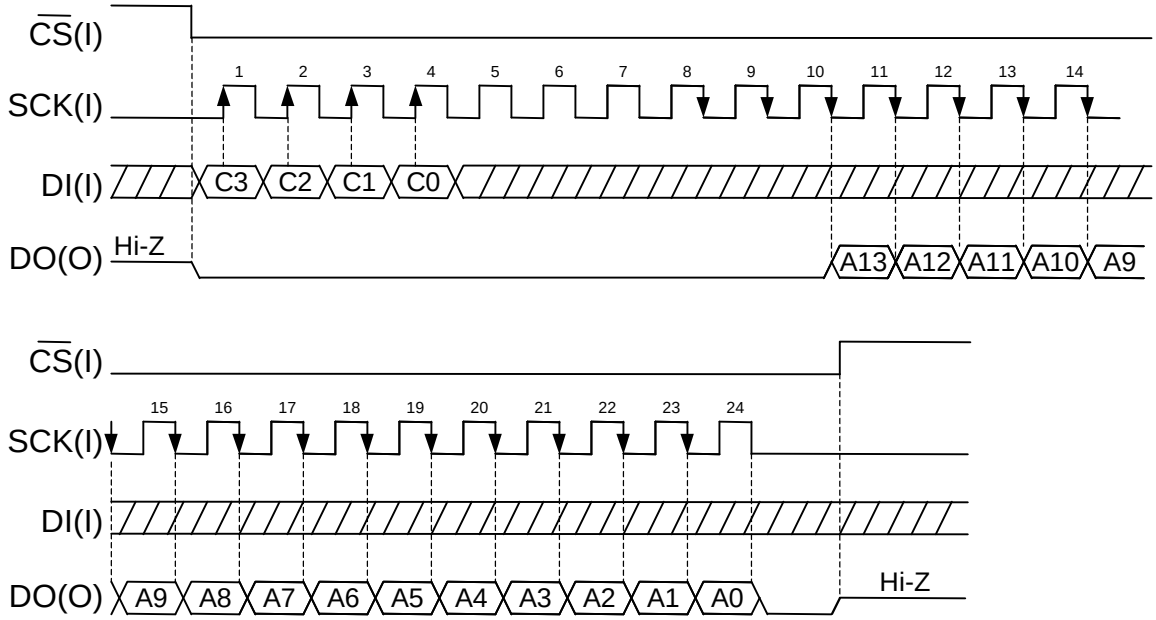
During delay cycles, the **DO** pin stays low.

The Read command is terminated by setting the $\overline{\textbf{CS}}$ pin high. Even if all data bits have not been read, the **DO** pin goes to the high impedance state.

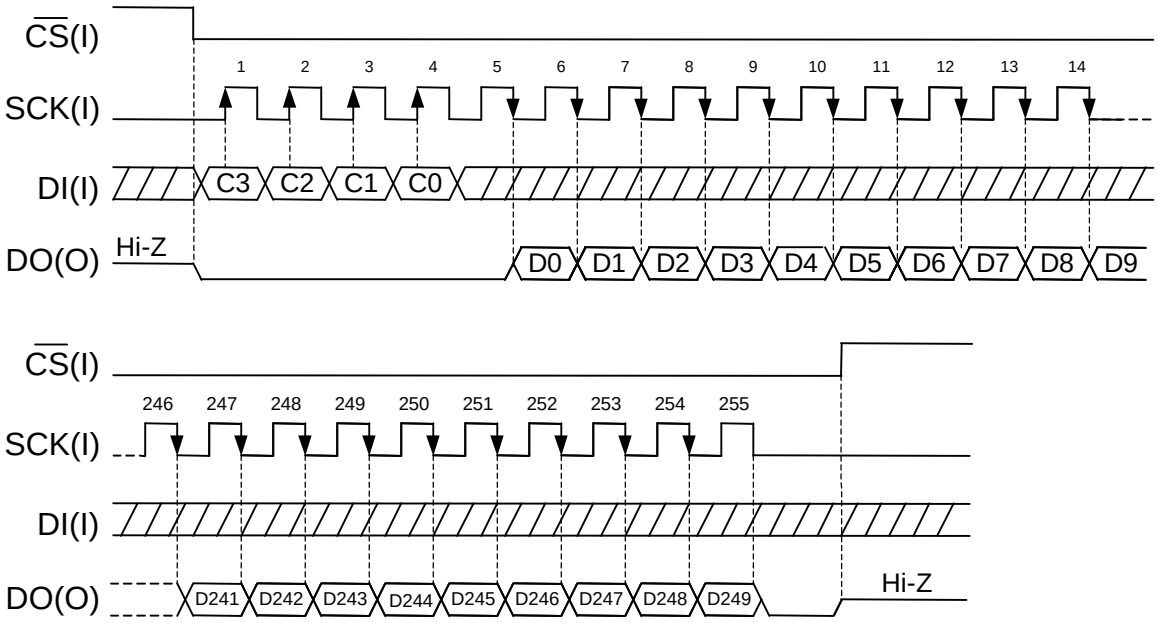
- **Status register read timing (*RDSTAT* command)**



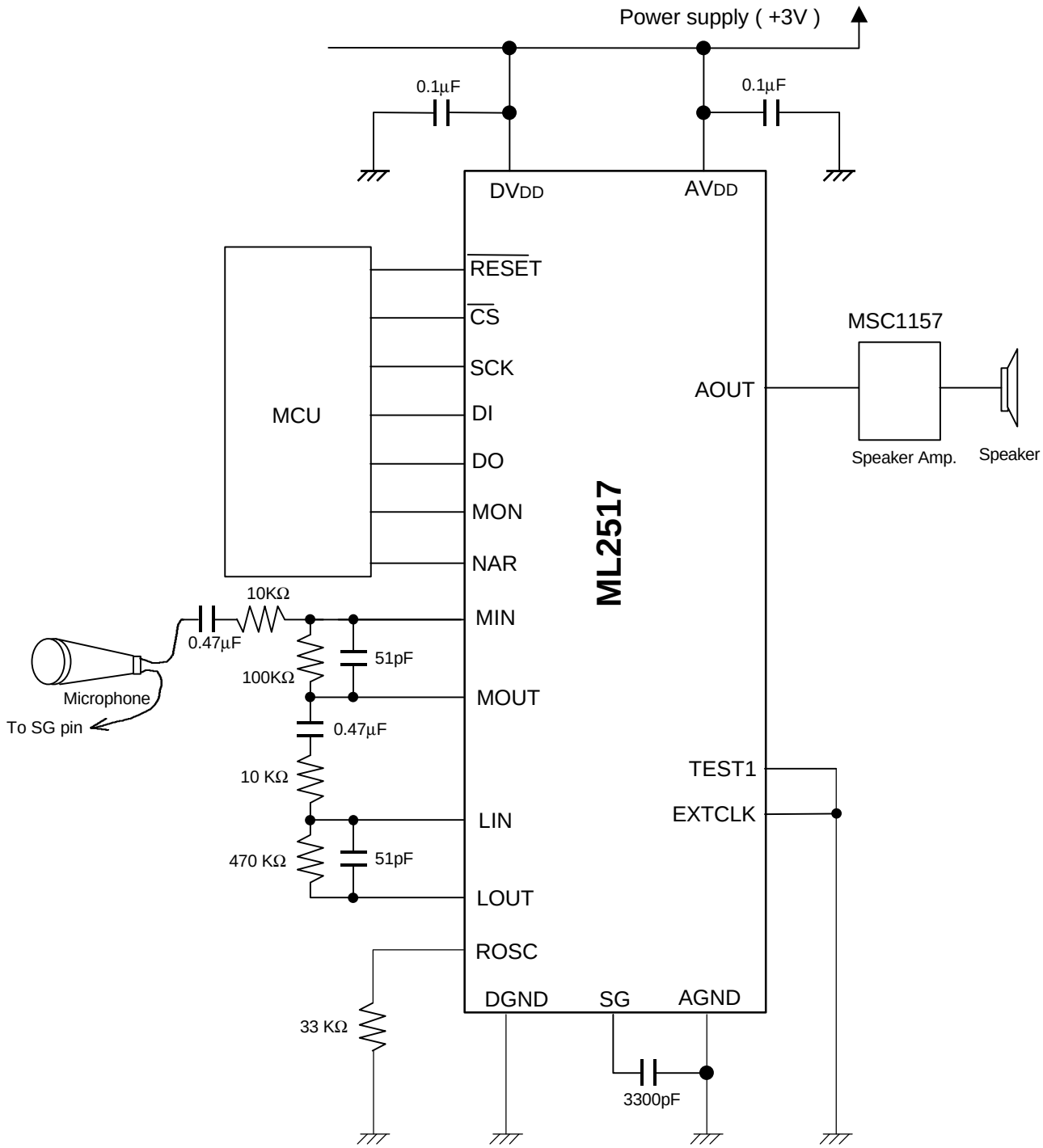
- **Memory address counter read timing (*RDADR* command)**



- **Digital data read timing (RDDT command)**



■ SAMPLE APPLICATION



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