FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16307-3E

32-Bit RISC Microcontroller

CMOS

FR Family MB91110 Series

MB91110/MB91V110

■ DESCRIPTION

The MB91110 series is a standard single-chip micro controller featuring various I/O resources and bus control mechanisms to incorporate the control with required for high performance high-speed CPU processes, having a 32-bit RISC CPU (FR30 series) in its core. Although external bus access is the basis for supporting a large address space accessible by a 32-bit CPU, a 1-KB instruction cache memory has been built-in to increase the instruction/ execution speed of the CPU.

This unit features the optimal specifications for incorporating applications that require high performance CPU processing power such as navigation systems, high performance facsimile systems, printer control, etc.

■ FEATURES

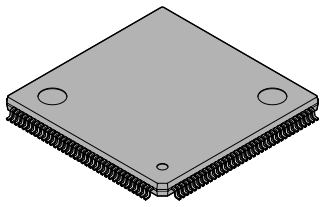
FR30CPU

- 32-bit RISC, load / store architecture, 5-level pipeline
- Operating frequency : external 25 MHz, internal 50 MHz
- Multi-purpose register : 32 bits × 16
- 16-bit fixed length instructions (basic instruction) , 1 instruction per cycle
- Instructions for barrel shift, bit processing and inter memory transfers : Instructions suited to loading purposes

(Continued)

■ PACKAGE

144-pin plastic LQFP



(FPT-144P-M08)

FUJITSU

(Continued)

- Function entry / exit instruction, multi load / store instruction of register details : Instruction capable of handling High level language instruction.
- Register Interlock function : Simplification of assembler description
- Branch instruction with delay slot : Reduction in overheads in case of branching
- Multiplier is built-in / Supported at instruction level
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interruption (saving PC and PS) : 6 cycles, 16 priority levels

Bus Interface

- 24-bit address bus (16 MB space)
- Operating frequency : 25 MHz
- 16- / 8-bit data bus
- Basic external bus cycle : 2 clock cycles
- Chip select output that can be set to a minimum 64-Kbyte units
- Interface support for various memories
  DRAM interface (areas 4, 5)
- Automatic waiting cycle : Can be randomly set from 0 to 7 cycles per area
- Unused data and address pins can be used as input/output ports.
- Supports “little endian” mode (One area is selected from areas 1 to 5)

DRAM Interface

- 2-bank individual control (area 4, 5)
- Normal mode / high speed page mode
- Basic bus cycles : normally 5 cycles, 1 cycle access is possible in high-speed page mode.
- Programmable waveform : 1 cycle waiting can be inserted automatically in RAS and CAS.
- DRAM refresh
  CBR refresh (Interval is randomly set using the 6-bit timer.)
  Self refresh mode
- Supports addresses for 8, 9, 10 and 12 columns
- 2CAS/1WE or 2WE/1CAS can be selected.

Cache Memory

- 1 KB instruction cache
- 2 way set associative
- 32 blocks / way, 4 entries (4 words) / block
- Lock function : Residing in the specified program codes at cache

DMA Controller (**DMAC**)

- 5 channels
- External $\rightarrow$ external 2.5 access cycles / transfer (if 2 clock cycles are defined as 1 access cycle)
- Internal $\rightarrow$ external 1.5 access cycles / transfer (if 2 clock cycles are defined as 1 access cycle)
- Address register (inc, dec, or reload are possible) : 32 bits $\times$ 5 channels
- Transfer count register (reload possible) : 16 bits $\times$ 5 channels
- Transfer factors : external pin / built-in resources interruption request / software
- Transfer sequence
  Step transfer / block transfer
  Burst / consecutive transfer
- Transfer data length : 8-bit, 16-bit or 32-bit can be selected
- Suspension is possible using NMI / interruption request

UART
- Fully duplicated double buffer
- Data length : 7 to 9 bits (without parity) , 6 to 8 bits (with parity)
- Asynchronous (start-stop synchronization) or CLK synchronized communication can be selected.
- Multiprocessor mode
- Dedicated baud rate generator is built-in.
- External clock can be used as the transfer clock
- Baud rate clock can be output
- Error detection : parity, frame, overrun

PPG Timer
- 16 bits, 6 channels (frequency setting register / duty setting register)
- PWM function or one-shot function can be selected
- Initiation : Software or external trigger can be selected

A/D Converter (**sequential conversion type**)
- 10-bit resolution, 8 channels
- Sequential comparison conversion : 5.6 μs in the case of 25 MHz
- Sample & hold circuit is built-in.
- Conversion mode : Single, scan or repeat conversion can be selected.
- Initiation : Software, external trigger or built-in timer can be selected.

Reloading Timer
- 16-bit timer : 2 channels
- Internal clock : 2 clock cycle resolutions, 2, 8 or 32 cycles can be selected.
- Pin input : event counter input / gate function
- Rectangular wave output

Other Interval Timer
- Watchdog timer : 1 channel

Bit Search Module
- Searches the first “1” / “0” change bit positions within 1 cycle from MSB in 1 word.

Interruption Controller
- External interruption input : Mask impossible interruption ($\overline{\text{NMI}}$) , normal interruption × 8 (INT0 to INT7)
- Internal interruption factors : UART, DMAC, A/D, reloading timer, PPG timer, delay interruption
- Priority levels are programmable except for mask impossible interruption (16 levels)

Reset Factors
- Power-on reset / hardware standby / watchdog timer / software reset / external reset

Low Power Consumption Mode
- Sleep / stop mode

Clock Control
- Gear functions : Operating clock frequencies peripheral to the CPU can be set randomly and independently. Gear locks can be selected from 1/1, 1/2, 1/4 or 1/8 (or 1/2, 1/4, 1/8, or 1/16) .

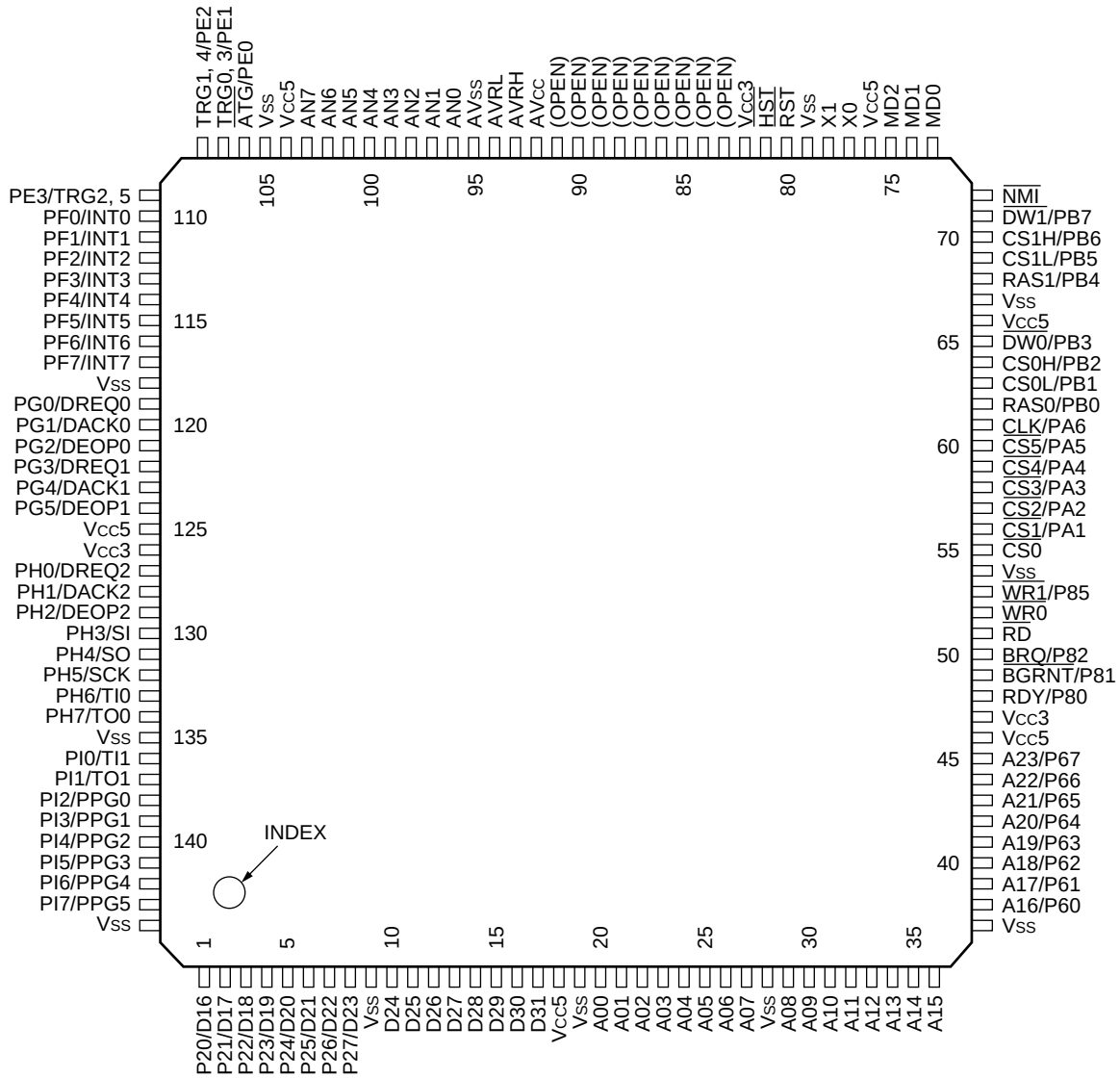
Others
- Package : LQFP-144
- CMOS technology : 0.35 μm
- Power : 5.0 V ± 10%, 3.3 V ± 5%

■ PRODUCT LINEUP

	MB91V110 (For evaluation)	MB91110 (I-RAM mounted version)
I-RAM	16 Kbyte	16 Kbyte
RAM	5 Kbyte	5 Kbyte
ROM	—	—
I-$	1 Kbyte	1 Kbyte
DSU3 evaluation function	Mounted	—

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-144P-M08)

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O*	Circuit type	Function
1 2 3 4 5 6 7 8	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	I/O	C	These pins use bits 16 to 23 of the external data bus. They can be used as a port (P20 to P27) if the external bus width is 8 bits.
10 11 12 13 14 15 16 17	D24 D25 D26 D27 D28 D29 D30 D31	I/O	C	These pins use bits 24 to 31 of the external data bus.
20 21 22 23 24 25 26 27	A00 A01 A02 A03 A04 A05 A06 A07	I/O	C	These pins use bits 00 to 07 of the external address bus.
29 30 31 32 33 34 35 36	A08 A09 A10 A11 A12 A13 A14 A15	I/O	C	These pins use bits 08 to 15 of the external address bus.
38 39 40 41 42 43 44 45	A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	I/O	C	These pins use bits 16 to 23 of the external address bus.
48	RDY/P80	I/O	C	This is for external ready input. “0” is input if the bus cycle being executed is incomplete. It can be used as a port when not otherwise used.
49	$\overline{\text{BGRNT}}$/P81	I/O	H	This is the external bus open reception output. “L” is output if the external bus is opened. It can be used as a port when not otherwise used.

(Continued)

<table>
<tr><th>Pin no.</th><th>Pin name</th><th>I/O*</th><th>Circuit type</th><th>Function</th></tr>
<tr><td>50</td><td>BRQ/P82</td><td>I/O</td><td>C</td><td>This is the external bus open request input. “1” is input if the external bus is to be opened. It can be used as a port when not otherwise used.</td></tr>
<tr><td>51</td><td>$\overline{RD}$</td><td>O</td><td>G</td><td>This is the external bus read strobe.</td></tr>
<tr><td>52</td><td>$\overline{WR0}$</td><td>O</td><td>G</td><td rowspan="2">This is the external bus write strobe.<table><tr><th></th><th>16-bit bus width</th><th>8-bit bus width</th></tr><tr><td>D31-24</td><td>$\overline{WR0}$</td><td>$\overline{WR0}$</td></tr><tr><td>D23-16</td><td>$\overline{WR1}$</td><td>(Port is possible)</td></tr></table></td></tr>
<tr><td>53</td><td>$\overline{WR1}$/P85</td><td>I/O</td><td>H</td></tr>
<tr><td>55</td><td>$\overline{CS0}$</td><td>O</td><td>G</td><td>Chip select 0 output (Low active)</td></tr>
<tr><td>56
57
58
59
60</td><td>$\overline{CS1}$/PA1
$\overline{CS2}$/PA2
$\overline{CS3}$/PA3
$\overline{CS4}$/PA4
$\overline{CS5}$/PA5</td><td>I/O</td><td>H</td><td>Chip select 1 output (Low active)
Chip select 2 output (Low active)
Chip select 3 output (Low active)
Chip select 4 output (Low active)
Chip select 5 output (Low active)
They can be used as ports when not otherwise used.</td></tr>
<tr><td>61</td><td>CLK/PA6</td><td>I/O</td><td>H</td><td>This is the system clock output. The same clock as the standard clock is output. This can be used as a port when not otherwise used.</td></tr>
<tr><td>62
63
64
65
68
69
70
71</td><td>RAS0/PB0
CS0L/PB1
CS0H/PB2
$\overline{DW0}$/PB3
RAS1/PB4
CS1L/PB5
CS1H/PB6
$\overline{DW1}$/PB7</td><td>I/O</td><td>H</td><td>RAS output with DRAM bank 0.
CASL output with DRAM bank 0.
$\overline{CASH}$ output with DRAM bank 0.
$\overline{WE}$ output with DRAM bank 0. (Low active)
RAS output with DRAM bank 1.
CASL output with DRAM bank 1.
$\overline{CASH}$ output with DRAM bank 1.
$\overline{WE}$ output with DRAM bank 1. (Low active)
They can be used as ports when not otherwise used.</td></tr>
<tr><td>72</td><td>$\overline{NMI}$</td><td>I</td><td>E</td><td>Non Maskable Interrupt (NMI) input. (Low active)</td></tr>
<tr><td>73
74
75</td><td>MD0
MD1
MD2</td><td>I</td><td>I</td><td>These are mode pins from 0 to 2.
Basic MCU operation modes are set using these pins.
They should be connected directly to V_{CC} or V_{SS} for use.</td></tr>
<tr><td>77
78</td><td>X0
X1</td><td>I
O</td><td>A</td><td>Clock (oscillation) input.
Clock (oscillation) output.</td></tr>
<tr><td>80</td><td>$\overline{RST}$</td><td>I</td><td>B</td><td>This is the external reset input. (Low active)</td></tr>
<tr><td>81</td><td>$\overline{HST}$</td><td>I</td><td>E</td><td>This is the hardware standby input. (Low active)</td></tr>
<tr><td>83</td><td>(OPEN)</td><td>—</td><td>—</td><td>Set this to OPEN.</td></tr>
<tr><td>84
85
86</td><td>(OPEN)
(OPEN)
(OPEN)</td><td>—</td><td>—</td><td>Set this to OPEN.</td></tr>
</table>

(Continued)

Pin no.	Pin name	I/O*	Circuit type	Function
87 88 89 90	(OPEN) (OPEN) (OPEN) (OPEN)	—	—	Set this to OPEN.
91	(OPEN)	—	—	Set this to OPEN.
92	AV_{CC}	—	—	V_{CC} power supply for the A/D converter.
93	AVRH	—	—	A/D converter reference voltage (high potential side). Be sure to turn on/off this pin with potential higher than AVRH applied to V_{CC}.
94	AVRL	—	—	A/D converter reference voltage (low potential side).
95	AV_{SS}	—	—	V_{SS} power supply for the A/D converter.
96 97 98 99 100 101 102 103	AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	I	D	[AN0 to 7] A/D converter analog input.
106	$\overline{ATG}$/PE0	I/O	H	[$\overline{ATG}$] This is the external trigger input for the A/D converter. This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped except when it is carried out intentionally.
				[PE0] This is a general-purpose input/output port.
107 108 109	TRG0, 3/PE1 TRG1, 4/PE2 TRG2, 5/PE3	I/O	H	[TRG0 to 5] These are external trigger input pins of the PPG.
				[PE1 to 3] These are general-purpose input/output ports.
110 111 112 113 114 115 116 117	INT0/PF0 INT1/PF1 INT2/PF2 INT3/PF3 INT4/PF4 INT5/PF5 INT6/PF6 INT7/PF7	I/O	F	[INT0 to 7] These are external interruption request inputs. This input is always used while the corresponding external interruption is permitted, so output using other functions should be stopped except when carried out intentionally.
				[PF0 to 7] These are general-purpose input/output ports.
119	DREQ0/PG0	I/O	H	[DREQ0] This is the DMA external transfer request input (ch 0) . This input is always used if selected as the transfer factor for DMAC, so outputs from other functions should be stopped except when carried out intentionally.
				[PG0] This is a multi-purpose input/output port.

(Continued)

Pin no.	Pin name	I/O*	Circuit type	Function
120	DACK0/PG1	I/O	C	[DACK0] This is the DMAC external transfer request reception output (ch 0) . This function is effective if the transfer request reception output specification of DMAC is permitted.
				[PG1] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specification of DMAC is prohibited.
121	DEOP0/PG2	I/O	C	[DEOP0] This is the DMA transfer end signal output (ch 0) . This function is effective if the transfer end signal output specification of DMAC is permitted.
				[PG2] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
122	DREQ1/PG3	I/O	H	[DREQ1] This is the DMA external transfer request input (ch 1) . This input is always used if selected as the transfer factor of DMAC, so output using other functions should be stopped except when carried out intentionally.
				[PG3] This is a multi-purpose input/output port.
123	DACK1/PG4	I/O	C	[DACK1] This is the DMAC external transfer request reception output (ch 1) . This function is effective if the transfer request reception output specification of DMAC is permitted.
				[PG4] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specification of DMAC is prohibited.
124	DEOP1/PG5	I/O	C	[DEOP1] This is the DMA transfer end signal output (ch 1) . This function is effective if the transfer end signal output specification of DMAC is permitted.
				[PG5] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
127	DREQ2/PH0	I/O	H	[DREQ2] This is the DMA external transfer request input (ch 2) . This input is always used if selected as the transfer factor of DMAC, so output using other functions should be stopped except when carried out intentionally.
				[PH0] This is a multi-purpose input/output port.
128	DACK2/PH1	I/O	C	[DACK2] This is the DMAC external transfer request reception output (ch 2) . This function is effective if the transfer request reception output specification of DMAC is permitted.
				[PH1] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specification of DMAC is prohibited.

(Continued)

Pin no.	Pin name	I/O*	Circuit type	Function
129	DEOP2/PH2	I/O	C	[DEOP2] This is the DMA transfer end signal output (ch 2) . This function is effective if the transfer end signal output specification of DMAC is permitted.
				[PH2] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
130	SI/PH3	I/O	H	[SI] This is UART data input. This input is always used while UART inputs, so outputs from other functions should be stopped except when carried out intentionally.
				[PH3] This is a general-purpose input/output port.
131	SO/PH4	I/O	C	[SO] This is UART data output. This function is effective when UART data output specification is permitted.
				[PH4] This is a general-purpose input/output port. This function is effective when UART data output specification is prohibited.
132	SCK/PH5	I/O	H	[SCK] This is UART clock input/output. Clock output is effective when UART clock output specification is permitted.
				[PH5] This is a general-purpose input/output port. This function is effective when UART clock output specification is prohibited.
133	TI0/PH6	I/O	H	[TI0] This is reload timer 0 input. It is always used when reload timer input is permitted, so outputs from other functions should be stopped except when carried out intentionally.
				[PH6] This is a general-purpose input/output port.
134	TO0/PH7	I/O	C	[TO0] This is reload timer 0 Output. This function is effective when reload timer specification is permitted.
				[PH7] This is a general-purpose input/output port. This function is effective when reload timer specification is prohibited.
136	TI1/PI0	I/O	H	[TI1] This is reload timer 1 input. It is always used when reload timer input is permitted, so outputs from other functions should be stopped except when carried out intentionally.
				[PI0] This is a general-purpose input/output port.
137	TO1/PI1	I/O	C	[T01] This is the reload timer 1 output. This function is effective if the output specification of the reload timer is permitted.
				[PI1] This is a multi-purpose input/output port. This function is effective if the output specification of the reload timer is prohibited.

(Continued)

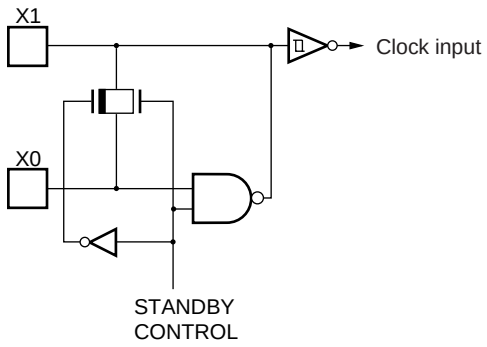
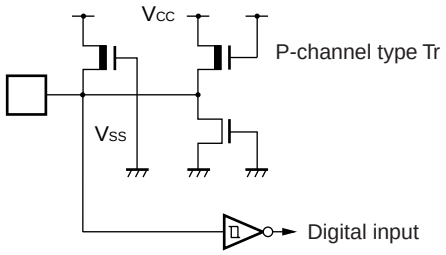
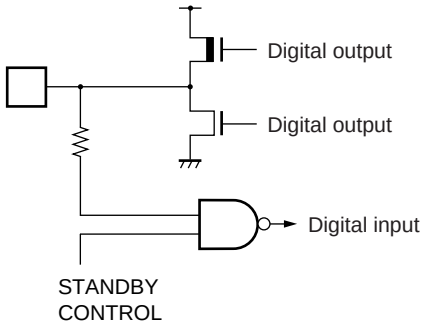
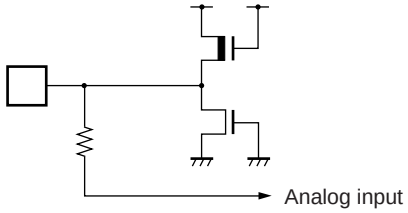
(Continued)

Pin no.	Pin name	I/O*	Circuit type	Function
138 139 140 141 142 143	PPG0/PI2 PPG1/PI3 PPG2/PI4 PPG3/PI5 PPG4/PI6 PPG5/PI7	I/O	C	[PPG0 to 5] This is the PPG timer 1 output. This function is effective if the output specification of the PPG timer is permitted. [PI2 to 7] This is a multi-purpose input/output port. This function is effective if the output specification of the PPG timer is prohibited.
18 46 66 76 104 125	$V_{CC}5$	—	—	This provides power for the 5 V digital circuit system.
47 82 126	$V_{CC}3$	—	—	This provides power for the 3 V digital circuit system.
9 19 28 37 54 67 79 105 118 135 144	V_{SS}	—	—	This is the earth level for digital circuits.

* : I/O shown above indicates input/output classification.

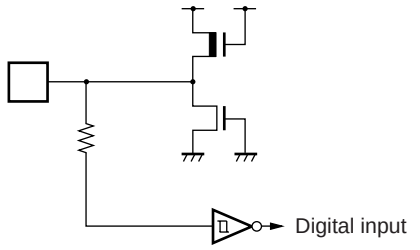
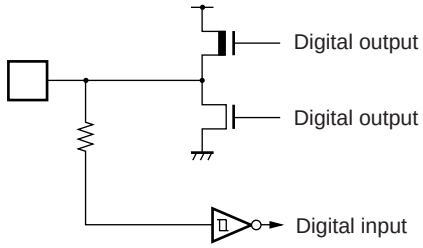
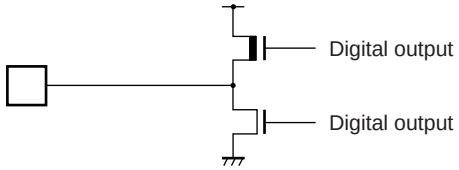
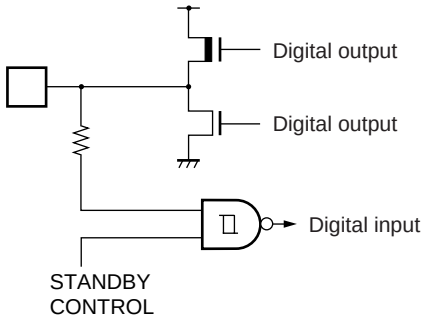
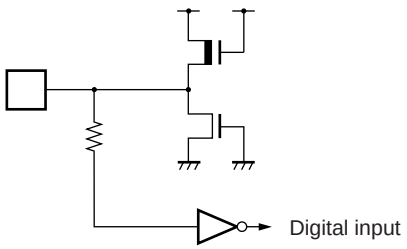
Note : The I/O port and resource input/outputs for most of the above pins are multiplexed, i.e. Pxx/xxxx. In the event of both the port and resource outputs were to use the same pins, the resource is given priority.

■ I/O CIRCUIT TYPE

Type	Circuit types	Remarks
A		• Oscillation feedback resistance : approximately 1 MΩ • 12.5 MHz oscillation
B		• CMOS level hysteresis input Without standby control With pull-up resistance
C		• CMOS level output CMOS level input With standby control
D		• A/D converter Analog input pin

(Continued)

(Continued)

Type	Circuit types	Remarks
E		• CMOS level hysteresis input Without standby control
F		• CMOS level output • CMOS level hysteresis input Without standby control
G		• CMOS level output
H		• CMOS level output • CMOS level hysteresis input With standby control
I		• CMOS level input Without standby control

■ HANDLING DEVICES

- **Preventing Latch-up**

The “Latch-up” phenomenon may be generated if a voltage in excess of V_{CC} or lower than V_{SS} is applied to the input/output pins, or if the voltage exceeds the rating between V_{CC} and V_{SS}. If latch-up is generated, the electrical current increases significantly and may destroy certain components due to the excessive heat, so great care must be taken to ensure that the maximum rating is not exceeded during use.

- **Handling Unused Input Pins**

Input pins that are not used should be pulled up or down as they may cause erroneous operations if they are left open.

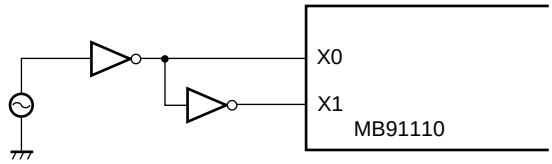
- **External Reset Input**

“L” level should be input to the $\overline{RST}$ pin, which is required for at least five machine cycles to ensure the internal status is reset.

- **Using External Clocks**

If external clock is used, X0 pin should be provided, and X1 pin should be provided with reverse phase to X0 pin input. If the STOP mode (oscillation stop mode) is used simultaneously, the X1 pin is stopped with the “H” output. So, when STOP mode is specified, approximately 1 kΩ of resistance should be added externally. An example of the external clock usage methods is shown in the following circuit.

Example of External Clock Usage (normal case)



Note : Resistance must be added to the X1 pin if the STOP mode (oscillation stop mode) is used.

- **Power Supply Pins**

In products with multiple Vcc or Vss pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect Vcc and Vss pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 F between Vcc and Vss pins near the device.

- **Crystal Oscillator Circuits**

Noise around the X0 or X1 pins may cause erroneous operation. Make sure to provide bypass capacitors via shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuits not cross the lines of other circuit.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended .

- **N.C. Pins**

N.C. pins must be opened for use.

- **Mode Pins** (**MD0** to **MD2**)

Those pins must be directly connected to V_{CC} or V_{SS} for use.

Pattern length between V_{CC} or V_{SS} and each mode pin on the printed-circuit board should be arranged to be as short as possible to prevent the test mode being erroneously turned on due to noise, they should also be connected with low impedance.

- **In the Event that Power Is Turned on**

The $\overline{RST}$ pin must be started from “L” level when the power is turned on, and when the power is adjusted to the V_{CC} level it should be changed to the “H” level after being left for at least five cycles of the internal operation clock.

- **Original Oscillation Input in the Event that Power Is Turned on**

The clock must be input until the waiting status for oscillation stability is reset in the event that power is turned on.

- **Hardware Standby in the Event that Power Is Turned on**

Standby is not set in the event that power is turned on while the $\overline{HST}$ pin is set at “L” level. The $\overline{HST}$ pin becomes effective after being reset, but it must first be returned to “H” level.

- **Power on Reset**

When power is turned on, “Power on reset” must be executed. If the power voltage falls below the guaranteed operating voltage, “Power on reset” must be executed by turning on power supply again.

- **Restrictions for Standby**

Programs to be set for stop and sleep must be placed address area of the external memory. If placed in the RAM address area on the I-bus, operation can not be guaranteed after returning.

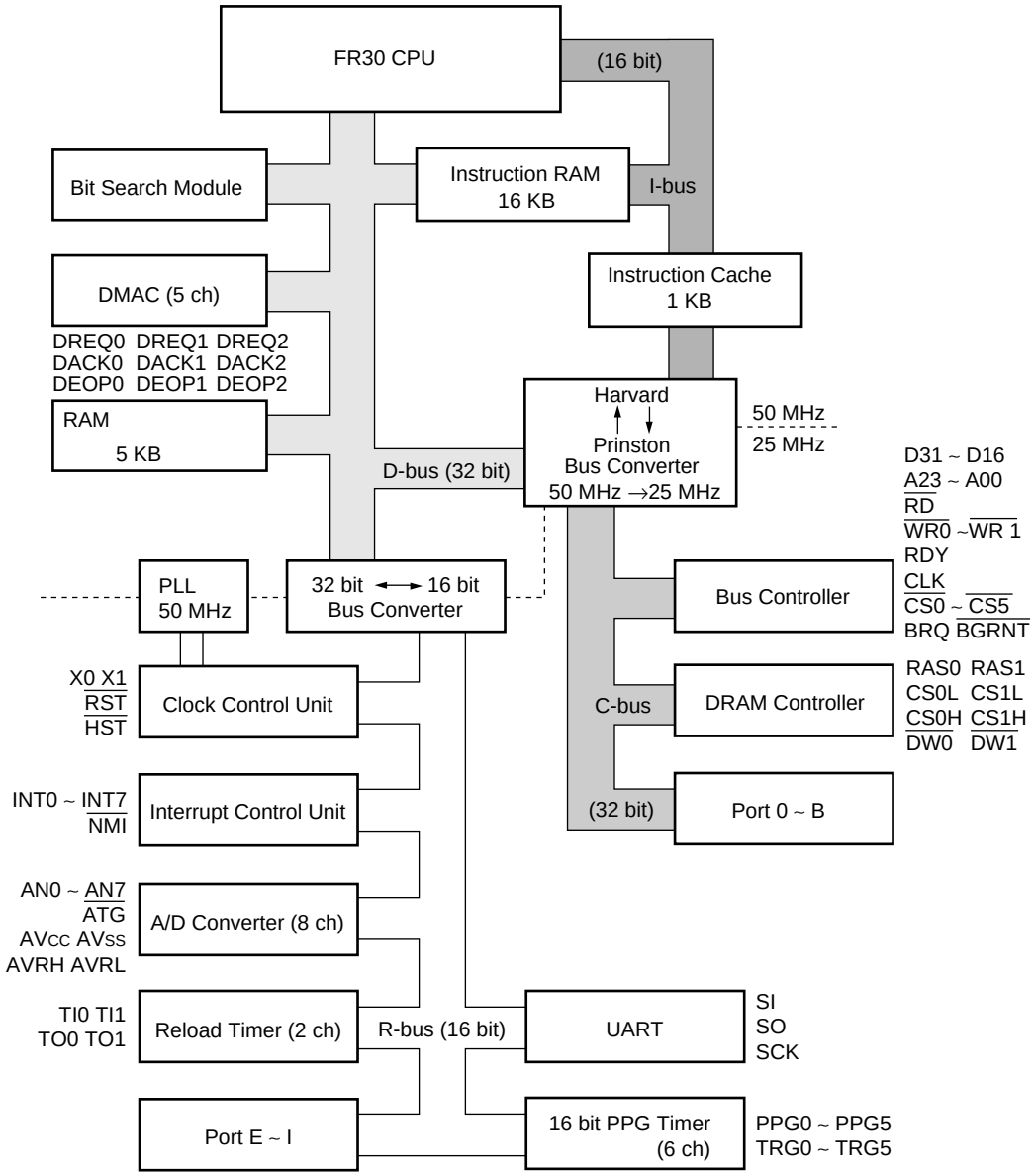
- **Execution of Programs in I-RAM Areas**

In the event that programs in the I-RAM areas are executed, enter the I-RAM areas in accordance with the JMP system instruction. Conversely, when changing from programs in the I-RAM area to those in other areas, exit in accordance with the JMP system instructions.

- **Caution on Operation during PLL Clock Mode**

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ BLOCK DIAGRAM

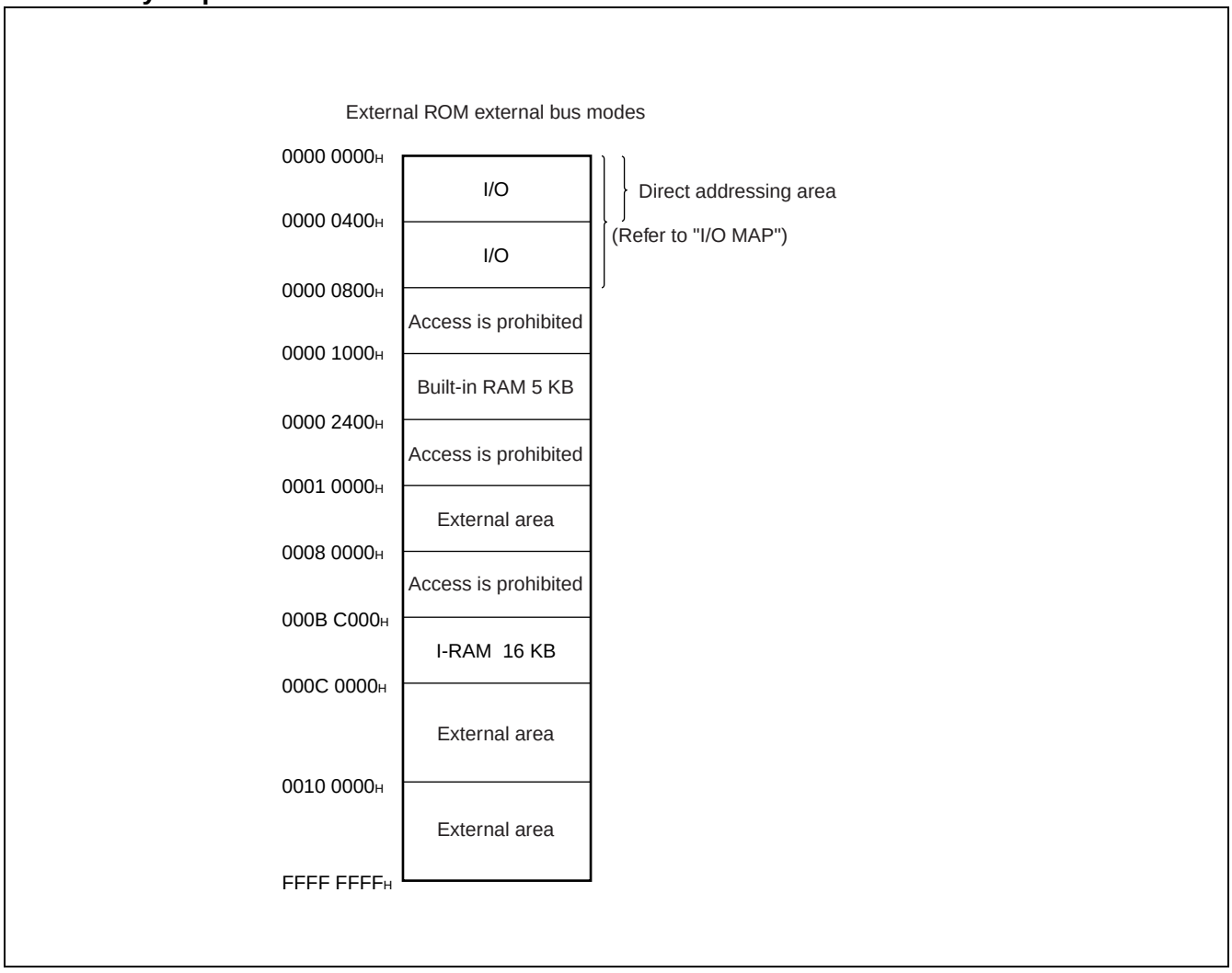


Notes : • Pins are described per function. Some of the pins are multiplexed.
• In the event that REALOS is used, an external interruption or built-in timer should be used to control the time.

■ MEMORY SPACE

The FR30 series has 4 Gbytes (2^{32} addresses) of logic address space which the CPU accesses linearly.

1. Memory Map



Note : MB91110 series only supports external ROM external bus mode.

- **Direct addressing area**

The following areas of the address space are used for I/O. This area is called the “direct addressing area” and the address of the operand can be specified directly during instruction. The direct area differs depending on data size to be accessed.

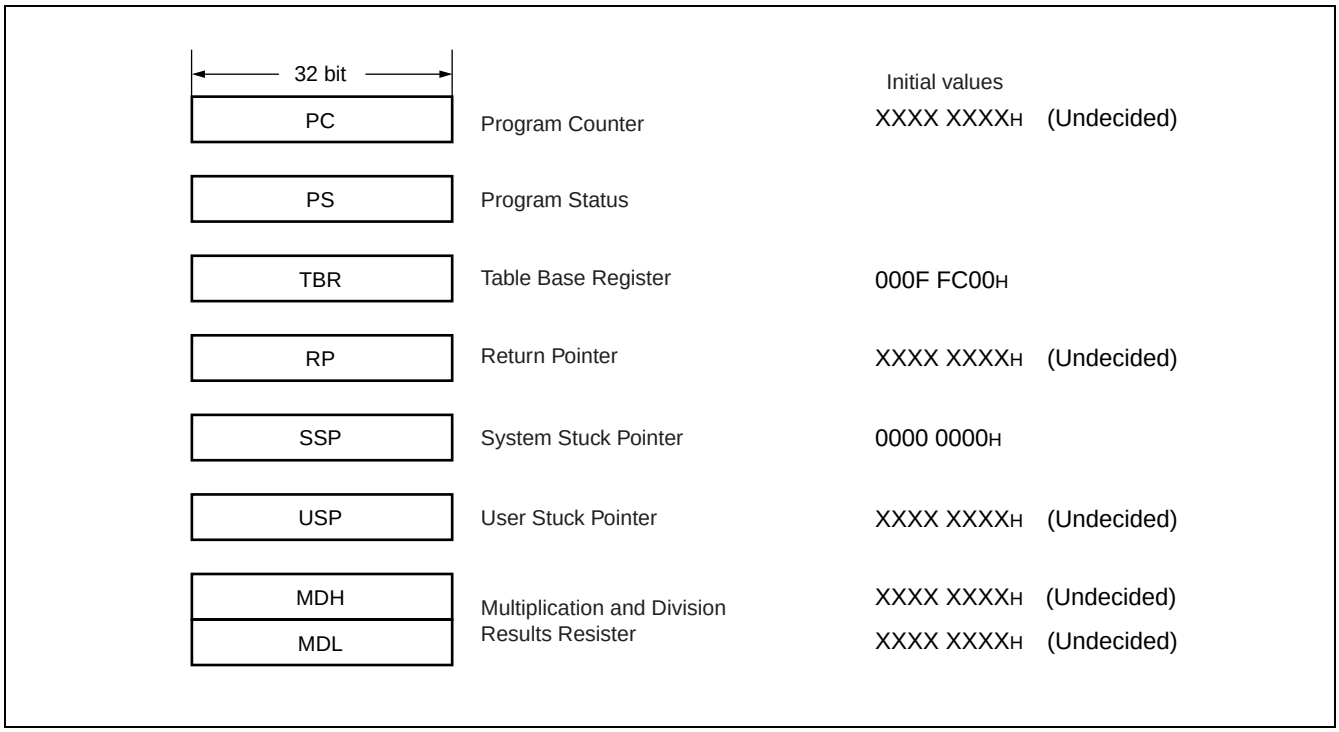
- Byte data access : 0-0FF$_H$
- Half-word data access : 0-1FF$_H$
- Word data access : 0-3FF$_H$

2. Registers

There are two types of multi-purpose registers in the FR family. One is a dedicated purpose register that exists within the CPU and the other is a multi-purpose register that exists in the memory.

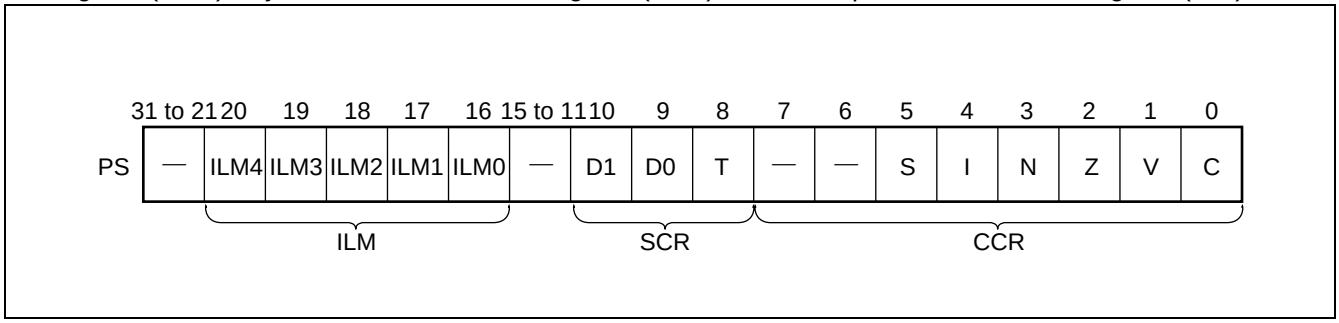
- **Dedicated Registers**

Program Counter (PC)	:	32-bit length; indicates instruction storage position.
Program Status (PS)	:	32-bit length; stores register pointers and condition codes.
Table Base Register (TBR)	:	Holds the starting address of the vector table to be used for Exception, Interruption and Trapping (EIT) .
Return Pointer (RP)	:	Holds the address to which you will return to from the sub-routine.
System Stuck Pointer (SSP)	:	Indicates the systems stuck position.
User Stuck Pointer (USP)	:	Indicates the user's stuck position.
Multiplication and Division Results Resister (MDH/MDL)	:	32-bit length; These are the registers for multiplication and division.



- **Program Status** (**PS**)

PS is the register that holds the program status and is classified into three categories, namely, Condition Code Register (CCR) , System Condition Code Register (SCR) and Interruption Level Master Register (ILM) .



- **Condition Code Register** (**CCR**)

  S flag : Specifies the stuck pointer to be used as R15.

  I flag : Controls permission and prohibition of user interruption requests.

  N flag : Indicates codes when the computation results are defined as integers that are expressed in complements of 2.

  Z flag : Indicates if arithmetic results were “0.”

  V flag : Indicates when operands are used for computation and defined as integers expressed in complements of 2, and indicates whether or not an overflow is generated as a result of the computation.

  C flag : Indicates whether carrying or borrowing is generated from the highest bit as a result of the computation.

- **System Condition Code Register** (**SCR**)

  T flag : Specifies whether or not the step- trace- trap will be valid.

- **Interruption Level Mask Register** (**ILM**)

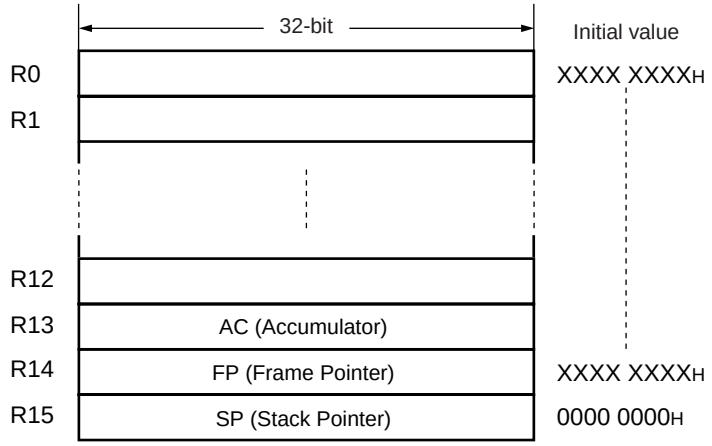
  ILM4 to ILM0 : Holds the interruption level mask values, and those values that are held by the ILM are used for the level mask. Interruption requests can only be accepted when the interruption levels handled within the interruption requests to be input into the CPU are stronger than the levels shown by the ILM.

ILM4	ILM3	ILM2	ILM1	ILM0	Interruption level	Strength
0	0	0	0	0	0	Strong
		⋮			⋮	↕
0	1	0	0	0	15	
		⋮			⋮	
1	1	1	1	1	31	Weak

■ MULTI-PURPOSE REGISTERS

The multi-purpose registers are CPU registers (R0 to R15) which are used as accumulators for various computations and memory access pointers (field that indicates the address) .

- **Register bank configuration**



Special purposes are assumed for the following three registers out of the 16 registers. Thus, some instructions are emphasized.

R13 : Virtual accumulator (AC)

R14 : Frame Pointer (FP)

R15 : Stack Pointer (SP)

Initial values for R0 to R14 on resetting are unspecified. The initial value of R15 will be 0000 0000H (SSP value) .

■ MODE SETTING

1. Pins

• **Mode pins and set mode**

Mode pins			Mode name	Reset vector access areas	External data bus width	Bus modes
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8-bit	External ROM external bus mode
0	0	1	External vector mode 1	External	16-bit	
0	1	0	—	—	—	Setting is prohibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single chip mode*
1	—	—	—	—	—	Usage is prohibited

* : MB91110 series is not supported single chip mode.

2. Register

• **Mode register (MODR) and set mode**

Address
0000 07FF$_H$

M1	M0	*	*	*	*	*	*

Bus mode set bit

Initial value: XXXXXXXX$_B$
Access: W

W : Write only
X : Undecided
* : “0” should always be written for bits other than M1 and M0.

• **Bus mode set bit and its functions**

M1	M0	Functions	Remarks
0	0	Single chip mode	Not supported
0	1	Internal ROM external bus mode	Not supported
1	0	External ROM external bus mode	
1	1	—	Setting is prohibited

■ I/O MAP

Address	Register				Internal resource
	+0	+1	+2	+3	
000000H	—	PDR2 (R/W) XXXXXXXX	—	—	Port data register
000004H	—	PDR6 (R/W) XXXXXXXX	—	—	
000008H	PDRB (R/W) XXXXXXXX	PDRA (R/W) -XXXXXX-	—	PDR8 (R/W) --X--XXX	
00000CH	—				
000010H	—	—	PDRE (R/W) ----XXXX	PDRF (R/W) XXXXXXXX	
000014H	PDRG (R/W) --XXXXXX	PDRH (R/W) XXXXXXXX	PDRI (R/W) XXXXXXXX	—	
000018H	—				Reserved
00001CH	—				Reserved
000020H	SSR (R/W) 00001-00	SIDR/SODR (R/W) XXXXXXXX	SCR (R/W) 00000100	SMR (R/W) 00000-00	UART
000024H	—	CDCR (R/W) 0--11111	—		
000028H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload timer 0
00002CH	—		TMCSR (R/W) ----0000 00000000		
000030H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload timer 1
000034H	—		TMCSR (R/W) ----0000 00000000		
000038H	ADCR (R) ------XX XXXXXXXX		ADCS (R/W) 00000000 00000000		A/D converter (Sequential comparison type)
00003CH	—				Reserved

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000040H	—				Reserved
000044H	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG0
000048H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
00004CH	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG1
000050H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
000054H	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG2
000058H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
00005CH	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG3
000060H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
000064H	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG4
000068H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
00006CH	Access is prohibited		PCSR (W) XXXXXXXX XXXXXXXX		PPG5
000070H	PDUT (W) XXXXXXXX XXXXXXXX		PCNH (R/W) 0000000-	PCNL (R/W) 00000000	
000074H	—				Reserved
000078H	—				
00007CH	—				
000080H	—				

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000084H	—				Reserved
000088H	—				
00008CH	—				
000090H	—				
000094H	EIRR (R/W) 00000000	ENIR (R/W) 00000000	—		External interruption/ NMI
000098H	ELVR (R/W) 00000000 00000000		—		
00009CH	—				Reserved
0000A0H	—				
0000A4H	—				
0000A8H	—				
0000ACH	—				
0000B0H	—				
0000B4H	—				
0000B8H	—				
0000BCH	—				
0000C0H	—				
0000C4H	—				

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
0000C8H	—				Reserved
0000CCH	—				
0000D0H	—	—	DDRE (W) ----0000	DDRF (W) 00000000	Data direction register
0000D4H	DDRG (W) --000000	DDRH (W) 00000000	DDRI (W) 00000000	—	
0000D8H to 0000FCH	—				Reserved
000100H to 0001FCH	—				Reserved
000200H	DMACS0 (R/W) 0-00-000	00--0000	XX-00000	----XX-X	DMA controller channel 0
000204H	DMACC0 (R/W) ----XXXX	XXXX-XXX	XXXXXXXX	XXXXXXXX	
000208H	DMASA0 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
00020CH	DMADA0 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
000210H	DMACS1 (R/W) 0-00-000	00--0000	XX-00000	----XX-X	DMA controller channel 1
000214H	DMACC1 (R/W) ----XXXX	XXXX-XXX	XXXXXXXX	XXXXXXXX	
000218H	DMASA1 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
00021CH	DMADA1 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000220H	DMACS2 (R/W) 0-00-000	00--0000	XX-00000	----XX-X	DMA controller channel 2
000224H	DMACC2 (R/W) ----XXXX	XXXX-XXX	XXXXXXXX	XXXXXXXX	
000228H	DMASA2 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
00022CH	DMADA2 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
000230H	DMACS3 (R/W) 0-00-000	00--0000	XX-00000	----XX-X	DMA controller channel 3
000234H	DMACC3 (R/W) ----XXXX	XXXX-XXX	XXXXXXXX	XXXXXXXX	
000238H	DMASA3 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
00023CH	DMADA3 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
000240H	DMACS4 (R/W) 0-00-000	00--0000	XX-00000	----XX-X	DMA controller channel 4
000244H	DMACC4 (R/W) ----XXXX	XXXX-XXX	XXXXXXXX	XXXXXXXX	
000248H	DMASA4 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
00024CH	DMADA4 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
000250H	DMACR (R/W) --------	--------	00------	-------0	Overall DMA controller
000254H	—				Reserved
000258H	—				
00025CH	—				
000260H	—				

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000264H	—				Reserved
000268H	—				
00026CH	—				
000270H	—				
000274H	—				
000278H to 0002FCH	—				
000300H to 0003E0H	—				
0003E4H	—			ICHCR (R/W) --000000	Instruction cache
0003E8H	—				Reserved
0003ECH	—			IRMC (R/W) -------0	I-RAM control
0003F0H	BSD0 (W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	Bit search module
0003F4H	BSD1 (R/W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
0003F8H	BSDC (W) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
0003FCH	BSRR (R) XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	
000400H	ICR00 (R/W) ---11111	ICR01 (R/W) ---11111	ICR02 (R/W) ---11111	ICR03 (R/W) ---11111	Interruption controller
000404H	ICR04 (R/W) ---11111	ICR05 (R/W) ---11111	ICR06 (R/W) ---11111	ICR07 (R/W) ---11111	

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000408H	ICR08 (R/W) ---11111	ICR09 (R/W) ---11111	ICR10 (R/W) ---11111	ICR11 (R/W) ---11111	Interruption controller
00040CH	ICR12 (R/W) ---11111	ICR13 (R/W) ---11111	ICR14 (R/W) ---11111	ICR15 (R/W) ---11111	
000410H	ICR16 (R/W) ---11111	ICR17 (R/W) ---11111	ICR18 (R/W) ---11111	ICR19 (R/W) ---11111	
000414H	ICR20 (R/W) ---11111	ICR21 (R/W) ---11111	ICR22 (R/W) ---11111	ICR23 (R/W) ---11111	
000418H	ICR24 (R/W) ---11111	ICR25 (R/W) ---11111	ICR26 (R/W) ---11111	ICR27 (R/W) ---11111	
00041CH	ICR28 (R/W) ---11111	ICR29 (R/W) ---11111	ICR30 (R/W) ---11111	ICR31 (R/W) ---11111	
000420H	ICR32 (R/W) ---11111	ICR33 (R/W) ---11111	ICR34 (R/W) ---11111	ICR35 (R/W) ---11111	
000424H	ICR36 (R/W) ---11111	ICR37 (R/W) ---11111	ICR38 (R/W) ---11111	ICR39 (R/W) ---11111	
000428H	ICR40 (R/W) ---11111	ICR41 (R/W) ---11111	ICR42 (R/W) ---11111	ICR43 (R/W) ---11111	
00042CH	ICR44 (R/W) ---11111	ICR45 (R/W) ---11111	ICR46 (R/W) ---11111	ICR47 (R/W) ---11111	
000430H	DICR (R/W) -------0	HRCL (R/W) ---11111	—	—	Delay interruption
000434H to 00047CH	—				Reserved
000480H	RSRR/WTCR (R/W) 1XXXX-00	STCR (R/W) 000111--	PDRR (R/W) ----0000	CTBR (W) XXXXXXXX	Clock control area
000484H	GCR (R/W) 110011-1	WPR (W) XXXXXXXX	—		
000488H	PCTR (R/W) 00--0---	—			PLL control register
00048CH to 0005FCH	—				Reserved

(Continued)

(Continued)

Address	Register				Internal resource
	+0	+1	+2	+3	
000600H	—	DDR2 (W) 00000000	—	—	Data direction register
000604H	—	DDR6 (W) 00000000	—	—	
000608H	DDRB (W) 00000000	DDRA (W) -000000-	—	DDR8 (W) --0--000	
00060CH	ASR1 (W) 00000000	00000001	AMR1 (W) 00000000	00000000	External bus interface
000610H	ASR2 (W) 00000000	00000010	AMR2 (W) 00000000	00000000	
000614H	ASR3 (W) 00000000	00000011	AMR3 (W) 00000000	00000000	
000618H	ASR4 (W) 00000000	00000100	AMR4 (W) 00000000	00000000	
00061CH	ASR5 (W) 00000000	00000101	AMR5 (W) 00000000	00000000	
000620H	AMD0 (R/W) ---00111	AMD1 (R/W) 0--00000	AMD32 (R/W) 00000000	AMD4 (R/W) 0--00000	
000624H	AMD5 (R/W) 0--00000	DSCR (W) 00000000	RFCR (R/W) --XXXXXX	0---0000	
000628H	EPCR0 (W) ----1100	-1111111	EPCR1 (W) --------	11111111	
00062CH	DMCR4 (R/W) 00000000	0000000-	DMCR5 (R/W) 00000000	0000000-	
000630H to 0007F8H	—				Reserved
0007FCH	—		LER (W) -----000	MODR (W) XXXXXXXX	"Little endian" register Mode register

Note : Do not execute RMW instructions to registers with write-only bits.

RMW instruction (RMW : Read / Modify / Write)

AND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
ANDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
ANDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri

Data in areas with "—" or reserved ones is undecided.

■ INTERRUPTION VECTOR

Interruption factor and allocation of interruption vectors / interruption control registers are described in the interruption vector table.

Interruption source	Interruption number		Interruption level *1	Offset	Interruption vector address to TBR of default *2
	Decimal	Hexadecimal			
Reset	0	00	—	$3FC_H$	$000FFFFC_H$
System reservation	1	01	—	$3F8_H$	$000FFFF8_H$
System reservation	2	02	—	$3F4_H$	$000FFFF4_H$
System reservation	3	03	—	$3F0_H$	$000FFFF0_H$
System reservation	4	04	—	$3EC_H$	$000FFFEC_H$
System reservation	5	05	—	$3E8_H$	$000FFFE8_H$
System reservation	6	06	—	$3E4_H$	$000FFFE4_H$
Coprocessor absence trap	7	07	—	$3E0_H$	$000FFFE0_H$
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$
INTE instruction	9	09	4 fixed	$3D8_H$	$000FFFD8_H$
System reservation	10	0A	—	$3D4_H$	$000FFFD4_H$
System reservation	11	0B	—	$3D0_H$	$000FFFD0_H$
Step trace trap	12	0C	4 fixed	$3CC_H$	$000FFFCC_H$
System reservation	13	0D	—	$3C8_H$	$000FFFC8_H$
Exceptions to undefined instructions	14	0E	—	$3C4_H$	$000FFFC4_H$
NMI request	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$
System reservation	16	10	ICR00	$3BC_H$	$000FFFBC_H$
System reservation	17	11	ICR01	$3B8_H$	$000FFFB8_H$
External interruption 0	18	12	ICR02	$3B4_H$	$000FFFB4_H$
External interruption 1	19	13	ICR03	$3B0_H$	$000FFFB0_H$
External interruption 2	20	14	ICR04	$3AC_H$	$000FFFAC_H$
External interruption 3	21	15	ICR05	$3A8_H$	$000FFFA8_H$
External interruption 4	22	16	ICR06	$3A4_H$	$000FFFA4_H$
External interruption 5	23	17	ICR07	$3A0_H$	$000FFFA0_H$
External interruption 6	24	18	ICR08	$39C_H$	$000FFF9C_H$
External interruption 7	25	19	ICR09	398_H	$000FFF98_H$
System reservation	26	1A	ICR10	394_H	$000FFF94_H$
UART reception completion	27	1B	ICR11	390_H	$000FFF90_H$
System reservation	28	1C	ICR12	$38C_H$	$000FFF8C_H$
System reservation	29	1D	ICR13	388_H	$000FFF88_H$
UART transmission completion	30	1E	ICR14	384_H	$000FFF84_H$
System reservation	31	1F	ICR15	380_H	$000FFF80_H$

(Continued)

Interruption source	Interruption number		Interruption level *1	Offset	Interruption vector address to TBR of default *2
	Decimal	Hexadecimal			
System reservation	32	20	ICR16	37C$_H$	000FFF7C$_H$
DMAC0 (end, error)	33	21	ICR17	378$_H$	000FFF78$_H$
DMAC1 (end, error)	34	22	ICR18	374$_H$	000FFF74$_H$
DMAC2 (end, error)	35	23	ICR19	370$_H$	000FFF70$_H$
DMAC3 (end, error)	36	24	ICR20	36C$_H$	000FFF6C$_H$
DMAC4 (end, error)	37	25	ICR21	368$_H$	000FFF68$_H$
System reservation	38	26	ICR22	364$_H$	000FFF64$_H$
System reservation	39	27	ICR23	360$_H$	000FFF60$_H$
System reservation	40	28	ICR24	35C$_H$	000FFF5C$_H$
A/D sequential conversion type	41	29	ICR25	358$_H$	000FFF58$_H$
Reload timer 0	42	2A	ICR26	354$_H$	000FFF54$_H$
Reload timer 1	43	2B	ICR27	350$_H$	000FFF50$_H$
16-bit PPG timer 0	44	2C	ICR28	34C$_H$	000FFF4C$_H$
16-bit PPG timer 1	45	2D	ICR29	348$_H$	000FFF48$_H$
16-bit PPG timer 2	46	2E	ICR30	344$_H$	000FFF44$_H$
16-bit PPG timer 3	47	2F	ICR31	340$_H$	000FFF40$_H$
16-bit PPG timer 4	48	30	ICR32	33C$_H$	000FFF3C$_H$
16-bit PPG timer 5	49	31	ICR33	338$_H$	000FFF38$_H$
System reservation	50	32	ICR34	334$_H$	000FFF34$_H$
System reservation	51	33	ICR35	330$_H$	000FFF30$_H$
System reservation	52	34	ICR36	32C$_H$	000FFF2C$_H$
System reservation	53	35	ICR37	328$_H$	000FFF28$_H$
System reservation	54	36	ICR38	324$_H$	000FFF24$_H$
System reservation	55	37	ICR39	320$_H$	000FFF20$_H$
System reservation	56	38	ICR40	31C$_H$	000FFF1C$_H$
System reservation	57	39	ICR41	318$_H$	000FFF18$_H$
System reservation	58	3A	ICR42	314$_H$	000FFF14
System reservation	59	3B	ICR43	310$_H$	000FFF10$_H$
System reservation	60	3C	ICR44	30C$_H$	000FFF0C$_H$
System reservation	61	3D	ICR45	308$_H$	000FFF08$_H$
System reservation	62	3E	ICR46	304$_H$	000FFF04$_H$
Delay interruption factor bit	63	3F	ICR47	300$_H$	000FFF00$_H$
System reservation (used under REALOS) *3	64	40	—	2FC$_H$	000FFEFC$_H$

(Continued)

(Continued)

Interruption source	Interruption number		Interruption level *1	Offset	Interruption vector address to TBR of default *2
	Decimal	Hexadecimal			
System reservation (used under REALOS) *3	65	41	—	$2F8_H$	$000FFEF8_H$
Used under INT instruction	66 to 255	42 to FF	—	$2F4_H$ to 000_H	$000FFEF4_H$ to $000FFD00_H$

*1 : ICR sets the interruption level for each interruption request using the register built into the interruption controller. ICR is prepared in accordance with each interruption request.

*2 : TBR is the register that indicates the starting address of the vector table for EIT. Addresses with added offset values that are specified per TBR and EIT factor will be the vector addresses.

*3 : REALOS OS/FR uses 0X40, 0X41 interruptions for system codes.

Reference :

The vector area for EIT is 1 KB in accordance with the address shown by TBR.
The size per vector is 4 bytes, and the relationship between the vector numbers and their addresses is shown as follows.

vctadr = TBR + vctofs
= TBR + $(3FC_H - 4 \times vct)$

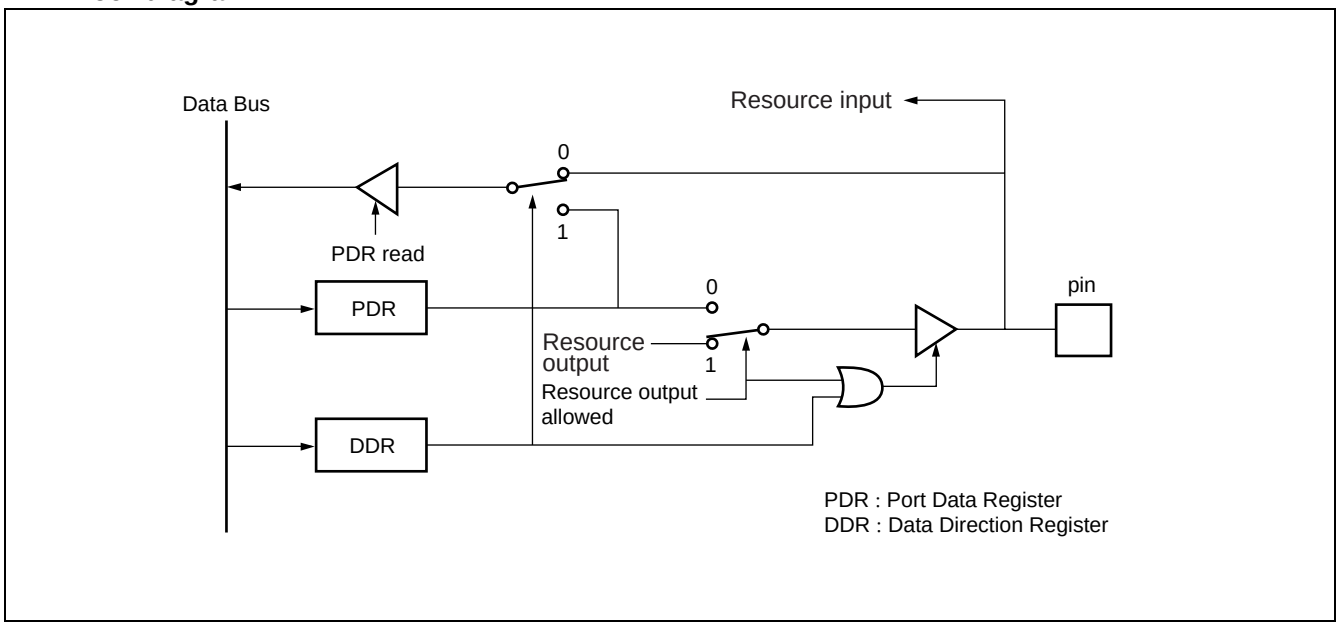
vctadr : vector address vctofs : vector offset vct : vector number

■ PERIPHERAL RESOURCES

1. I/O Port

MB91110 series can be used as the I/O port when settings for resources that handle each pin do not to use the pins for input/output.

- **Block diagram**



- **I/O Port Registers**

I/O port is composed of the Port Data Register (PDR) and Data Direction Register (DDR) .

- In cases where the input mode is DDR = “0”

  For PDR reading : Level of external pins to be handled is read out.

  For PDR writing : Set value is written in PDR.

- In cases where the output mode is DDR = “1”

  For PDR reading : PDR value is read out.

  For PDR writing : Set value is written in PDR and the PDR value is simultaneously output to the externally handled pin.

2. Port Data Register (PDR)

Port Data Register (PDR2-I) is the input/output data register for the I/O port.

Input/output control is carried out by the handled data direction register (DDR2-I) .

- **Port Data Register** (**PDR**)

		7	6	5	4	3	2	1	0	Initial value	Access
PDR2	Address : 000001H	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB	R/W
PDR6	Address : 000005H	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB	R/W
PDR8	Address : 00000BH	—	—	P85	—	—	P82	P81	P80	- - X- - XXXB	R/W
PDRA	Address : 000009H	—	PA6	PA5	PA4	PA3	PA2	PA1	—	- XXXXXX- B	R/W
PDRB	Address : 000008H	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	XXXXXXXXB	R/W
PDRE	Address : 000012H	—	—	—	—	PE3	PE2	PE1	PE0	- - - - XXXXB	R/W
PDRF	Address : 000013H	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	XXXXXXXXB	R/W
PDRG	Address : 000014H	—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - XXXXXXB	R/W
PDRH	Address : 000015H	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	XXXXXXXXB	R/W
PDRI	Address : 000016H	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	XXXXXXXXB	R/W

3. Data Direction Register (DDR)

The Data Direction Register (DDR2-I) controls the input/output direction of the I/O port per bit.
0 is used for input and 1 is used to execute output control.

- **Data Direction Register** (**DDR**)

DDR2
Address : 000601H

7	6	5	4	3	2	1	0	Initial value	Access
P27	P26	P25	P24	P23	P22	P21	P20	00000000B	W

DDR6
Address : 000605H

7	6	5	4	3	2	1	0	Initial value	Access
P67	P66	P65	P64	P63	P62	P61	P60	00000000B	W

DDR8
Address : 00060BH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	P85	—	—	P82	P81	P80	- - 0 - - 000B	W

DDRA
Address : 000609H

7	6	5	4	3	2	1	0	Initial value	Access
—	PA6	PA5	PA4	PA3	PA2	PA1	—	- 000000 -B	W

DDRB
Address : 000608H

7	6	5	4	3	2	1	0	Initial value	Access
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	W

DDRE
Address : 0000D2H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	PE3	PE2	PE1	PE0	- - - - 0000B	W

DDRF
Address : 0000D3H

7	6	5	4	3	2	1	0	Initial value	Access
PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	00000000B	W

DDRG
Address : 0000D4H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - 000000B	W

DDRH
Address : 0000D5H

7	6	5	4	3	2	1	0	Initial value	Access
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000B	W

DDRI
Address : 0000D6H

7	6	5	4	3	2	1	0	Initial value	Access
PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	00000000B	W

4. Instruction Cache

The instruction cache is a temporary storage memory. In the event that the instruction codes are accessed from a low speed external memory, it holds the accessed codes internally, and is used to increase the access speed for all subsequent accesses.

Direct read or write access can not be done by instruction cache or instruction cache tag using software.

- **Cacheable area of the instruction cache**

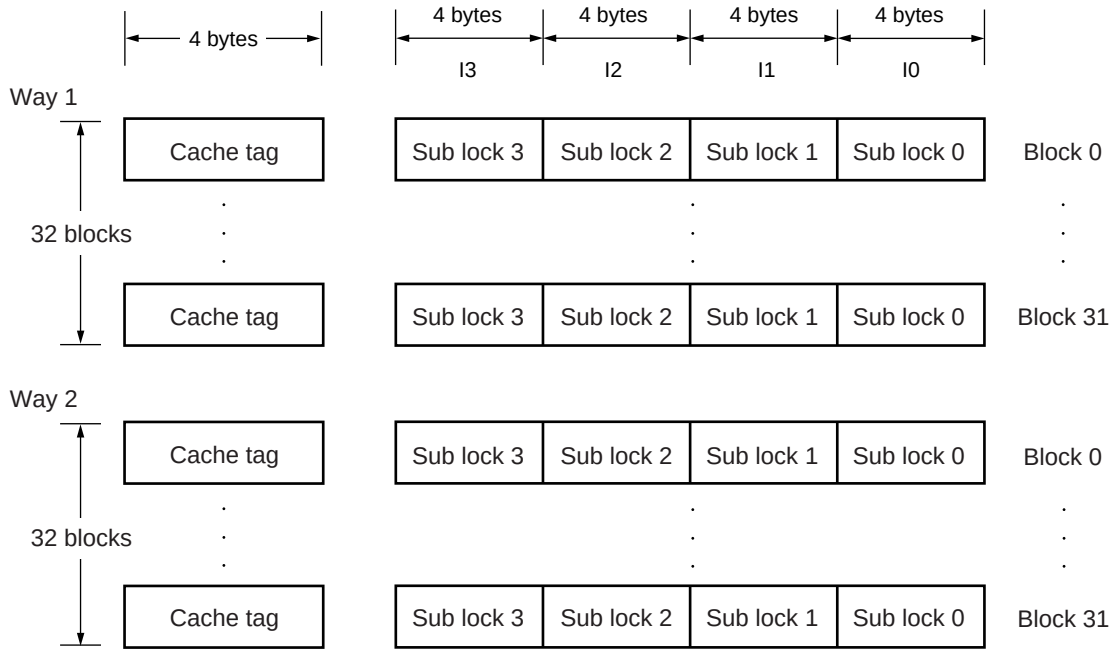
Instruction cache allows all space to become a cacheable area.

- Even though details of the external memory are updated by DMA transfer, it is not coherent with the cache details. In this case, coherency should be established by flushing the cache.

- **Instruction cache configuration**
- Basic instruction length of FR series : 2 bytes
- Block layout : 2-way set associative type
- Block
  1 way is configured of 32 blocks.
  1 block is 16 bytes (= 4 sub blocks)
  1 sub block is 4 bytes (= 1 bus access unit)

The instruction cache configuration is shown in the following figure.

Instruction Cache Configuration

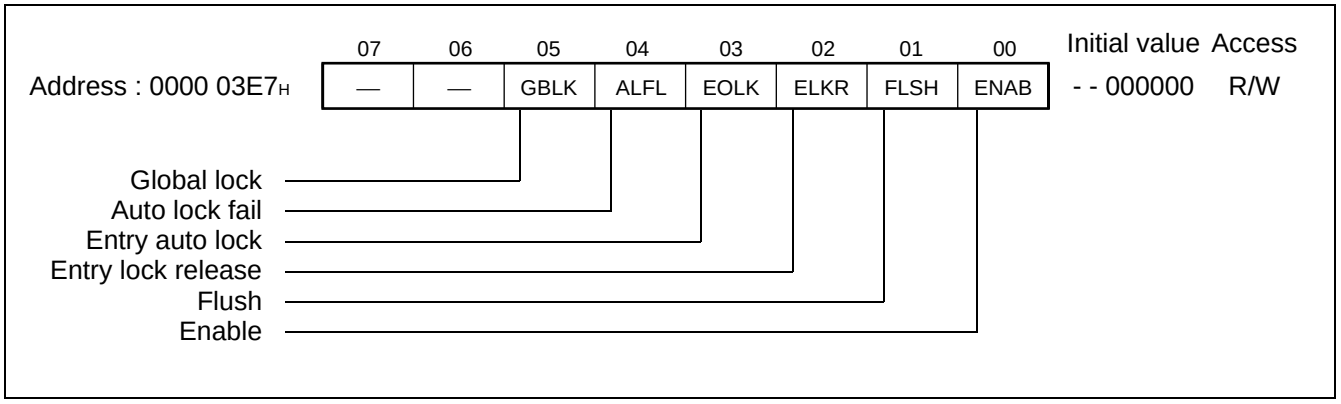


5. Instruction Cache Control Register (ICHCR)

The Instruction Cache Control Register (ICHCR) controls the operation of the instruction cache. Writing to ICHCR may effect the cache operation of instructions to be retrieved within the next three cycles.

- **Instruction Cache Control Register** (**ICHCR**)

Instruction Cache Control Register (ICHCR) is shared for use by ways 1 and 2.



6. Clock Generator (Low power consumption mechanism)

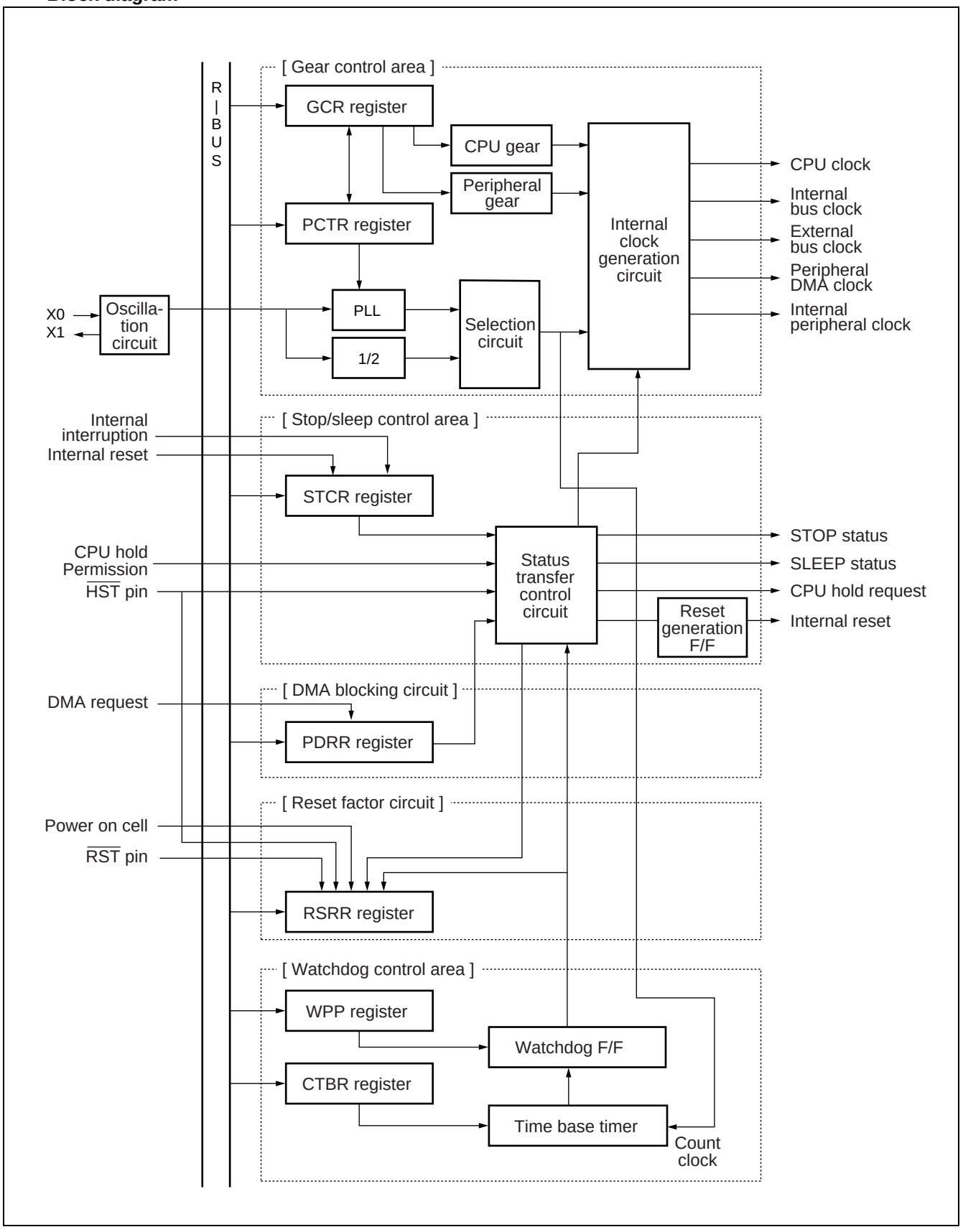
The clock generation area is a module with the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and holding factors
- Standby function (including hardware standby)
- Restraining DMA request
- PLL (Phase Locked Loop) is built in

- **Register list**

Address	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Initial value	Access
000480H	RSRR/WTCR								STCR								1XXXX- 00B	R/W
000481H																	000111 - - B	R/W
000482H					PDRR				CTBR								- - - - 0000B	R/W
000483H																	XXXXXXXXB	W
000484H	GCR								WPR								110011- 1B	R/W
000485H																	XXXXXXXXB	W
000488H	PCTR																00 - - 0 - - - B	R/W

- **Block diagram**



7. Bus Interface Outline

The bus interface controls the interface with external memory and external I/O.

- **Bus Interface Characteristics**
- 24-bit (16 MB) address output
- 6 individual banks using chip selection function
  Random positional setting is possible on the logical address space at minimum 64-KB units.
  Total 16 MB × 6 areas can be set using the address pin and chip selection pin.
- 16/8-bit bus width can be set per chip selection area.
- Insertion of programmable “automatic memory wait” (maximum of 7 cycles)
- Supports DRAM interface
  3 types of DRAM interface
    Double CAS DRAM (Normal DRAM I/F)
    Single CAS DRAM
    Hyper DRAM
  2-bank individual control (control signal i.e. RAS and CAS)
  DRAM can be selected from 2CAS/1WE or 1CAS/2WE.
  Supports high-speed page mode
  Supports CBR / self refresh
  Programmable corrugation
- Unused addresses / data pins can be used as I/O ports.
- Supports “little endian” mode
- Using clock doubler : Internal 50 MHz, external bus 25 MHz operation

- **Chip Selection Area**

A total of six types of chip selection areas are prepared for the bus interface. The position of each area can be randomly arranged per 64 KB at least using area selection registers (ASR1 to 5) and area mask registers (AMR1 to 5) in an area of 4 GB. In the event that access to an external bus is attempted in areas that are specified by those registers, the supported chip selection signals ($\overline{CS0}$ to $\overline{CS5}$) become activated to “L”. Such pins other than $\overline{CS0}$ are deactivated to “H” when reset.

Note : The area 0 is allocated to space outside the area specified by ASR1 to ASR5. External areas other than 0001 0000_H to 0005 $FFFF_H$ are deemed area 0 on resetting.

- **Interface**

The bus interface has the following interface types.

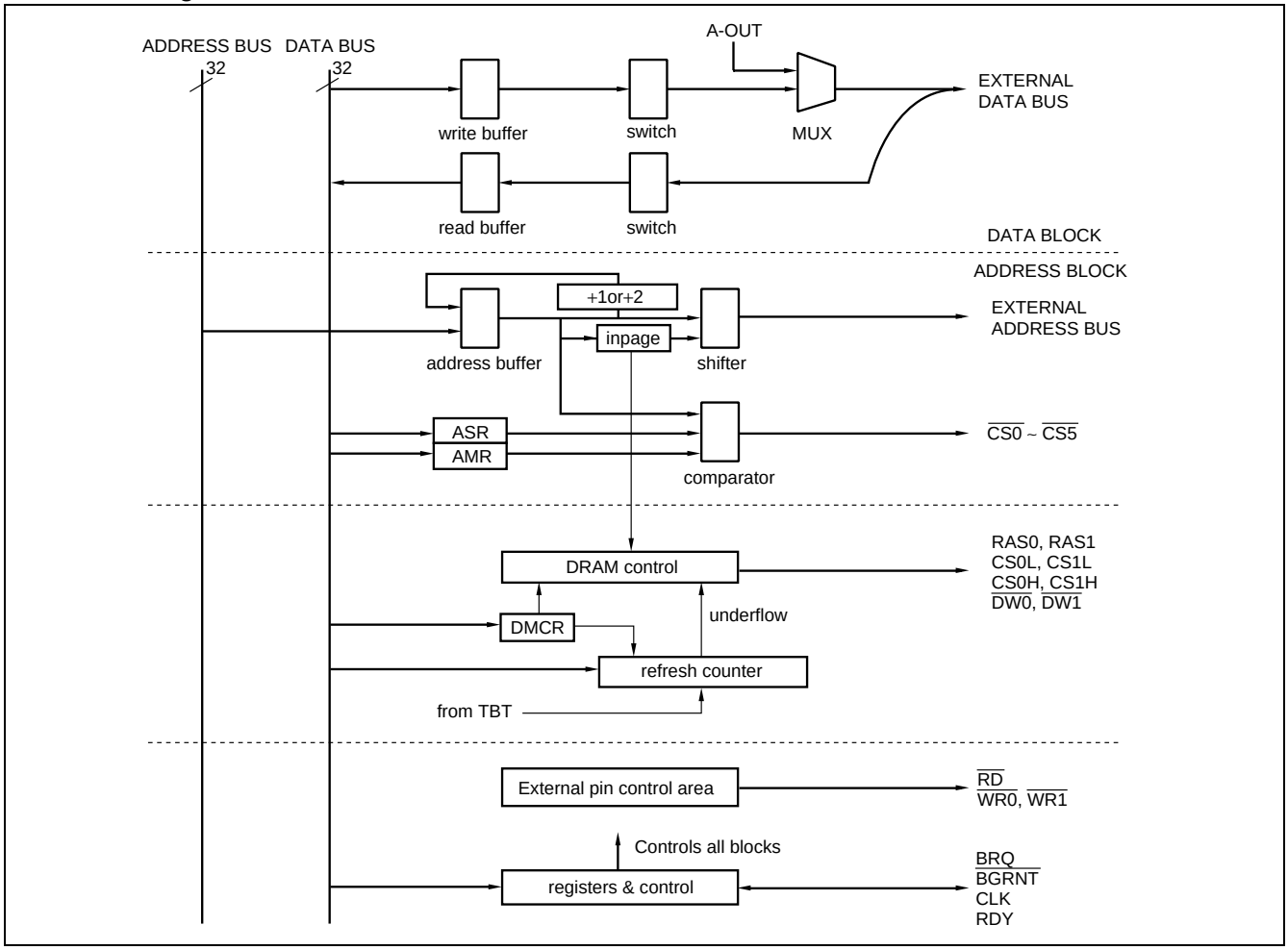
- Normal bus interface
- DRAM interface

These interfaces can only be used in predetermined areas. The following table shows each chip selection area and the usable interface functions.Which interface is to be used is selected in the Area Mode Register (AMD) . If no selection is made, it defaults to the normal bus interface.

Chip Selection Area and Selectable Bus Interfaces

Areas	Selectable bus interface			Remarks
	Normal bus	Time division	DRAM	
0	○	—	—	On resetting
1	○	—	—	
2	○	—	—	
3	○	—	—	
4	○	—	○	
5	○	—	○	

- **Block Diagram**



- **Register List**

Address	31 ---------- 24	23 ---------- 16	15 ---------- 8	7 ---------- 0	Initial value	Access
00060CH 00060EH	ASR1 (Area Select Reg. 1)		AMR1 (Area Mode Reg. 1)		00000000 00000001B 00000000 00000000B	W W
000610H 000612H	ASR2 (Area Select Reg. 2)		AMR2 (Area Mode Reg. 2)		00000000 00000010B 00000000 00000000B	W W
000614H 000616H	ASR3 (Area Select Reg. 3)		AMR3 (Area Mode Reg. 3)		00000000 00000011B 00000000 00000000B	W W
000618H 00061AH	ASR4 (Area Select Reg. 4)		AMR4 (Area Mode Reg. 4)		00000000 00000100B 00000000 00000000B	W W
00061CH 00061EH	ASR5 (Area Select Reg. 5)		AMR5 (Area Mode Reg. 5)		00000000 00000101B 00000000 00000000B	W W
000620H 000622H	AMD0 *1	AMD1 *1	AMD32 *1	AMD4 *1	- - - 00111 0- - 00000B 00000000 0- - 00000B	R/W R/W
000624H 000626H	AMD5 *1	DSCR *2	RFCR (Refresh Control Register)		0- - 00000 00000000B - -XXXXXX 0- - - 0000B	R/W R/W
000628H 00062AH	EPCR0 (External Pin Control 0)		EPCR1 (External Pin Control 1)		- - - - 1100 - 0000000B - - - - - - - - 11111111B	W W
00062CH 00062EH	DMCR4 (DRAM Control Reg. 4)		DMCR5 (DRAM Control Reg. 5)		00000000 0000000- B 00000000 0000000- B	R/W R/W
0007FCH			LER *3	MODR *4	- - - - - - 00 XXXXXXXX B	W

*1 : AMD (Area MoDe register)
*2 : DSCR (DRAM Signal Control Register)
*3 : LER (Little Endian Register)
*4 : MODR (MODe Register)

8. 16-bit Reload Timer

The 16-bit timer is composed of a 16-bit down counter, 16-bit reload register, a pre-scalar for internal count clock preparation and a control register. Selection of the input clock can be made from three types of internal clock (machine clocks with 2, 8 and 32 cycles) and an external clock are selectable for input clock.

- **Characteristics of the 16-bit reload timer**

The Pin Output (TO) outputs a toggle waveform whenever underflow is generated in reload mode, and outputs rectangular waves indicating that it is counting in the case of one shot mode.

Pin Input (TI) can be used for event input in the case of external event count mode, trigger input or gate input for internal clock mode.

If the external event count function is used as the reload mode, it can be used as the cycle device for the external clock.

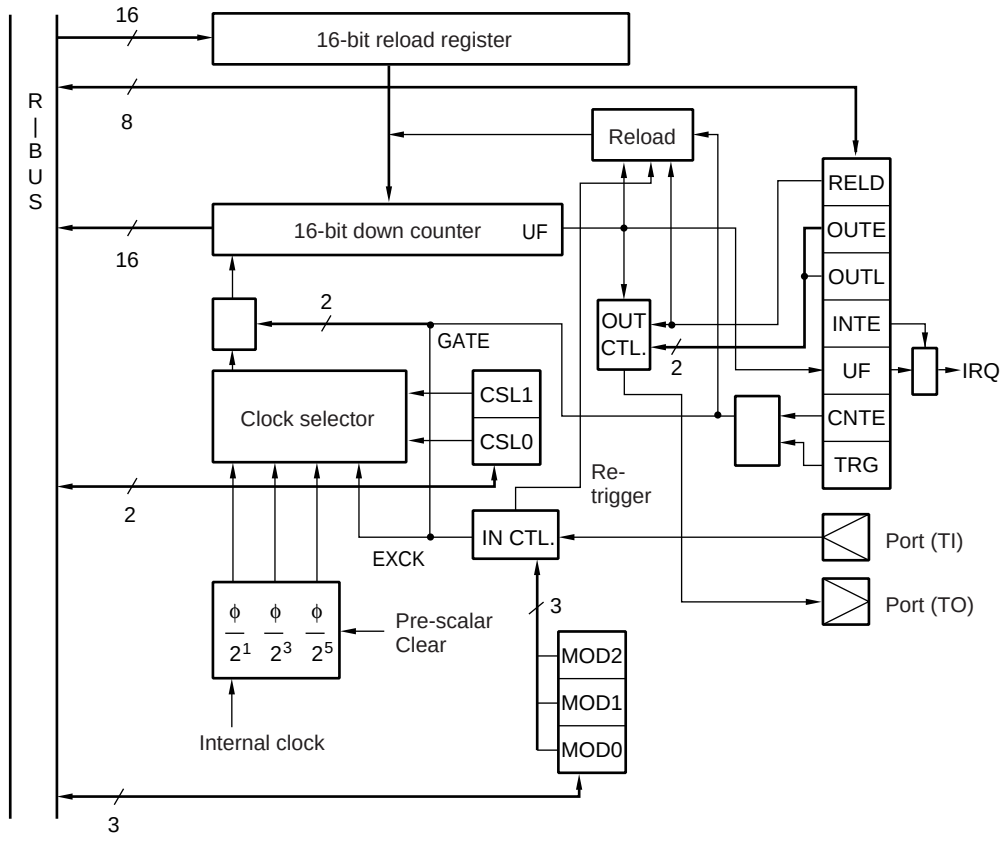
In this type, a 2-channel timer is built-in.

Channel 0 of the reload timer can start up DMA transfer using the interruption request signal.

The DMA controller clears the interruption flag of the reload timer at the same time as receiving the transfer request.

The TO output from channel 0 for the reload timer is connected to the A/D converter inside the LSI. Thus, A/D conversion can be started on a cycle set at the reload register.

- **Block Diagram**



- **Register List**

- Control status register (TMCSR)

Address	15	14	13	12	11	10	9	8	Initial value	Access
000036H	—	—	—	—	CSL1	CSL0	MOD2	MOD1	- - - - 0000B	R/W
	7	6	5	4	3	2	1	0		
000037H	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000B	R/W

- 16-bit timer register (TMR)

Address	15	0	Initial value		Access
00002AH			XXXXXXXX	XXXXXXXXB	W
000032H			XXXXXXXX	XXXXXXXXB	

- 16-bit reload register (TMRLR)

Address	15	0	Initial value		Access
000028H			XXXXXXXX	XXXXXXXXB	W
000030H			XXXXXXXX	XXXXXXXXB	

9. PPG Timer

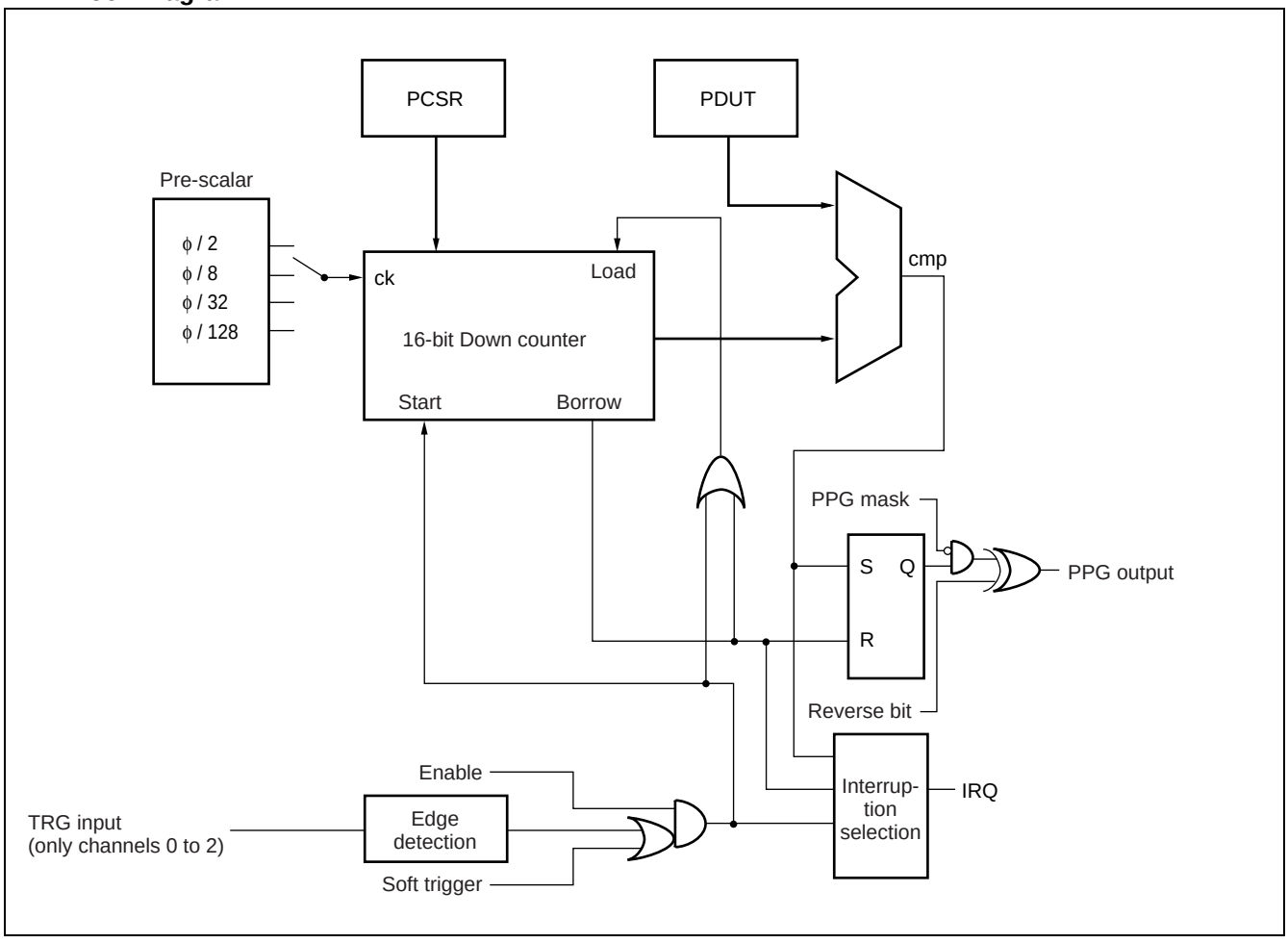
The PPG timer can output pulses that are synchronized with soft triggers or externally. Also, the cycle and duty of the output pulses can be changed randomly by replacing the two 16-bit register values. In this type, there are 6 built-in channels with this function.

- **PPG timer function**

The PPG timer has two functions as follows.

- PWM function
  This can be synchronized to the trigger and is programmable to output pulses while rewriting the above register values. It can also be used as a D/A converter by using an additional circuit.
- One-shot function
  This detects the edge of the trigger input and outputs a single pulse.

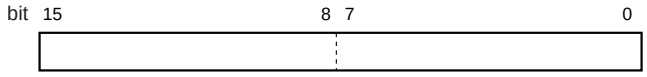
- **Block Diagram**



- **Register List**

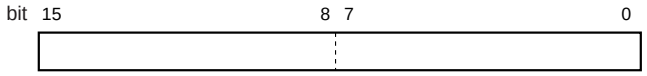
- Cycle setting register (PCSR)

Address	Initial value	Access
000046H 00004EH 000056H 00005EH 000066H 00006EH	XXXXXXXX XXXXXXXXB	W



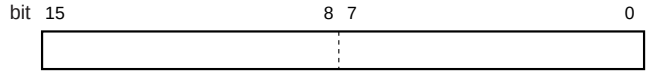
- Duty setting register (PDUT)

Address	Initial value	Access
000048H 000050H 000058H 000060H 000068H 000070H	XXXXXXXX XXXXXXXXB	W



- Control/status register (PCNH/PCNL)

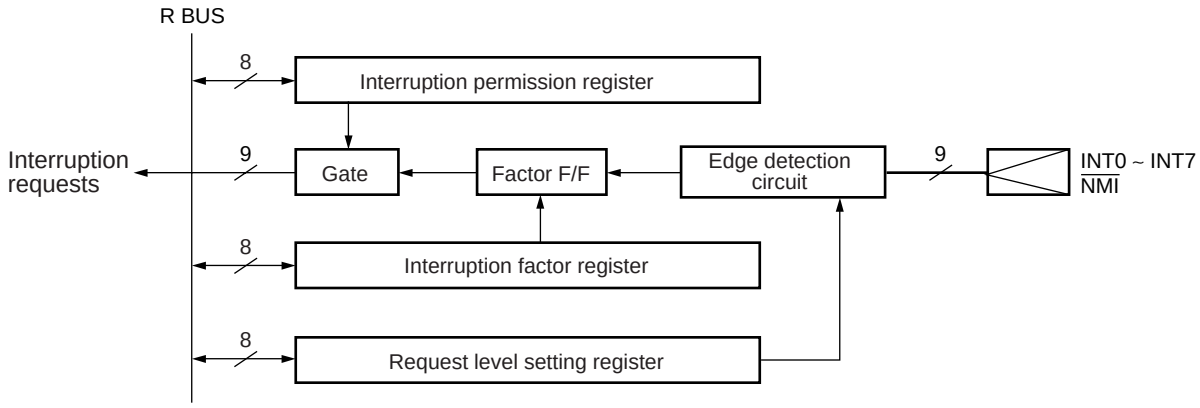
Address	Initial value	Access
00004AH 000052H 00005AH 000062H 00006AH 000072H	0000000 - 00000000B	R/W



10. External Interruption/NMI Control Area

The external interruption / NMI control area controls the external interruption requests to be input to the $\overline{\text{NMI}}$ and INT0 to INT7. “H” or “L” and “rising edge” or “falling edge” can be selected as the requested detection level (except for NMI) . Also, four requests from INT0 to INT3 can be used as the DMA request.

- **Block diagram**



- **Register list**

- External interruption permission register (ENIR)

Address	bit 7	6	5	4	3	2	1	0	Initial value	Access
000095H	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	00000000B	R/W

- External interruption factors register (EIRR)

Address	bit 15	14	13	12	11	10	9	8	Initial value	Access
000094H	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	00000000B	R/W

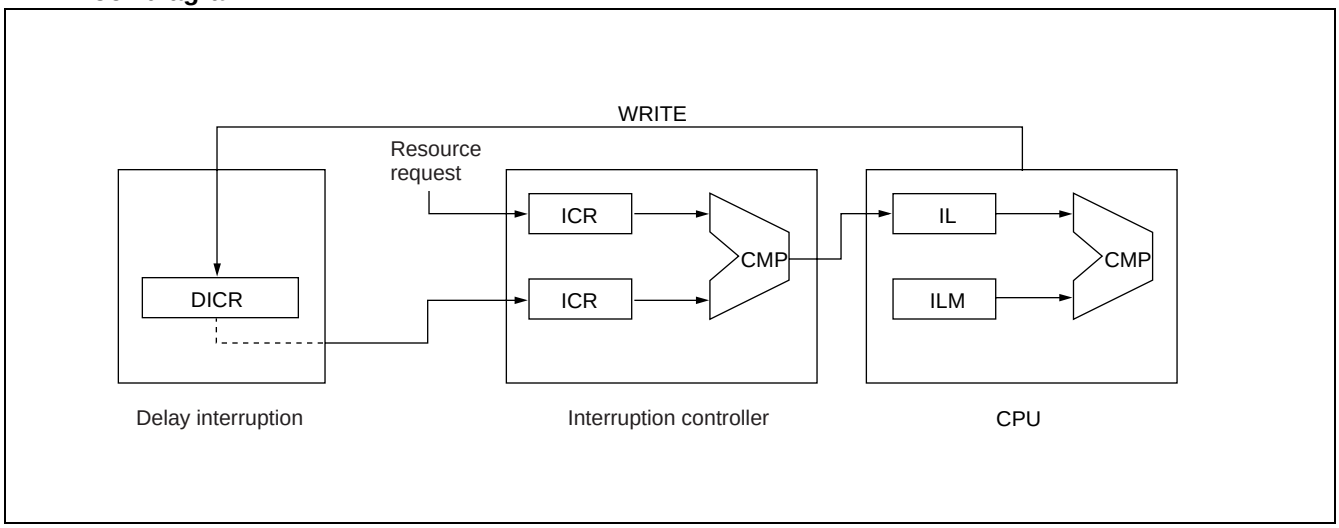
- Request level setting register (ELVR)

Address	bit 15	14	13	12	11	10	9	8	Initial value	Access
000098H	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	00000000B	R/W
	bit 7	6	5	4	3	2	1	0		
000099H	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000B	R/W

11. Delay Interruption Modules

This is a module to generate interruptions to switch tasks. This module can be used with software to generate/ cancel interruption requests to the CPU.

- **Block diagram**



- **Register list**

Address	bit	7	6	5	4	3	2	1	0	Initial value	Access
000430H		—	—	—	—	—	—	—	DLYI	- - - - - - - 0B	R/W

12. Interruption Controller

The interruption controller carries out interruption reception and arbitration.

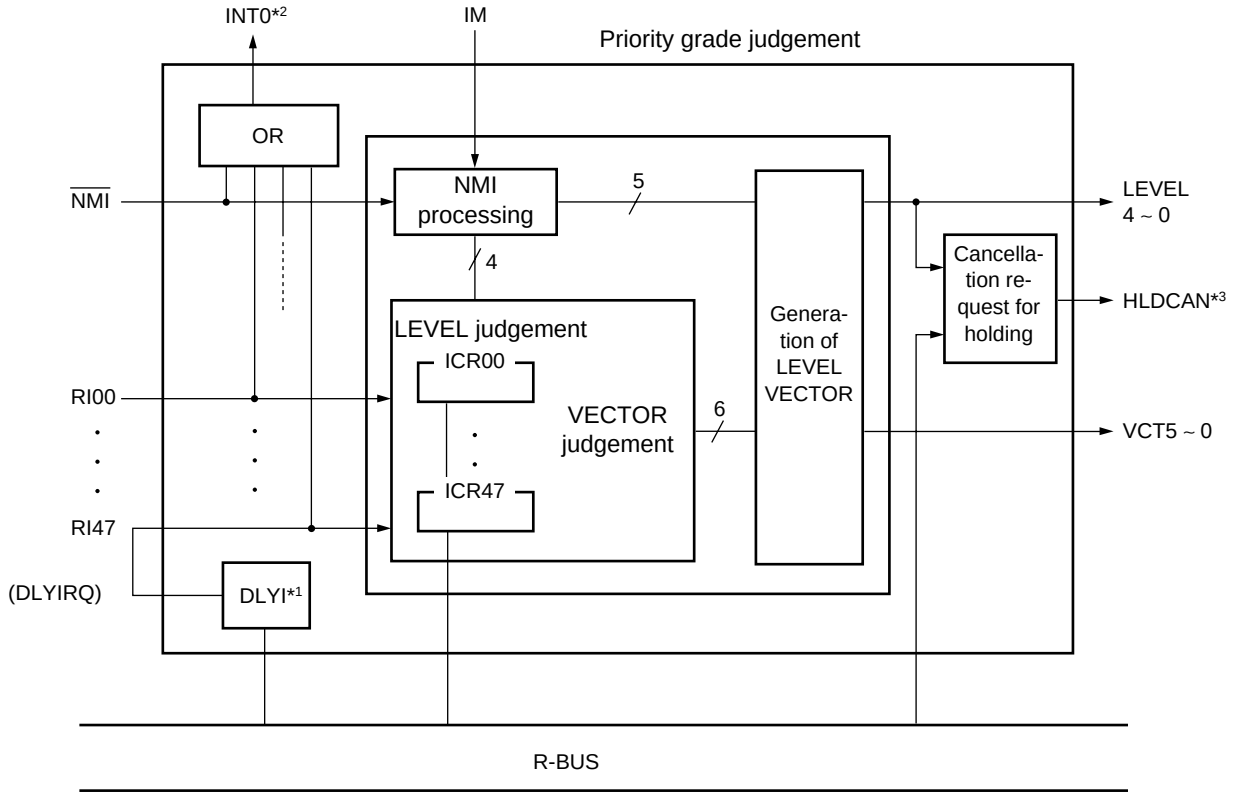
- **Hardware configuration of the interruption controller**

This module is configured for the following items.
- ICR register
- Interruption priority judgement circuit
- Interruption level, interruption number (vector) generation area
- Cancellation request generation area for HOLD request

- **Major interruption controller functions**

This module has the following functions.
- Detection of NMI request / interruption request
- Priority grade judgement (depending on the level and number)
- Transferring interruption level of factors for the judgement results (to CPU)
- Transferring interruption number of factors for the judgement results (to CPU)
- Recovery instruction from stop mode by generating NMI / interruption
- Cancellation of HOLD request to the bus master

- **Block Diagram**



*1 : DLYI indicates delay interruption. (Refer to the chapter on delay interruption module for details.)
*2 : INTO is the wake-up signal to the clock control area in case of sleep or stop.
*3 : HLDCAN is the bus vacation request signal to bus masters other than the CPU.

- **Register list**

Address	bit 7	6	5	4	3	2	1	0		Initial value	Acces
000400H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00	- - - 11111	R/W
000401H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01	- - - 11111	R/W
000402H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02	- - - 11111	R/W
000403H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03	- - - 11111	R/W
000404H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04	- - - 11111	R/W
000405H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05	- - - 11111	R/W
000406H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06	- - - 11111	R/W
000407H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07	- - - 11111	R/W
000408H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08	- - - 11111	R/W
000409H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09	- - - 11111	R/W
00040AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10	- - - 11111	R/W
00040BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11	- - - 11111	R/W
00040CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12	- - - 11111	R/W
00040DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13	- - - 11111	R/W
00040EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14	- - - 11111	R/W
00040FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15	- - - 11111	R/W
000410H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16	- - - 11111	R/W
000411H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17	- - - 11111	R/W
000412H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18	- - - 11111	R/W
000413H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19	- - - 11111	R/W
000414H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20	- - - 11111	R/W
000415H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21	- - - 11111	R/W
000416H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22	- - - 11111	R/W
000417H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23	- - - 11111	R/W
000418H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24	- - - 11111	R/W
000419H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25	- - - 11111	R/W
00041AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26	- - - 11111	R/W
00041BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27	- - - 11111	R/W
00041CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28	- - - 11111	R/W
00041DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29	- - - 11111	R/W
00041EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30	- - - 11111	R/W
00041FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31	- - - 11111	R/W
000420H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32	- - - 11111	R/W
000421H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33	- - - 11111	R/W
000422H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34	- - - 11111	R/W
000423H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35	- - - 11111	R/W
000424H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36	- - - 11111	R/W
000425H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37	- - - 11111	R/W
000426H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38	- - - 11111	R/W
000427H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39	- - - 11111	R/W
000428H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40	- - - 11111	R/W
000429H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41	- - - 11111	R/W
00042AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42	- - - 11111	R/W
00042BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43	- - - 11111	R/W
00042CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44	- - - 11111	R/W
00042DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45	- - - 11111	R/W
00042EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46	- - - 11111	R/W
00042FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47	- - - 11111	R/W
				R	R/W	R/W	R/W	R/W			
000431H	—	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL	- - - 11111	R/W
				R	R/W	R/W	R/W	R/W			

13. Interruption Control Register (ICR)

This function is set up per interruption input and sets the interruption level of interruption requests to be handled.

- **Register list**

bit 7	6	5	4	3	2	1	0
—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
			R	R/W	R/W	R/W	R/W

[bit 4 to 0] ICR4 to 0

The interruption level of the interruption requests that are handled is specified by the interruption level setting bit. In cases where the interruption level that is set in this register is the same as or more than the level mask value that is set (has been set) in the ILM register of the CPU, the interruption request is masked at the CPU side. It is initialized to 11111_B on resetting. The settable interruption level setting bit and interruption level are shown in following Table.

Interruption Level Setting Bit and Interruption Level

ICR4	ICR3	ICR2	ICR1	ICR0	Interruption level	
0	0	0	0	0	0	↕ System reservation
0	1	1	1	0	14	
0	1	1	1	1	15	NMI
1	0	0	0	0	16	Maximum settable level
1	0	0	0	1	17	↑ (High)
1	0	0	1	0	18	
1	0	0	1	1	19	
1	0	1	0	0	20	
1	0	1	0	1	21	
1	0	1	1	0	22	
1	0	1	1	1	23	
1	1	0	0	0	24	
1	1	0	0	1	25	
1	1	0	1	0	26	
1	1	0	1	1	27	
1	1	1	0	0	28	
1	1	1	0	1	29	
1	1	1	1	0	30	↓ (Low)
1	1	1	1	1	31	Interruption is prohibited

Note: ICR 4 is fixed as “1” and can not be written as “0”.

14. 10-bit A/D Converter

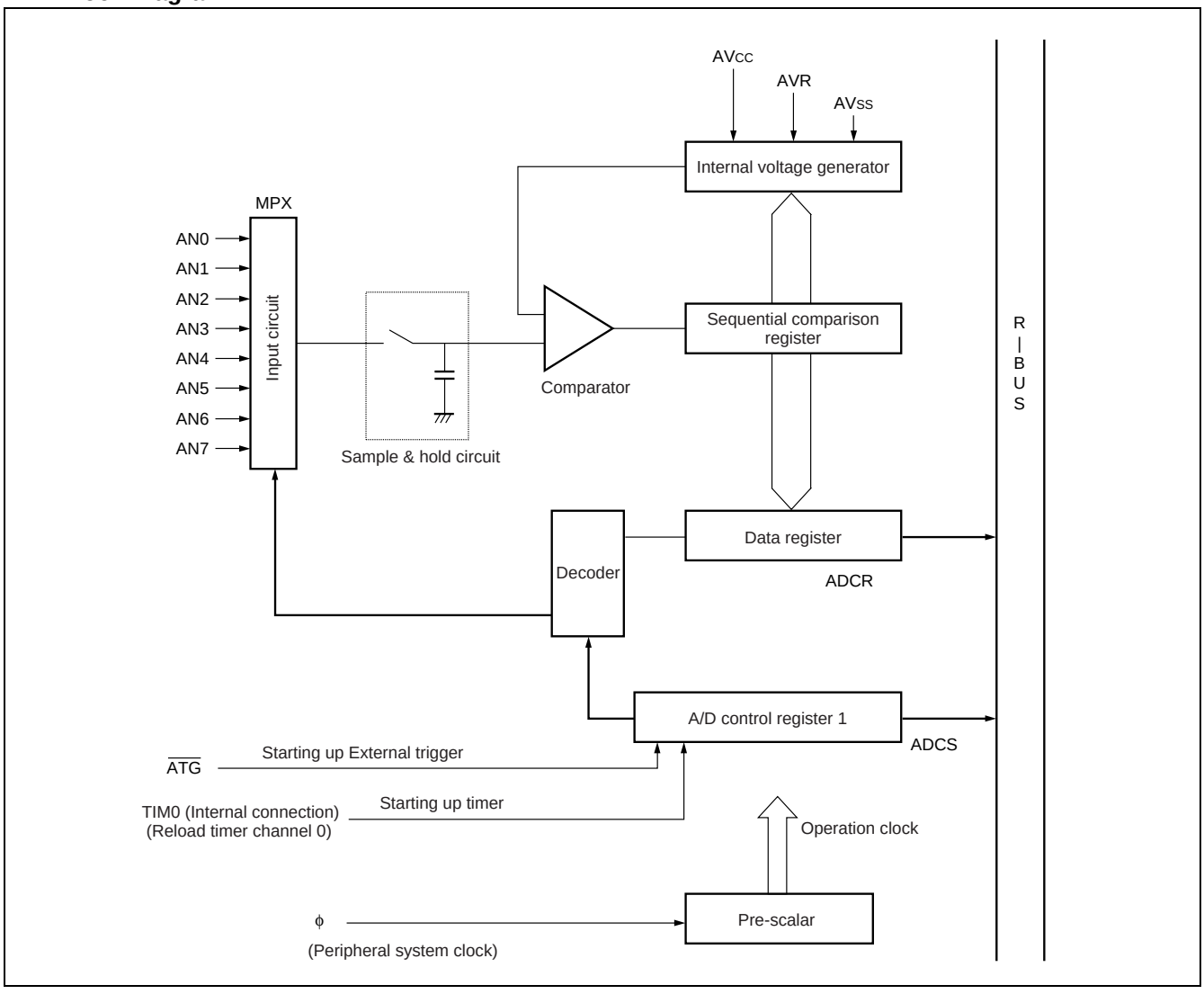
The A/D converter is the module that converts analog input voltages to a digital value.

- **Characteristics of A/D Converter**
- Minimum converting time : 5.6 µs/channel
- Sample & hold circuit is built-in.
- Resolution : 10 bits
- Selection can be made for analog input from 8 channels.

Single conversion mode	:	1 channel is selected for conversion
Scan conversion mode	:	Converts multiple number of consecutive channels. Maximum 8 channels are programmable.
Consecutive conversion mode	:	Repeatedly converts the specified channel.
Suspension / conversion mode	:	Suspends after converting 1 channel and waits until the next one is started up (synchronization for starting conversion is possible)

- Initiation of DMA transfer by interruption is possible.
- Initiation factor can be selected from software, external trigger (falling edge) or reload timer (rising edge) .

- **Block Diagram**



- **Register List**

• Control Status Register (ADCS)

Address	bit	15	14	13	12	11	10	9	8	Initial value	Access
00003A$_H$		BUSY	INT	INTE	PAUS	STS1	STS0	STRT	—	00000000$_B$	R/W

Address	bit	7	6	5	4	3	2	1	0	Initial value	Access
00003B$_H$		MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000$_B$	R/W

• Data Register (ADCR)

Address	bit	15	14	13	12	11	10	9	8	Initial value	Access
000038$_H$		—	—	—	—	—	—	9	8	- - - - - - XX$_B$	R

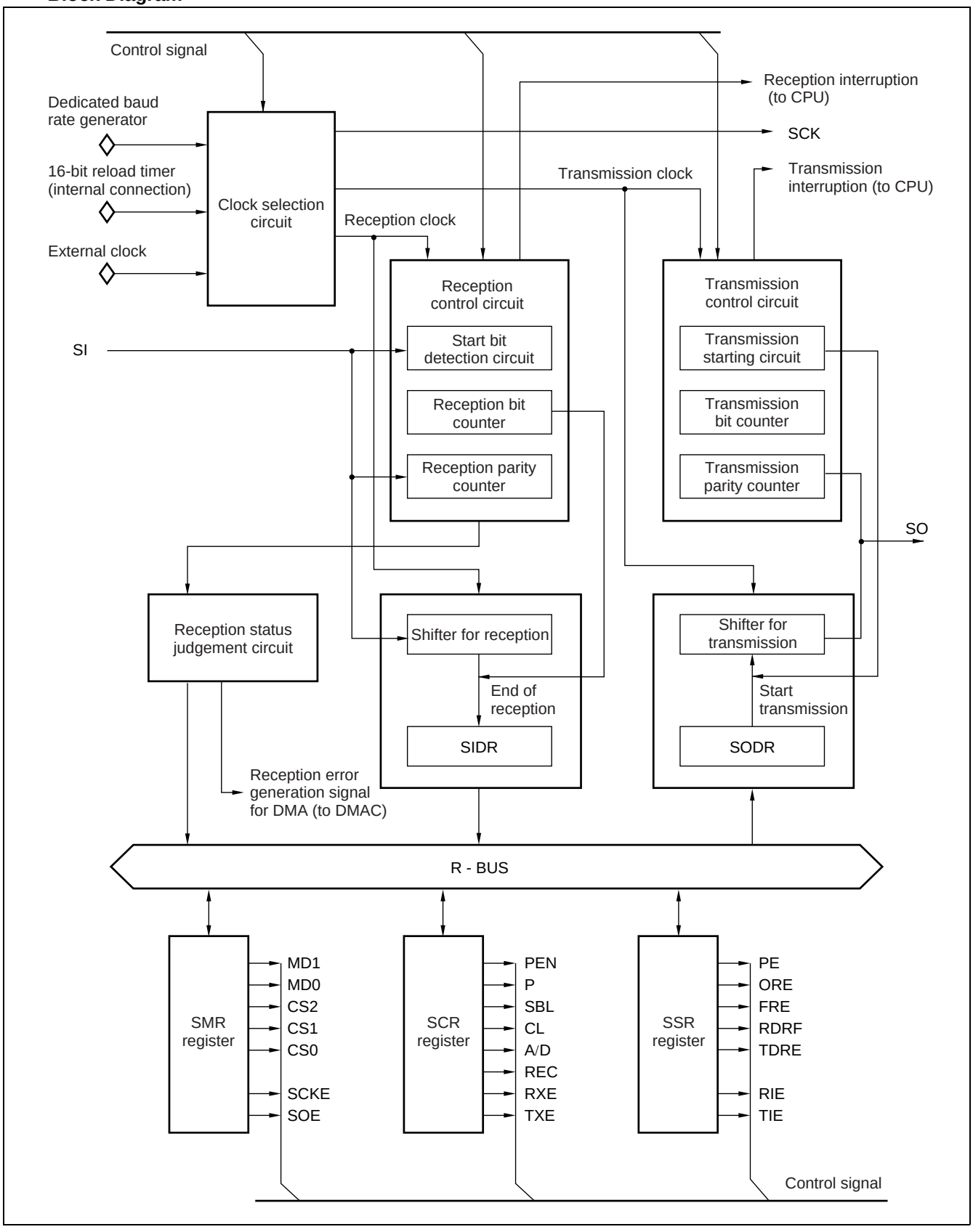
Address	bit	7	6	5	4	3	2	1	0	Initial value	Access
000039$_H$		7	6	5	4	3	2	1	0	XXXXXXXX$_B$	R

15. UART

UART is the serial I/O port for carrying out asynchronous (start-stop synchronization) or CLK synchronous communication.

- **Characteristics of UART**
- FDX double buffer
- Asynchronous (start-stop synchronization) and CLK synchronous communication are possible.
- Supports multi processor mode
- Dedicated baud rate generator is built-in.
- Free baud rate can be set using an external clock.
- Error detection function (parity, framing, overrun)
- Transfer signal is NRZ code
- Initiation of DMA transfer is possible by interruption.

- **Block Diagram**



- **Register List**

- Serial Mode Register (SMR)

Address	bit	7	6	5	4	3	2	1	0	Initial value	Access
000023H		MD1	MD0	CS2	CS1	CS0	—	SCKE	SOE	00000 - 00B	R/W

- Serial Control Register (SCR)

	bit	15	14	13	12	11	10	9	8	Initial value	Access
000022H		PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B	R/W

- Serial Input Data Register/Serial Output Data Register (SIDR/SODR)

	bit	7	6	5	4	3	2	1	0	Initial value	Access
000021H		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB	R/W

- Serial Status Register (SSR)

	bit	15	14	13	12	11	10	9	8	Initial value	Access
000020H		PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	00001 - 00B	R/W

- Communication Pre-scalar Control Register (CDCR)

	bit	7	6	5	4	3	2	1	0	Initial value	Access
000025H		MD	—	—	DIV4	DIV3	DIV2	DIV1	DIV0	0 - - 11111B	R/W

16. DMA Controller (DMAC)

The DMA controller is the module to realize Direct Memory Access (DMA) transfers with FR 30 series devices. DMA transfers controlled by this module enable quick and direct transfer of all data without using the CPU and thus system performance is increased.

- **Hardware Configuration of DMA Controller**

This module is mainly configured of the following items.

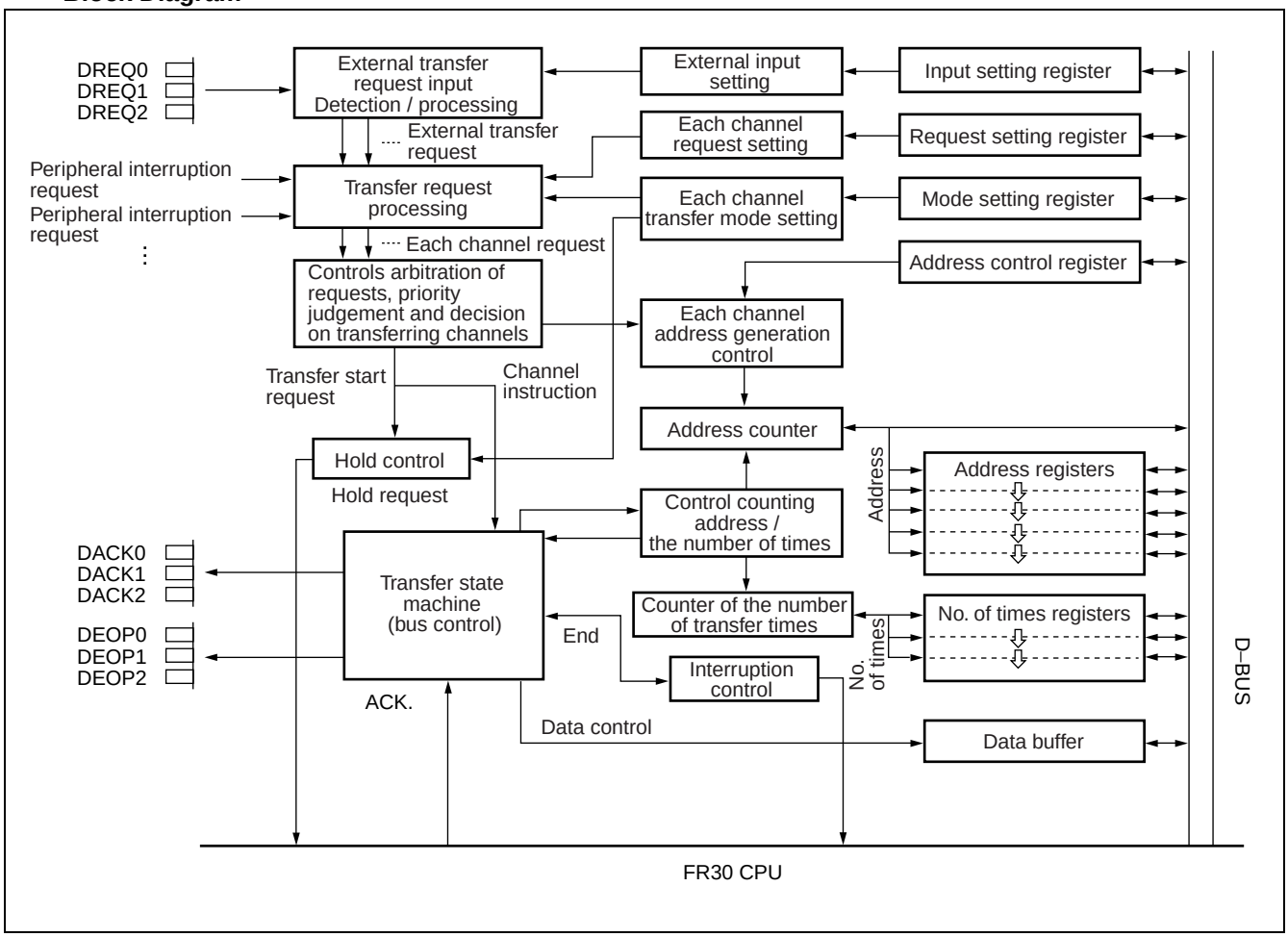
- Internal I/O access control circuit
- 32-bit address counters (possible reload specification : 10)
- 16-bit transfer number counters (possible reload specification : 5)
- External transfer request input pin : DREQ0, DREQ1, DREQ2
- External transfer request reception output pin : DACK0, DACK1, DACK2 (external bus synchronization)
- External transfer termination output pin : DEOP0, DEOP1, DEOP2 (external bus synchronization)

- **Major Function of DMA Controller**

There are the following functions for data transfer using this module.

- Independent data transfer of a number of channels is possible (5 ch)
- Priority ranking amongst channels
  Fixed ranking (ch.0 > ch.1 > ch.2 > ch.3 > ch.4)
  Ranking between channel 0 and 1 can be reversed.
- Transfer request
  Dedicated external pin input (Edge detection / level detection selection are possible for channels 0 to 2 only.)
  Built-in peripheral request (interruption requests are shared. External interruption is included.)
  Software request (register writing)
- Transfer sequence
  Consecutive / burst transfer
  Step transfer / block transfer (Maximum 16 words are settable.)
- Addressing mode : 32-bit full address specification (increase / decrease / fix)
- Data types : Byte, half word, word length
- Single shot or reload can be selected.

- **Block Diagram**



- **Register List**

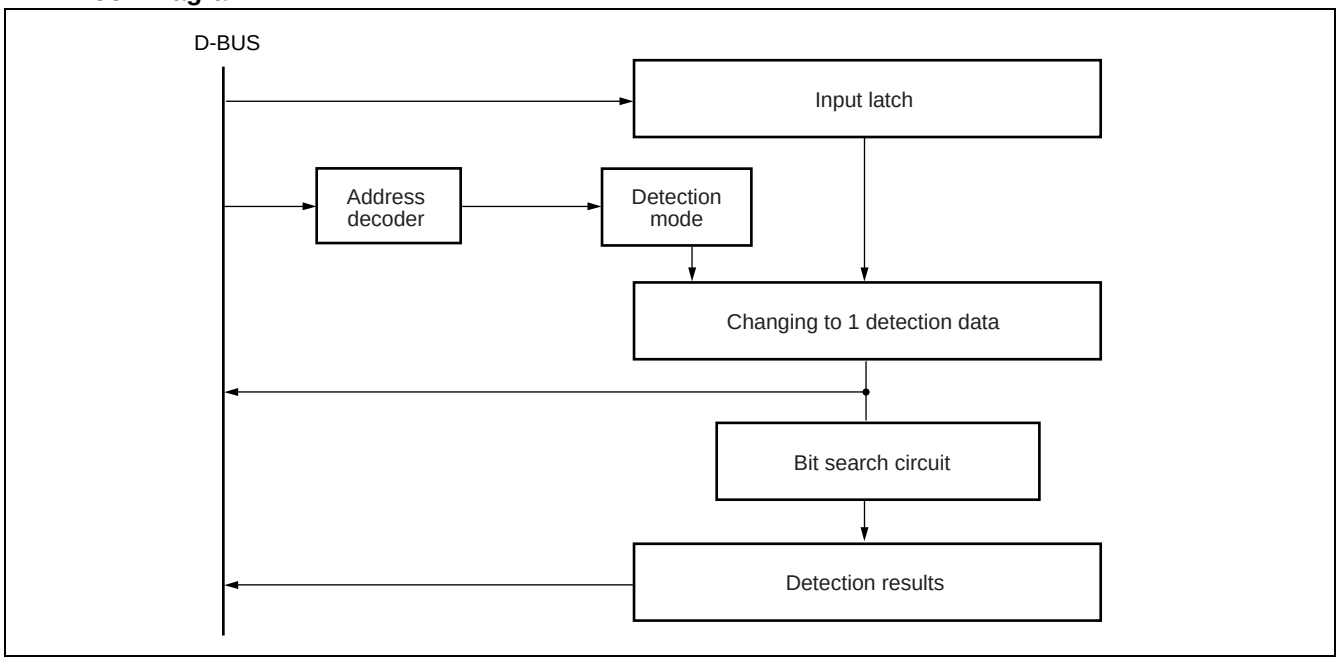
Address	bit 31		0	Initial value	Access
000200H	ch.0	Control/status register	DMACS0	0-00-000000--0000B XX-000000----XX-XB	R/W
000204H	ch.0	Addressing/transfer counting register	DMACC0	----XXXX XXXX-XXXB XXXXXXXX XXXXXXXXB	R/W
000208H	ch.0	Transfer originator address register	DMASA0	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
00020CH	ch.0	Destination address register	DMADA0	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
000210H	ch.1	Control/status register	DMACS1	0-00-000000--0000B XX-000000----XX-XB	R/W
000214H	ch.1	Addressing/transfer counting register	DMACC1	----XXXX XXXX-XXXB XXXXXXXX XXXXXXXXB	R/W
000218H	ch.1	Transfer originator address register	DMASA1	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
00021CH	ch.1	Destination address register	DMADA1	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
000220H	ch.2	Control/status register	DMACS2	0-00-000000--0000B XX-000000----XX-XB	R/W
000224H	ch.2	Addressing/transfer counting register	DMACC2	----XXXX XXXX-XXXB XXXXXXXX XXXXXXXXB	R/W
000228H	ch.2	Transfer originator address register	DMASA2	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
00022CH	ch.2	Destination address register	DMADA2	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
000230H	ch.3	Control/status register	DMACS3	0-00-000000--0000B XX-000000----XX-XB	R/W
000234H	ch.3	Addressing/transfer counting register	DMACC3	----XXXX XXXX-XXXB XXXXXXXX XXXXXXXXB	R/W
000238H	ch.3	Transfer originator address register	DMASA3	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
00023CH	ch.3	Destination address register	DMADA3	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
000240H	ch.4	Control/status register	DMACS4	0-00-000000--0000B XX-000000----XX-XB	R/W
000244H	ch.4	Addressing/transfer counting register	DMACC4	----XXXX XXXX-XXXB XXXXXXXX XXXXXXXXB	R/W
000248H	ch.4	Transfer originator address register	DMASA4	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
00024CH	ch.4	Destination address register	DMADA4	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
000250H		Overall control register	DMACR	----------B 00----------0B	R/W

*: Shaded areas indicate where nothing exists.

17. Bit Search Module

Bit search module searches for 0, 1 or change points on data that has been written in the input register, and returns the detected bit position.

- **Block Diagram**



- **Registers List**

Address	31 — 0	Initial value	Access
0003F0H	Data register for 0 detection(BSD0)	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	W
0003F4H	Data register for 1 detection(BSD1)	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R/W
0003F8H	Data Register for Change Point Detection(BSDC)	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	W
0003FCH	Detection Results Register(BSRR)	XXXXXXXX XXXXXXXXB XXXXXXXX XXXXXXXXB	R

18. I-RAM

This type has 16 KB of built-in I-RAM. Efficient processing becomes possible by pre-arranging interruption processing programs and such like in this area. Writing on I-RAM is possible via the data bus and is available as RAM for data.

- **Register List**

IRMC
Address : 0003EFH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	—	—	—	IRMD	- - - - - - - 0	R/W

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = AVRL = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power voltage	$V_{CC}5$	$V_{CC}3$ – 0.3	V_{SS} + 6.0	V	*1
	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 3.6	V	*1
Analog power voltage	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6	V	*2
Standard analog voltage	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 3.6	V	*2
Input voltage	V_I	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Maximum “L” level output current	I_{OL}	—	10	mA	*3
Average “L” level output current	I_{OLAV}	—	4	mA	*4
Maximum total “L” level output current	ΣI_{OL}	—	100	mA	
Average “L” level total output current	ΣI_{OLAV}	—	50	mA	*5
Maximum “H” level output current	I_{OH}	—	–10	mA	*3
Average “H” level output current	I_{OHAV}	—	–4	mA	*4
Maximum total “H” level output current	ΣI_{OH}	—	–50	mA	
Average “H” level total output current	ΣI_{OHAV}	—	–20	mA	*5
Electricity consumption	P_D	—	650	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : $V_{CC}3$/$V_{CC}5$ must not be lower than V_{SS} – 0.3 V.

*2 : Care must be taken that AV_{CC}, AVRH and AVRL do not exceed V_{CC} + 0.3 V when the power is turned on. Also care must be taken that AVRH and AVRL do not exceed AV_{CC}, and keep AVRH ≥ AVRL.

*3 : Peak value of the pin concerned is regulated as the maximum output current.

*4 : Average current within 100 ms flowing in the pin concerned is regulated as the average output current.

*5 : Average current within 100 ms flowing in all pins concerned is regulated as the average total output current.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = AVRL = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power voltage	$V_{CC}5$	4.5	5.5	V	Keeping RAM status in the case of normal operations / stopping
	$V_{CC}3$	3.135	3.465		
Analog power voltage	AV_{CC}	V_{SS} – 3.0	V_{SS} + 3.465	V	
Standard analog voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Input excluding following	—	0.65 × $V_{CC}3$	—	$V_{CC}5$ + 0.3	V	
	V_{IHS}	Refer to *	—	0.8 × $V_{CC}3$	—	$V_{CC}5$ + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	Input excluding following	—	V_{SS} – 0.3	—	0.25 × $V_{CC}3$	V	
	V_{ILS}	Refer to *	—	V_{SS} – 0.3	—	0.2 × $V_{CC}3$	V	Hysteresis input
"H" level output voltage	V_{OH}	—	$V_{CC}5$ = 4.5 V I_{OH} = –4.0 mA	$V_{CC}5$ – 0.5	—	—	V	
"L" level output voltage	V_{OL}	—	$V_{CC}5$ = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	—	$V_{CC}5$ = 5.5 V 0.45 V < V_I < $V_{CC}5$	–5	—	+5	µA	
Pull-up resistance value	R_{PULL}	$\overline{RST}$	$V_{CC}5$ = 5.5 V V_I = 0.45 V	25	50	200	kΩ	
Power current	I_{CC}	$V_{CC}5$	f_C = 12.5 MHz $V_{CC}5$ = 5.5 V $V_{CC}3$ = 3.465 V	—	50	70	mA	(4 times) in case of 50 MHz operation
		$V_{CC}3$		—	100	150	mA	
	I_{CCS}	$V_{CC}5$	f_C = 12.5 MHz $V_{CC}5$ = 5.5 V $V_{CC}3$ = 3.465 V	—	20	30	mA	In case of sleeping
		$V_{CC}3$		—	50	70	mA	
	I_{CCH}	$V_{CC}5$	T_A = 25 °C $V_{CC}5$ = 5.5 V $V_{CC}3$ = 3.465 V	—	10	20	µA	In case of stopping
		$V_{CC}3$		—	200	900	µA	
Input capacity	C_{IN}	Other than V_{CC}, AV_{CC}, AV_{SS} and V_{SS}	—	—	10	—	pF	

* : Hysteresis input pins : $\overline{RST}$, $\overline{HST}$, $\overline{NMI}$, PE0/$\overline{ATG}$, PE1/TRG0, 3, PE2/TRG1, 4, PE3/TRG2, 5, PF0/INT0 to PF7/INT7, PG0/$\overline{DREQ0}$, PG3/$\overline{DREQ1}$, PH0/$\overline{DREQ2}$, PH3/SI, PH5/SCK, PH6/TI0, PI0/TI1, $\overline{BGRNT}$/P81, $\overline{WR1}$/P85, $\overline{CS1}$/PA0 to CLK/PA6, RAS0/PB0 to $\overline{DW1}$/PB7

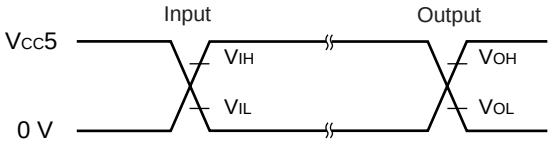
4. AC Characteristics

Measurement Conditions

The following conditions are applied to items without particular specifications.

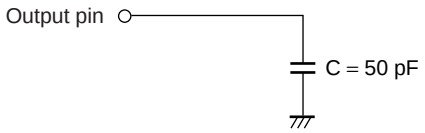
- Alternating current standard measurement condition

  $V_{CC}5$: 5.0 V ± 10%



V_{IH}	2.4 V	V_{OH}	2.4 V
V_{IL}	0.8 V	V_{OL}	0.8 V

- Load condition



(1) Clock Timing

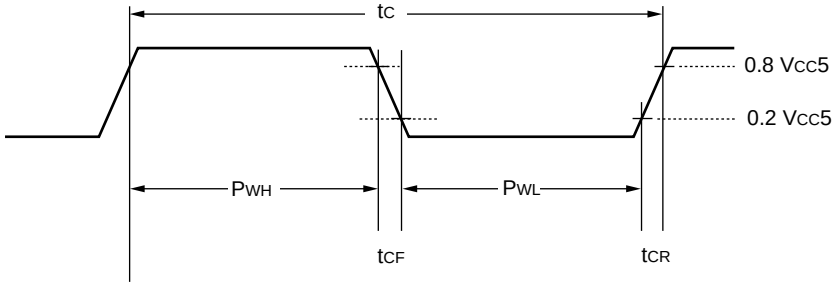
($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock frequency (1)	f_C	X0 X1	—	10.0	12.5	MHz	Self oscillation 12.5 MHz Internal 50 MHz operation (via PLL, 4 times)
Clock cycle time	t_C	X0 X1		80	100	ns	
Clock frequency (2)	f_C	X0 X1	—	10	25	MHz	Self oscillation (1/2 cycle input)
Clock frequency (3)	f_C	X0 X1		10	25	MHz	External clock (1/2 cycle input)
Clock cycle time	t_C	X0 X1		40	100	ns	
Input clock pulse width	P_{WH} P_{WL}	X0 X1		10	—	ns	Clock is input to X0/X1
	P_{WH}	X0		25	—	ns	Clock is input to X0 only
Input clock rising/falling time	t_{CR} t_{CF}	X0 X1	—	—	8	ns	(t_{CR} + t_{CF})
Internal operation clock frequency	f_{CP}		—	0.625*1	50	MHz	CPU system
	f_{CPB}			0.625*1	25*2		Bus system
	f_{CPP}			0.625*1	25		Peripheral system
Internal operation clock cycle time	t_{CP}			20	1600*1	ns	CPU system
	t_{CPB}			40*2	1600*1		Bus system
	t_{CPP}			40	1600*1		Peripheral system

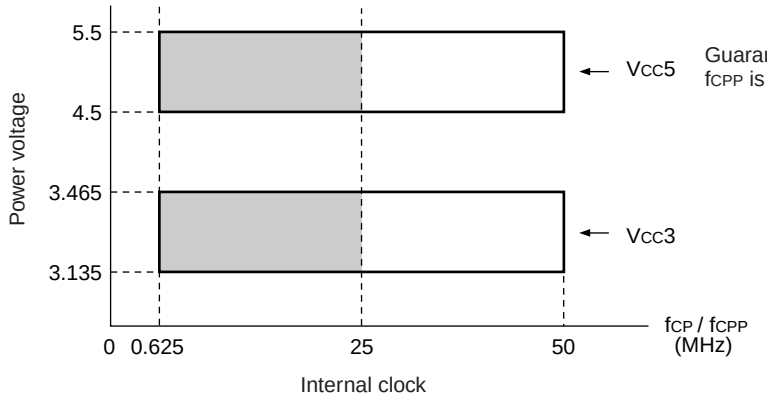
*1 : This is the value when 10 MHz, which is the minimum value of the clock frequency, is input to X0 and 1/2 cycle of the oscillation circuit and gearing of 1/8 are used.

*2 : This is the value when doubler is used with a 50 MHz CPU.

- Clock timing standard measurement conditions

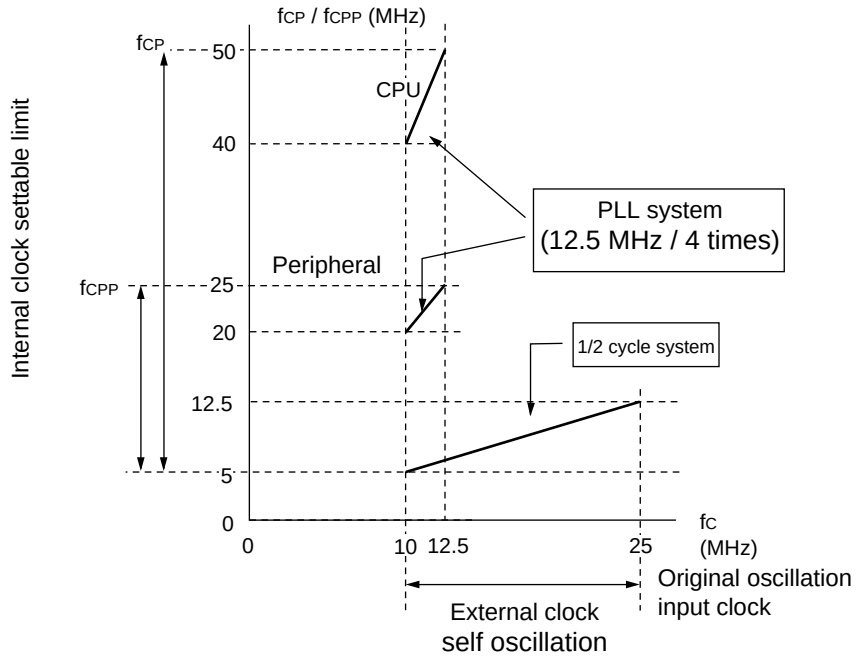


- Guaranteed operating area



Guaranteed operating area (T_A = 0 ~ +70 °C)
f_{CPP} is the shaded area.

- External/internal clock settable area

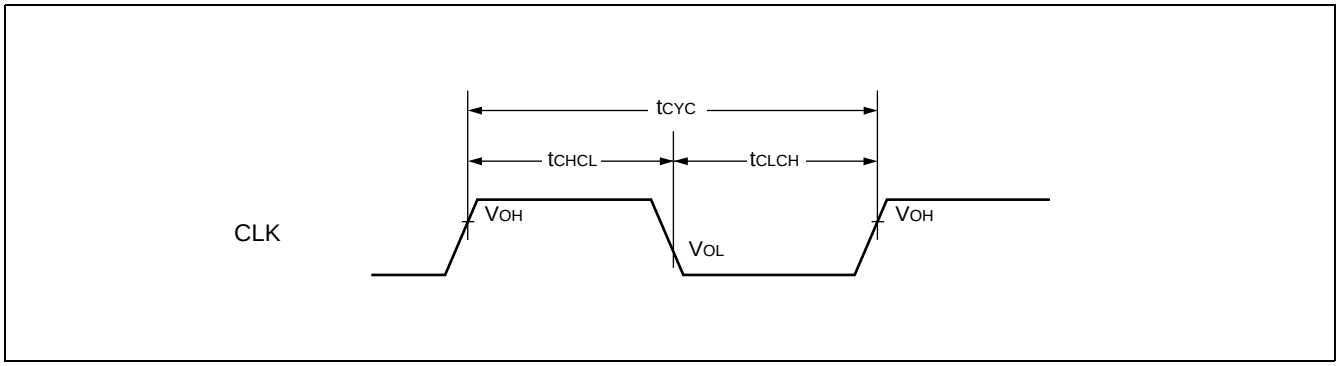


Notes: • 10.0 MHz to 12.5 MHz must be input for external clock input when PLL is used.
• PLL oscillation stabilization time should be larger than 100 µs.
• Internal clock gear should be set within the above range.

(2) Clock Output Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
				$2 \times t_{CP}$	—		In case of using doubler
CLK ↑ → CLK ↓	t_{CHCL}	CLK		$1 / 2 \times t_{CYC} - 10$	$1 / 2 \times t_{CYC} + 10$	ns	*2
CLK ↓ → CLK ↑	t_{CLCH}	CLK		$1 / 2 \times t_{CYC} - 10$	$1 / 2 \times t_{CYC} + 10$	ns	*3



*1 : t_{CYC} is frequency of 1 clock cycle including the gear cycle.

*2 : This standard value is in the case where the gear cycle is 1.
If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.
- Minimum : $(1 - n / 2) \times t_{CYC} - 10$
- Maximum : $(1 - n / 2) \times t_{CYC} + 10$

Gear cycle of 1 should be taken when using a doubler.

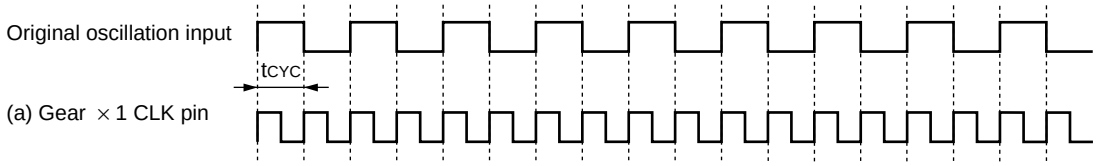
*3 : This standard value is in the case where the gear cycle is 1.
If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.
- Minimum : $n / 2 \times t_{CYC} - 10$
- Maximum : $n / 2 \times t_{CYC} + 10$

Gear cycle of 1 should be taken when using a doubler.

The relationship between the CLK pin set using CHC/CCK1/CCK0 bit of the “Gear Control Register” (GCR) and original oscillation input is as follows. However, original oscillation input indicates “X0 input clock” in this figure.

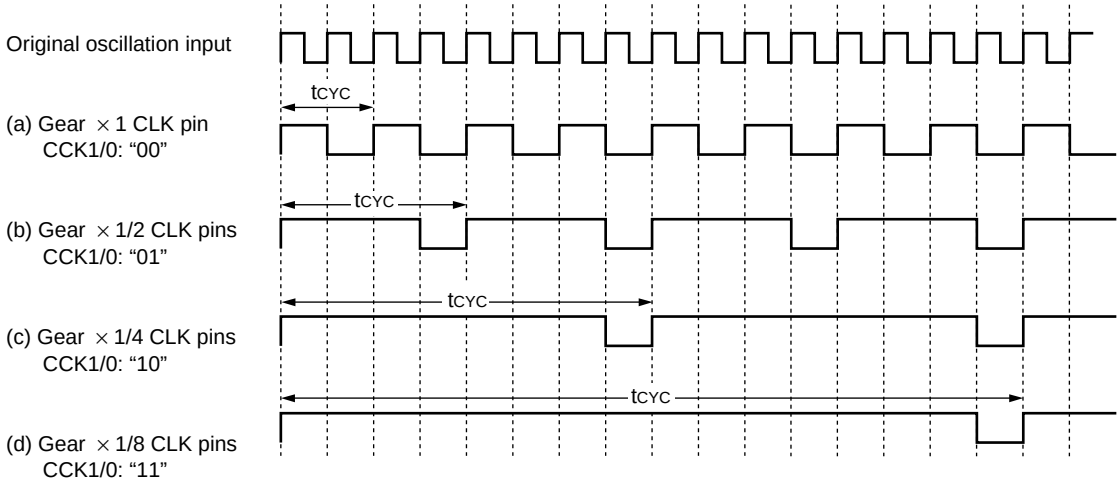
(When using doubler)

- **PLL system** (**CHC bit of GCR** : “**0**”**setting**)



(CCK1/0 : "00" SLCT1, 0 : 01) or (CCK1, 0 : 01 SLCT1, 0 : 1X)

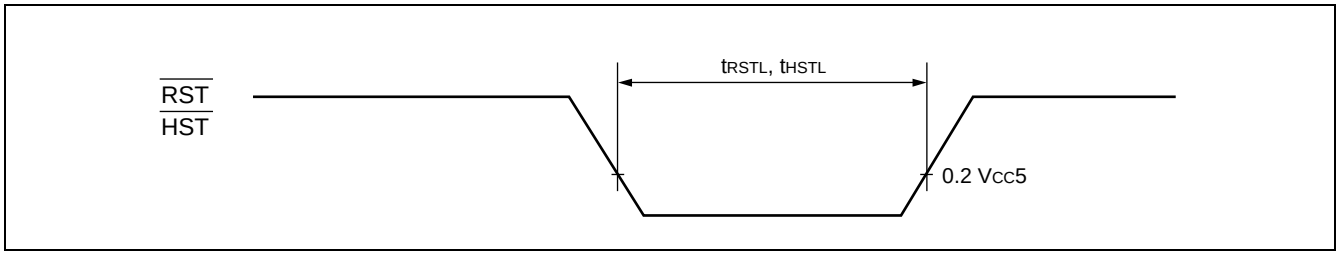
- **2 cycles system** (**CHC bit of GCR** : “**1**”**setting**)



(3) Reset / Hardware Standby Input

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

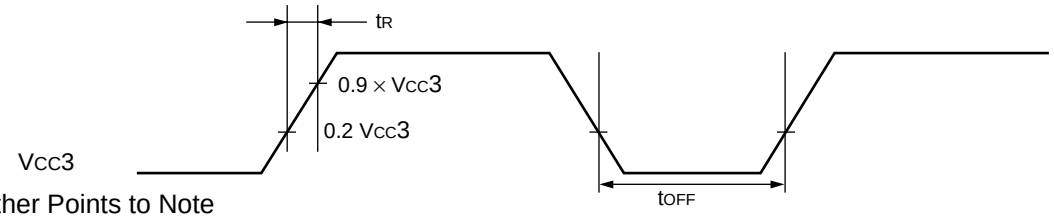
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$	—	$t_{CP} \times 5$	—	ns	



(4) Power On Reset

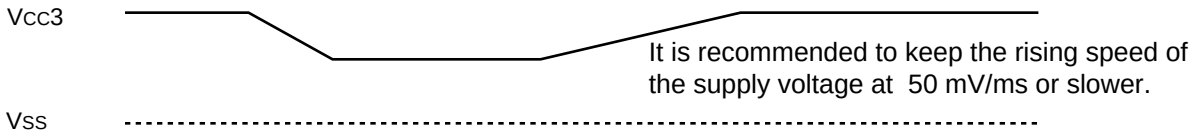
($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power startup time	t_R	$V_{CC}5$	$V_{CC}5$ = 5 V	—	30	ms	V_{CC} is less than 0.2 V before power is turned on.
			$V_{CC}3$ = 3.3 V		18		
Power cut time	t_{OFF}	$V_{CC}3$	—	1	—	ms	Repeated operation

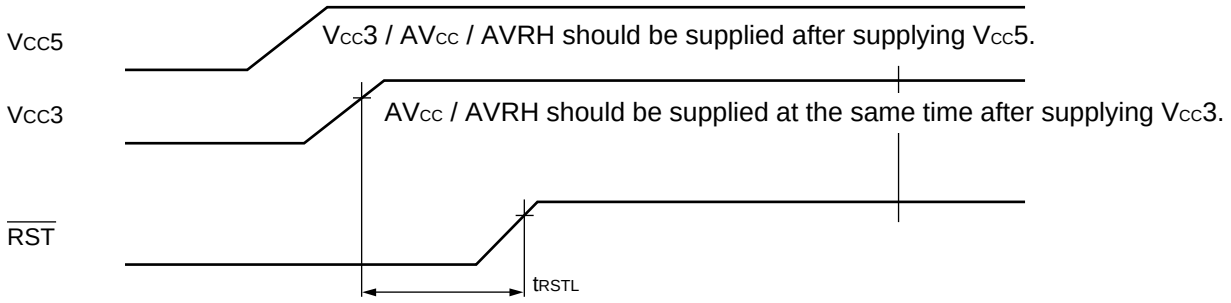


• Other Points to Note

(1) Sudden changes in the power supply voltage may cause a power-on reset .To change the power supply voltage while the device is in operation, it is recommended to rise the voltage smoothly to suppress fluctuations as shown below.



(2) When power is turned on, it must be started while the $\overline{RST}$ pin is set to “L” level, after which wait for t_{RSTL} and change the level to “H” once the Vcc power level is reached.



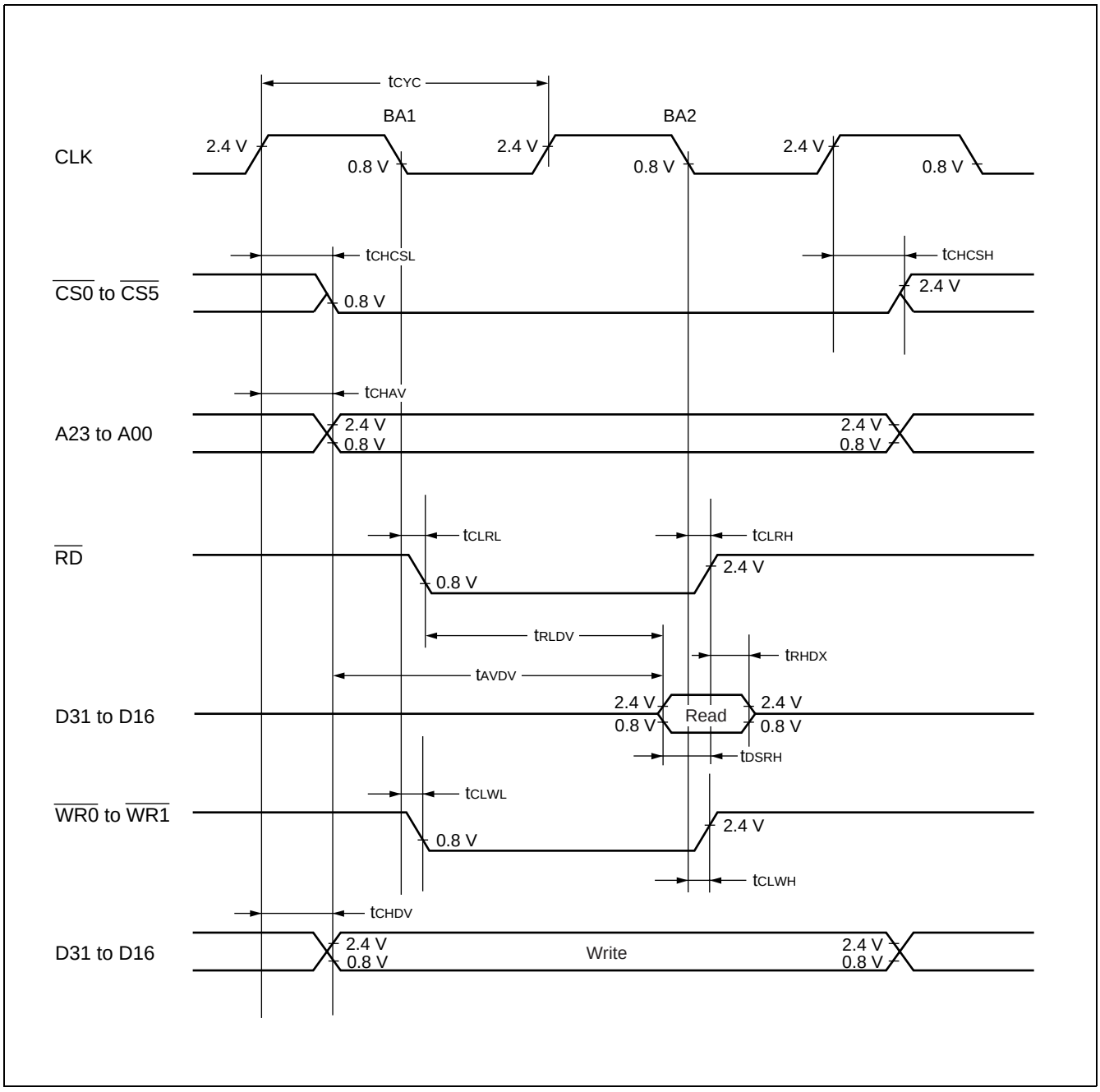
(5) Normal Bus Access Read/Write Operation

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
$\overline{CS0}$ to $\overline{CS5}$ delay time		t_{CHCSL}	CLK $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
$\overline{CS0}$ to $\overline{CS5}$ delay time		t_{CHCSH}			—	15	ns	
Address delay time		t_{CHAV}	CLK A23 to A00		—	15	ns	
Data delay time (write)		t_{CHDV}	CLK D31 to D16		—	15	ns	
$\overline{RD}$ delay time		t_{CLRL}	CLK $\overline{RD}$		—	10	ns	
$\overline{RD}$ delay time		t_{CLRH}			—	10	ns	
$\overline{WR0}$ to $\overline{WR1}$ delay time		t_{CLWL}	CLK $\overline{WR0}$ to $\overline{WR1}$		—	10	ns	
$\overline{WR0}$ to $\overline{WR1}$ delay time		t_{CLWH}			—	10	ns	
Valid address → Valid data input time	Read	t_{AVDV}	A23 to A00 D31 to D16		—	3 / 2 × t_{CYC} – 40	ns	*1 *2
$\overline{RD}$ ↓ → Valid data input time		t_{RLDV}	$\overline{RD}$ D31 to D16		—	t_{CYC} – 25	ns	*1
Data setup → $\overline{RD}$ ↑ time		t_{DSRH}			25	—	ns	
$\overline{RD}$ ↑ → Data holding time		t_{RHDX}			0	—	ns	

*1 : Time (t_{CYC} × number of cycles extended) needs to be added to this standard if the bus is extended by automatic waiting insertion and RDY input.

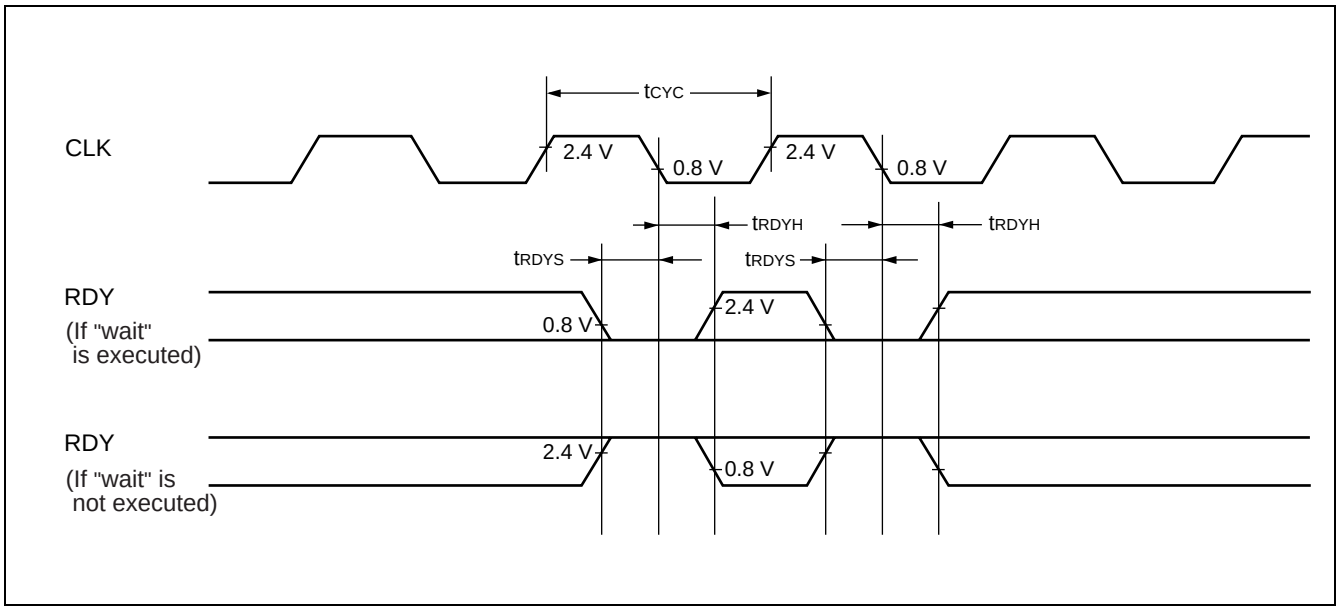
*2 : Values of this standard are in case of gear cycle × 1.
If the gear cycle is set to 1/2, 1/4 or 1/8, calculations should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.
- Calculation formula : (2 – n / 2) × t_{CYC} – 40


tCYC
BA1
BA2
CLK
2.4 V
0.8 V
tCHCSL
tCHCSH
CS0 to CS5
tCHAV
A23 to A00
tCLRL
tCLRH
RD
tRLDV
tRHDX
tAVDV
D31 to D16
Read
tDSRH
tCLWL
tCLWH
WR0 to WR1
tCHDV
Write

(6) Ready Input Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time → CLK ↓	t_{RDYS}	RDY CLK	—	20	—	ns	
CLK ↓ → RDY holding time	t_{RDYH}	RDY CLK		0	—	ns	

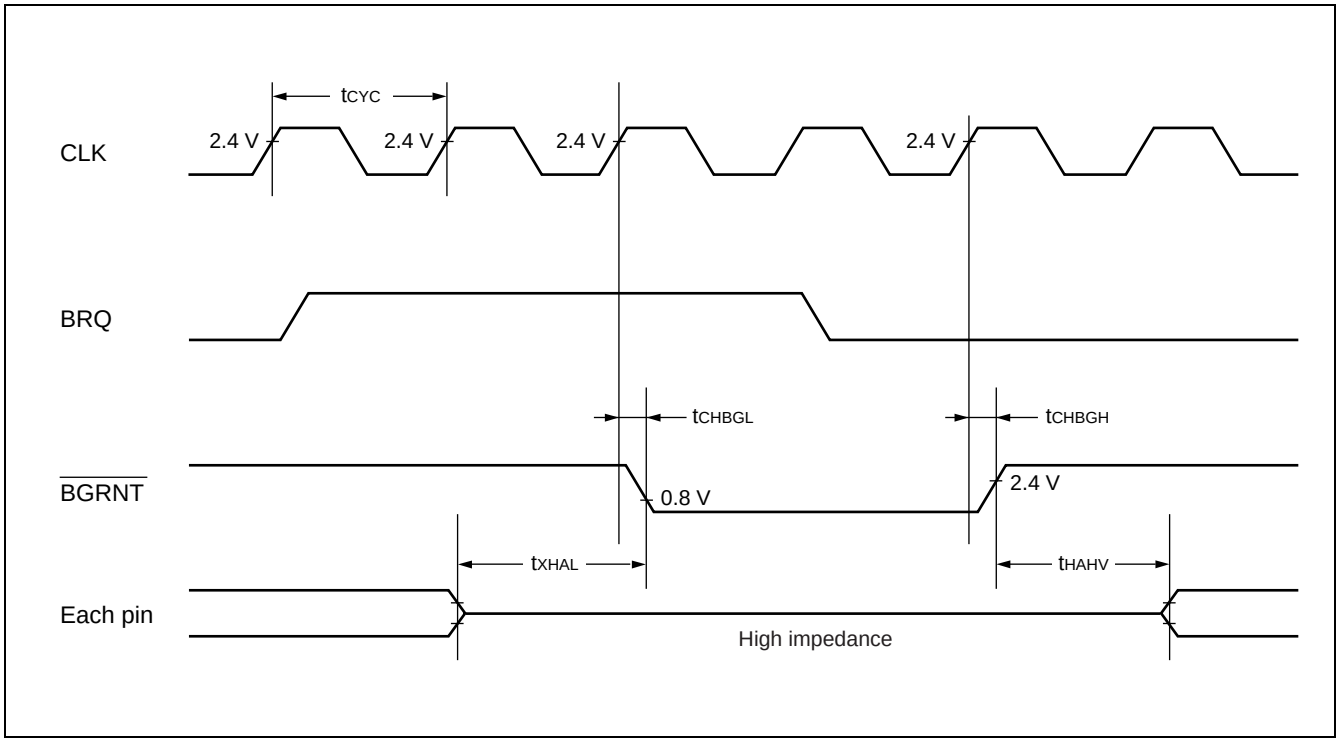


(7) Holding timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{BGRNT}$ delay time	t_{CHBGL}	CLK $\overline{BGRNT}$	—	—	10	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}			—	10	ns	
Pin floating → $\overline{BGRNT}$ ↓ time	t_{XHAL}	$\overline{BGRNT}$		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$ ↑ → Pin valid time	t_{HAHV}			t_{CYC} – 10	t_{CYC} + 10	ns	

Note : It takes at least one cycle from loading the BRQ to when $\overline{BGRNT}$ is changed.



(8) Read/Write Cycle of the Normal DRAM Mode

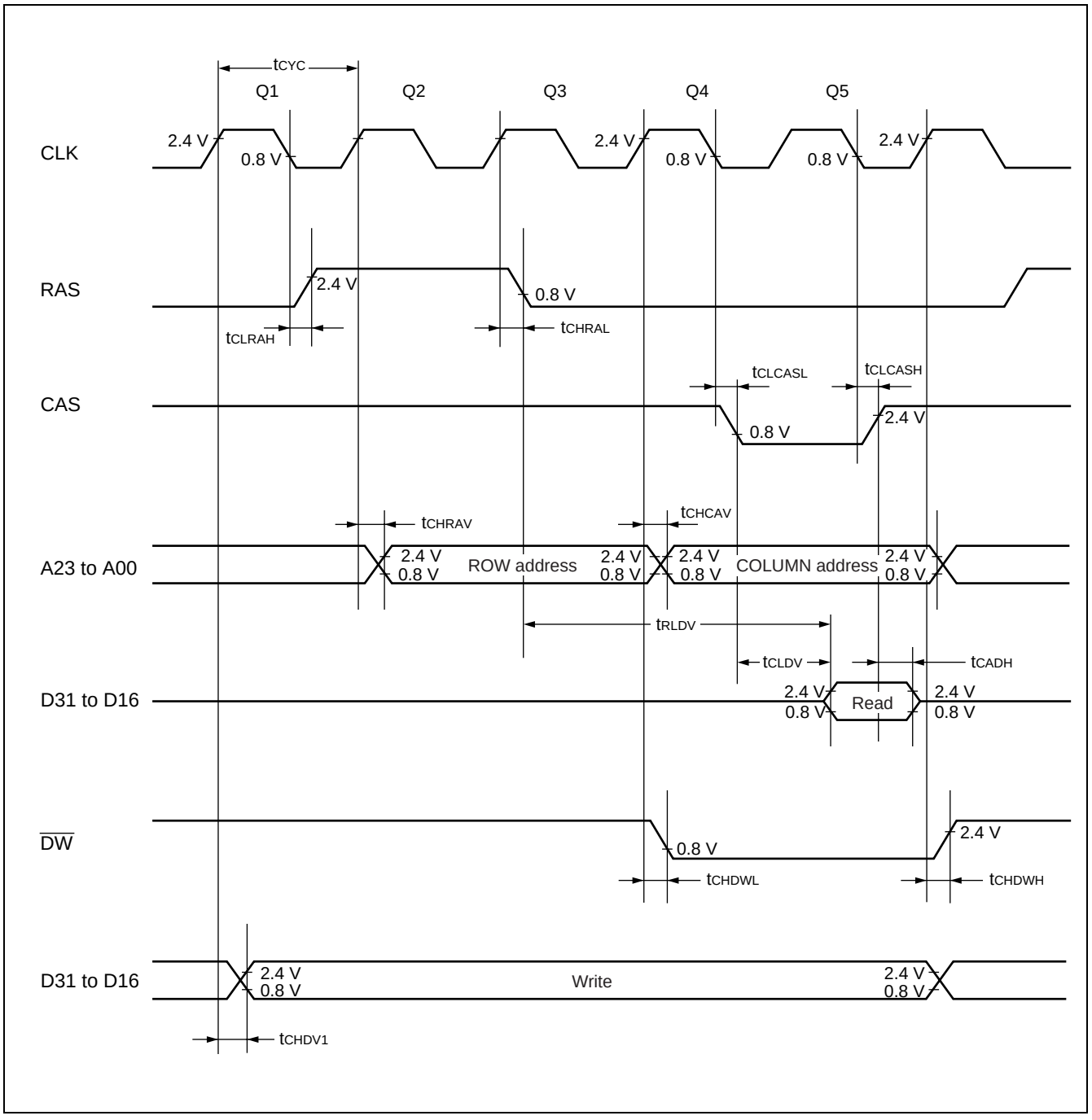
($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	10	ns	
RAS delay time	t_{CHRAL}			—	10	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	10	ns	
CAS delay time	t_{CLCASH}			—	10	ns	
ROW address delay time	t_{CHRAV}	CLK A23 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}			—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL}	CLK $\overline{DW}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH}			—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
RAS ↓ → valid data input time	t_{RLDV}	RAS D31 to D16		—	5 / 2 × t_{CYC} – 20	ns	*1 *2
CAS ↓ → valid data input time	t_{CLDV}	CAS D31 to D16		—	t_{CYC} – 17	ns	*1
CAS ↑ → data holding time	t_{CADH}			0	—	ns	

*1 : If either the Q1 or A4 cycle is extended for one cycle, the t_{CYC} time needs to be added to this standard.

*2 : Values of this standard are in case of gear cycle × 1.
If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.

- Calculation formula : $(3 - n / 2) \times t_{CYC} - 20$

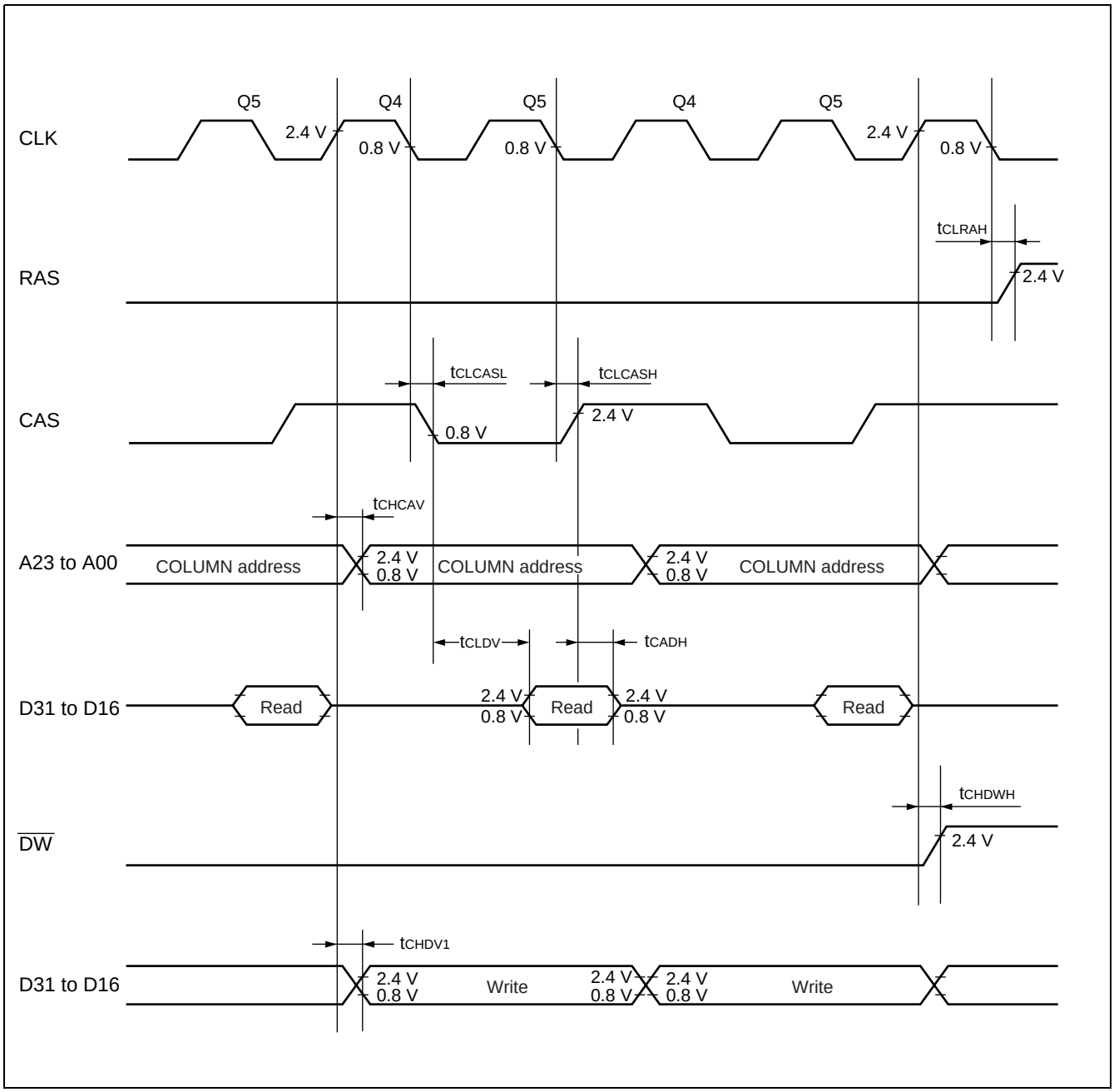

tCYC
Q1
Q2
Q3
Q4
Q5
CLK
2.4 V
0.8 V
RAS
tCLRAH
tCHRAL
CAS
tCLCASL
tCLCASH
A23 to A00
tCHRAV
tCHCAV
ROW address
COLUMN address
tRLDV
tCLDV
tCADH
D31 to D16
Read
DW
tCHDWL
tCHDWH
Write
tCHDV1

(9) High Speed Page Read/Write Cycle of the Normal DRAM Mode

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	10	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	10	ns	
CAS delay time	t_{CLCASH}			—	10	ns	
COLUMN address delay time	t_{CHCAV}	CLK A23 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH}	CLK, $\overline{DW}$		—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
CAS ↓ → valid data input time	t_{CLDV}	CAS D31 to D16		—	t_{CYC} – 17	ns	*
CAS ↑ → data holding time	t_{CADH}			0	—	ns	

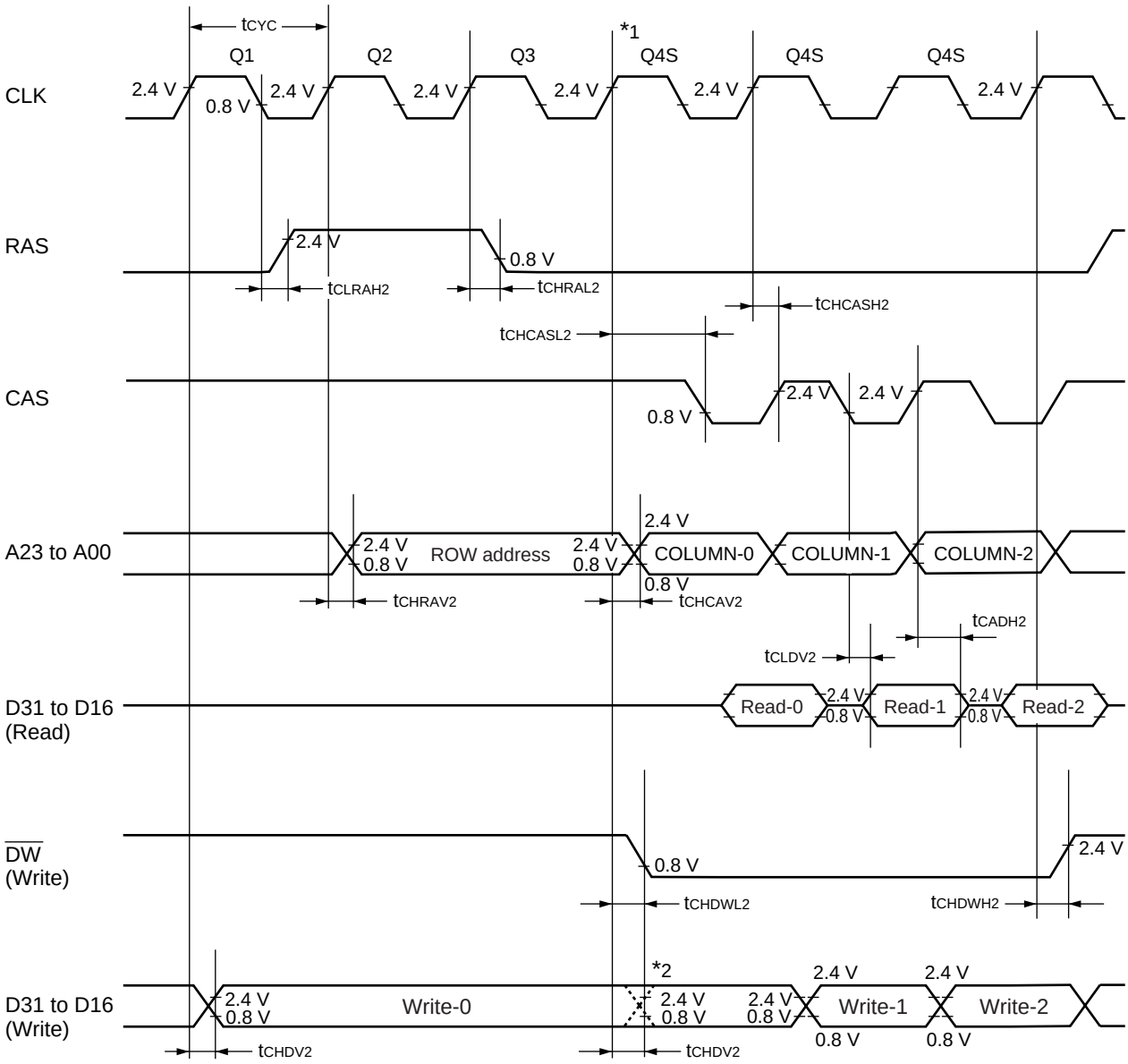
* : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.


Q5
Q4
Q5
Q4
Q5
CLK
2.4 V
0.8 V
0.8 V
2.4 V
0.8 V
tCLRAH
RAS
2.4 V
tCLCASL
tCLCASH
CAS
0.8 V
2.4 V
tCHCAV
A23 to A00
COLUMN address
2.4 V
0.8 V
COLUMN address
2.4 V
0.8 V
COLUMN address
tCLDV
tCADH
D31 to D16
Read
2.4 V
0.8 V
Read
2.4 V
0.8 V
Read
tCHDWH
DW
2.4 V
tCHDV1
D31 to D16
2.4 V
0.8 V
Write
2.4 V
0.8 V
2.4 V
0.8 V
Write

(10) Single DRAM Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH2}	CLK RAS	—	—	10	ns	
RAS delay time	t_{CHRAL2}			—	10	ns	
CAS delay time	$t_{CHCASL2}$	CLK CAS		—	n / 2 × t_{CYC} + 8	ns	
CAS delay time	$t_{CHCASH2}$			—	10	ns	
ROW address delay time	t_{CHRAV2}	CLK A23 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}			—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL2}	CLK $\overline{DW}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH2}			—	15	ns	
Output data delay time	t_{CHDV2}	CLK D31 to D16		—	15	ns	
CAS ↓ → valid data input time	t_{CLDV2}	CAS D31 to D16		—	(1 – n / 2) × t_{CYC} – 17	ns	
CAS ↑ → data holding time	t_{CADH2}			0	—	ns	

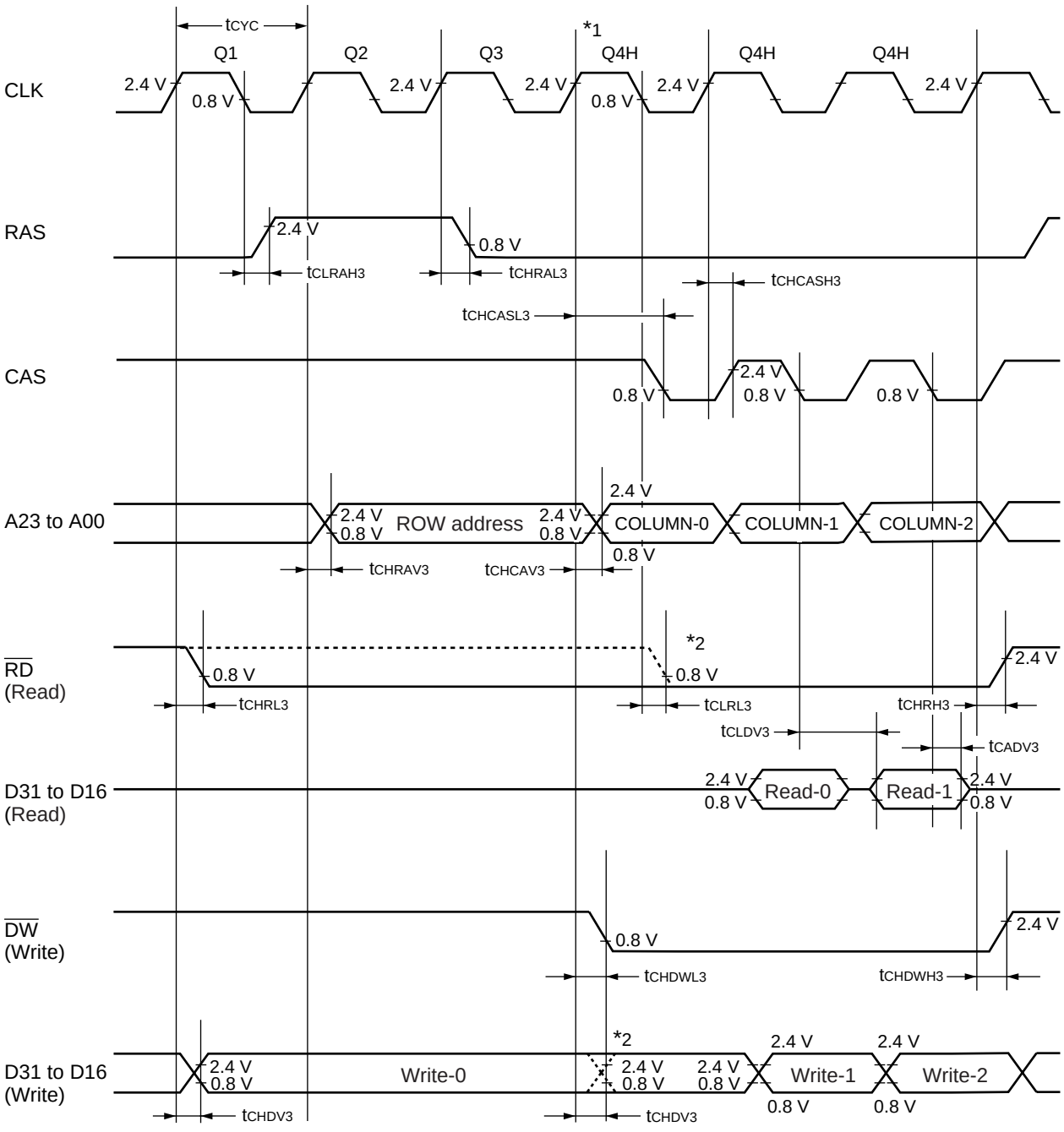


*1 : Q4S cycle indicates the Q4SR (read) or Q4SW (write) cycle of the Single DRAM cycle.
*2 : - - - - - - indicates when a bus cycle is started from the high-speed page mode.

(11) Hyper DRAM Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH3}	CLK RAS	—	—	10	ns	
RAS delay time	t_{CHRAL3}			—	10	ns	
CAS delay time	$t_{CHCASL3}$	CLK CAS		—	n / 2 × t_{CYC} + 8	ns	
CAS delay time	$t_{CHCASH3}$			—	10	ns	
ROW address delay time	t_{CHRAV3}	CLK A23 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}			—	15	ns	
$\overline{RD}$ delay time	t_{CHRL3}	CLK $\overline{RD}$		—	15	ns	
$\overline{RD}$ delay time	t_{CHRH3}			—	15	ns	
$\overline{RD}$ delay time	t_{CLRL3}			—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL3}	CLK $\overline{DW}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH3}			—	15	ns	
Output data delay time	t_{CHDV3}	CLK D31 to D16		—	15	ns	
CAS ↓ → valid data input time	t_{CLDV3}	CAS D31 to D16		—	t_{CYC} – 20	ns	
CAS ↓ → data holding time	t_{CADH3}			0	—	ns	

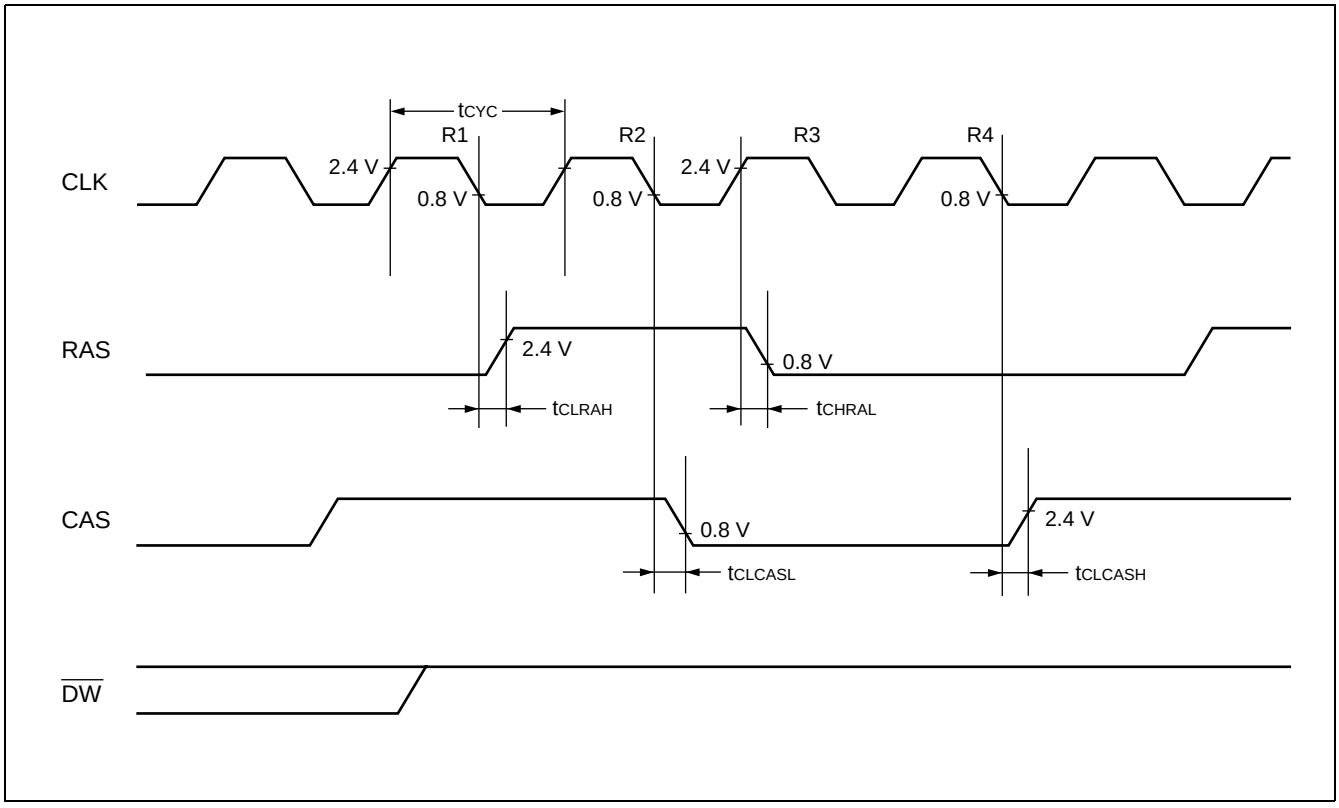


*1 : Q4H cycle indicates the Q4HR (read) or Q4HW (write) cycle of the Hyper DRAM cycle.
*2 : - - - - - - indicates when a bus cycle is started from the high-speed page mode.

(12) CBR Refresh

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

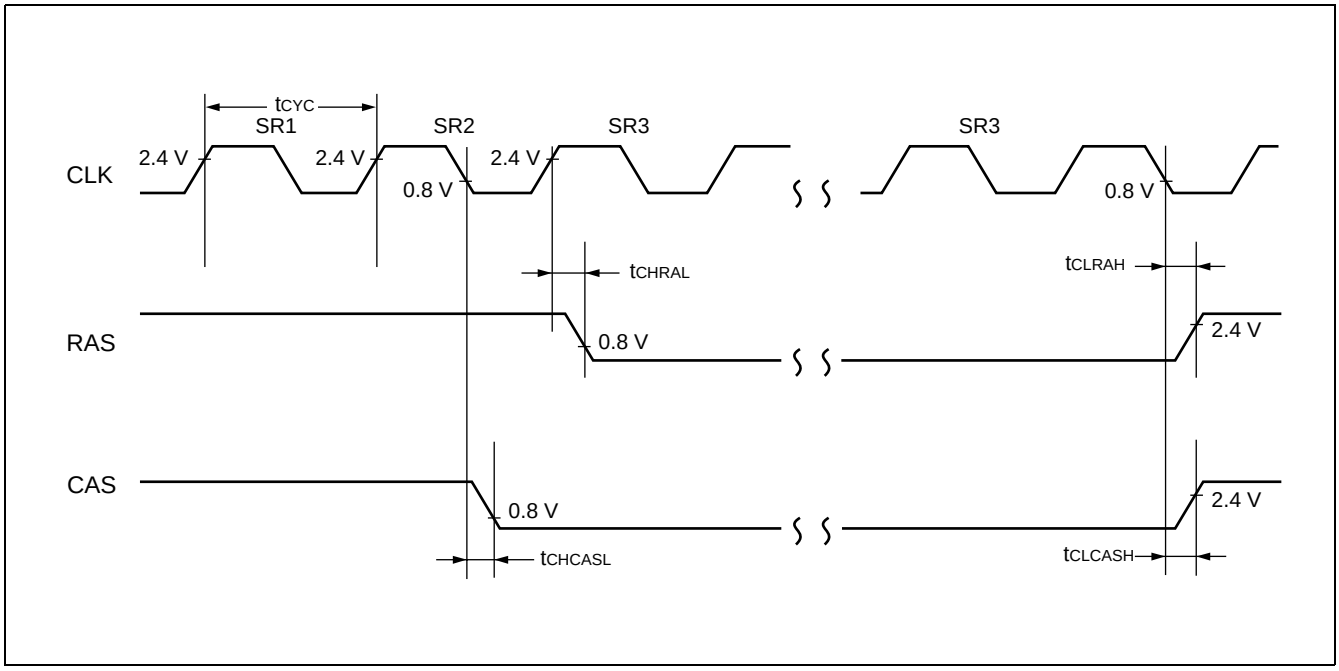
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	10	ns	
RAS delay time	t_{CHRAL}			—	10	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	10	ns	
CAS delay time	t_{CLCASH}			—	10	ns	



(13) Self Refresh

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	10	ns	
RAS delay time	t_{CHRAL}			—	10	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	10	ns	
CAS delay time	t_{CLCASH}			—	10	ns	



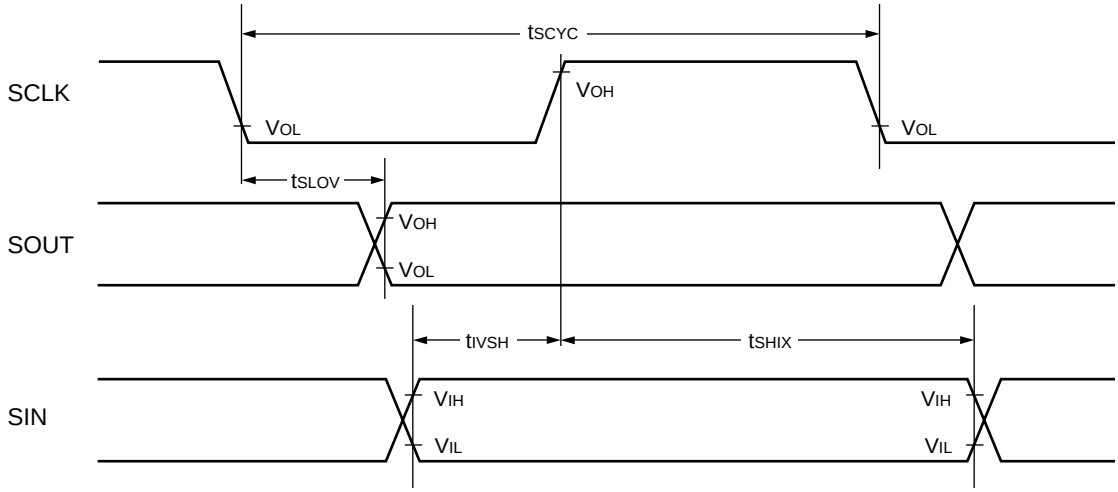
(14) UART Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

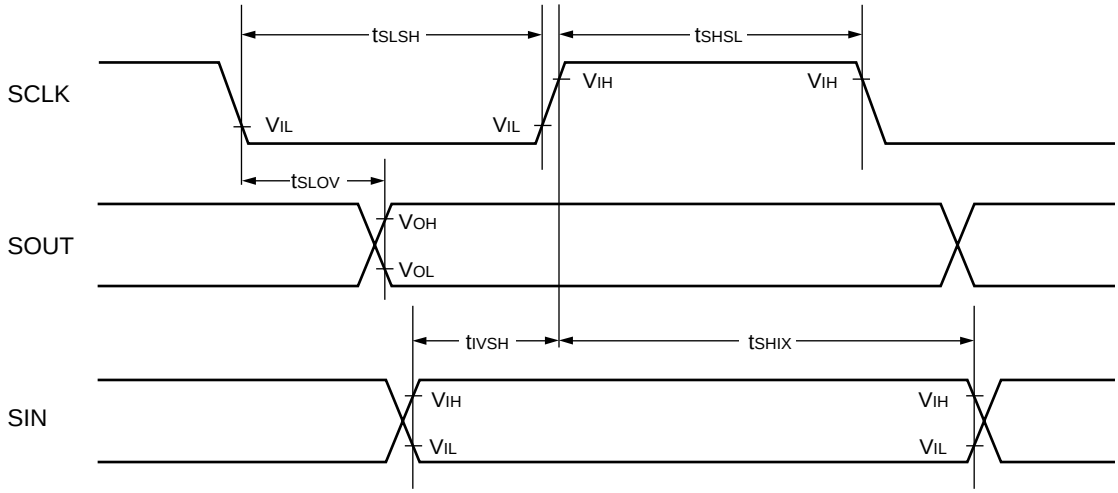
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	8 t_{CYCP}	—	ns	
SCLK ↓ → SOUT Delay time	t_{SLOV}	—		–80	80	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		100	—	ns	
SCLK ↑ → Valid SIN holding lock	t_{SHIX}	—		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode	4 t_{CYCP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CYCP}	—	ns	
SCLK ↓ → SOUT Delay time	t_{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t_{IVSH}	—		60	—	ns	
SCLK ↑ → Valid SIN holding lock	t_{SHIX}	—		60	—	ns	

Notes : • This is the AC standard in the case of CLK synchronous mode.
• t_{CYCP} is the cycle time of the peripheral system clock.

- Internal shift clock mode



- External shift clock mode

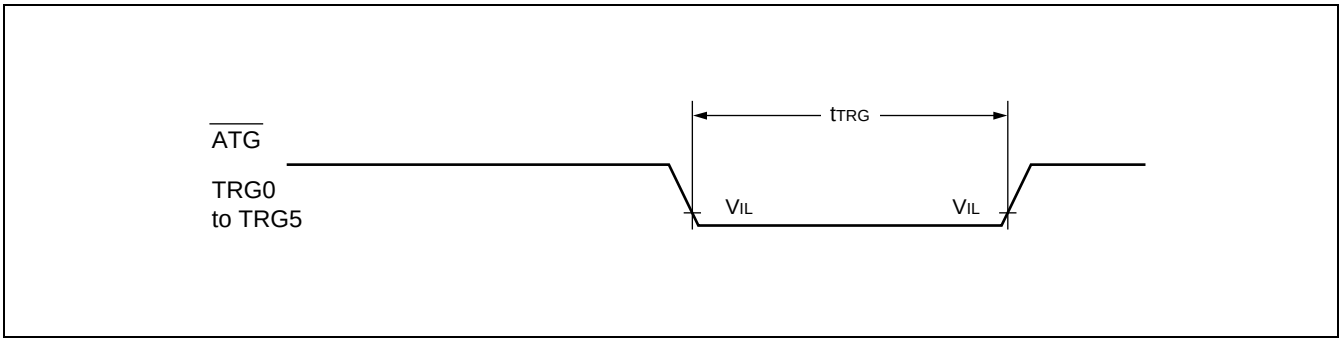


(15) Trigger System Input Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
A/D initiation trigger input time	t_{TRG}	$\overline{ATG}$	—	5 t_{CYCP}	—	ns	
PPG initiation trigger input time		TRG0 to TRG5				ns	

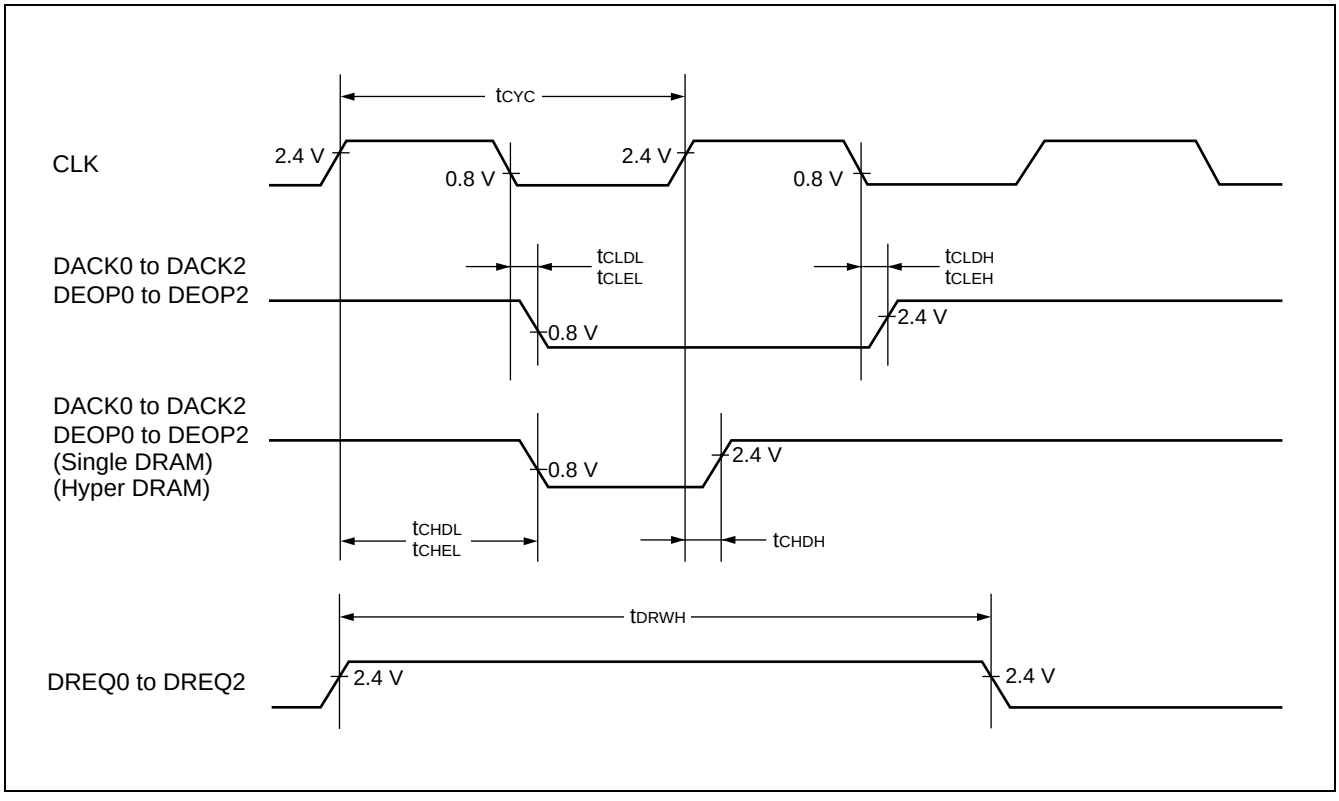
Note : t_{CYCP} is the cycle time of the peripheral system clock.



(16) DMA Controller Timing

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	2 t_{CYC}	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK DACK0 to DACK2		—	6	ns	
	t_{CLDH}			—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK DEOP0 to DEOP2		—	6	ns	
	t_{CLEH}			—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK DACK0 to DACK2		—	n / 2 × t_{CYC}	ns	
	t_{CHDH}			—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK DEOP0 to DEOP2		—	n / 2 × t_{CYC}	ns	
	t_{CHEH}			—	6	ns	



5. A/D Converter Electrical Characteristics

($V_{CC}5$ = 5 V ± 10%, $V_{CC}3$ = AV_{CC} = AVRH = 3.3 V ± 5%, V_{SS} = AV_{SS} = AVRL = 0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	BIT
Conversion error	—	—	—	—	±3.0	LSB
Linearity error	—	—	—	—	±2.5	LSB
Differential linearity error	—	—	—	—	±1.9	LSB
Zero transition error	V_{OT}	AN0 to AN7	–1.5	+0.5	+2.5	LSB
Full-scale transition error	V_{FST}	AN0 to AN7	AVRH – 4.5	AVRH – 1.5	AVRH + 0.5	LSB
Conversion time	—	—	5.6*1	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V
Standard voltage	—	AVRH	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
	I_{AH}		—	—	5*2	µA
Standard voltage current supplied	I_R	AVRH	—	110	—	µA
	I_{RH}		—	—	5*2	µA
Tolerance between channels	—	AN0 to AN7	—	—	4	LSB

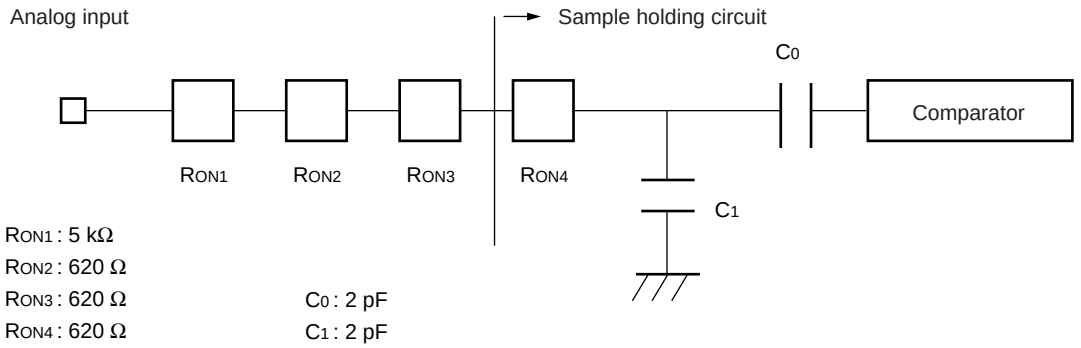
*1 : In case of $V_{CC}3$ = AV_{CC} = 3.3 V ± 5%, machine clock 25 MHz

*2 : This is the current in the case that the A/D converter is not activated and the CPU is stopped (in case of $V_{CC}3$ = A_{VCC} = AVRH = 3.465 V)

Notes : • As the AVRH becomes smaller, the tolerance becomes relatively larger.
• Output impedance of external circuits other than analog input must be used under the following condition.

Output impedance of external circuits < 7 kΩ

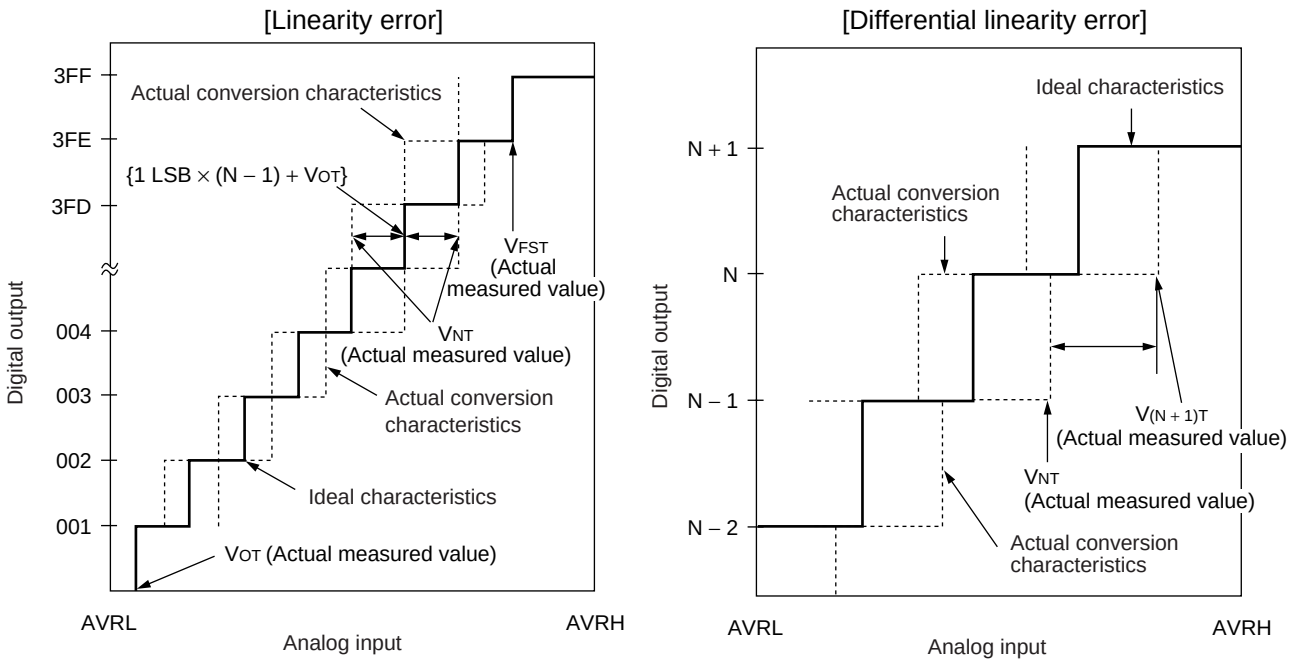
If the output impedance of the external circuits is too high, the sampling time for the analog voltage may be insufficient.



Note : Figures described above should be considered as standard.

Definition of A/D Converter Terms

- Resolution
  Analog changes that can be identified by A/D converter
- Linearity error
  Difference between the straight line linking the zero transition point (00 0000 0000 ←→ 00 0000 0001) to the full-scale transition point (11 1111 1110 ←→ 11 1111 1111) and actual conversion characteristics.
- Differential linearity error
  Difference compared to the ideal input voltage value required to change the output code 1LSB



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

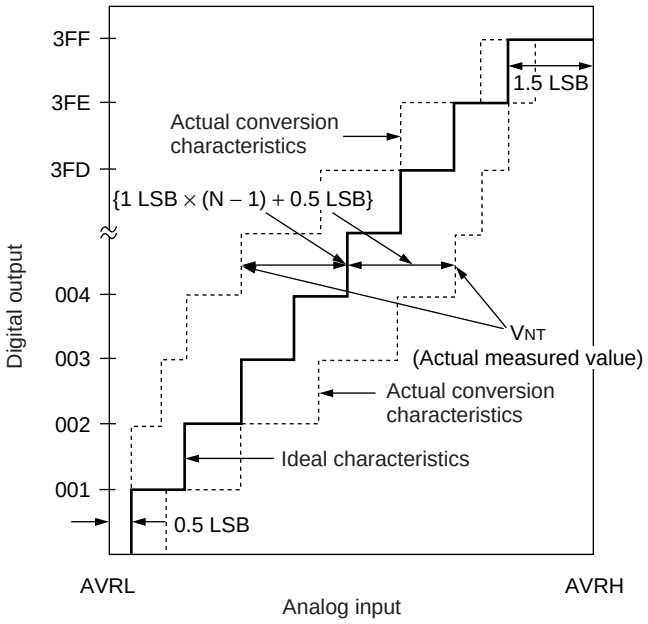
V_{OT} : Voltage with digital output transferred from $(000)_H$ to $(001)_H$

V_{FST} : Voltage with digital output transferred from $(3FE)_H$ to $(3FF)_H$

V_{NT} : Voltage with digital output transferred from $(N - 1)_H$ to N

- Total error
  This indicates the difference between the actual and theoretical values and includes zero transition, full-scale transition and linearity error.

[Total error]



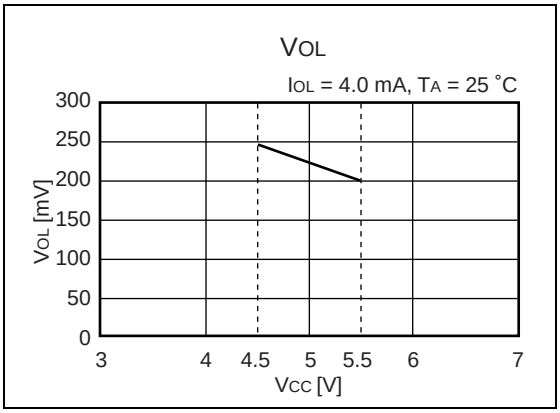
$$\text{Total tolerance of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

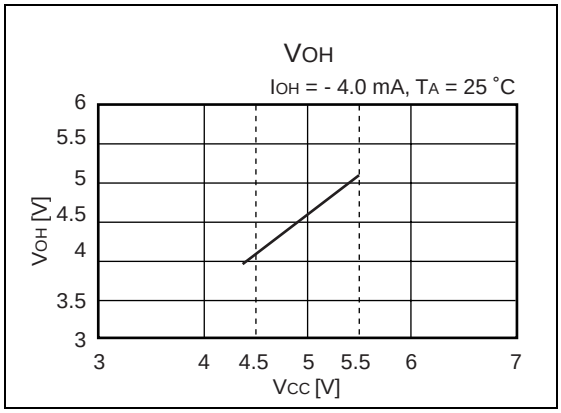
V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

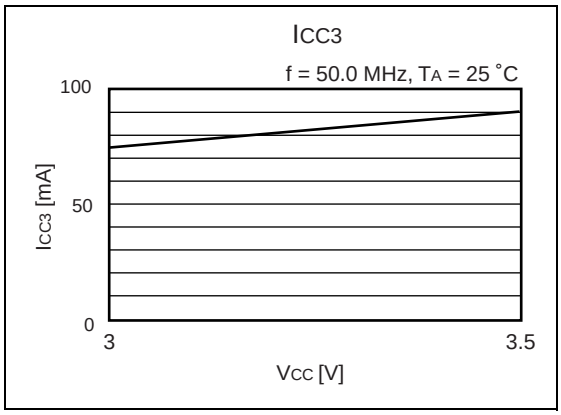
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

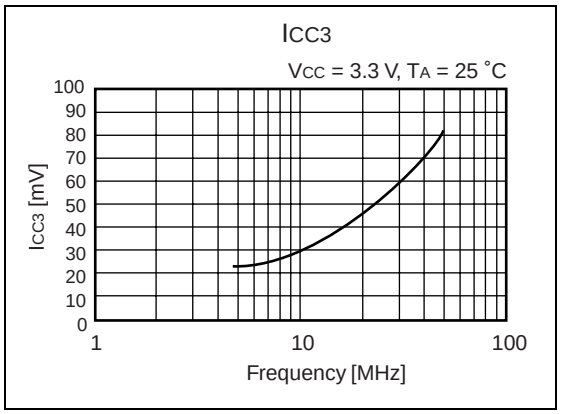
V_{NT} : Voltage with digital output transferred from $(N - 1)_H$ to N

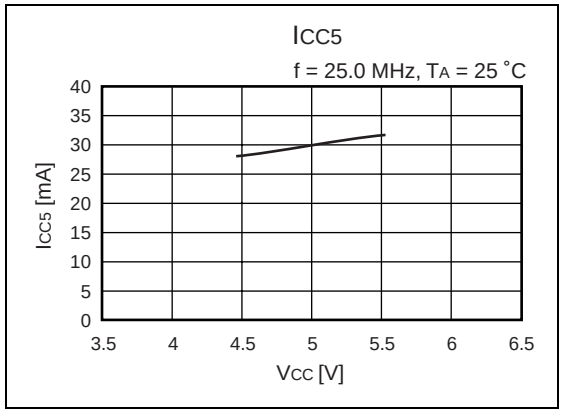
■ EXAMPLE CHARACTERISTICS

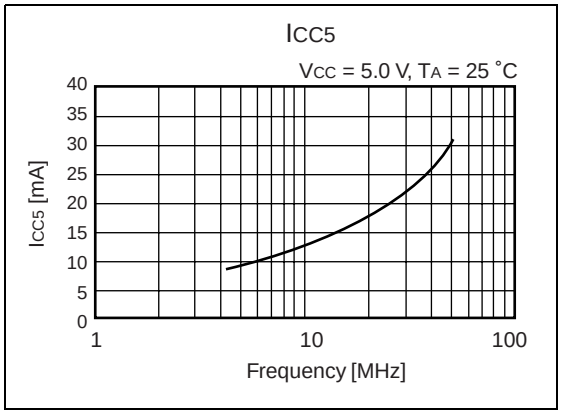


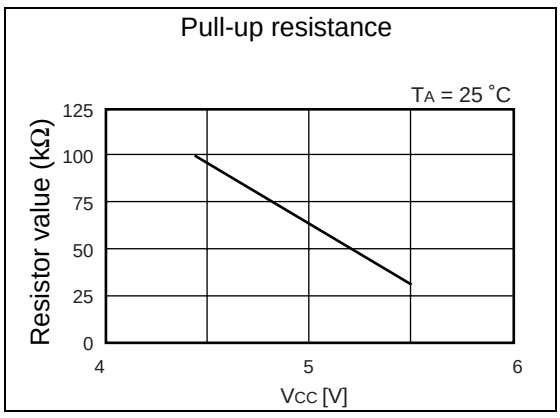




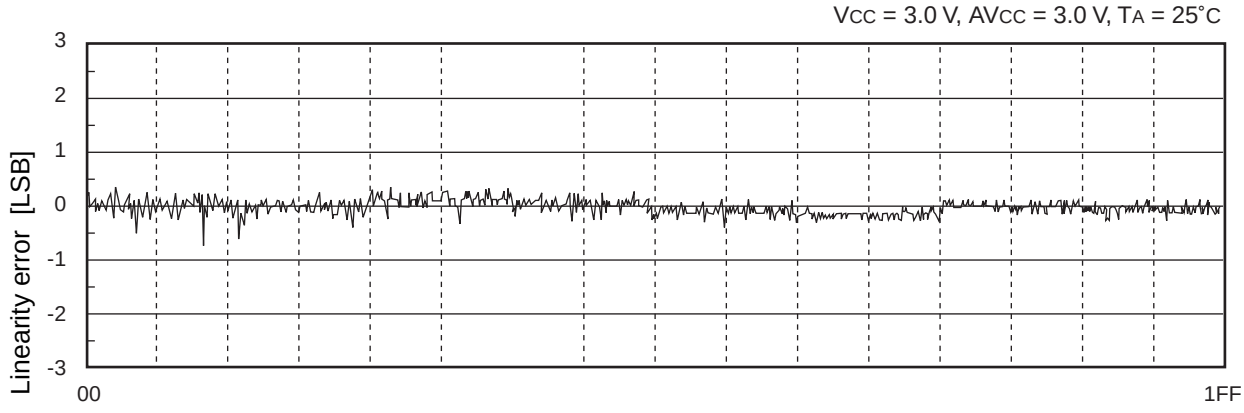




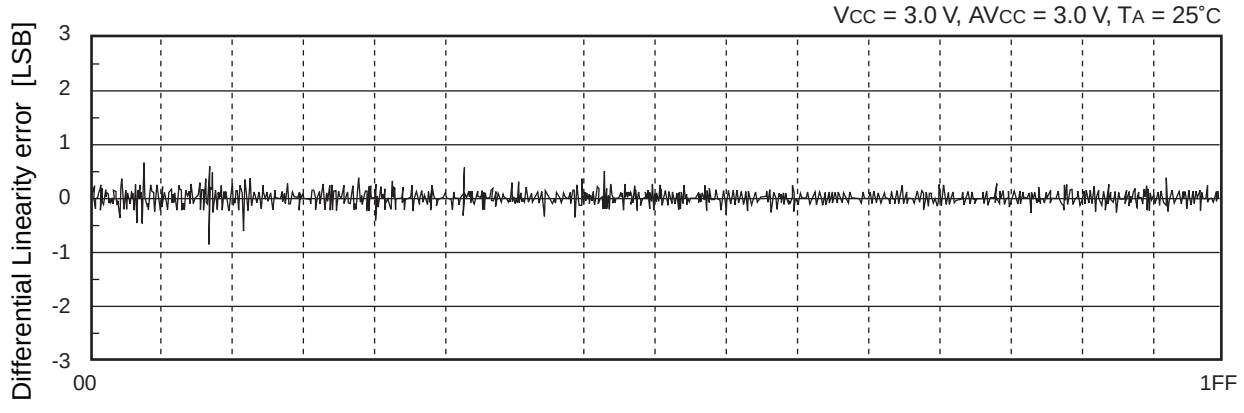




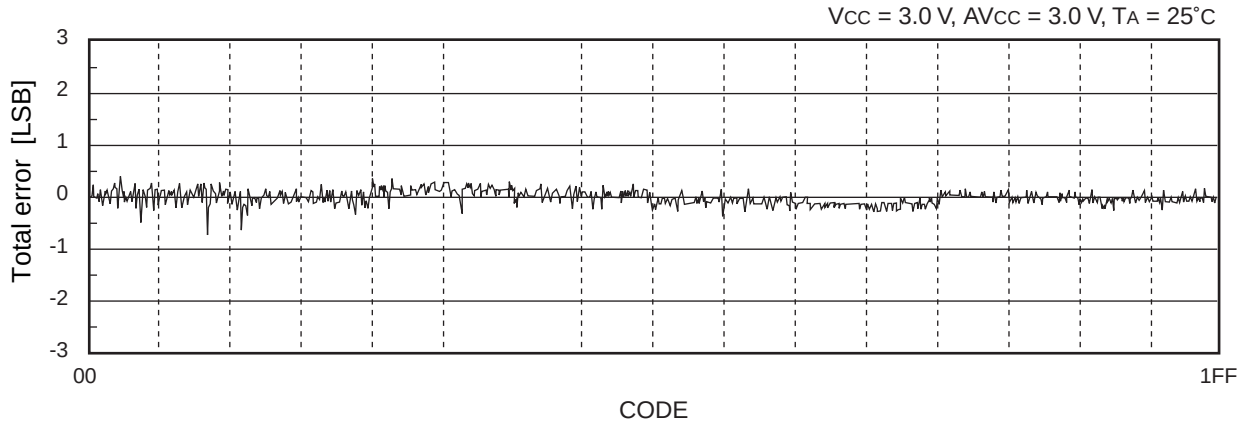
MB91110 Linearity error



MB91110 Differential linearity error



MB91110 Total error

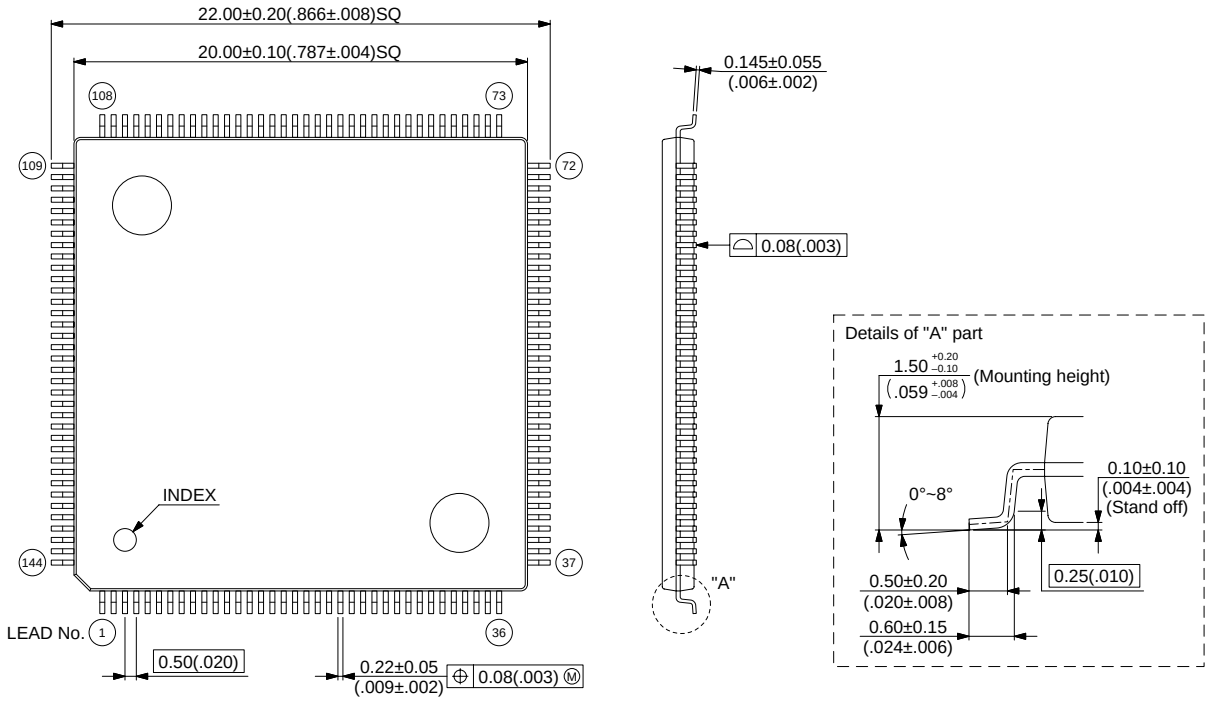


■ ORDERING INFORMATION

Part number	Package	Remarks
MB91110PMT2	144-pin plastic LQFP (FPT-144P-M08)	
MB91V110CR	PGA-299C-A01	

■ PACKAGE DIMENSION

144-pin plastic LQFP
(FPT-144P-M08)



Dimensions in mm (inches) .

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0204