Differential Receiver/Equalizer

The EL9110 is a single channel differential receiver and equalizer. It contains a high speed differential receiver with 5 programmable poles. The outputs of these pole blocks are then summed into an output buffer. The equalization length is set with the voltage on a single pin. The EL9110 also contains a three-statable output, enabling multiple devices to be connected in parallel and used in a multiplexing application.

The gain can be adjusted up or down by 6dB using the V_{GAIN} control signal. In addition, a further 6dB of gain can be switched in to provide a matched drive into a cable.

The EL9110 has a bandwidth of 150MHz and consumes just 33mA on ±5V supply. A single input voltage is used to set the compensation levels for the required length of cable.

The EL9110 is available in the 16-pin QSOP package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL9110IU	16-Pin QSOP	-	MDP0040
EL9110IU-T7	16-Pin QSOP	7”	MDP0040
EL9110IU-T13	16-Pin QSOP	13”	MDP0040

Features

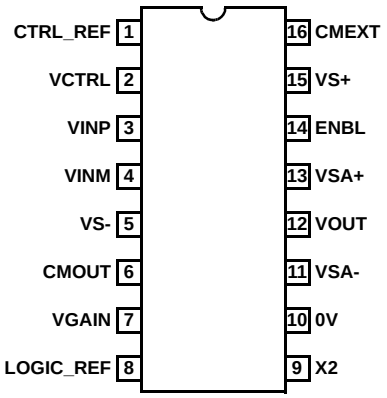
- 150MHz -3dB bandwidth
- CAT-5 compensation
  - 75MHz @ 1000 ft
  - 125MHz @ 500 ft
- 33mA supply current
- Differential input range 3.2V
- Common mode input range ±4.5V
- ±5V supply
- Output to within 1.5V of supplies
- Available in 16-pin QSOP package

Applications

- Twisted-pair receiving/equalizer
- KVM (Keyboard/Video/Mouse)
- VGA over twisted-pair
- Security video

Pinout

EL9110
(16-PIN QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- 12V
Maximum Continuous Output Current 30mA
Power Dissipation . . . . . See Curves
Pin Voltages . . . . . V_S- -0.5V to V_S+ +0.5V

Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Lead Temperature . . . . . 260°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{SA}+ = V_A+ =+5V, V_{SA}- = V_A- = -5V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	Bandwidth	See Figure 1		150		MHz
SR	Slew Rate	V_{IN} = -1V to +1V, V_G = 0.35, V_C = 0, R_L = 75 + 75Ω		1.5		V/ns
THD	Total Harmonic Distortion	10MHz 1V pk-to-pk out, V_G = 0.35V, X2 gain, V_C = 0		-50		dBc
DC PERFORMANCE						
V_{OS}	Offset Voltage	X2 gain, no equalization	-300	-10	300	mV
INPUT CHARACTERISTICS						
CMIR	Common-mode Input Range	Common-mode extension off		-4/+3.5		V
CMIRx	Extended CMIR	Common-mode extension on		±4.5		V
O_{NOISE}	Output Noise	V_G = 0.35, X2 gain, 75+75Ω load, V_C = 0.6		25		mV RMS
CMRR	Common-mode Rejection Ratio	Measured at 10kHz		60		dB
CMRR+	Common-mode Rejection Ratio	Measured at 10MHz		50		dB
CMBW	CM Amplifier Bandwidth	10K || 10pF load		50		MHz
CM_{SLEW}	CM Slew Rate	Measured @ +1V to -1V		100		V/µs
C_{INDIFF}	Differential Input Capacitance	Capacitance V_{INP} to V_{INM}		600		fF
R_{INDIFF}	Differential Input Resistance	Resistance V_{INP} to V_{INM}	1	2.4		MΩ
C_{INCM}	CM Input Capacitance	Capacitance V_{INP} = V_{INM} to ground		1.2		pF
R_{INCM}	CM Input Resistance	Resistance V_{INP} = V_{INM} to ground	1	2.8		MΩ
$+I_{IN}$	Positive Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
$-I_{IN}$	Negative Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
V_{INDIFF}	Differential Input Range	V_{INP} - V_{INM} when slope gain falls to 0.9	2.5	3.2		V
OUTPUT CHARACTERISTICS						
V_O	Output Voltage Swing	R_L = 150Ω		±3.5		V
I_{OUT}	Output Drive Current	R_L = 10Ω, V_{INP} = 1V, V_{INM} = 0V, X2 = gain, V_G = 0.35	50	60		mA
R_{OUTCM}	CM Output Resistance	at 100kHz		30		Ω
L_{OUTCM}	CM Output Inductance	at 100kHz		1		µH
DiffGain	Differential Gain	V_C = 0, V_G = 0.35, X2 = 5, R_L = 75+75Ω	0.85	1.0	1.1	

Electrical Specifications $V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{SON}	Supply Current	$V_{ENBL} = 5$, $V_{INM} = 0$	27		34	mA
I_{SOFF}	Supply Current	$V_{ENBL} = 0$, $V_{INM} = 0$	0.4		0.8	mA
PSRR	Power Supply Rejection Ratio	DC to 100kHz, ±5V supply		60		dB
LOGIC CONTROL PINS						
V_{HI}	Logic High Level	V_{IN} - V_{LOGIC} ref for guaranteed high level	1.35			V
V_{LOW}	Logic Low Level	V_{IN} - V_{LOGIC} ref for guaranteed low level			0.8	V
I_{LOGICH}	Logic High Input Current	$V_{IN} = 5V$, $V_{LOGIC} = 0V$			50	µA
I_{LOGICL}	Logic Low Input Current	$V_{IN} = 0V$, $V_{LOGIC} = 0V$			15	µA

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN FUNCTION
1	CTRL_REF	Input	Reference voltage for V_{GAIN} and V_{CTRL} pins
2	VCTRL	Input	Control voltage (0V - 1V) to set equalization
3	VINP	Input	Positive differential input
4	VINM	Input	Negative differential input
5	VS-	Power	-5V to core of chip
6	CMOUT	Output	Output of common mode voltage present at inputs
7	VGAIN	Input	Control voltage to set overall gain (0V - 1V)
8	LOGIC_REF	Input	Reference voltage for all logic signals
9	X2	Logic Input	Logic signal; low - gain = 1, high - gain = 2
10	0V		0V reference for output voltage
11	VSA-	Power	-5V to output buffer
12	VOUT	Output	Single-ended output voltage reference to pin 10
13	VSA+	Power	+5V to output buffer
14	ENBL	Logic Input	Logic signal to enable pin; low - disabled, high - enabled
15	VS+	Power	+5V to core of chip
16	CMEXT	Logic Input	Logic signal to enable CM range extension; active high

Typical Performance Curves

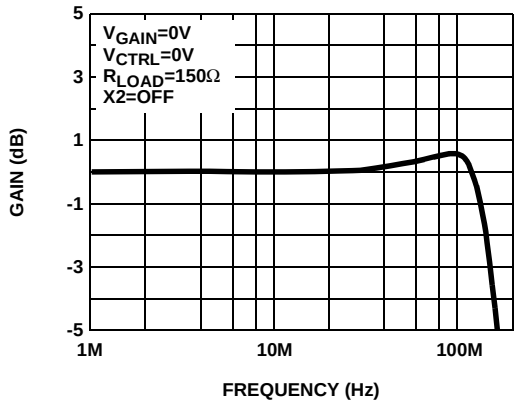


FIGURE 1. FREQUENCY RESPONSE

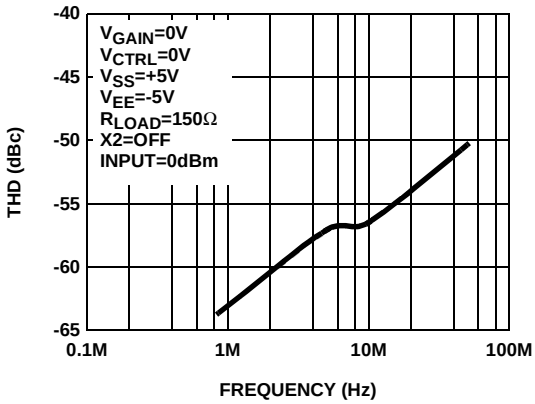


FIGURE 2. TOTAL HARMONIC DISTORTION

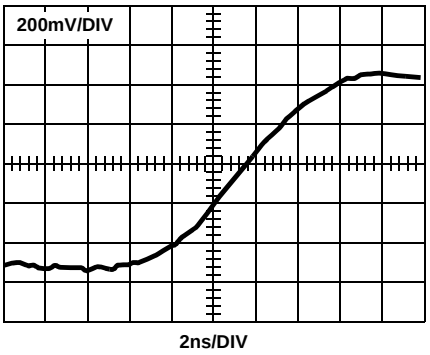


FIGURE 3. RISE TIME

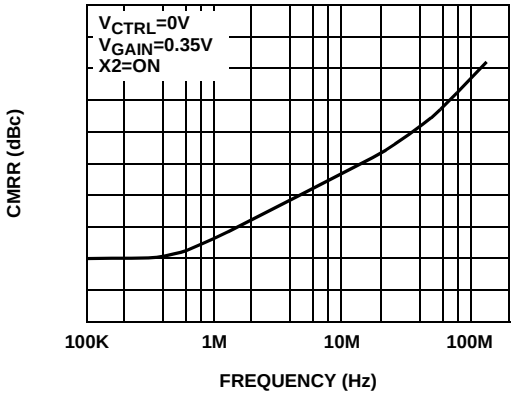


FIGURE 4. COMMON MODE REJECTION

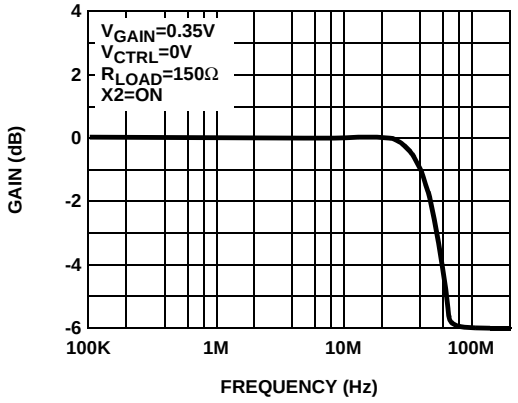


FIGURE 5. CM AMPLIFIER BANDWIDTH

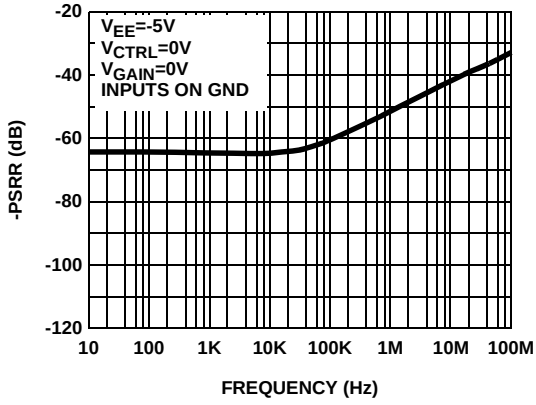


FIGURE 6. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

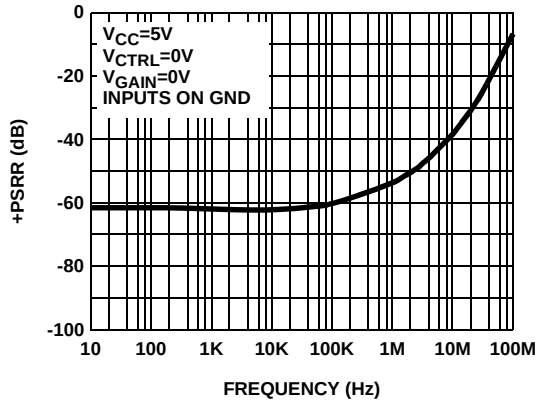


FIGURE 7. PSRR vs FREQUENCY

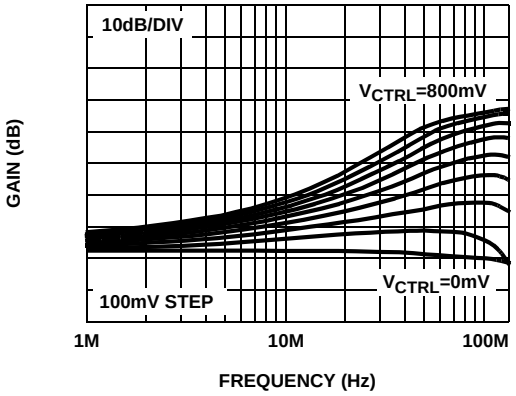


FIGURE 8. GAIN AS THE FUNCTION OF V_{CTRL}

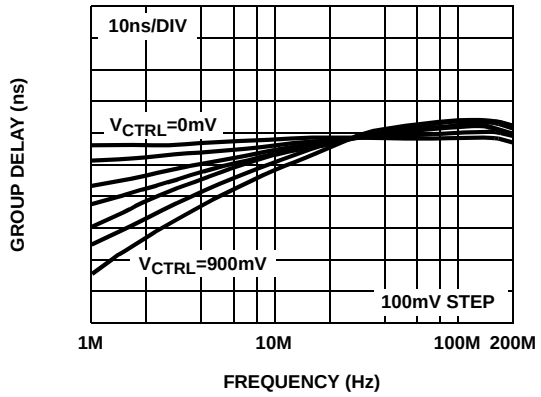


FIGURE 9. GROUP DELAY AS THE FUNCTION OF THE FREQUENCY REPONSE CONTROL VOLTAGE (V_{CTRL})

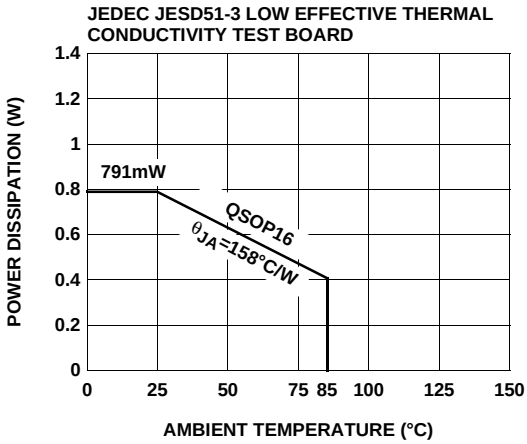


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

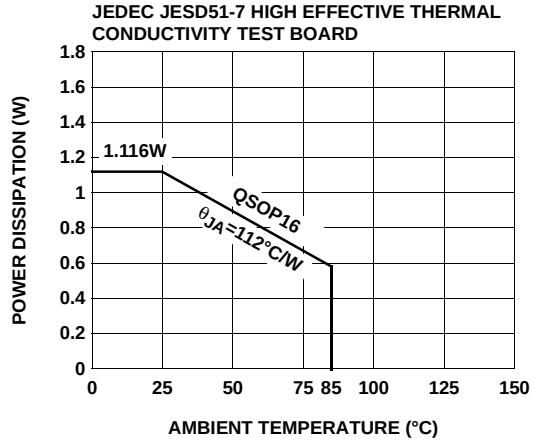


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Logic Control

The EL9110 has three logical input pins, Chip Enable (ENBL), Common Mode Extend (CMEXT), and Switch Gain (X2). The logic circuits all have a nominal threshold of 1.1V above the potential of the logic reference pin. In most applications it is expected that this chip will run from a +5V, 0V, -5V supply system with logic being run between 0V and +5V. In this case the logic reference voltage should be tied to the 0V supply. If the logic is referenced to the -5V rail, then the logic reference should be connected to -5V. The logic reference pin sources about 60µA and this will rise to about 200µA if all inputs are true (positive).

The logic inputs all source up to 10µA when they are held at the logic reference level. When taken positive, the inputs sink a current dependent on the high level, up to 50µA for a high level 5V above the reference level.

The logic inputs, if not used, should be tied to the appropriate voltage in order to define their state.

Control Reference and Signal Reference

Analog control voltages are required to set the equalizer and contrast levels. These signals are voltages in the range 0V - 1V, which are referenced to the control reference pin. It is expected that the control reference pin will be tied to 0V and the control voltage will vary from 0V to 1V. It is; however, acceptable to connect the control reference to any potential between -5V and 0V to which the control voltages are referenced.

The control voltage pins themselves are high impedance. The control reference pin will source between 0µA and 200µA depending on the control voltages being applied.

The control reference and logic reference effectively remove the necessity for the 0V rail and operation from ±5V (or 0V and 10V) only is possible. However we still need a further reference to define the 0V level of the single ended output signal. The reference for the output signal is provided by the 0V pin. The output stage cannot pull fully up or down to either supply so it is important that the reference is positioned to allow full output swing. The 0V reference should be tied to a 'quiet ground' as any noise on this pin is transferred directly to the output. The 0V pin is a high impedance pin and draws dc bias currents of a few µA and similar levels of AC current.

Common Mode Extension

The common mode extension circuitry extends the range of input common mode voltage before the input differential amplifier is overloaded. It does this by reducing the voltage equally at both inputs of the first differential amplifier as the common mode signal rises towards the supply. Similarly, when the common mode input signal goes low, the inputs to the first differential amplifier are raised whilst preserving the differential signal and maintain the amplifier within its common mode operating range.

This operation may not always be desirable. A problem occurs because the EL9110 sinks or sources a common mode current though its input pins to create the common mode offset voltage. Assuming the system has been set up so that the differential line has a well-balanced impedance, then a problem will only occur when the common mode impedance to ground is not low. This will occur in systems where the inputs to the EL9110 are AC coupled. In such systems it is recommended that the common mode extension be disabled. In systems where the differential input signal is directly coupled and has its common mode level defined by a low impedance line driver, the common mode extension circuitry can extend the total common mode range by 2V - 3V.

Equalizing

When transmitting a signal across a twisted pair cable, it is found that the high frequency (above 1MHz) information is attenuated more significantly than the information at low frequencies. The attenuation is predominantly due to resistive skin effect losses and has a loss curve which depends on the resistivity of the conductor, surface condition of the wire and the wire diameter. For the range of high performance twisted pair cables based on 24awg copper wire (Cat 5 etc.) these parameters vary only a little between cable types, and in general cables exhibit the same frequency dependence of loss. (The lower loss cables can be compared with somewhat longer lengths of their more lossy brothers.) This enables a single equalizing law equation to be built into the EL9110.

With a control voltage applied between pins 2 and 1, the frequency dependence of the equalization is shown in Figure 12. The equalization matches the cable loss up to about 100MHz. Above this, system gain is rolled off rapidly to reduce noise bandwidth. The roll-off occurs more rapidly for higher control voltages, thus the system (cable + equalizer) bandwidth reduces as the cable length increases. This is desirable, as noise becomes an increasing issue as the equalization increases.

The cable loss for 100m, 200m, and 300m of CAT 5 cable, based on manufacturer's loss curves is shown in Figure 13.

Thus:

- 100m requires V_C = 0.2V
- 200m requires V_C = 0.6V

and:

- 300m requires V_C = 1.0V approximately

Contrast

By varying the voltage between pins 7 and 1, the gain of the signal path can be changed in the ratio 4:1. The gain change varies almost linearly with control voltage. For normal

operation it is anticipated the X2 mode will be selected and the output load will be back matched. A unity gain to the output load will then be achieved with a gain control voltage of about 0.35V. This allows the gain to be trimmed up or down by 6dB to compensate for any gain/loss errors that affect the contrast of the video signal. Figure 14 shows an example plot of the gain to the load with gain control voltage.

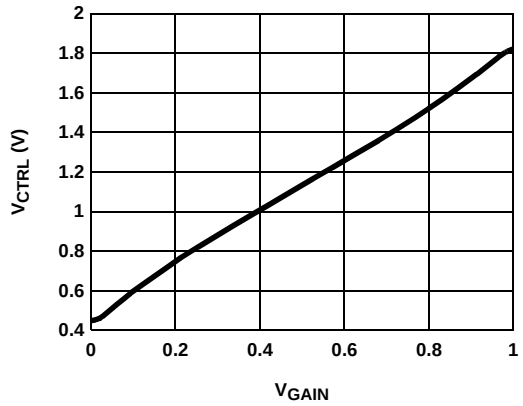


FIGURE 12. VARIATION OF GAIN WITH GAIN CONTROL VOLTAGE

Circuit and Layout Recommendation

The interconnection cable is a transmission line therefore for proper function it should be treated like transmission line, a refection-free termination is necessary.

A reflection-free termination is a real "ohmic" resistor with as less as possible reactive parasitic.

The traces of the layout, up to the point where of the termination resistor placed, are part of the transmission line which also includes the cable's connector. A connector with a better controlled impedance is an obligation for good picture quality. The termination resistor should be placed close to the inputs of the device's pins (pin 3 and pin 4.) The small capacitance differential and common mode capacitance of the input pins of the device makes it possible to connect parallel to the termination resistor.

The cable will work as an antenna for all the RF spectrum which is "in the air" where the cable is used. The spectrum, particularly its common mode components, could and will contain high energy level of transients which are above the built-in protection level of the device and easily could damage its inputs. Using a transient protection circuit according to the given application is recommended.

Since the used signal's bandwidth is in the range of 100MHz, for layout and power supply bypassing the roles of RF design should be applied.

The following picture is taken from the DB9110 demo-board's layout. For better visibility the ground plain is removed.

The ground plane is shown in the following picture.

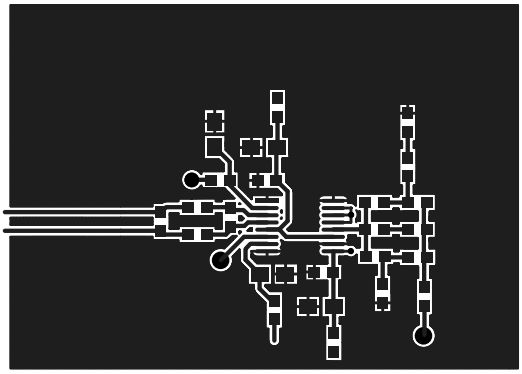


FIGURE 13. DEMO BOARD LAYOUT

The accompanying circuit diagram looks like:

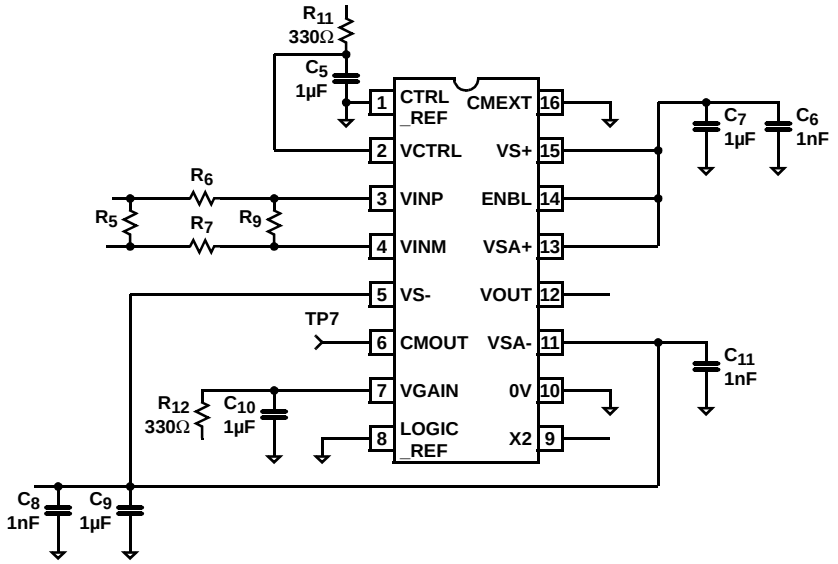
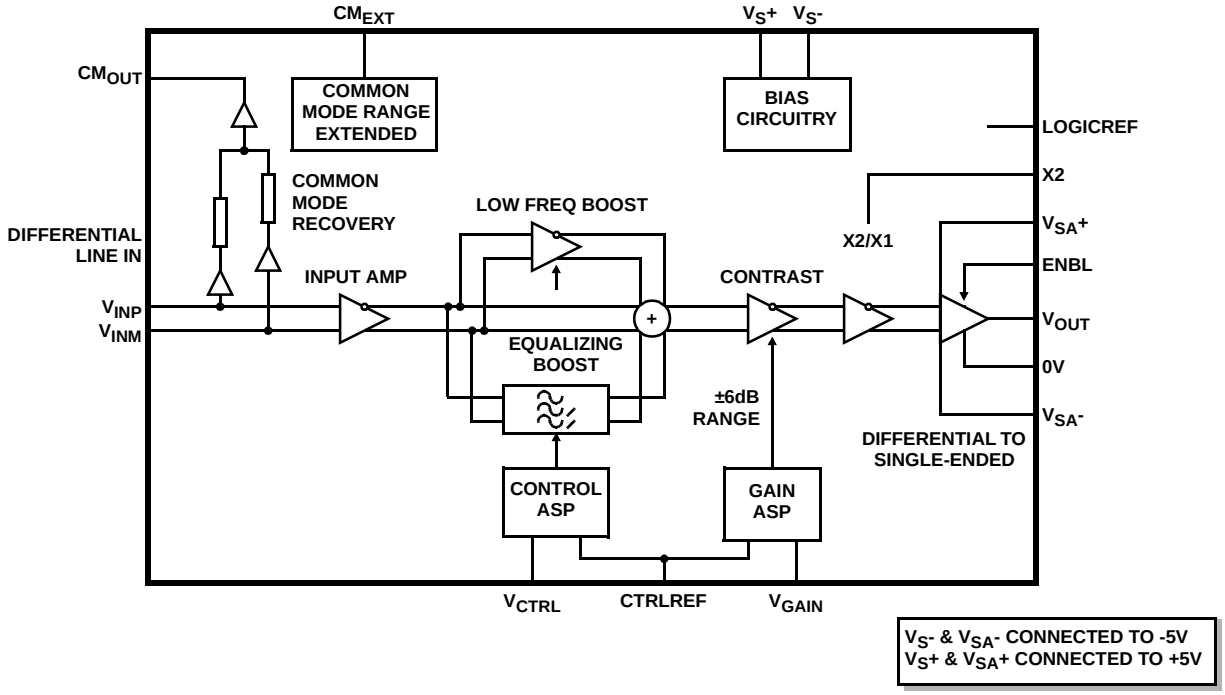


FIGURE 14. CIRCUIT DIAGRAM

Block Diagram



Typical Application