PM5342

SPECTRA-155

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER

REVISION E DEVICE ERRATA

ISSUE 1: NOVEMBER 2000
PRODUCTION

PRODUCTION

ERRATA

PMC-2001737

PMC-Sierra, Inc.

ISSUE 1

PM5342 SPECTRA-155

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REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	November 2000	Document created.

PRODUCTION   **PMC** *PMC-Sierra, Inc.*   **PM5342 SPECTRA-155**

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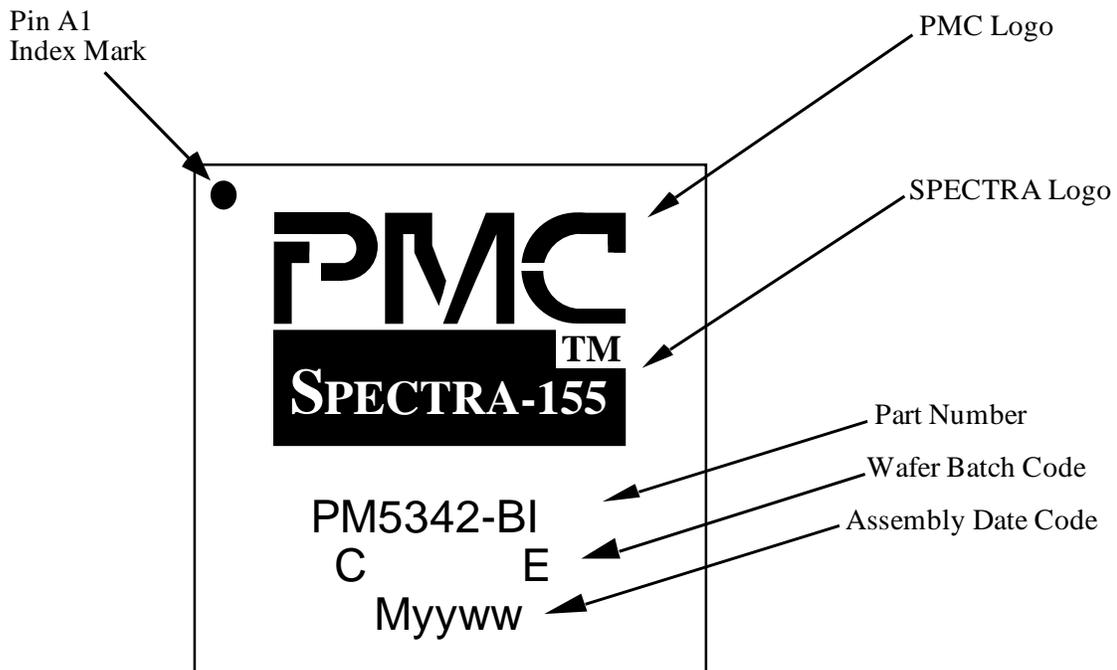*PMC-Sierra, Inc.*   **PM5342 SPECTRA-155**

1 ISSUE 1 ERRATA

This document is the errata notice for Revision E, production release of the SPECTRA-155 (PM5342-BI) and issue 4 SPECTRA-155 datasheet. The issue 4 SPECTRA-155 datasheet (PMC-1970133) and issue 1 errata supersede all prior editions and versions of the datasheet.

1.1 Device Identification

The information in this document applies to the PM5342 SPECTRA-155 revision E device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5342 SPECTRA-155 Revision E is packaged in a 256 pin Super BGA package.

Figure 1: PM5342 SPECTRA-155 Branding Format

Pin A1 Index Mark

PMC Logo

SPECTRA Logo

Part Number

Wafer Batch Code

Assembly Date Code

PMC™

SPECTRA-155

PM5342-BI
C   E
Myyww

TOP VIEW
SCALE : 2:1
(APPROX.)

2 FUNCTIONAL DEFICIENCIES OVERVIEW

This section outlines the known functional discrepancies between the PM5342 SPECTRA-155 revision E production release device and the Issue 4 SPECTRA-155 datasheet. The errata are explained in more detail in section 3 of this document. Please note that the errata contained in this document are preliminary.

Table 1   FUNCTIONAL DEFICIENCIES SUMMARY LIST

#	Discrepancy	Workaround?	Modes Affected
3.1 Device Reset/Reconfiguration			
3.1.1	FIFO Locked in Overflow/Underflow Condition	Yes	Reset/Reconfiguration

3   SPECTRA-155 REVISION E FUNCTIONAL DEFICIENCY DETAILS

3.1   Device Reset/Reconfiguration

3.1.1 FIFO Locked in Overflow/Underflow Condition

Description

The SPECTRA-155 device may exhibit a failure where the Elastic Store FIFO in the RTAL or TTAL blocks does not recover normally from an underflow or overflow caused by a hardware or software reset, or service-affecting event.

Most of the time, the FIFO will recover automatically from overflow or underflow conditions. However, there is a small probability that the FIFO will not recover by itself and will need to be manually reset. The rate of failure varies from 0% to 1%. Service-affecting events include LOS, LOF, AU-LOP, AU-NDF, and AU-AIS.

If this failure occurs, data will be corrupted and the ESEI bit in the RTAL or TTAL Interrupt Status and Control register will be set high continuously.

Please note that the same symptoms will occur if there are board-level problems with the Telecom bus signals generated externally to SPECTRA-155. If the external system is generating Telecom bus inputs for SPECTRA-155 that are incorrect, the ESEI bit in the RTAL or TTAL will be set high continuously and data will be corrupted. When these symptoms are the result of incorrect input signals from the external system, resetting the internal FIFO will not solve the problem.

Users who see these symptoms very frequently, particularly while a board is being debugged, should first verify that all Telecom bus input signals meet the specified timing requirements. This includes confirming that the ACK and DCK clocks are the proper frequency and that the AC1J1V1, APL, and DFP input signals are correct according to the specifications in the data sheet. Please contact PMC-Sierra Applications (apps@pmc-sierra.com) for assistance in debugging board-level Telecom bus timing issues.

Workaround

To verify that the device is in the failure condition:

1. After reset/reconfiguration or service-affecting event, read the ESEI bit in the RTAL and TTAL Interrupt Status and Control registers 141h, 181h, 1C1h, 129h, 169h, and 1A9h.

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2. Read the registers at least twice, waiting 500 us (minimum) between reads. If ESEI is high on the second read, *and if there are no timing problems on the Telecom bus*, the FIFO is in the failure condition and needs to be reset.

    Note: for STM-1/AU4 mode, read registers 141h and 129h only; for STM-1/AU3 mode, read all listed registers.

To reset the FIFO:

3. Reset the FIFO by toggling the Reserved bit 7 in the RTAL and TTAL Control registers corresponding to the affected RTAL/TTAL (Register 140h, 180h, 1C0h, 128h, 168h, and/or 1A8h). Hold the Reserved bit 7 high for 10 us (minimum) to ensure clean reset of the FIFO, then clear the bit.

4. After clearing the Reserved bit, wait 250us (minimum) to allow the FIFO to start up again. Repeat the reads of the ESEI bit in the affected RTAL/TTAL as described in Steps 1 and 2, to confirm that the ESEI bit clears.

Performance without workaround

If the failure occurs, the FIFO will remain locked in the overflow/underflow condition until it is reset. Data will continue to be corrupted. AIS-P will be inserted if it is enabled due to FIFO overflow/underflow conditions.

The FIFO lock condition can occur only after a reset/reconfiguration or service-affecting event. Once the FIFO is operating properly, this failure will not occur during normal operation. *If the above symptoms occur during normal operation, particularly while the board is being debugged, they are probably due to board-level problems with Telecom bus signals generated by the external system.*

4   SPECTRA-155 REVISION E DATASHEET ERRATA

This section contains errata in the issue 4 SPECTRA-155 datasheet.

1. unaltered text is unchanged to add context to changes

2. ***new material is bold and italicized***

3. *comments specific to this document are in italics*

4.1   DISV1 bit description correction – page 336

The DISV1 bit description should be modified as shown below:

DISV1:

When set high, the DISV1 bit configures the DC1J1V1, and GC1J1V1 outputs to mark only the frame and synchronous payload envelope (virtual container) alignments (C1 and J1 bytes). DC1J1V1 and GC1J1V1 will not indicate the tributary multiframe alignment. When DISV1 is set low, DC1J1V1 and GC1J1V1 mark all three of the frame, payload envelope and tributary multiframe alignments.

It is recommended that DISV1 be set high in normal operation to disable the V1 pulse on DC1J1V1. PMC-Sierra's tributary-processing devices (PM5362 TUPP+, PM5363 TUPP+622, PM5365 TEMAP, and PM8315 TEMUX) interpret the H4 byte in the path overhead to identify the tributary multiframe alignment, so they do not require the V1 pulse.

In applications that do not use tributaries, there is no definition for multiframe and therefore no need for the V1 pulse on DC1J1V1.

The DISV1 bit must be set high when byte or nibble data mode as selected by the SMODE[2:0] inputs is in operation. The DISV1 bit must also be set high when the built-in DROP bus PRBS generator and monitor are used.

4.2   RTIMINS and RTIUINS bit description correction – page 195

The RTIMINS and RTIUINS bit descriptions in register 1Dh currently read:

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low"

This description should be modified to read:

This bit is active regardless of the state of the ALLONES bit in the RLOP Control/Status register

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