1 PRODUCT OVERVIEW

S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8-series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C80E5/C80E7 MICROCONTROLLER

The S3C80E5/C80E7 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process, based on Samsung's newest CPU architecture.

The S3C80E5/C80E7 is the microcontroller which has 16/24-Kbyte mask-programmable ROM. The S3P80E5/P80E7 is the microcontroller which has 16/24-Kbyte one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers developed the S3C80E5/C80E7 by integrating the following peripheral modules with the powerful SAM87 core:

— Four programmable I/O ports, including three 8-bit ports and one 2-bit port, for a total of 26 pins.

— Internal LVD circuit and twelve bit-programmable pins for external interrupts.

— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).

— One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.

— One 8-bit counter with auto-reload function and one-shot or repeat control.

The S3C80E5/C80E7 is a versatile general-purpose microcontroller which is especially suitable for use as unified remote transmitter controller. It is currently available in a 32-pin SOP and SDIP package for S3C80E5 and S3C80E7. And available in 40 DIP package only for S3C80E7.

OTP

The S3P80E5/P80E7 is an OTP (One Time Programmable) version of the S3C80E5/C80E7 microcontroller. The S3P80E5/P80E7 microcontroller has an on-chip 16/24-Kbyte one-time-programmable EPROM instead of a masked ROM. The S3P80E5/P80E7 is comparable to the S3C80E5/C80E7, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 16-Kbyte internal program memory (ROM): S3C80E5
- 24-Kbyte internal program memory (ROM): S3C80E7
- 256-byte internal (RAM): 8000–80FFH
- Data memory: 317-byte internal register file

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 750 ns at 8 MHz f_{OSC} (minimum)

Interrupts

- Six interrupt levels and 18 interrupt sources
- 15 vectors (14 sources have a dedicated vector address and four sources share a single vector)
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Three 8-bit I/O ports (P0–P2) and one 2-bit port (P3) for a total of 26 bit-programmable pins
- Twelve input pins for external interrupts

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture, and PWM
- One 16-bit timer/counter (Timer 1) with two operating modes; Interval and Capture

Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

Back-up mode

- When reset pin is low level or when V_{DD} is lower than V_{LVD}, the chip enters back-up mode to reduce current consumption.

Low Voltage Detect Circuit

- Low voltage detect for reset or back-up mode input.
- Low level detect voltage :
  2.2 V (Typ) –100 mV/+ 200 mV

Operating Temperature Range

- – 40°C to + 85 °C

Operating Voltage Range

- 2.0 V to 5.5 V at 4 MHz f_{OSC}
- 2.1 V to 5.5 V at 8 MHz f_{OSC}

Package Type

- 32-pin SOP
- 32-pin SDIP
- 40-pin DIP

BLOCK DIAGRAM

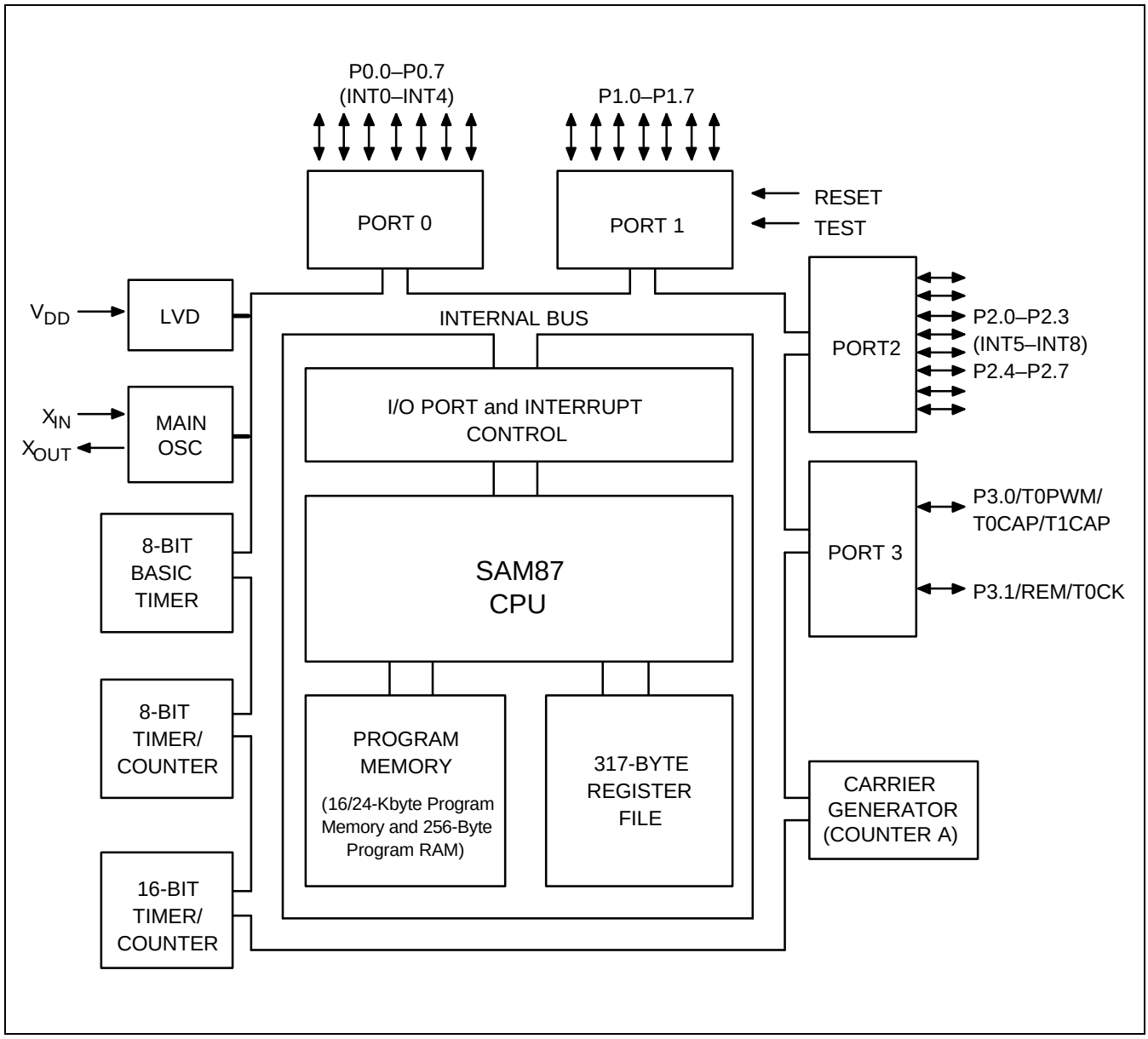


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

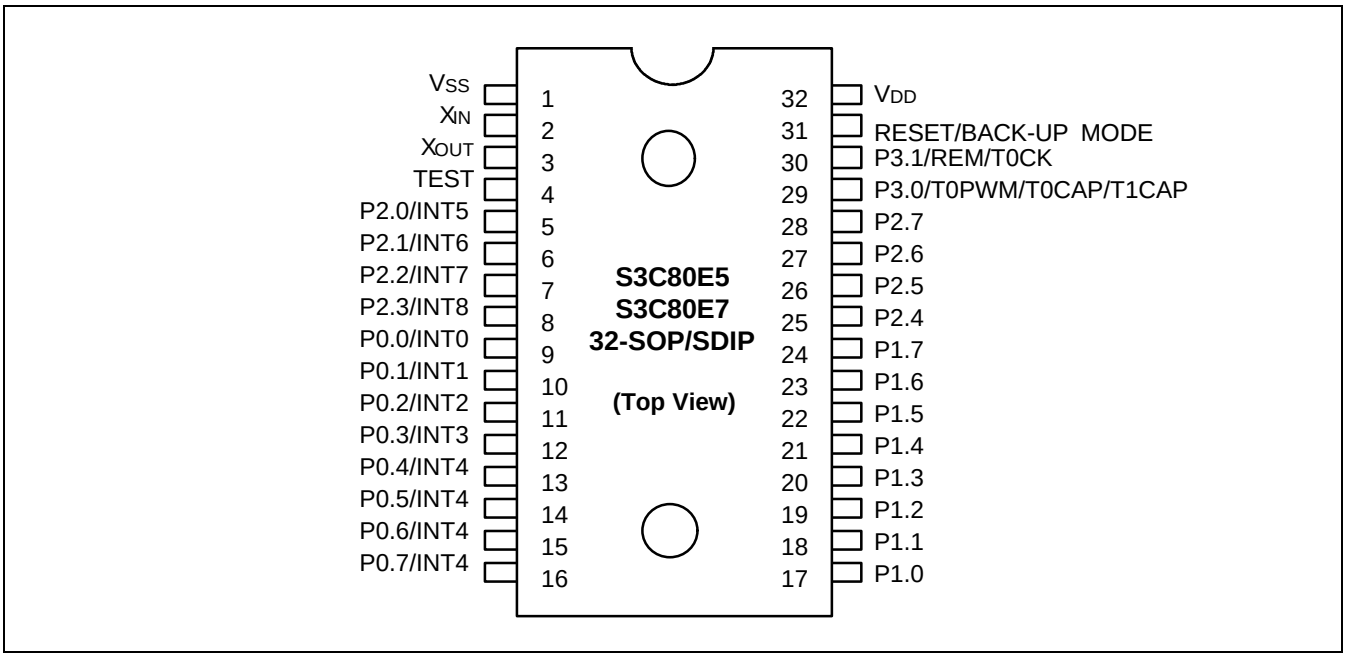


Figure 1-2. Pin Assignment (32-Pin SOP/SDIP Package)

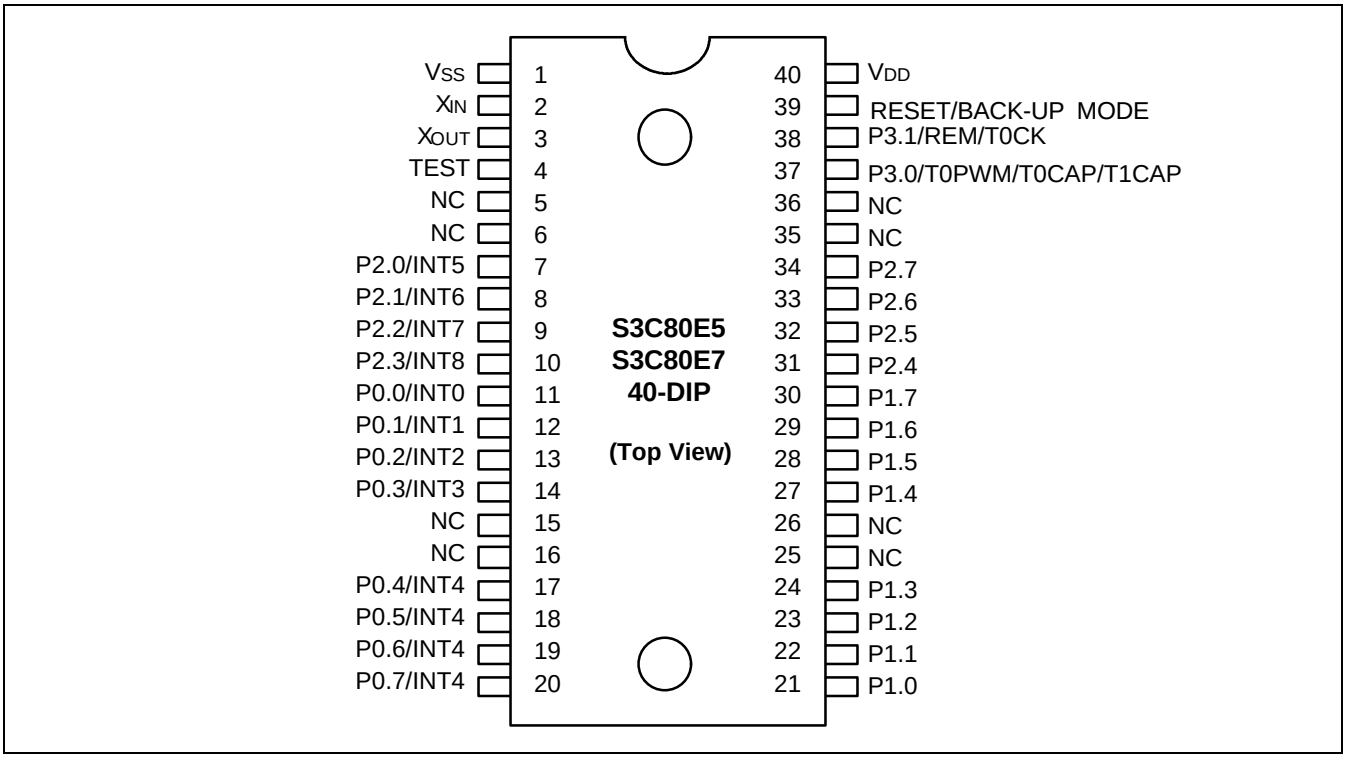
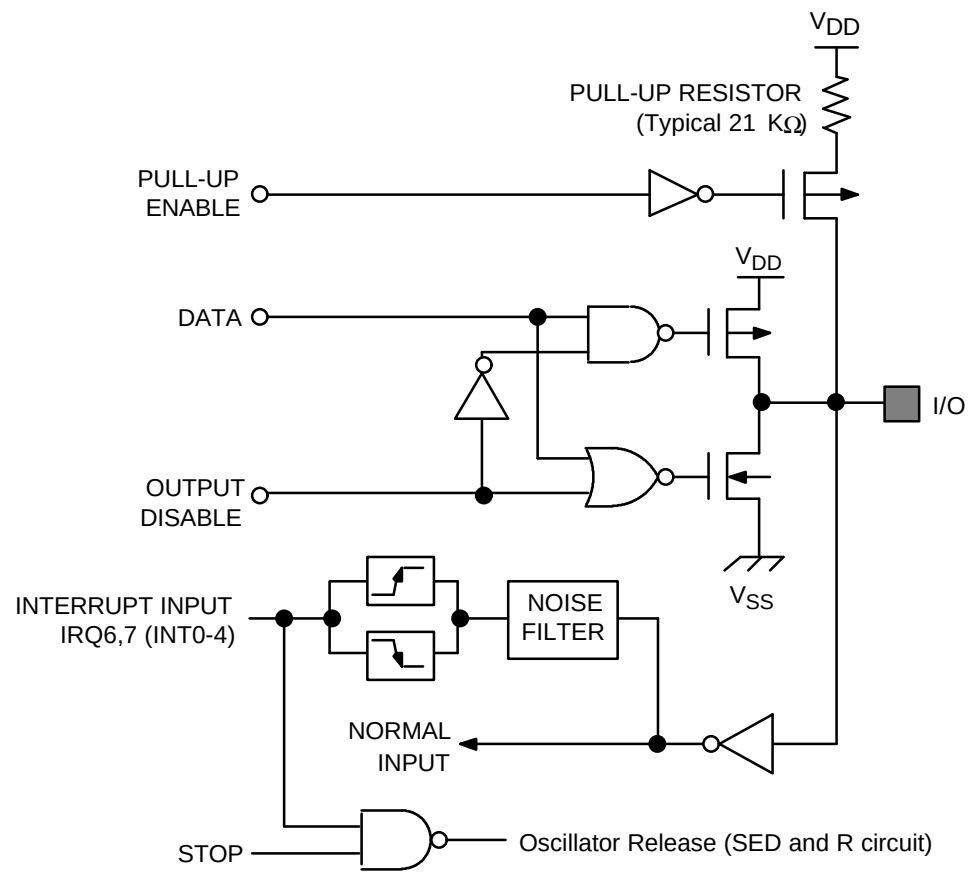


Figure 1-3. Pin Assignment (40-Pin DIP Package)

Table 1-1. Pin Descriptions

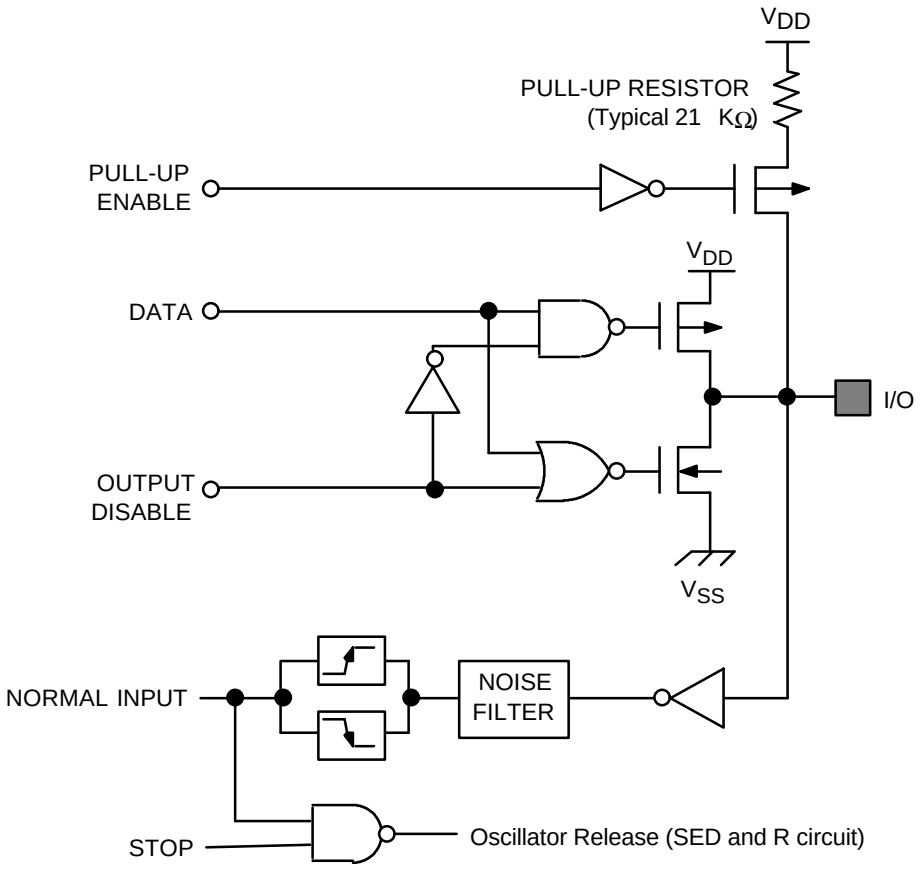
Pin Names	Pin Type	Pin Description	Circuit Type	Pin No. (32-pin)	Pin No. (40-pin)	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	1	9–16	11–14, 17–20	INT0–INT4
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to C-MOS input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type. Pull-up resistors are assignable by software.	2	17–24	21–24, 27–30	–
P2.0–P2.3 P2.4–P2.7	I/O	General-purpose I/O port with bit-programmable pins. Configurable to C-MOS input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. Lower nibble pins, P2.3–P2.0, can be assigned as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	3 4	5–8, 25–28	7–10, 31–34	INT5–INT8 –
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to C-MOS input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. The two port 3 pins have high current drive capability.	5	29 30	37 38	T0PWM/ T0CAP/ T1CAP/ REM/T0CK
X_{IN}, X_{OUT}	–	System clock input and output pins	–	2, 3	2, 3	–
RESET/ BACK-UP MODE	I	System reset signal input pin and back-up mode input pin. The pin circuit is a C-MOS input.	6	31	39	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS}).	–	4	4	–
V_{DD}	–	Power supply input pin	–	32	40	–
V_{SS}	–	Ground pin	–	1	1	–

PIN CIRCUITS



NOTE: To prevent and recover from abnormal stop status caused by battery bouncing, the S3P80E5 has a special logic_ SED and R circuit –related to P0 and P1. This is a specific function for key input/output of universal remote controller. When these ports (P0, P1) are used as a normal input pin, unexpected stop mode recovery can occur by input level switching. Hence, the user should be aware of input level switching, if P0 and P1 are to be used as normal input ports.

Figure 1-4. Pin Circuit Type 1 (Port 0)



NOTE: To prevent and recover from abnormal stop status caused by battery bouncing, the S3P80E5 has a special logic –SED and R circuit –related to P0 and P1. This is a specific function for key input/output of universal remote controller. When these ports (P0, P1) are used as a normal input pin, unexpected stop mode releasing can occur by input level switching. Hence, the user should be aware of input level switching, if P0 and P1 are to be used as normal input ports.

Figure 1-5. Pin Circuit Type 2 (Port 1)

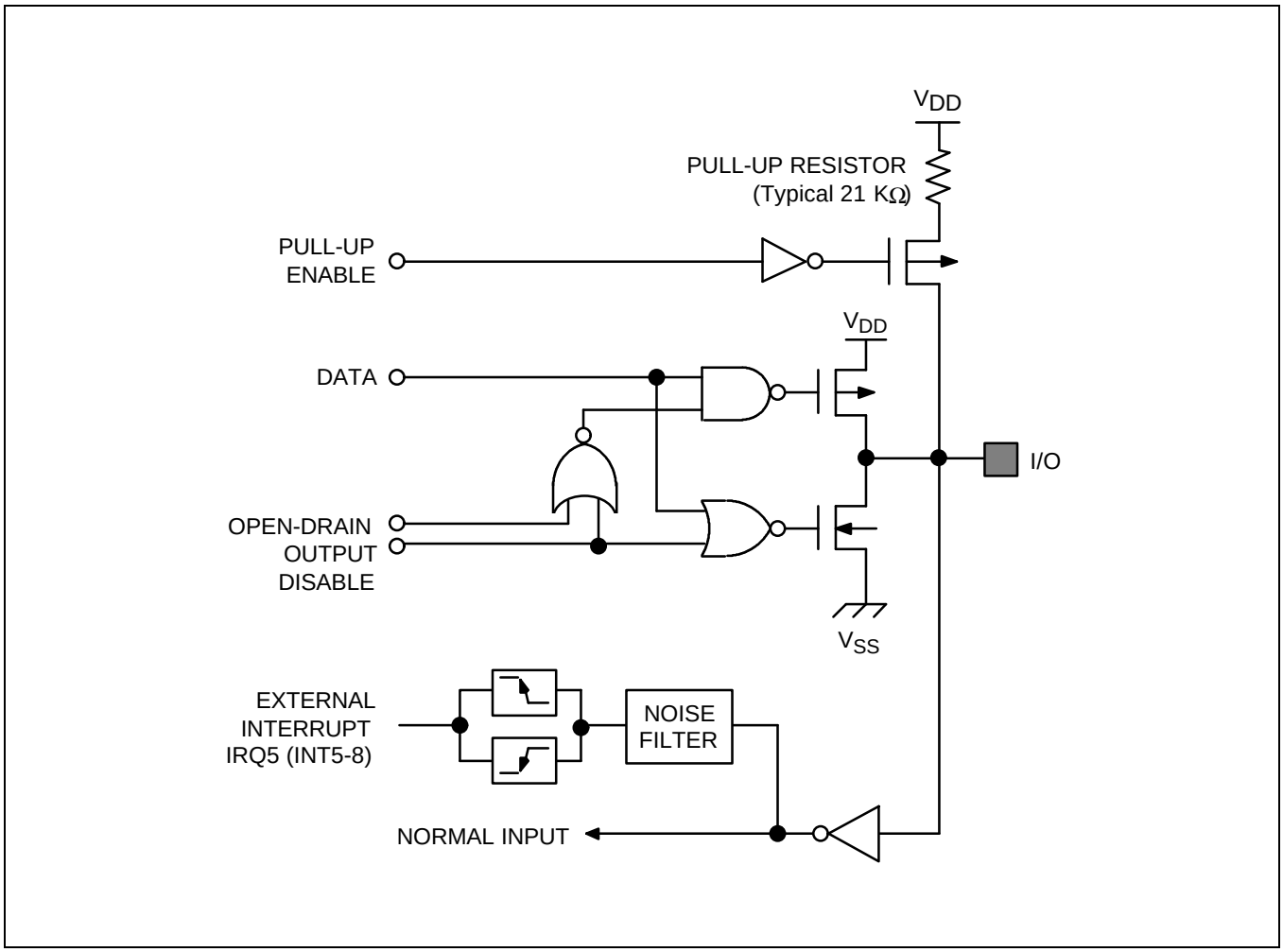


Figure 1-6. Pin Circuit Type 3 (Ports 2.0–2.3)

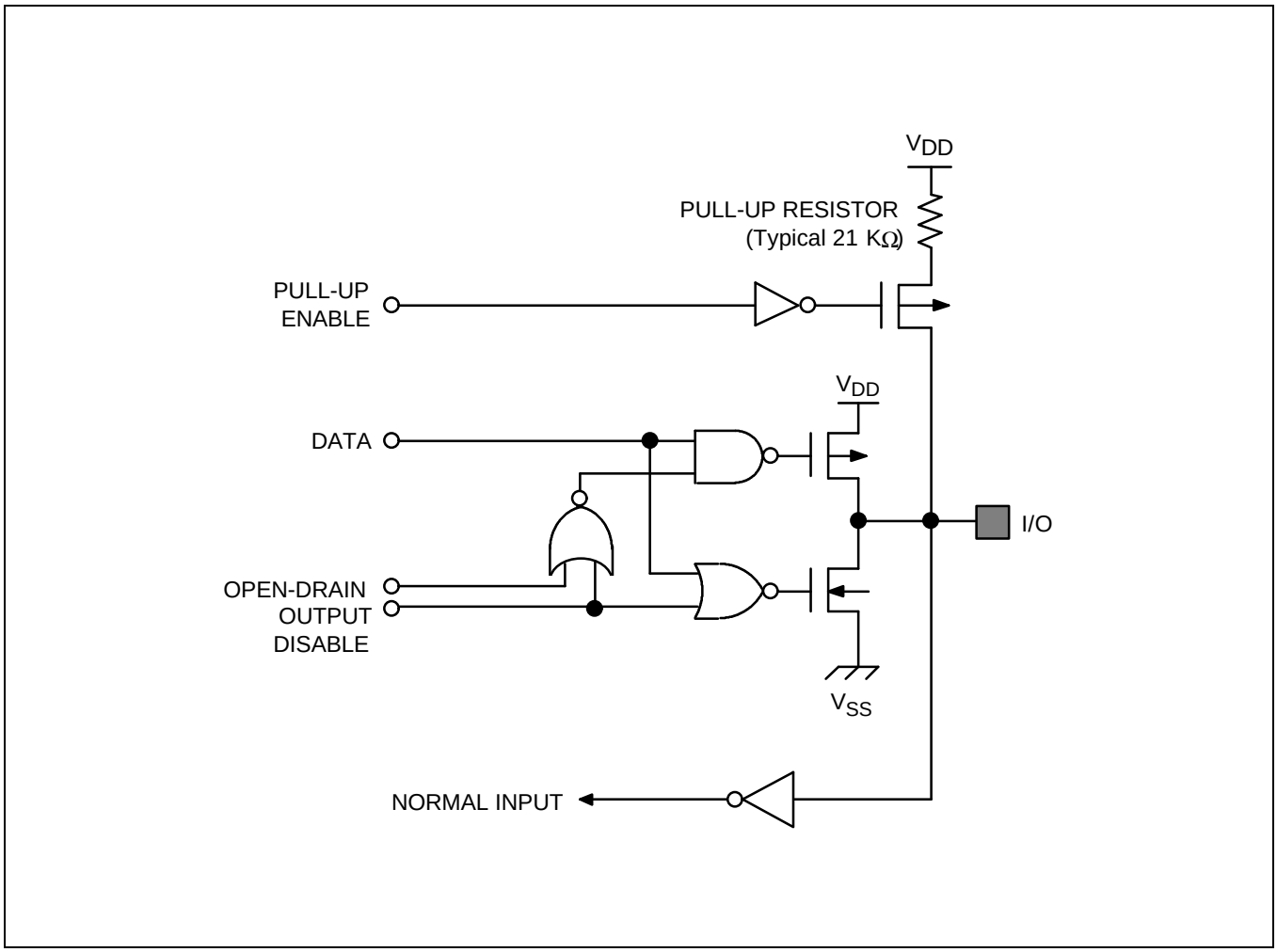


Figure 1-7. Pin Circuit Type 4 (P2.4–P2.7)

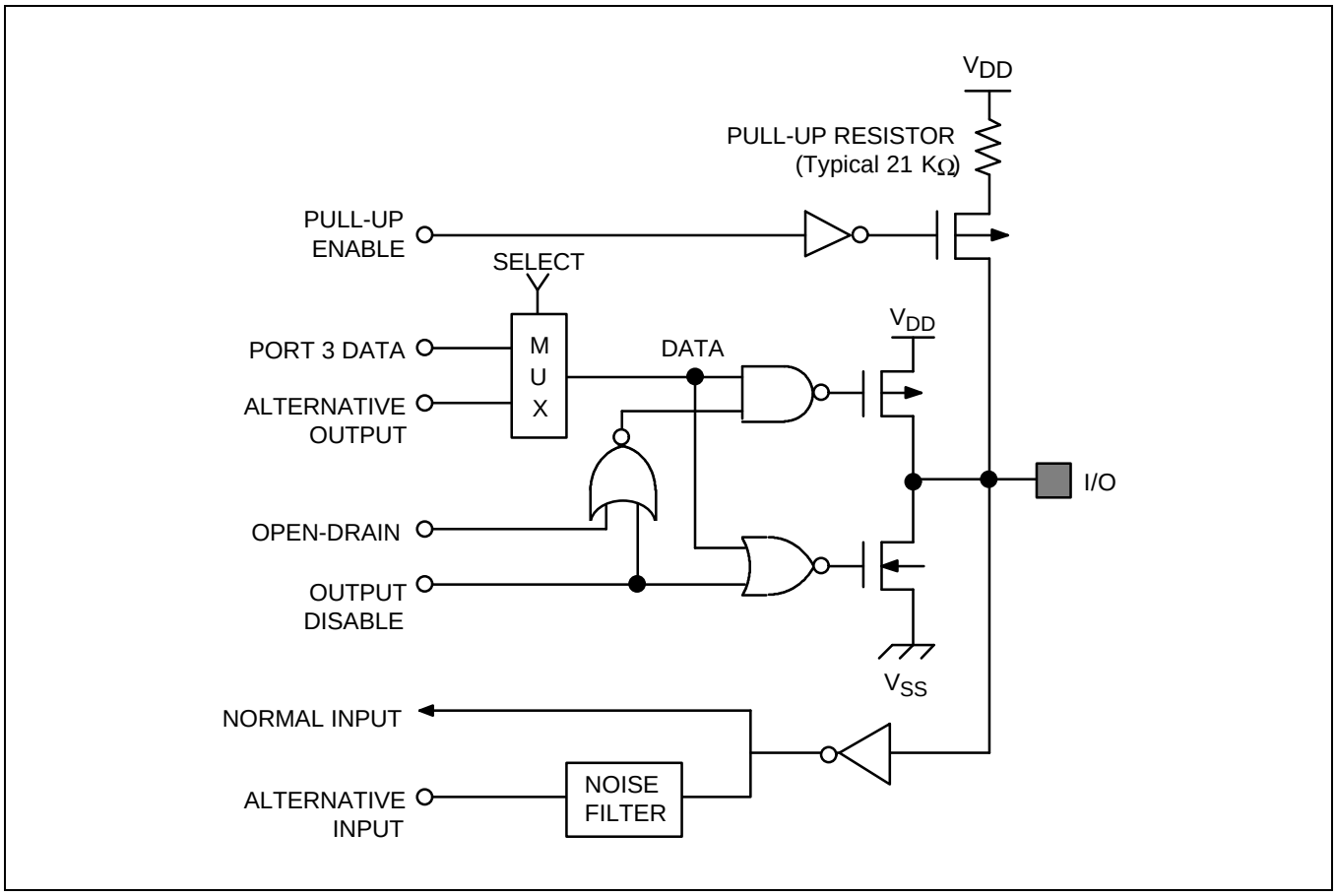


Figure 1-8. Pin Circuit Type 5 (P 3)

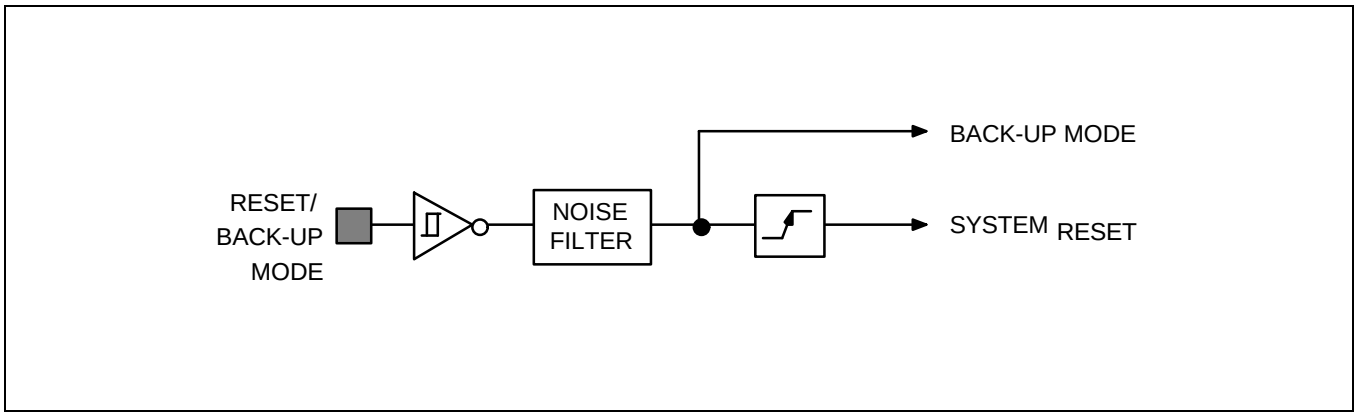


Figure 1-9. Pin Circuit Type 6 (RESET/BACK-UP MODE)

14 ELECTRICAL DATA

OVERVIEW

In this section, the S3C80E5/C80E7 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— Characteristics of low voltage detect circuit
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by an external interrupt
— Stop mode release timing when initiated by a RESET
— Stop mode release timing when initiated by a LVD
— I/O capacitance
— A.C. electrical characteristics
— Input timing for external interrupts (port 0, P2.3–P2.0)
— Input timing for RESET
— Oscillation characteristics
— Oscillation stabilization time
— Operating voltage range

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_{IN}	–	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All output pins	– 0.3 to V_{DD} + 0.3	V
Output current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, and 2	+ 100	
		Total pin current for port 3	+ 40	
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 8 MHz (Instruction clock = 1.33 MHz)	2.1	–	5.5	V
		f_{OSC} = 4 MHz (Instruction clock = 0.67 MHz)	2.0	–	5.5	
Input High voltage	V_{IH1}	All input pins except V_{IH2} and V_{IH3}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	RESET	0.85 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}	V_{DD} – 0.3		V_{DD}	
Input Low voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	0	–	0.2 V_{DD}	V
	V_{IL2}	RESET			0.4 V_{DD}	
	V_{IL3}	X_{IN}			0.3	
Output High voltage	V_{OH1}	V_{DD} = 2.4 V; I_{OH} = – 6 mA Port 3.1 only; T_A = 25 °C	V_{DD} – 0.7	–	–	V
	V_{OH2}	V_{DD} = 2.4 V; I_{OH} = – 3 mA Port 3.0 only; T_A = 25 °C	V_{DD} – 0.7			

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High voltage	V_{OH3}	V_{DD} = 5 V; I_{OH} = – 3 mA Port 2.7 only; T_A = 25°C	V_{DD} – 0.25	–	–	V
		V_{DD} = 2 V; I_{OH} = – 1 mA Port 2.7 only; T_A = 25°C				
	V_{OH4}	V_{DD} = 3.0 V; I_{OH} = – 1 mA All output pins except P3 and P2.7 port; T_A = 25°C	V_{DD} – 1			
Output Low voltage	V_{OL1}	V_{DD} = 2.4 V; I_{OL} = 15 mA Port 3.1 only; T_A = 25°C	–	0.4	0.5	V
	V_{OL2}	V_{DD} = 2.4 V; I_{OL} = 5 mA Port 3.0 only; T_A = 25°C		0.4	0.5	
	V_{OL3}	I_{OL} = 1 mA Port 0, 1, and 2; T_A = 25°C		0.4	1	
Input High leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and X_{OUT}	–	–	1	µA
	I_{LIH2}	V_{IN} = V_{DD}, X_{IN}, and X_{OUT}			20	
Input Low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, and RESET	–	–	– 1	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN} and X_{OUT}			– 20	
Output High leakage current	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	1	µA
Output Low leakage current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 1	µA
Pull-up resistors	R_{L1}	V_{IN} = 0 V; V_{DD} = 2.4 V T_A = 25 °C; Ports 0–3	44	55	82	kΩ
		V_{DD} = 5.5 V	15	21	32	

Table 14-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I_{DD1}	Operating mode V_{DD} = 5 V ± 10 % 8 MHz crystal	–	6	11	mA
		4 MHz crystal		4.5	9	
	I_{DD2}	Idle mode V_{DD} = 5 V ± 10 % 8 MHz crystal		1.8	3.5	
		4 MHz crystal		1.6	3	
	I_{DD3}	Stop mode V_{DD} = 6.0 V		20	35	µA
		V_{DD} = 5.5 V		18	25	
		V_{DD} = 3.3 V		12	15	
		V_{DD} = 0.7 V		1.0	1.5	

NOTE: Supply current does not include the current drawn through internal pull-up resistors or external output current loads.

Table 14-3. Characteristics of Low Voltage Detect Circuit

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresys Voltage of LVD(Slew Rate of LVD)	ΔV	LVDCON = 10001111B	–	10	100	mV
Low level detect voltage	V_{LVD}	LVDCON = 10001111B	2.10	2.20	2.40	V

NOTE: The reset values of bit 1 and bit 0 are in a unknown status, so is recommended to input the value #8FH in LVDCON for typical V_{LVD} (2.2 V –100/+200 mV).

Table 14-4. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.0	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.0 V Stop mode	–	–	1	µA

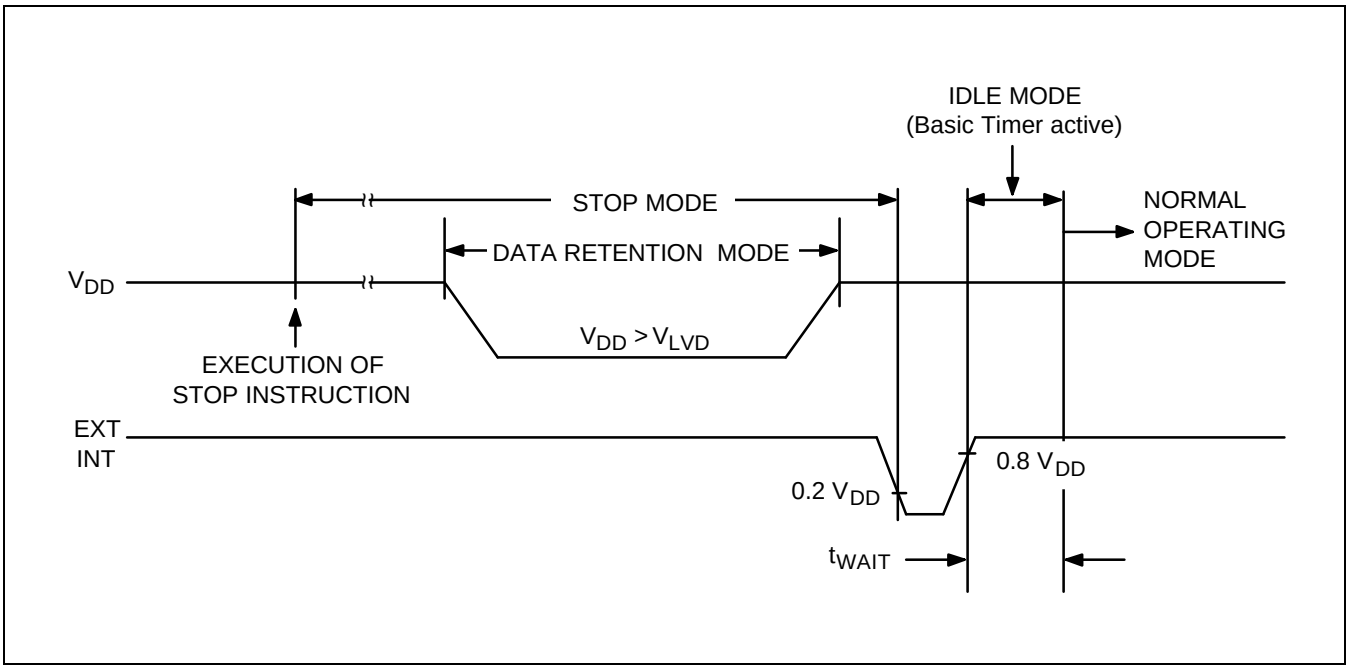


Figure 14-1. Stop Mode Release Timing When Initiated by an External Interrupt

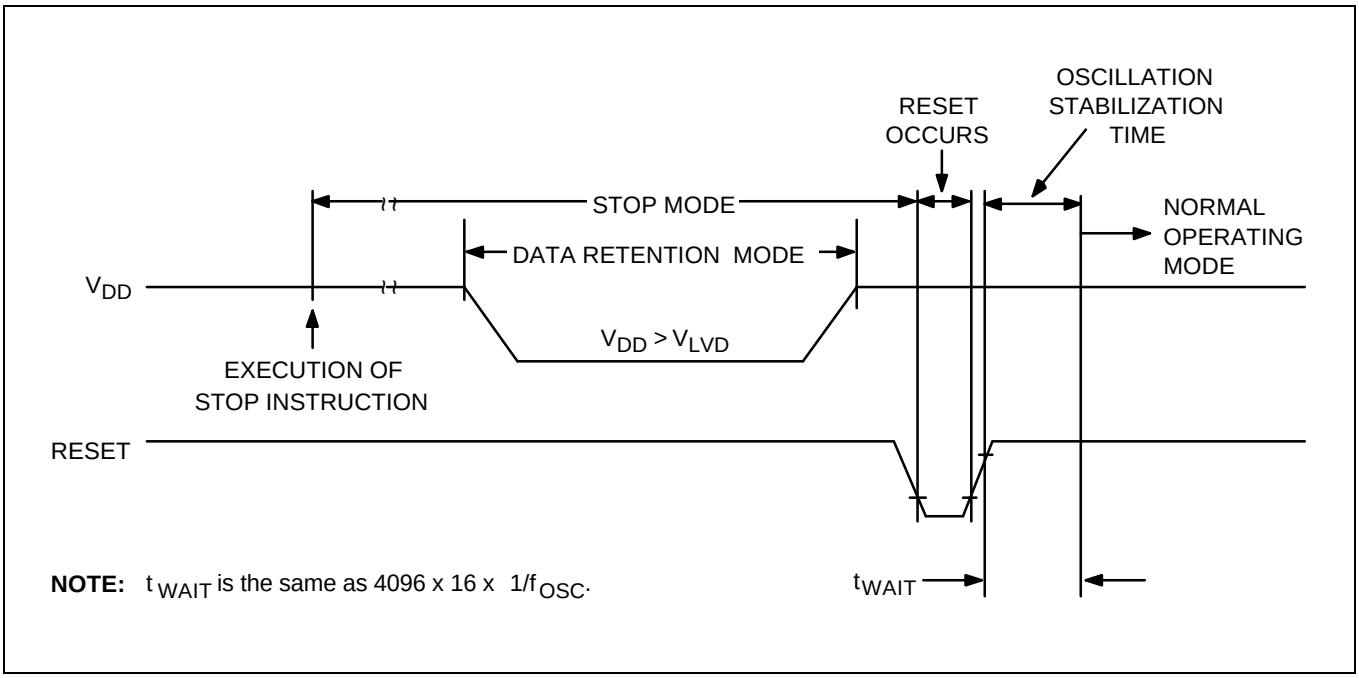


Figure 14-2. Stop Mode Release Timing When Initiated by a RESET

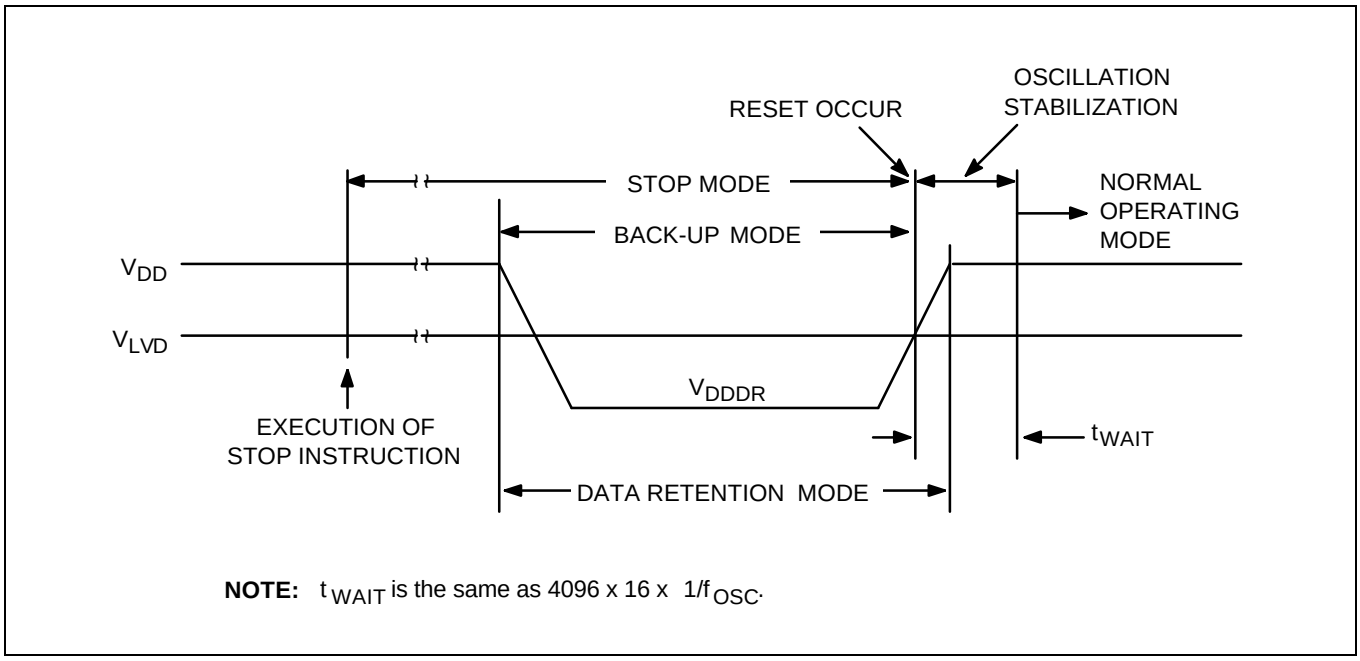


Figure 14-3. Stop Mode Release Timing When Initiated by a LVD

Table 14-5. Input/output Capacitance

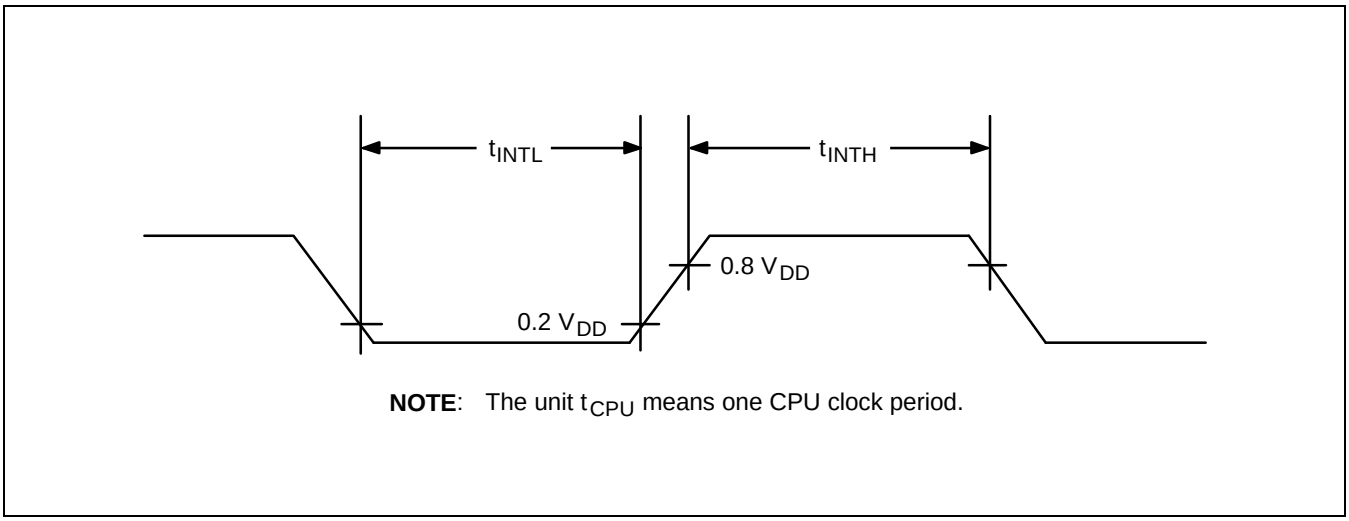
(T_A = – 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 14-6. A.C. Electrical Characteristics

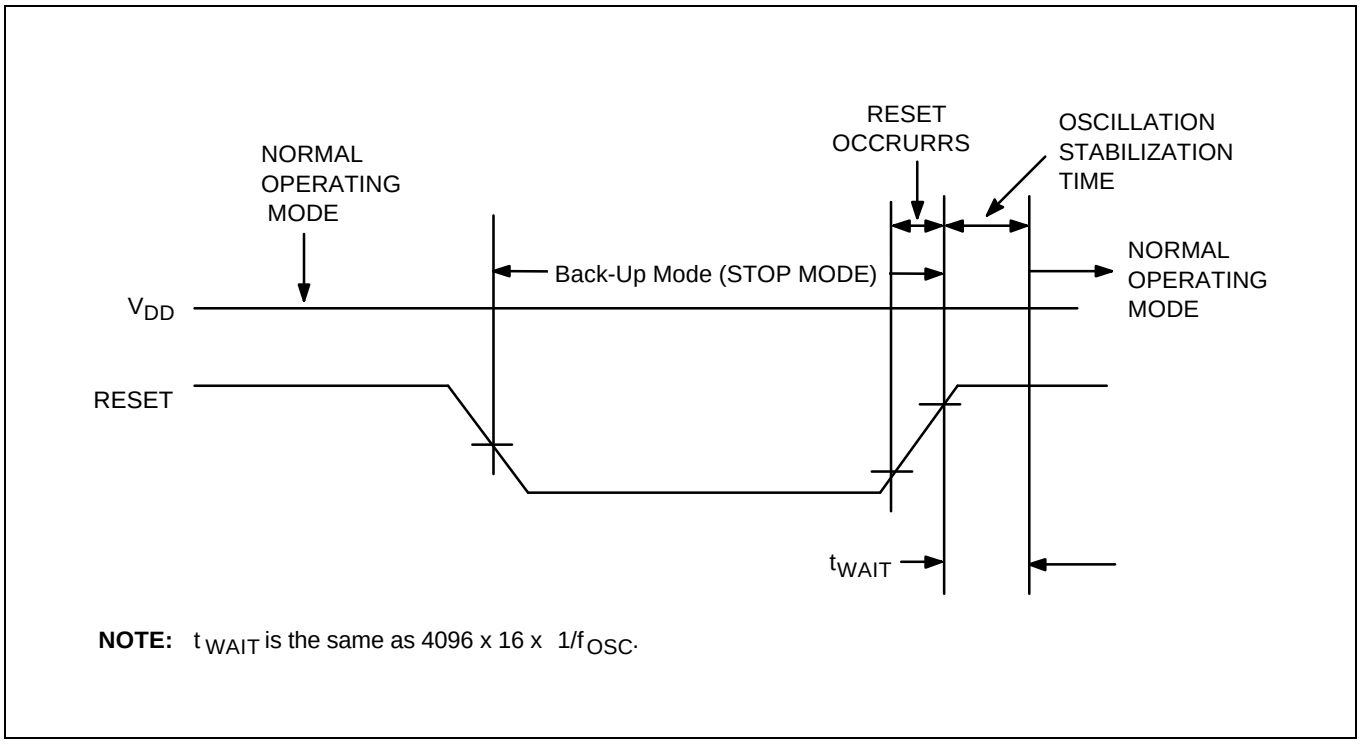
(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	t_{INTH}, t_{INTL}	P0.0–P0.7, P2.3–P2.0 V_{DD} = 5 V	200	300	–	ns
RESET input Low width	t_{RSL}	Input V_{DD} = 5 V	1000	–	–	



NOTE: The unit t_{CPU} means one CPU clock period.

Figure 14-4. Input Timing for External Interrupts (Port 0, P2.3–P2.0)



NOTE: t_{WAIT} is the same as 4096 x 16 x $1/f_{OSC}$.

Figure 14-5. Input Timing for RESET

Table 14-7. Oscillation Characteristics

(T_A = – 40 °C + 85 °C)

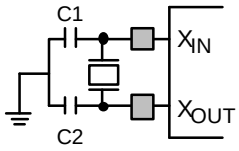
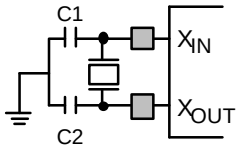
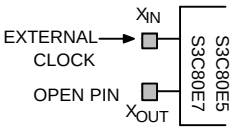
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	–	8	MHz
Ceramic		CPU clock oscillation frequency	1	–	8	MHz
External clock		X_{IN} input frequency	1	–	8	MHz

Table 14-8. Oscillation Stabilization Time

(T_A = – 40 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	f_{OSC} > 400 kHz	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock (main system)	X_{IN} input High and Low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator stabilization Wait time	t_{WAIT} when released by a reset (1)	–	$2^{16}/f_{OSC}$	–	ms
	t_{WAIT} when released by an interrupt (2)	–	–	–	ms

NOTES:
1. f_{OSC} is the oscillator frequency.
2. The duration of the oscillation stabilization time (t_{WAIT}) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

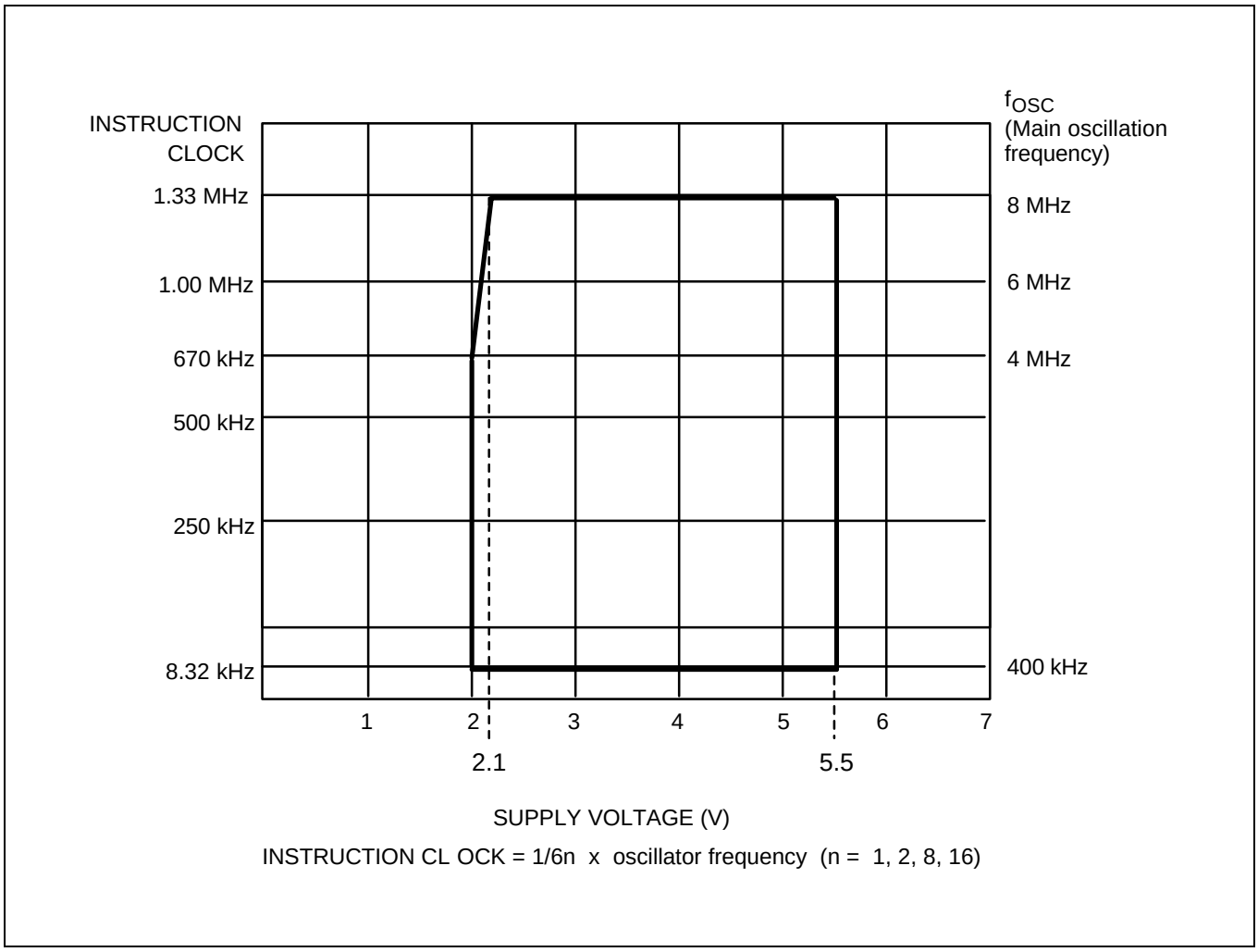
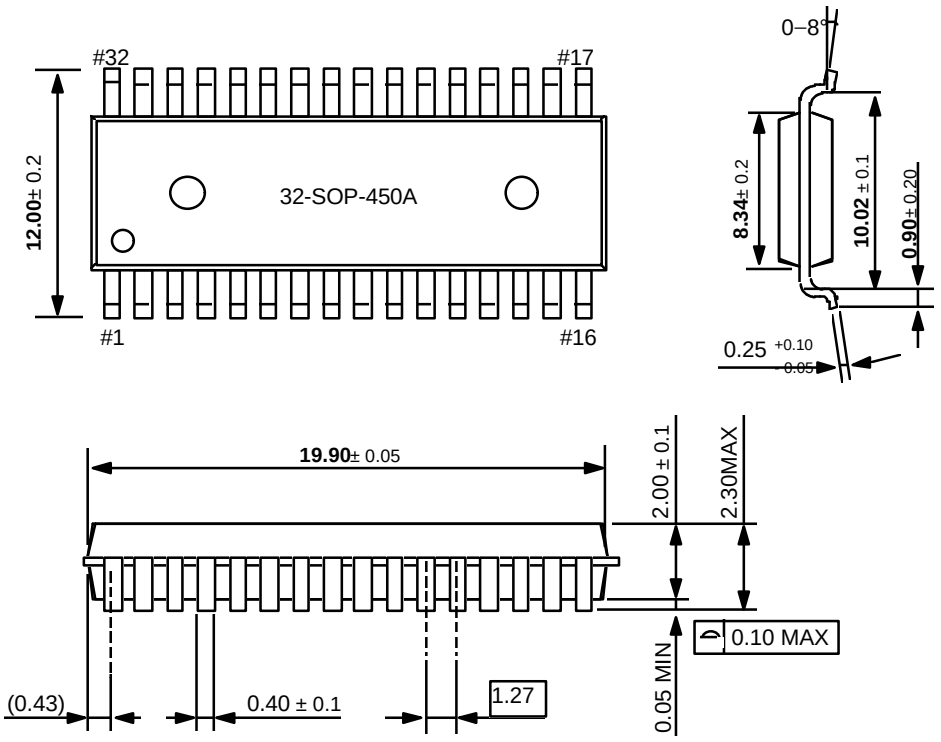


Figure 14-6. Operating Voltage Range of S3P80E5/P80E7

15 MECHANICAL DATA

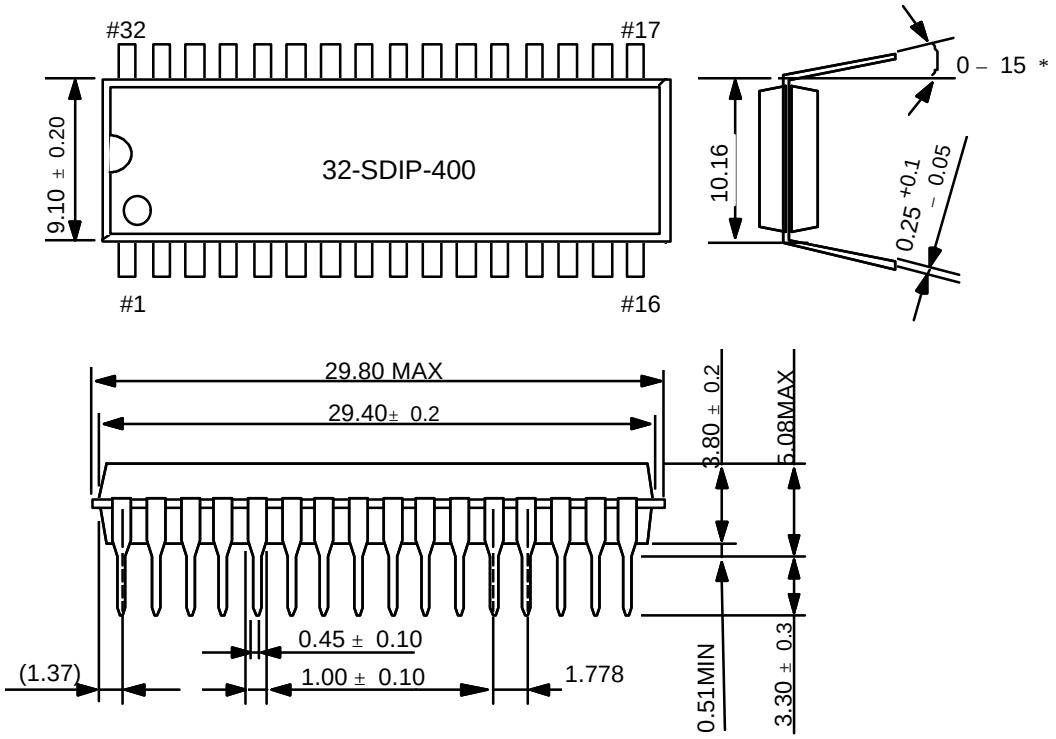
OVERVIEW

The S3C80E5/C80E7 microcontroller is currently available in 32-pin SOP and SDIP package. The S3C80E7 is also available in 40 DIP package.



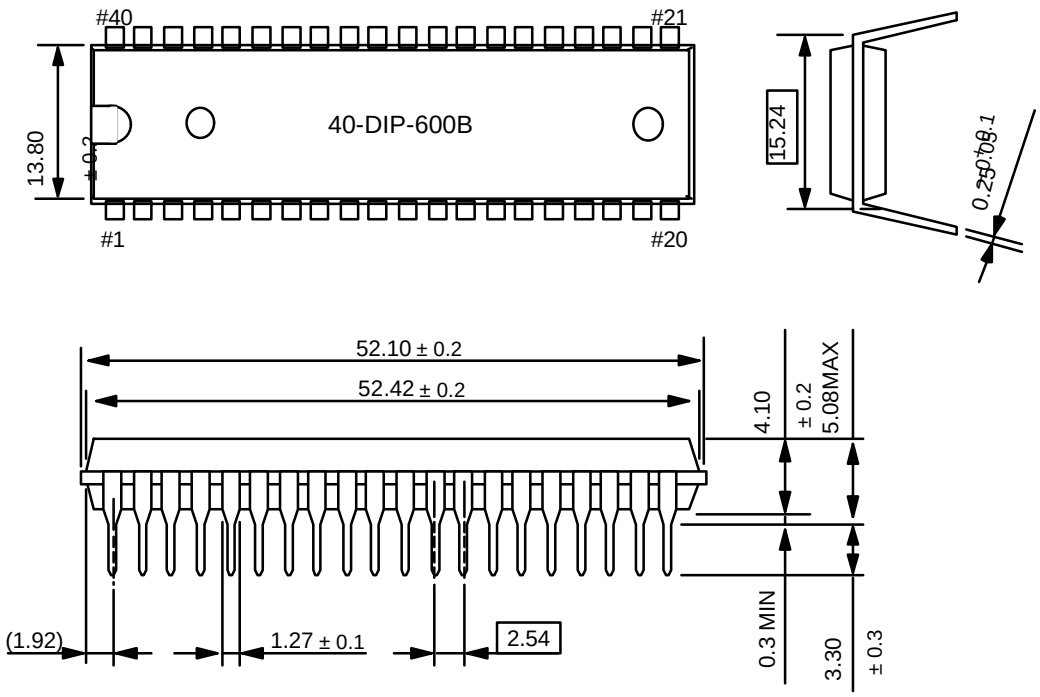
NOTE: Dimensions are in millimeters.

Figure 15-1. 32-Pin SOP Package Mechanical Data



NOTE: Dimensions are in millimeters.

Figure 15-2. 32-Pin SDIP Package Mechanical Data



NOTE: Dimensions are in millimeters.

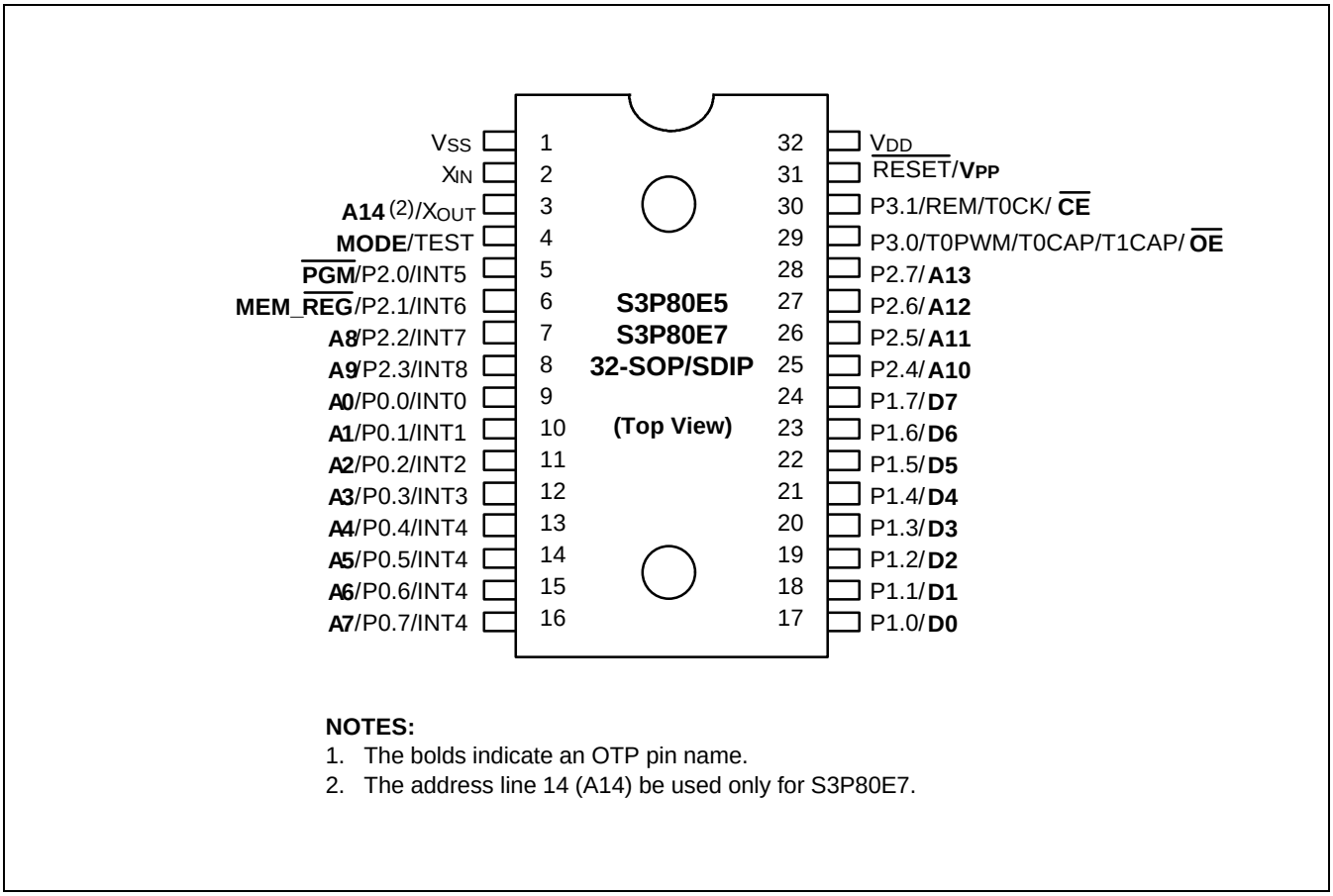
Figure 15-3. 40-Pin DIP Package Mechanical Data

16 S3P80E5/P80E7 OTP

OVERVIEW

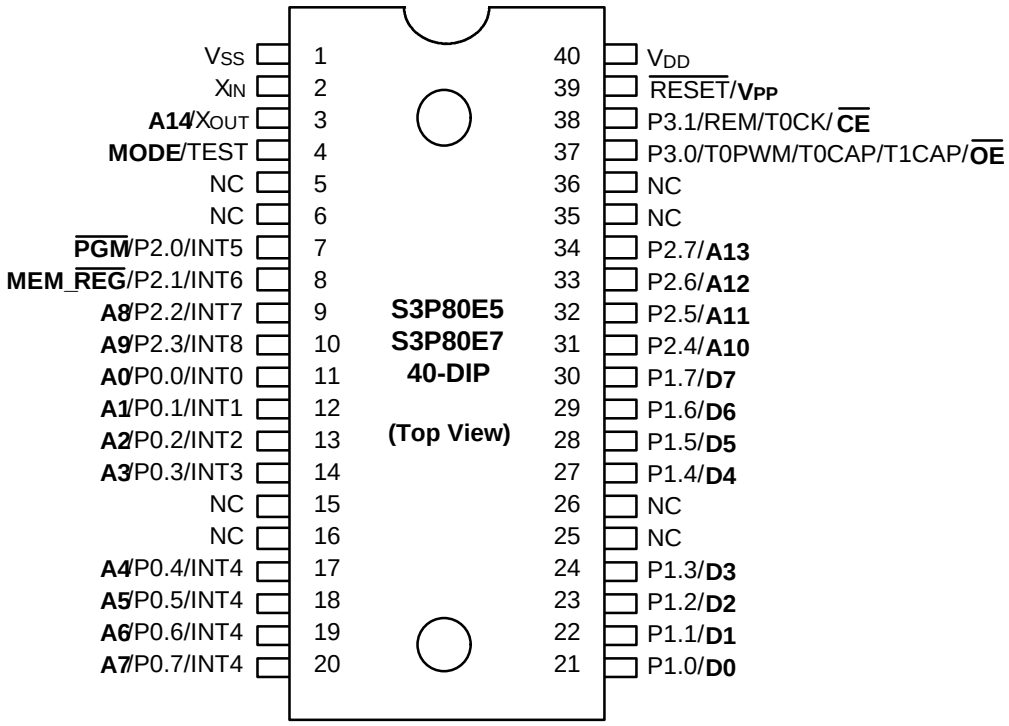
The S3P80E5/P80E7 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C80E5/C80E7microcontroller. It has an on-chip EPROM instead of a masked ROM.

The S3P80E5/P80E7 is fully compatible with the S3C80E5/C80E7, both in function and in pin configuration. Because of its simple programming requirements, the S3P80E5/P80E7 is ideal as an evaluation chip for the S3C80E5/C80E7.



NOTES:
1. The bolds indicate an OTP pin name.
2. The address line 14 (A14) be used only for S3P80E7.

Figure 16-1. S3P80E5/P80E7 Pin Assignments of 32SOP/32SDIP



NOTES:
1. The bolds indicate an OTP pin name.
2. The address line 14 (A14) be used only for S3P80E7.

Figure 16-2. S3P80E5/P80E7 Pin Assignments of 40DIP

Table 16-1. 32 SOP/SDIP Pin Descriptions Used to Read/Write the EPROM

Pin Name	Pin No.	I/O	Function
A0–A14	3, 7– 6, 25–28	O	Address lines to read/write EPROM
D0–D7	17–24	I/O	8-bit data input/output lines to read/write EPROM
MODE	4	–	Select EPROM mode.
CE	30	I	Chip enable (Connect to V_{SS}, when read/write EPROM)
OE	29	I	Output enable
PGM	5	I	EPROM Program enable
MEM_REG	6	I	Select Memory space of EPROM
V_{DD}	32	–	Supply voltage (normally 5 V)
V_{PP}	31	–	EPROM Program/Verify voltage (normally 12.5 V)
V_{SS}	1	–	GROUND
X_{IN}	2	–	System Clock input pin

CHARACTERISTICS OF EPROM OPERATION

When +12.5 V is supplied to V_{PP} and MODE pins of the S3P80E5/P80E7, the EPROM programming mode is entered. The operating mode (read, write) is selected according to the input signals to the pins listed in Table 16-2 as below.

Table 16-2. Operating Mode Selection Criteria

V_{DD}	MODE	V_{PP}	PGM	MEM	OE	Mode
5 V	V_{PP}	12.5 V	1	1	0	READ
			0	1	1	PROGRAM
			1	1	0	PROGRAM VERIFY

NOTE: "0" means Low level; "1" means High level.

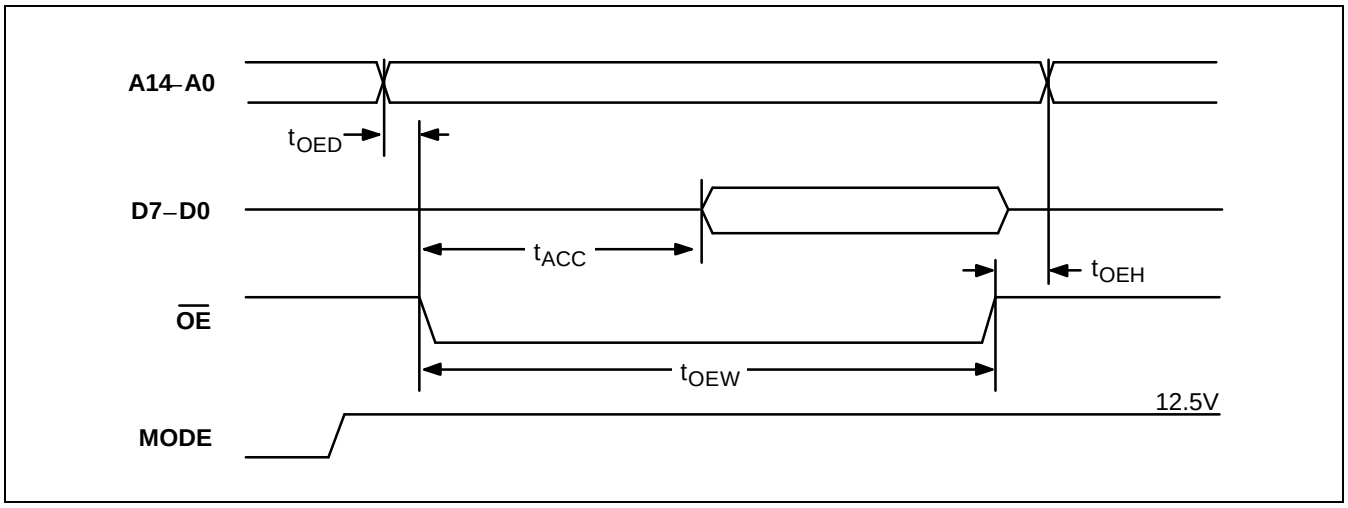


Figure 16-3. OTP Read Timing

Table 16-3. OTP Read Characteristics

(T_A = 25 °C ± 5 °C, V_{DD} = 5 V ± 5 %, V_{PP} = 12.5 V ± 0.25V)

Parameter	Symbol	Min	Typ	Max	Units
Address to Output Delay	t_{ACC}	–	–	75	ns
OE to Address Delay	t_{OED}	0	–	–	
OE Pulse Width	t_{OEW}	75	–	–	
Output hold from OE whichever occurs first	T_{OEH}	0	–	–	

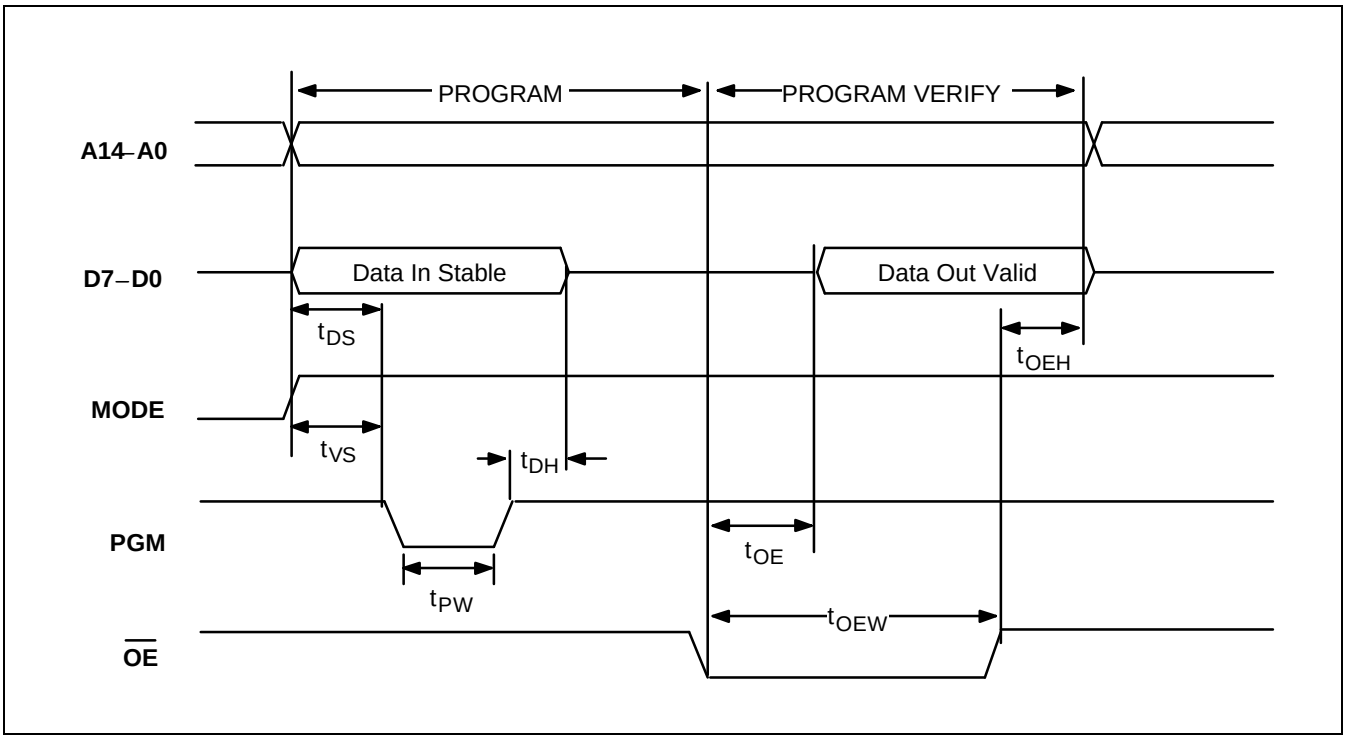


Figure 16-4. Program Memory Write Timing

Table 16-4. OTP Program/Program Verify Characteristics

(T_A = 25 °C ± 5 °C, V_{DD} = 5 V ± 5 %, V_{PP} = 12.5 V ± 0.25 V)

Parameter	Symbol	Min	Typ	Max	Units
V_{PP} Setup Time	t_{VS}	–	2	–	µs
Data Setup Time	t_{DS}	–	2	–	
Data Hold Time	t_{DH}	–	2	–	
PGM Pulse Width	t_{PW}	–	300	500	
Data Valid from OE	t_{OE}	75	–	–	ns
OE Pulse Width	t_{OEW}	75	–	–	
Output Enable to Output Float Delay	t_{OEH}	0	–	130	

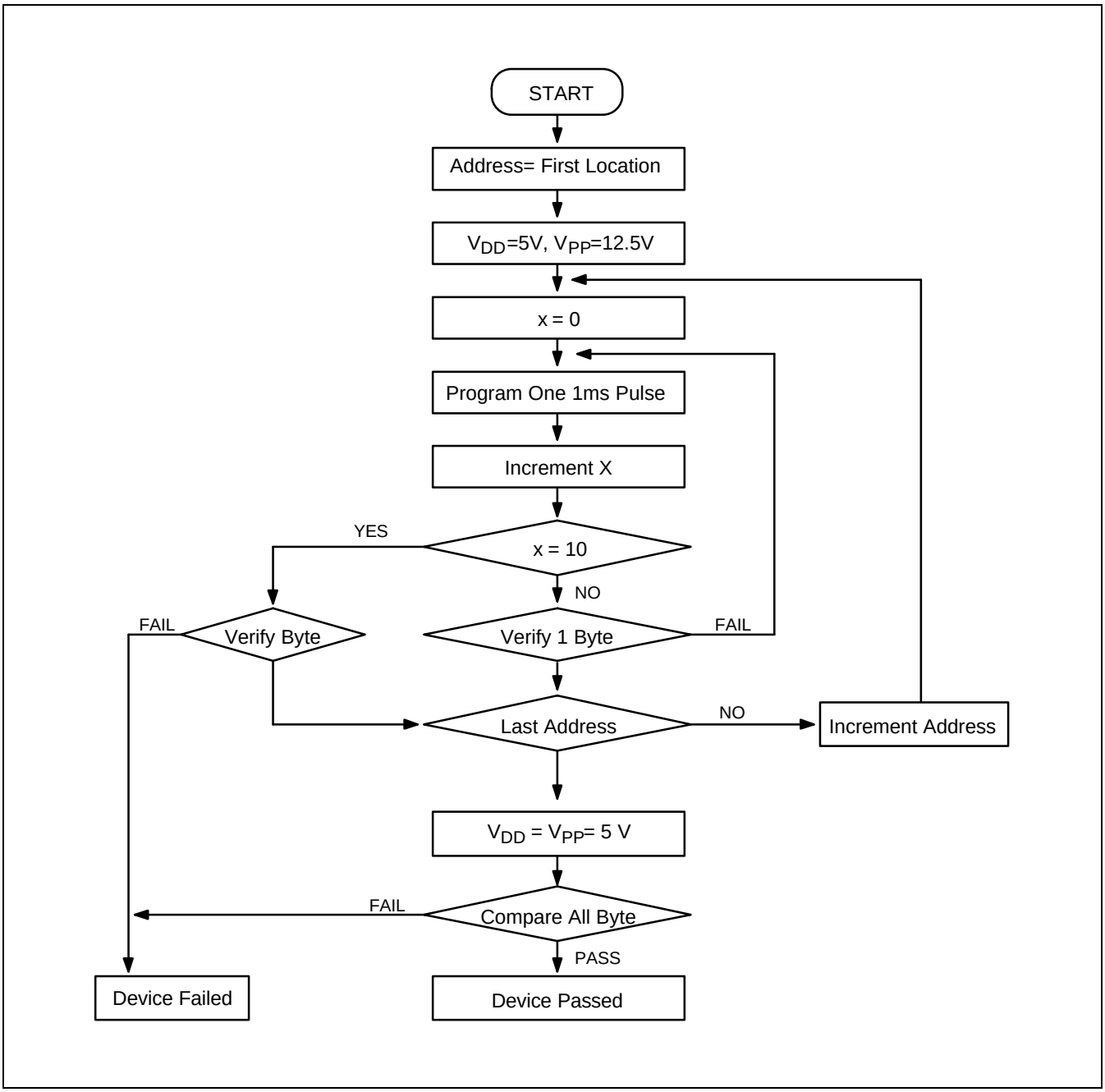


Figure 16-5. OTP Programming Algorithm

Table 16-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 8 MHz (Instruction clock = 1.33 MHz)	2.1	–	5.5	V
		f_{OSC} = 4 MHz (Instruction clock = 0.67 MHz)	2.0	–	5.5	
Input High voltage	V_{IH1}	All input pins except V_{IH2} and V_{IH3}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	RESET	0.85 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}	V_{DD} – 0.3		V_{DD}	
Input Low voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	0	–	0.2 V_{DD}	V
	V_{IL2}	RESET			0.4 V_{DD}	
	V_{IL3}	X_{IN}			0.3	
Output High voltage	V_{OH1}	V_{DD} = 2.4 V; I_{OH} = – 6 Ma Port 3.1 only; T_A = 25 °C	V_{DD} – 0.7	–	–	V
	V_{OH2}	V_{DD} = 2.4 V; I_{OH} = – 3 mA Port 3.0 only; T_A = 25 °C	V_{DD} – 0.7			
Output High voltage	V_{OH3}	V_{DD} = 5 V; I_{OH} = – 3 mA Port 2.7 only; T_A = 25 °C	V_{DD} – 0.25	–	–	V
		V_{DD} = 2 V; I_{OH} = – 1 mA Port 2.7 only; T_A = 25 °C				
	V_{OH4}	V_{DD} = 3.0 V; I_{OH} = – 1 mA All output pins except P3 and P2.7 port; T_A = 25 °C	V_{DD} – 1			
Output Low voltage	V_{OL1}	V_{DD} = 2.4 V; I_{OL} = 15 mA Port 3.1 only; T_A = 25 °C	–	0.4	0.5	V
	V_{OL2}	V_{DD} = 2.4 V; I_{OL} = 5 mA Port 3.0 only; T_A = 25 °C		0.4	0.5	
	V_{OL3}	I_{OL} = 1 mA Port 0, 1, and 2; T_A = 25 °C		0.4	1	
Input High leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and X_{OUT}	–	–	1	µA
	I_{LIH2}	V_{IN} = V_{DD}, X_{IN}, and X_{OUT}			20	

Table 16-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, and RESET	–	–	– 1	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN} and X_{OUT}			– 20	
Output High leakage current	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	1	µA
Output Low leakage current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 1	µA
Pull-up resistors	R_{L1}	V_{IN} = 0 V; V_{DD} = 2.4 V T_A = 25 °C; Ports 0–3	44	55	82	kΩ
		V_{DD} = 5.5 V	15	21	32	
Supply current (note)	I_{DD1}	Operating mode V_{DD} = 5 V ± 10 % 8 MHz crystal	–	6	11	mA
		4 MHz crystal		4.5	9	
	I_{DD2}	Idle mode V_{DD} = 5 V ± 10 % 8 MHz crystal		1.8	3.5	
		4 MHz crystal		1.6	3	
	I_{DD3}	Stop mode; V_{DD} = 6.0 V		20	35	µA
		V_{DD} = 5.5 V		18	25	
		V_{DD} = 3.3 V		12	15	
		V_{DD} = 0.7 V		1.0	1.5	

NOTE: Supply current does not include the current drawn through internal pull-up resistors or external output current loads.

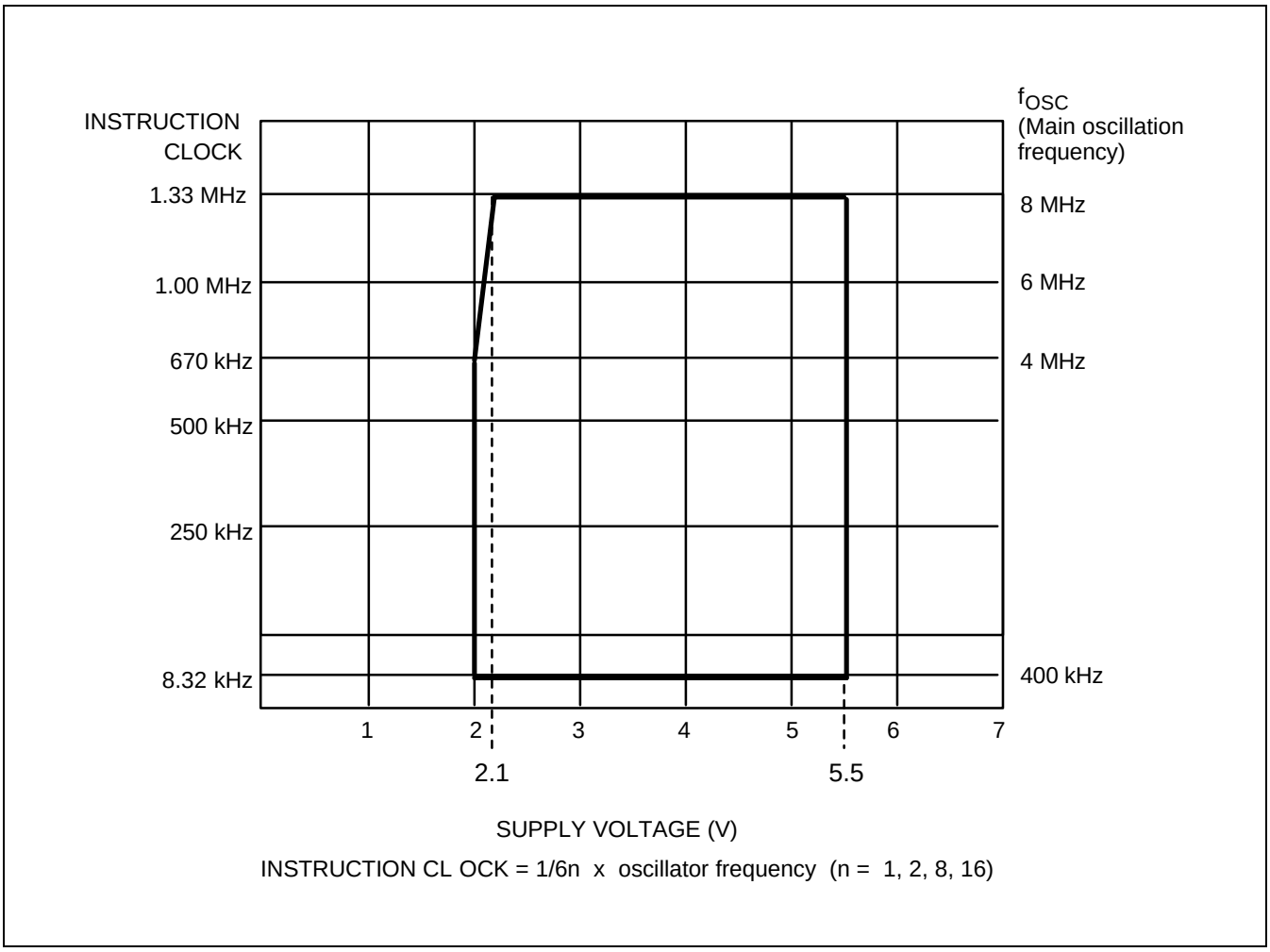


Figure 16-6. Operating Voltage Range