UM91531

Parallel Input Tone/Pulse Dialer

Features

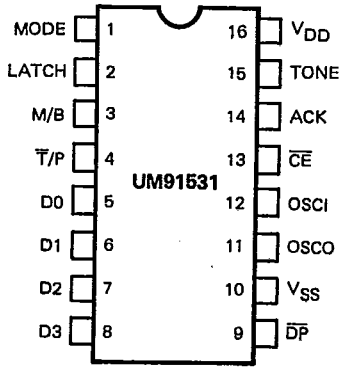
- 4-bit parallel data input from microcomputer
- TTL compatible inputs and outputs
- Uses TV crystal standard (3.58 MHz) to derive all frequencies thus providing high accuracy and stability
- Low total harmonic distortion for DTMF signaling
- Operating voltage 2.5 to 5.5 volts
- M/B ratio is selectable
- 10PPS Dial rate
- DTMF signaling of 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #, A, B, C and D
- Pulse signaling 0-E
- High group tone pre-emphasis: 2dB
- RS-470 and CEPT compatible

General Description

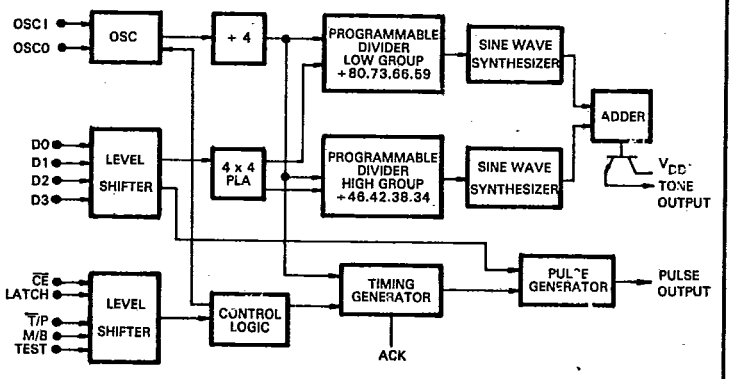
The UM91531 provides 4 bit data input and handshaking signal to serve as an interface with the microcomputer. Under the microcomputer control, UM91531 generates both DTMF signal and PULSE output to make a telephone number dialihg. All necessary dual-tone frequencies and dial pulse output are derived from the widely used TV crystal standard, providing high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform thus generated has little total harmonic distortion.

Slave Dialer

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... −0.3V to +5.5V

Operating Temperature (T_{OP}) ..... −20°C to +60°C

Storage Temperature (T_{stg}) ..... −55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(V_{SS} = 0V, V_{DD} = 3.5V, Fx'tal = 3.579545 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Voltage	V_{DD}	2.5		5.5	V	
Standby Current	I_{DD}			10	μA	V_{DD} = 5.0V, $\overline{CE}$ = V_{DD}
Operating Current	I_{DD}			2.5	mA	V_{DD} = 5.0V, $\overline{CE}$ = V_{SS} All Outputs Not Loaded
Row Tone Output	V_R		95		mVrms	V_{DD} = 2.5V, RL = 2.2K Ohm
			190		mVrms	V_{DD} = 5.0V, RL = 2.2K Ohm
Column Tone Output	V_C		120		mVrms	V_{DD} = 2.5V, RL = 2.2K Ohm
			240		mVrms	V_{DD} = 5.0V, RL = 2.2K Ohm
D0, D1, D2, D3, T/P, M/B, LATCH, $\overline{CE}$	THESE PINS ARE TTL COMPATIBLE I/O					
Input High Voltage	V_{IH}	2.4		5.0	V	V_{DD} = 5.0V
Input Low Voltage	V_{IL}			0.4	V	V_{DD} = 5.0V
Input High Current	I_{IH}		0.05		μA	
Input Low Current	I_{IL}		−0.05		μA	
MODE Pull Up Resistance	R_M	40			K Ohm	V_{DD} = 2.5V
		20			K Ohm	V_{DD} = 5.0V
$\overline{DP}$ Sink Current	I_{OLDP}	1			mA	V_{DD} = 2.5V, $V_{\overline{DP}}$ = 0.4V
		3			mA	V_{DD} = 5.0V, $V_{\overline{DP}}$ = 0.4V
$\overline{DP}$ Off Current	I_{LKG}		0.001		μA	V_{DD} = 5.0V, $V_{\overline{DP}}$ = 5.0V
ACK Source Current	I_{OHACK}	1.6			mA	V_{DD} = 5.0V, V_{ACK} = 2.4V
ACK Sink Current	I_{OLACK}	4.0			mA	V_{DD} = 5.0V, V_{ACK} = 0.4V
Oscillator Start Up Time	t_{START}			5	mS	

Table 1. Input data vs. Output Signaling

D3	D2	D1	D0	DTMF Signaling	PULSE Signal (O/P Pulse No.)
0	0	0	0	0	10
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	*	10
1	0	1	1	#	11
1	1	0	0	A	12
1	1	0	1	B	13
1	1	1	0	C	14
1	1	1	1	D	Forbidden input

Table 2. Comparisons of Specified vs. Actual Tone Frequencies Generated by UM91531

Active Input	Output Frequency Hz		% Error*
	Specified	Actual	
R1	697	699.1	+0.30
R2	770	766.2	–0.49
R3	852	847.4	–0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	–0.32
C3	1,477	1,471.9	–0.35
C4	1,633	1,645.0	+0.73

*Note: % error does not include oscillator drift.

Pin Description

4-bit Parallel Input (D0, D1, D2, D3)

These 4 bit parallel input data are generated by the microcomputer. The input data versus output signal is shown in Table 1. The valid input data should be presented at these inputs before and during the rising edge of the LATCH signal.

LATCH

UM91531 latches the 4-bit input data and $\overline{T}/P$ input when the LATCH signal goes from low to high (at the rising edge). The LATCH input must not change from high to low immediately until ACK output falls low. Also, a new data must not be latched when the ACK output is low.

Acknowledge (ACK)

This pin provides an acknowledge signal to the microcomputer. This output is high when UM91531 is ready to dial out the next digit. And this output falls low immediately after the rising edge of the LATCH signal.

Tone/Pulse Switch ($\overline{T}/P$)

This input determines whether pulse dialing or DTMF dialing should be implemented. And it is latched together with the 4-bit data.

Make/Break Ratio (M/B)

The M/B input selects the two make/break ratio available. A high input selects the M/B ratio of 2/3 and a low input selects the M/B ratio of 1/2. The M/B input is to be connected to V_{DD} or V_{SS} only. Changing state when $\overline{CE}$ is active (low) would enable the test mode.

Output Mode (MODE)

This input affects the tone output mode only. The tone output and ACK output remain normal when this input is high. An input low will force this circuit generating continuously the DTMF signaling and that being output and the new input data will be ignored.

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ (chip enable) input controls the onset of oscillation, and serves as the master reset of this device.

Dial Pulse Output ($\overline{DP}$)

This dial pulse output stage consists of an N-channel open drain device. During dial pulse BREAK periods the output device is switched on (sinking current to V_{SS}) and is switched off during the other states. The DPR (dial pulse rate) is 9.71 PPS and the PDP (post digit pause) is 823 ms. The output of this pin at TEST mode will be discussed later.

Tone Output (TONE)

This pin consists of an npn transistor output whose collector is connected to V_{DD} and this pin is connected to the emitter output. The internally generated DTMF signaling is delivered to the base of the npn transistor and is amplified as the transistor connected in common collector or darlington output forms. The DTMF signaling output time is 70 ms and the inter-digit interval is 70 ms. The output impedance of the DTMF signaling is typically 1.25K Ohm, and the h_{FE} of the npn transistor is at least 30 at Ic = 3mA.

Oscillator (OSCI, OSCO)

UM91531 contains an oscillator circuit with the necessary parasitic capacitance and feedback resistor on chip so that it is only necessary to connect a standard 3.58 MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. An external clock input can be applied to the OSCI pin directly. The Oscillator is enabled when $\overline{CE}$ input low.

Power (V_{DD}, V_{SS})

These are the power supply input. The UM91531 is designed to operate from 2.5 to 5.5 Volts.

Test Mode

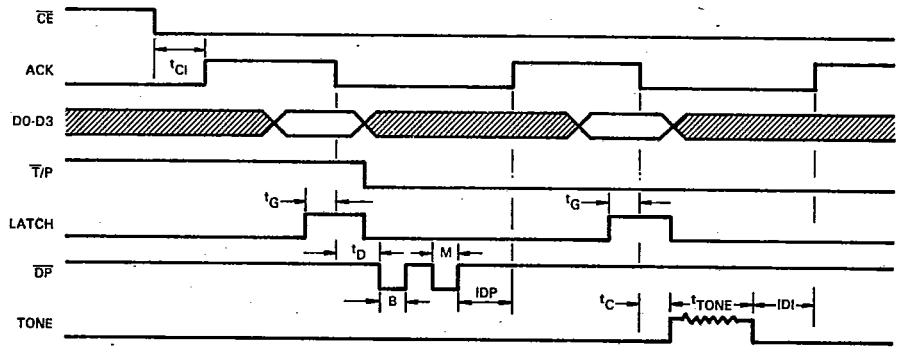
The UM91531 provides high speed PULSE/TONE output for testing consideration. If the M/B input changes state after chip is enabled, the test mode is initiated and UM91531 will stay in test mode unless chip is disabled. Table 3 shows the input data versus the output signal at PULSE/TONE test mode.

Table 3. Input Data vs. Output Signal at PULSE/TONE Test Mode

D3, D2, D1, D0 Input In Hex Code	Tone O/P Frequencies and Test Mode		Pulse O/P Frequencies and Test Mode
	Tone Pin O/P	$\overline{DP}$ Pin O/P	$\overline{DP}$ Pin O/P
0	948.0	1,331.7 x 8	10 x 48
1	699.1	1,215.9 x 8	1 x 48
2	1,331.7	699.1 x 8	2 x 48
3	1,417.9	699.1 x 8	3 x 48
4	1,215.9	766.2 x 8	4 x 48
5	1,331.7	766.2 x 8	5 x 48
6	766.2	1,471.9 x 8	6 x 48
7	847.4	1,215.9 x 8	7 x 48
8	1,331.7	847.4 x 8	8 x 48
9	1,471.9	847.4 x 8	9 x 48
A	1,215.9	948.0 x 8	10 x 48
B	1,471.9	948.0 x 8	11 x 48
C	1,645.0	699.1 x 8	12 x 48
D	1,645.0	766.2 x 8	13 x 48
E	1,645.0	847.4 x 8	14 x 48
F	1,645.0	948.0 x 8	0

Note: Tone Pin O/P in sine wave, $\overline{DP}$ Pin O/P in square ware. The normal timing is reduced to 1/8 at tone test mode and 1/48 at pulse test mode.

Timing Diagram



t_{CI}: Circuit initial time 5 ms
t_G: Two gate delay time
t_D: Typical 15 ms
t_C: Typical 70 us

t_{TONE}: 70 ms
IDP : 823 ms
IDI : 70 ms
B/M : Break/Make