M34550Mx-XXXFP

SINGLE-CHIP CMOS MICROCOMPUTER for INFRARED REMOTE CONTROL TRANSMITTER

OUTLINE

The M34550Mx-XXXFP is a 4-bit one chip microcomputer designed with CMOS technology for remote controller. It's core CPU is an enhanced version of the MELPS 720 which has a simple and high-speed instruction set. It has a built-in remote control carrier wave output circuit and an LCD control circuit and is suitable for remote control transmitters designed for VCR_S and air conditioners.

The M34550Mx-XXXFP family has several models with different built-in memory size. An internal PROM version is also available.

APPLICATION

Various remote control transmitters

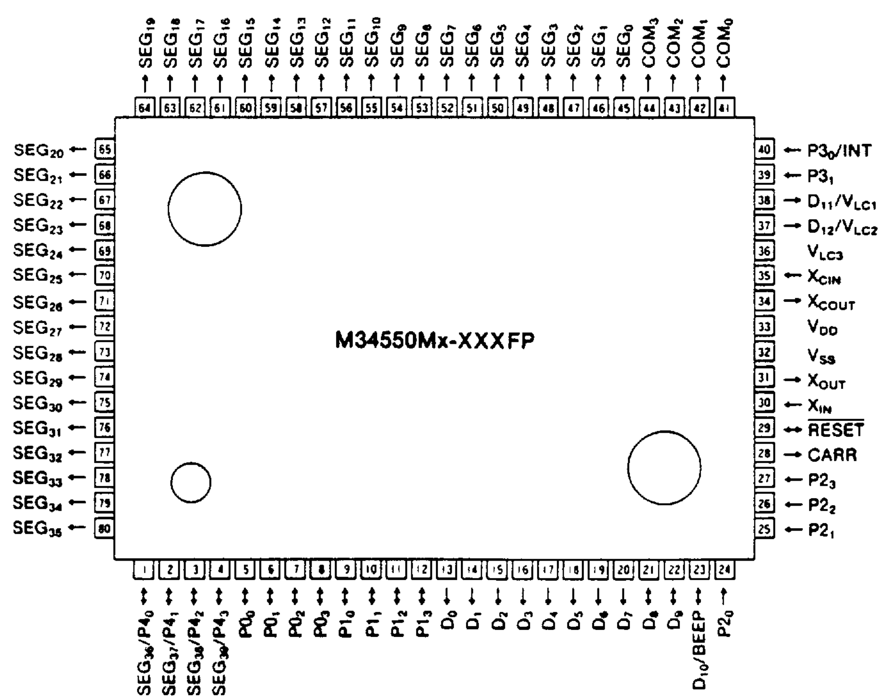
DISTINCTIVE FEATURES

- Number of basic instructions ········ 100
- Instruction execution time ········ 3.3μs
  (shortest instruction at 910kHz oscillating frequency)
- Supply voltage ········ 2.2V to 3.6V
- Timer
  Timer 1 ········ 9-bit timer with reload register
  Timer 2 ········ 4-bit×2
  Timer 3 ········ 8-bit timer with reload register
- Interrupt function ········ 3 sources
- Clock generating circuit ········ Built-in 2 circuits
- Remote control carrier wave output function
- Built-in LCD controller/driver
  Segment output ········ 40
  Common output ········ 4

Type name	ROM (PROM) size (×10 bits)	ROM size (×4 bits)	Package	ROM characteristics
M34550M6-XXXFP	6144 words	368 words	80P6N	Mask ROM
M34550M8-XXXFP	8192 words			
M34550E8-XXXFP ★★				One-time PROM
M34550E8FS ★★			80D0	EPROM

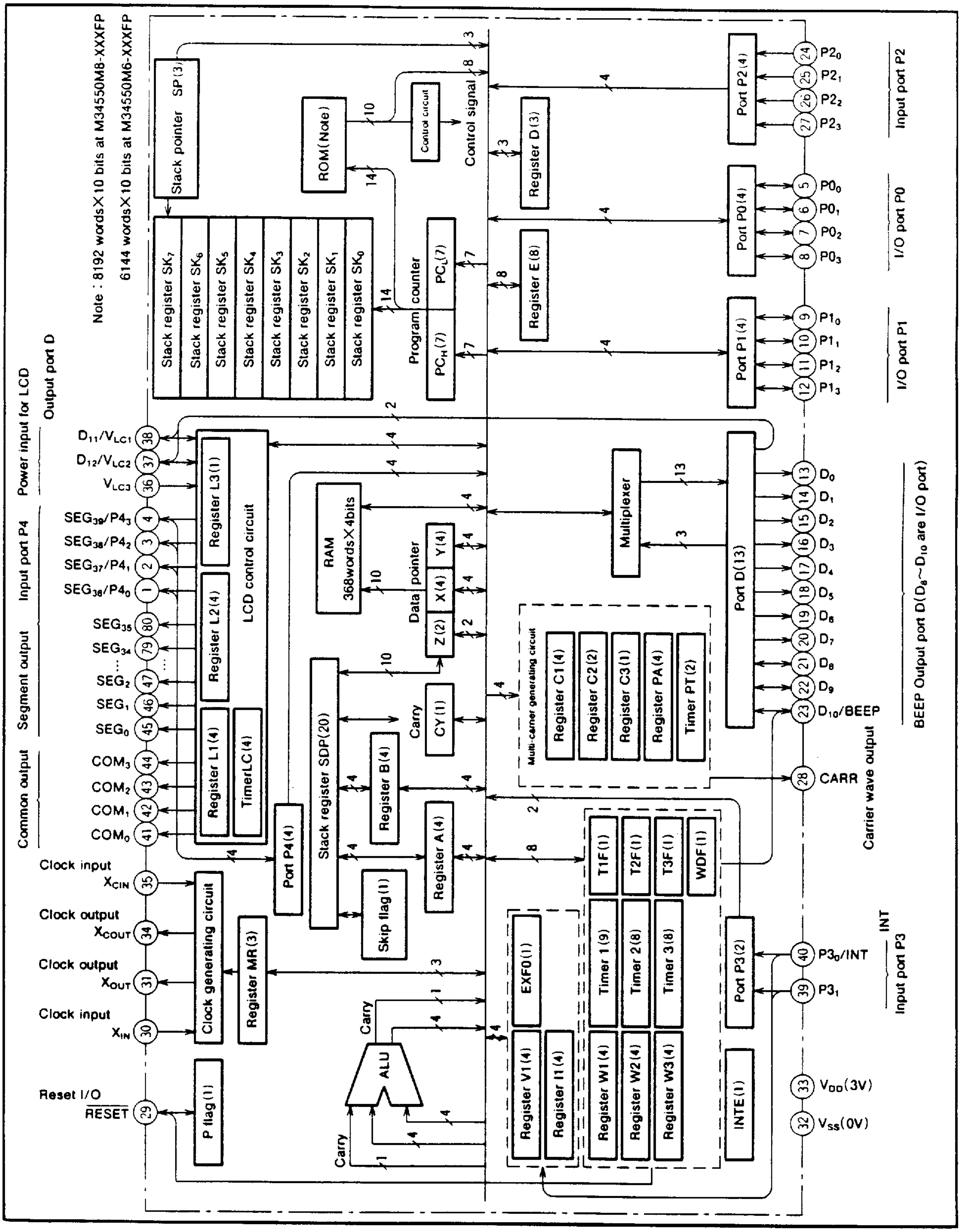
★★ : Under development

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

BLOCK DIAGRAM



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PERFORMANCE OVERVIEW

Parameter			Functions
Number of basic instructions			100
Instruction execution time			3.3μs (shortest instruction at 910kHz clock frequency)
Clock	Main clock frequency		910kHz
	Sub-clock frequency		32kHz
Memory size	ROM	M34550M6	6144 words×10 bits
		M34550M8	8192 words×10 bits
	RAM		368 words×4 bits (including 40 words×4 bits for LCD RAM)
Input/Output pins	D_0~D_7 D_{11}, D_{12}	Output	1 bits×10 D_{11} pin is shared with power supply input pin V_{LC1} for LCD and D_{12} pin is shared with power input pin V_{LC2} for LCD.
	D_8~D_{10}	I/O	1 bits×3 D_{10} pin is shared with buzzer output pin BEEP.
	$P0_0$~$P0_3$	I/O	4 bits×1, Built-in pull-up transistor Key-on wakeup function
	$P1_0$~$P1_3$	I/O	4 bits×1, Built-in pull-up transistor Key-on wakeup function
	$P2_0$~$P2_3$	Input	4 bits×1 Pins $P2_0$ and $P2_1$ have each key-on wakeup function.
	$P3_0$, $P3_1$	Input	2 bits×1 Built-in programmable pull-up transistor $P3_0$ pin is shared with interrupt input INT and has a key-on wakeup function
	$P4_0$~$P4_3$	Input	4 bits×1 Switched with pins SEG_{36}~SEG_{39} by software
Remote control carrier wave output			Variable period carrier wave output (software carrier output enabled)
Timer	Timer 1		9-bit programmable timer with reload register
	Timer 2		4-bit fixed dividing frequency ×2
	Timer 3		8-bit programmable timer with reload register
Interrupts	Sources		3 sources (both edges sense external ×1, timer ×2)
	Nesting		1 level
Subroutine nesting			8 level
LCD	Selected bias value		1/2, 1/3 bias
	Selected duty value		2, 3, 4 duty
	Common output		4
	Segment output		40
	Internal resistance for power supply		200kΩ (Typical) ×3
Device structure			CMOS silicon gate process
Package			80 pin plastic molded QFP
Operating temperature range			−20℃~70℃
Supply voltage			2.2V~3.6V
Dissipation current	at operation		1mA (at 910kHz clock frequency, Typical)
	at clock operation		4μA (at 32kHz clock frequency, Typical)
	at stop		Less than 0.1μA (Normal temperature, Typical)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{DD}	Power supply	—	This pin is connected to plus power supply.
V_{SS}	Ground	—	This pin is connected to 0V power supply.
$\overline{RESET}$	Reset I/O	I/O	$\overline{RESET}$ pin is the I/O pin of the reset pulse. "L" level is output when reset is occurred by the watchdog timer. The output format is N channel open drain.
X_{IN}	Main clock input	Input	Pins X_{IN} and X_{OUT} are the main clock generating circuit I/O pins. A ceramic oscillator is connected between X_{IN} pin and X_{OUT} pin. A feedback resistance is built-in between X_{IN} pin and X_{OUT} pin.
X_{OUT}	Main clock output	Output	
X_{CIN}	Sub-clock input	Input	Pins X_{CIN} and X_{COUT} are the sub-clock generating circuit I/O pins. A 32kHz crystal oscillator is connected between X_{CIN} pin and X_{COUT} pin. A feedback resistance is built-in between X_{CIN} pin and X_{COUT} pin.
X_{COUT}	Sub-clock output	Output	
D_0~D_7 D_{11}/V_{LC1} D_{12}/V_{LC2}	Output port D	Output	Output port D has a 1-bit unit output function. D_{11} pin is shared with power supply input pin V_{LC1} for LCD and D_{12} pin is shared with power input pin V_{LC2} for LCD.
D_8~D_{10}	I/O port D	I/O	I/O port D has a 1-bit unit I/O function. Input is enabled when the output latch is set to "1". D_{10} pin is shared with the buzzer output pin BEEP.
$P0_0$~$P0_3$	I/O port P0	I/O	I/O ports P0 and P1 have each 4-bit unit I/O function. Input is enabled when the output latch is set to "1". Each pin has a key-on wakeup function and has a built-in pull-up transistor.
$P1_0$~$P1_3$	I/O port P1		
$P2_0$~$P2_3$	Input port P2	Input	Input port P2 has a 4-bit unit input function. Pins $P2_0$ and $P2_1$ have each key-on wakeup function.
$P3_0$/INT $P3_1$	Input port P3	Input	Input port P3 has a 2-bit unit input function. Each pin has a built-in pull-up transistor that can be turned on/off by software. $P3_0$ pin is shared with both edges sense (rising edge and falling edge) interrupt input pin INT. $P3_0$ pin has a key-on wakeup function which can be switched between "H" and "L" level sense by software.
$SEG_{36}/P4_0$ ~$SEG_{39}/P4_3$	Input port P4	Input	Input port P4 has a 4-bit unit input function. These pins are shared with pins SEG_{36}~SEG_{39} and are set by software.
CARR	Carrier output	Output	CARR pin is the remote control carrier wave output pin. C4 flag (1 bit) can be output in addition to hardware carrier method using a dedicated hardware.
V_{LC1}~V_{LC3}	Power input for LCD	Input	Pins V_{LC1}~V_{LC3} are the power supply input pin for LCD. Connect V_{LC3} pin to V_{DD} pin when using an internal resistance and connect through a resistance if brightness adjustment is necessary. Apply voltage such that $0 \leq V_{LC1} \leq V_{LC2} \leq V_{LC3} \leq V_{DD}$ when using an external power.
SEG_0~SEG_{39}	Segment output	Output	Pins SEG_0~SEG_{39} are the LCD segment output pin.
COM_0~COM_3	Common output	Output	Pins COM_0~COM_3 are the LCD common output pin. Pins COM_0~COM_1 are used at 1/2 duty, pins COM_0~COM_2 are used at 1/3 duty, and pins COM_0~COM_3 are used at 1/4 duty.

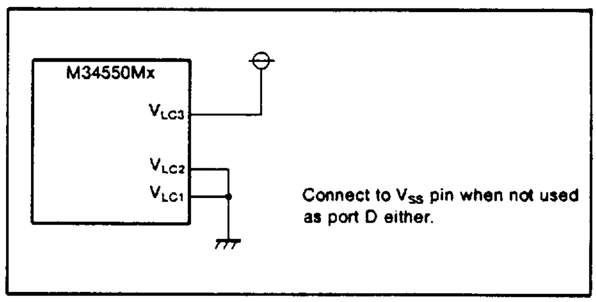
SETTING OF UNUSED PINS

Pin	Setting	Pin	Setting
X_{OUT}	Open (when selecting an external clock)	$P2_0$~$P2_3$	Connect to V_{SS}
X_{CIN}	Connect to V_{SS}	$P3_0$~$P3_1$	Connect to V_{DD}
X_{COUT}	Open	$SEG_{36}/P4_0$~ $SEG_{39}/P4_3$	When selecting port P4 function, connect to V_{SS} When selecting SEG pin function, open (Note 1)
D_0~D_7, D_{11}/V_{LC1}, D_{12}/V_{LC2}	Connect to V_{SS} (Note 2)	CARR	Open
		V_{LC3}	When not using LCD Connect to V_{DD} (Note 3)
D_8~D_{10}	Connect to V_{SS}		
$P0_0$~$P0_3$	Open	SEG_0~SEG_{35}	Open
$P1_0$~$P1_3$	Open	COM_0~COM_3	Open

Notes : 1. The SEG pin function is selected at reset.

2. Pins D_{11} and D_{12} are shared with pins V_{LC1} and V_{LC2} respectively. When not used, set the LCD control register (L3) to "0_2" and disconnect from the internal LCD power supply (L3="0_2" at reset).

3. When LCD is not used, set the LCD control register (L1) to "0000_2" and turn off the LCD (L1="0000_2" at reset).

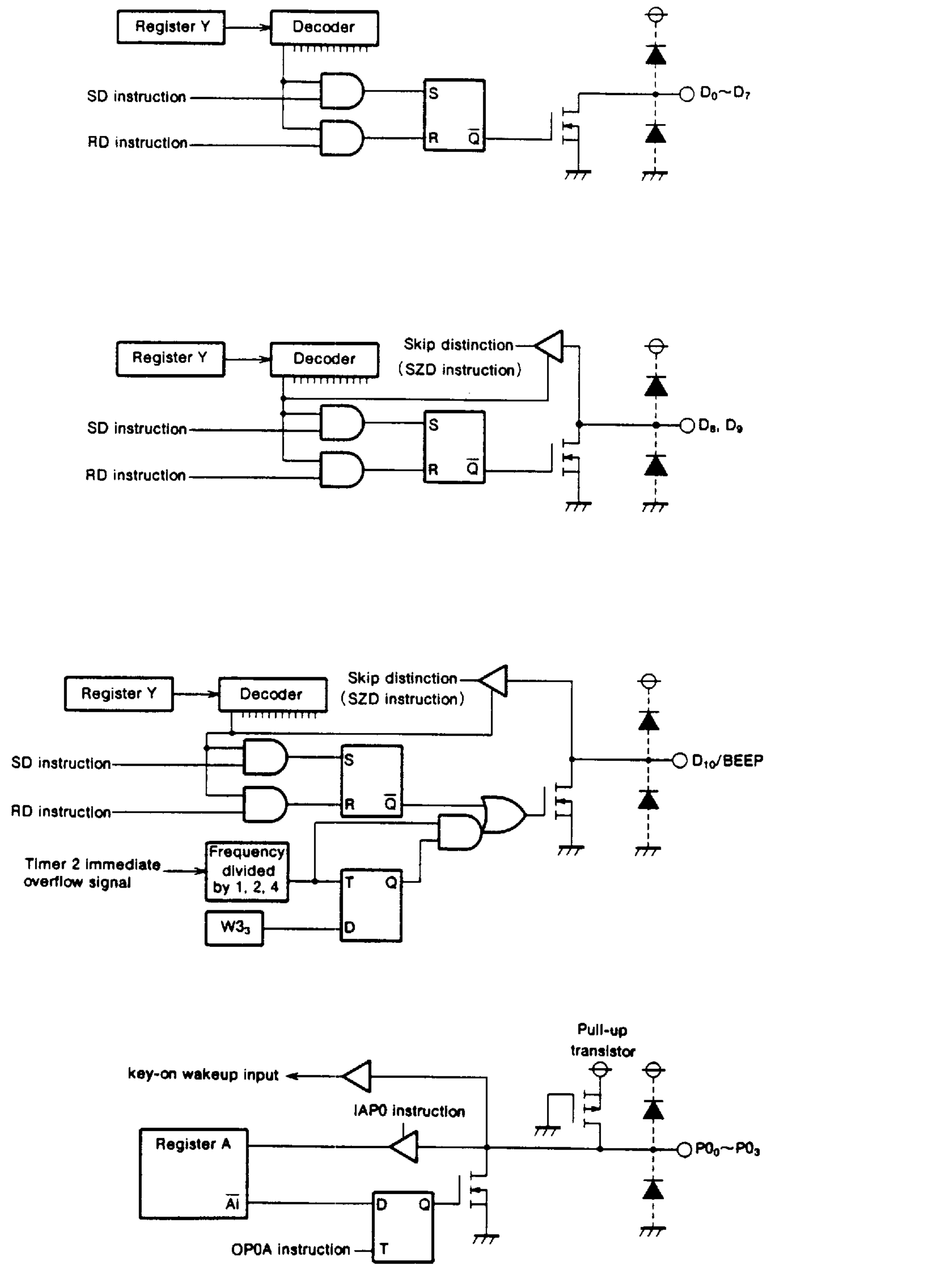


Handling of unused LCD power supply input pins

PORT FUNCTIONS

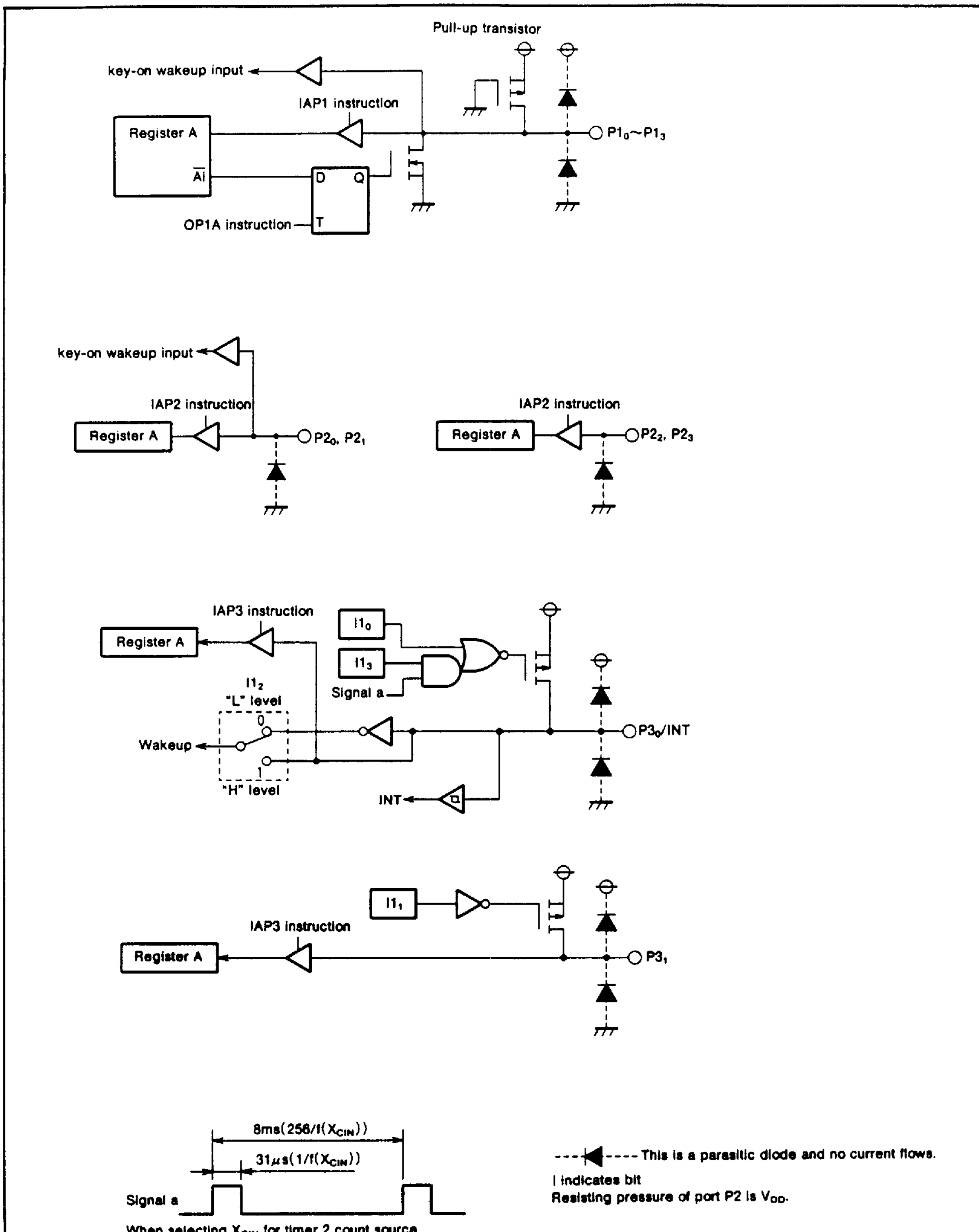
Port	Pin	Input/ Output	Output format	Control units	Control instructions	Double function	Control registers	Remarks
Port D	D_0~D_7, D_{11}/V_{LC1}, D_{12}/V_{LC2}, D_8, D_9, D_{10}/BEEP	Output (10) I/O (3)	N-channel open drain	1 bit	SD, RD, CLD SZD	 V_{LC1} V_{LC2} BEEP	L1, L3 W3	
Port P0	$P0_0$~$P0_3$	I/O (4)	N-channel open drain	4 bits	OP0A, IAP0	Key-on wakeup		Built-in pull-up transistor
Port P1	$P1_0$~$P1_3$	I/O (4)	N-channel open drain	4 bits	OP1A, IAP1	Key-on wakeup		Built-in pull-up transistor
Port P2	$P2_0$, $P2_1$ $P2_2$, $P2_3$	Input (4)		4 bits	IAP2	Key-on wakeup		
Port P3	$P3_0$/INT $P3_1$	Input (2)		2 bits	IAP3	INT Key-on wakeup	I1	Built-in programmable pull-up transistor
Port P4	$SEG_{36}/P4_0$~ $SEG_{39}/P4_3$	Input (4)		4 bits	IAP4	SEG_{36}~ SEG_{39}	L2	

PORT BLOCK DIAGRAM



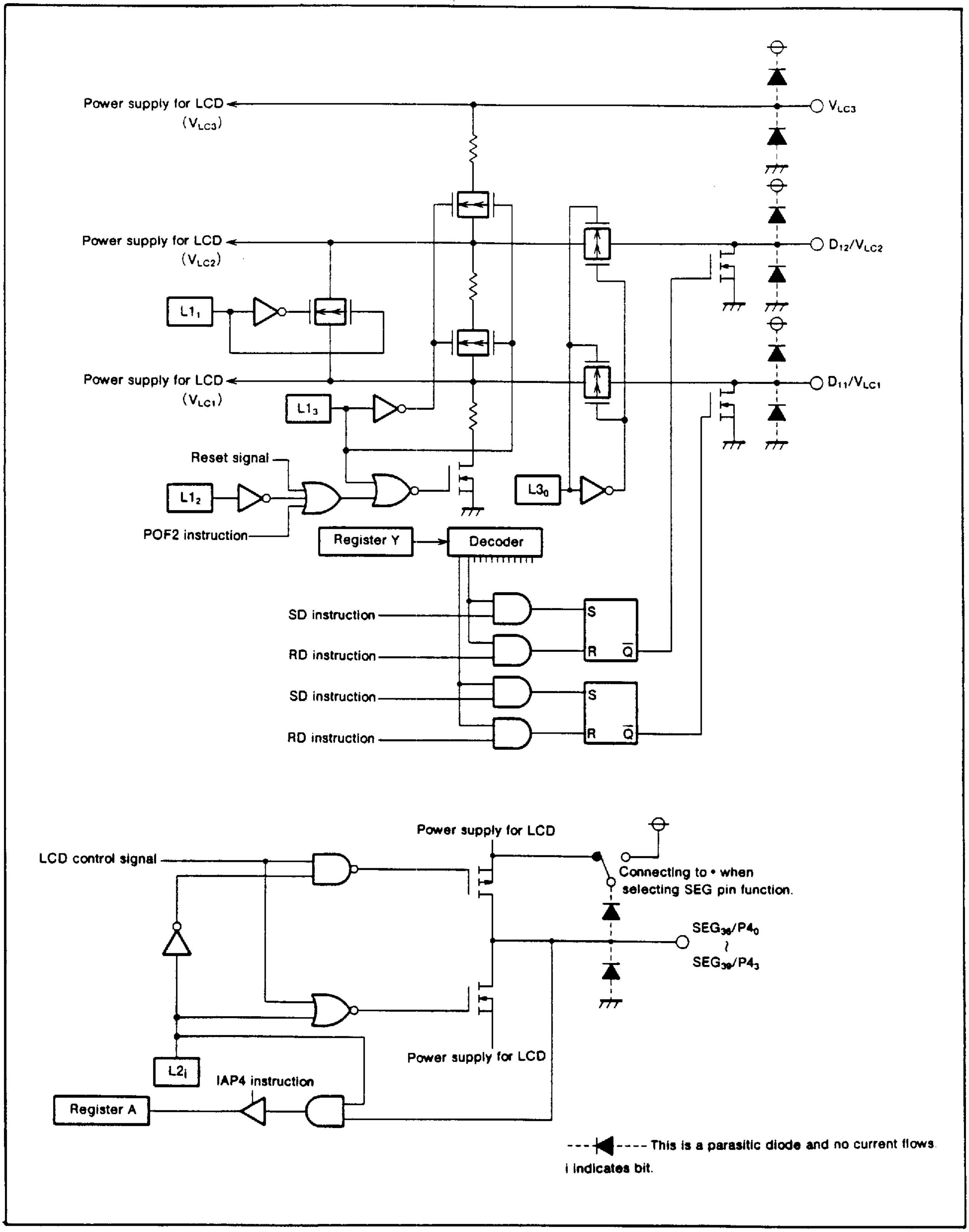
---◀--- This is a parasitic diode and no current flows.
i indicates bit.

PORT BLOCK DIAGRAM (continued)

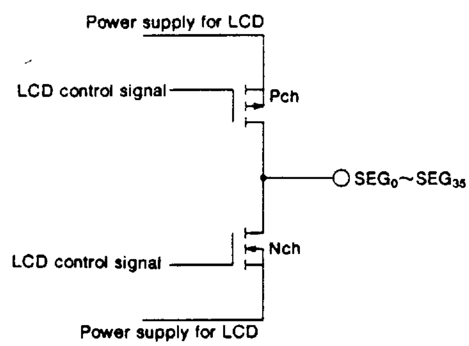


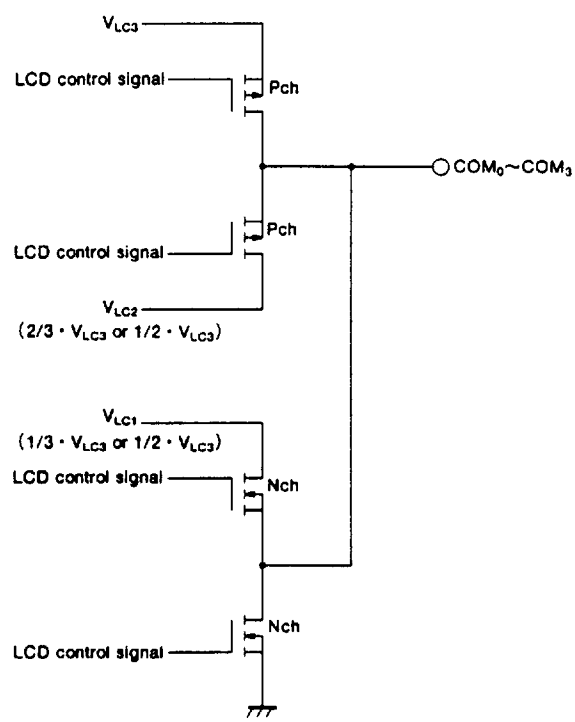
----◀---- This is a parasitic diode and no current flows.
I indicates bit
Resisting pressure of port P2 is V_{DD}.

PORT BLOCK DIAGRAM (continued)



PORT BLOCK DIAGRAM (continued)





FUNCTION BLOCK OPERATIONS

4-BIT ARITHMETIC LOGIC UNIT (ALU)

This unit performs 4-bit arithmetic such as 4-bit addition, comparison, AND, OR, and bit manipulation.

REGISTER A AND CARRY FLAG

Register A is a 4-bit register used for arithmetic, transfer, exchange, and I/O operations.

The carry flag is a 1-bit flag that is set to "1" when there is a carry after executing the AMC instruction (it is unchanged after executing the A n instruction or the AM instruction). After executing the RAR instruction, the value of A_0 is stored in the carry flag. The carry flag is set to "1" by the SC instruction and reset to "0" by the RC instruction.

REGISTERS B, E

Register B is a 4-bit register and is used for temporary storage for 4-bit data and for 8-bit data transfer together with register A.

Register E is an 8-bit register. It can be used for 8-bit data transfer with register B used as the high-order 4 bits and register A as the low-order 4 bits.

REGISTER D

Register D is a 3-bit register. It is used together with register A to store a 7-bit ROM address and is used as a pointer within the specified page when executing the TABP p, BLA p, or BMLA p instruction.

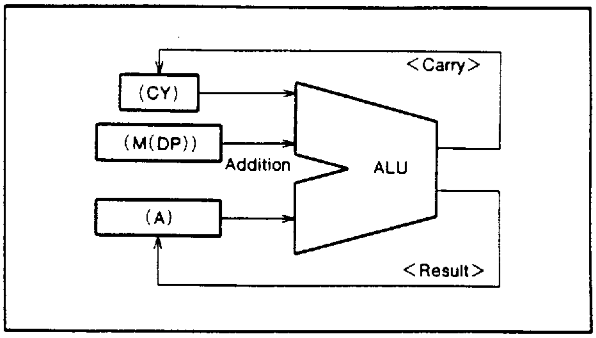


Fig. 1 AMC instruction execution example

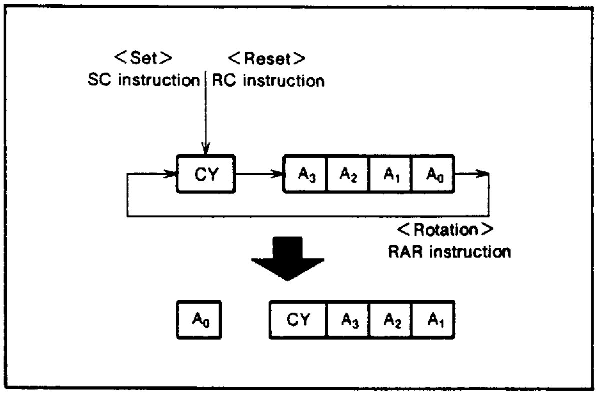


Fig. 2 RAR instruction execution example

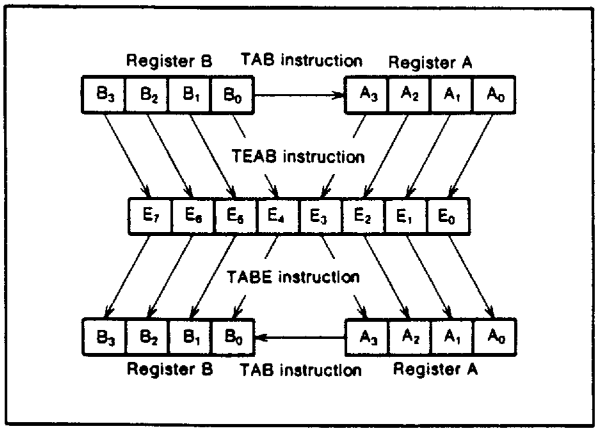


Fig. 3 Registers A, B and register E

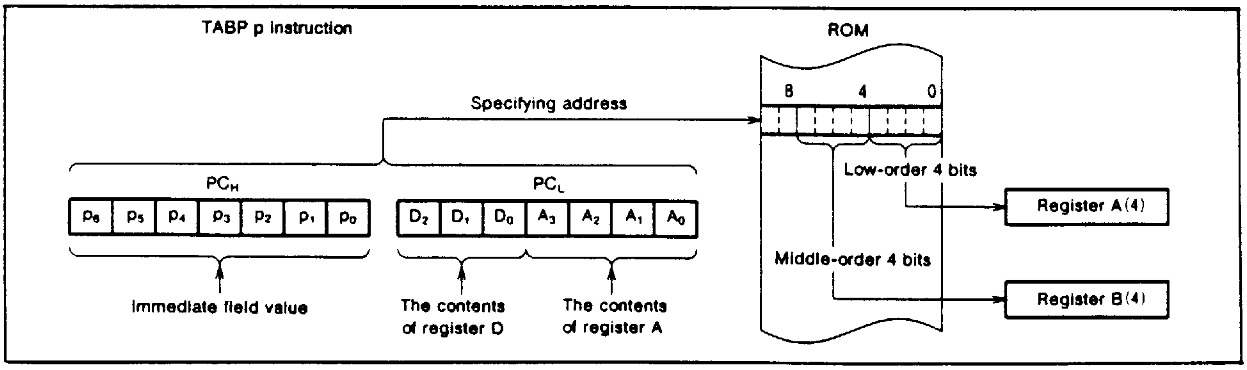


Fig. 4 TABP p instruction execution example

STACK REGISTER (SK)

This register is used to temporarily store the contents of program counter just before branching until returning to the original routine when branching to an interrupt service routine (referred to as interrupt service routine), performing a subroutine call, or executing a table reference instruction (TABP p instruction).

The stack register (SK) has 8 stages so that subroutines can be nested up to 8 levels. However, 1 stage is used respectively when using an interrupt service routine or executing a table reference instruction. Therefore, be sure the stack is not exhausted when performing these operations together. The contents of the register SK are destroyed when 8 levels are exceeded.

The register SK nesting level is indicated automatically by a 3-bit stack pointer (SP). The contents of this stack pointer can be transferred to register A with the TASP instruction.

STACK REGISTER (SDP)

This register is used to temporarily store until returning to the original routine, the data pointer, carry flag, skip flag, and contents of registers A and B just before an interrupt when an interrupt occurs. The stack register (SDP) is a 1 stage register.

This register cannot be used during a subroutine call or when executing a table reference instruction as with the SK.

SKIP FLAG

This flag controls skip distinction for the conditional skip instruction and continuous described skip instructions. When an interrupt occurs, the contents of the skip flag are stored automatically to the stack register (SDP) and the skip condition is retained.

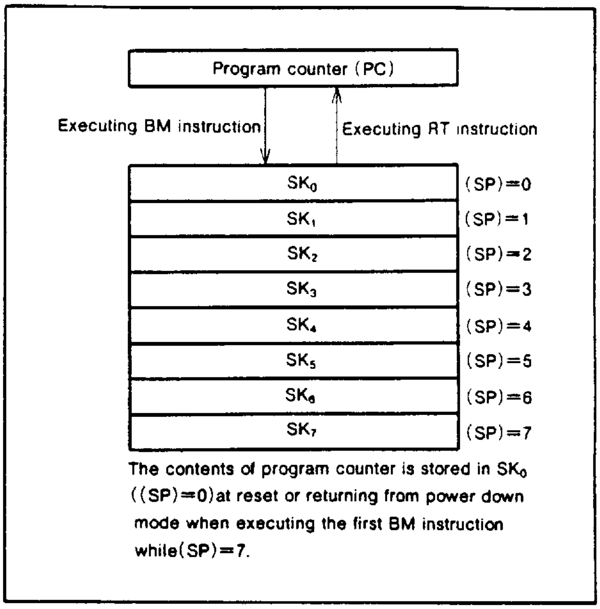


Fig. 5 Stack register (SK) structure

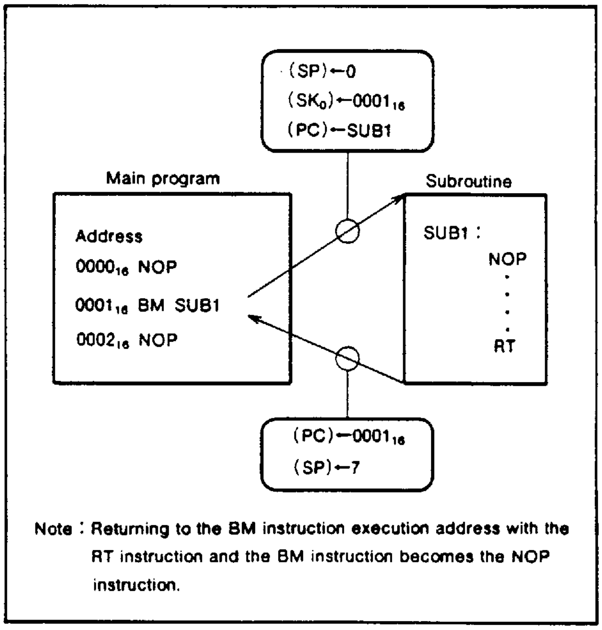


Fig. 6 Operation at subroutine call

PROGRAM MEMORY (ROM)

The program memory is the mask ROM consisting of 10 bits per 1 word. It is divided into 128 words by the unit of page (addresses 0 to 127).

Table 1 ROM size and pages

Type name	ROM size (×10 bits)	Pages
M34550M8-XXXFP	8192 words	64
M34550M6-XXXFP	6144 words	48

A part of page 1 (addresses 0080_{16} to $00FF_{16}$) is reserved for interrupt addresses. When an interrupt occurs, the address (interrupt address) corresponding to each interrupt is set in the program counter and the instruction at the interrupt address is executed. When using an interrupt service routine to process an interrupt, write the instruction to branch to that routine at the interrupt address.

Page 2 (addresses 0100_{16} to $017F_{16}$) is the special page for subroutine calls. Subroutines written in this page can be called from any page with a 1-word instruction (BM). Subroutines extending from page 2 to other page can also be called with the BM instruction if it starts on page 2.

All pages can be used as data area with the TABP p instruction.

PROGRAM COUNTER (PC)

Program counter (PC) is used to specify a ROM address (page and address). It determines the sequence in which the instructions stored in ROM are read. It is the binary counter that is incremented each time an instruction is executed. However, the value changes to the specified address when a branch, subroutine call, return, or table reference instruction (TABP p) is executed.

The program counter consists of PC_H (most significant bit to bit 7) which points to a ROM page and PC_L (bit 6 to 0) which points to an address within a page. After it reaches the last address (address 127) of a page, it points to address 0 of the next page.

Make sure that the PC_H does not point beyond the last page of internal ROM.

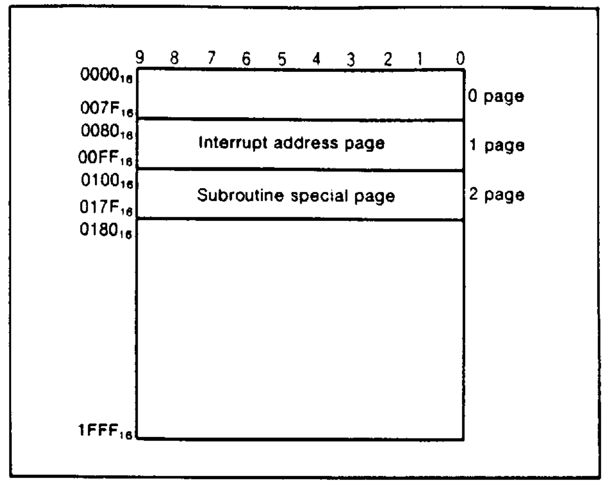


Fig. 7 ROM map of M34550M8-XXXFP

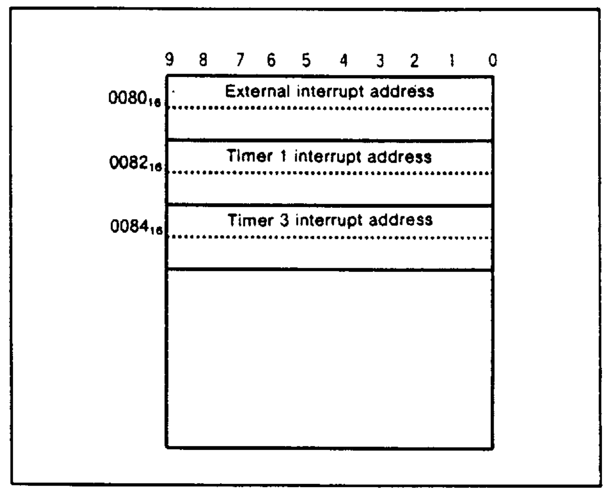


Fig. 8 1 page structure

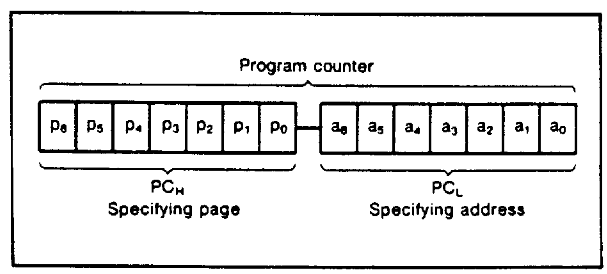


Fig. 9 Program counter structure

DATA MEMORY (RAM)

The RAM consists of 4-bit words, but bit manipulation (with the SB j, RB j, and SZB j instruction) is enabled for the entire memory area. A RAM address is specified by a data pointer consisting of registers Z, X, and Y. Set the contents of data pointer certainly when executing an instruction related RAM.

Table 2 RAM size

Type name	RAM size
M34550M8-XXXFP	368 words×4 bits
M34550M6-XXXFP	(1472 bits)

The RAM includes the area corresponding to the LCD. A segment is displayed automatically when "1" is written in the bit corresponding to the segment.

DATA POINTER (DP)

Data pointer (DP) is used to specify a RAM address and consists of registers Z, X, and Y. Register Z specifies a RAM file group, register X specifies a file, and register Y specifies a RAM digit. Register Y is also used to specify the port D bit position.

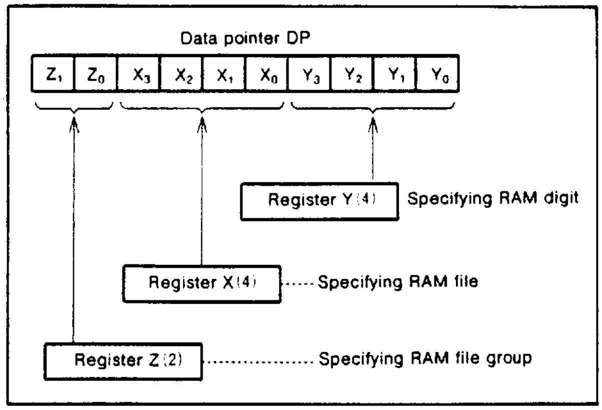


Fig. 10 Data pointer (DP) structure

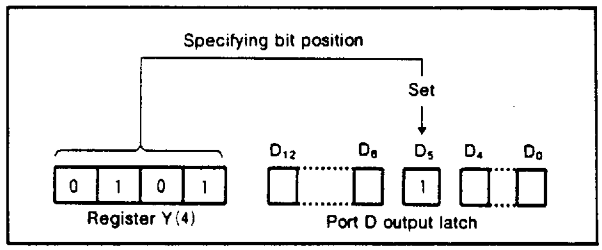


Fig. 11 SD instruction execution example

Register Z	0				1								
Register X	0	1	…	15	0	…	3	4	5	6	7	8	9
Register Y 0								—	—	—	—	—	—
1								—	—	—	—	—	—
2								—	—	—	—	—	—
3								—	—	—	—	—	—
4								—	—	—	—	—	—
5								—	—	—	—	—	—
6								—	—	—	—	—	—
7								—	—	—	—	—	—
8								0	8	16	24	32	
9								1	9	17	25	33	
10								2	10	18	26	34	
11								3	11	19	27	35	
12								4	12	20	28	36	
13								5	13	21	29	37	
14								6	14	22	30	38	
15								7	15	23	31	39	

Notes 1. The area marked "—" (Z=1, X=4~9, Y=0~7) is not a memory area.
2. The numbers in the shaded area indicate the corresponding segment output pin numbers.

Fig. 12 RAM map

INTERRUPT FUNCTION

The interrupt format is a vectored interrupt branching to different address (interrupt address) according to each interrupt source. An interrupt occurs when :

- Activated condition is satisfied (request flag="1")
- Interrupt enable bit is enabled ("1")
- Interrupt enable flag is enabled (INTE="1")

Table 3 shows the activated condition and interrupt address for each interrupt.

(1) Interrupt enable flag (INTE)

The interrupt enable flag (INTE) controls whether the every interrupt enable/disable. Interrupts are enabled when INTE flag is set to "1" with the EI instruction and disabled when INTE flag is set to "0" with the DI instruction. When any interrupt occurs, the INTE flag is automatically reset to "0" and interrupt is disabled until the EI instruction is executed.

(2) Interrupt enable bit

The occurrence of each interrupt can be controlled by software. When interrupt is not used, whether the activated condition is satisfied (whether request flag="1") can be checked with the skip instruction. Select whether to use an interrupt or the skip instruction with the interrupt enable bit.

(3) Interrupt request flag

When the activated condition for each interrupt is satisfied, the corresponding request flag is set to "1". Each request flag is reset to "0" when

- An interrupt occurs
- Next instruction is skipped with a skip instruction

Each request flag is set when an activated condition is satistied even if the interrupt is disabled by the interrupt enable flag (INTE) or the interrupt enable bit. Once set, it retains set until a reset condition is satisfied. Therefore, an interrupt occurs when the interrupt disable state is removed while the request flag is set.

Table 3 Interrupt source and interrupt address

Priority level	Interrupt source		Interrupt address
	Interrupt name	Activated condition	
1	External interrupt	Level change of INT pin ("H"→"L" and "L"→"H")	Address 0 in page 1
2	Timer 1 interrupt	Timer 1 overflow	Address 2 in page 1
3	Timer 3 interrupt	Timer 3 overflow	Address 4 in page 1

Table 4 Interrupt enable bit function

Interrupt enable bit	Occurrence of interrupt	Skip instruction
1	enabled	Invalid
0	disabled	Valid

Table 5 Interrupt enable bit and skip instruction

Interrupt name	Request flag	Enable bit	Skip instruction
External interrupt	EXF0	$V1_0$	SNZ0
Timer 1 interrupt	T1F	$V1_1$	SNZT1
Timer 3 interrupt	T3F	$V1_2$	SNZT3

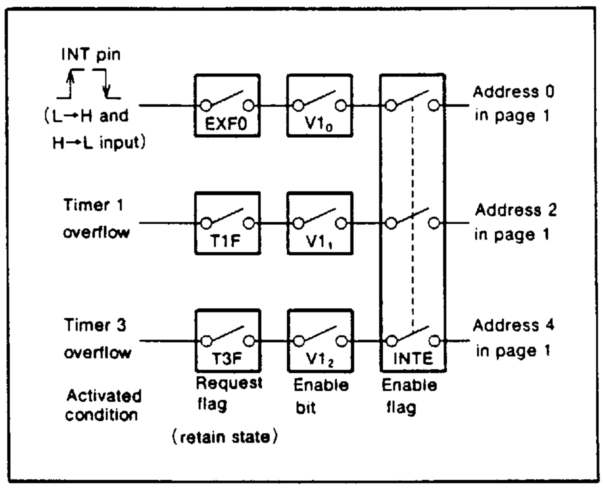


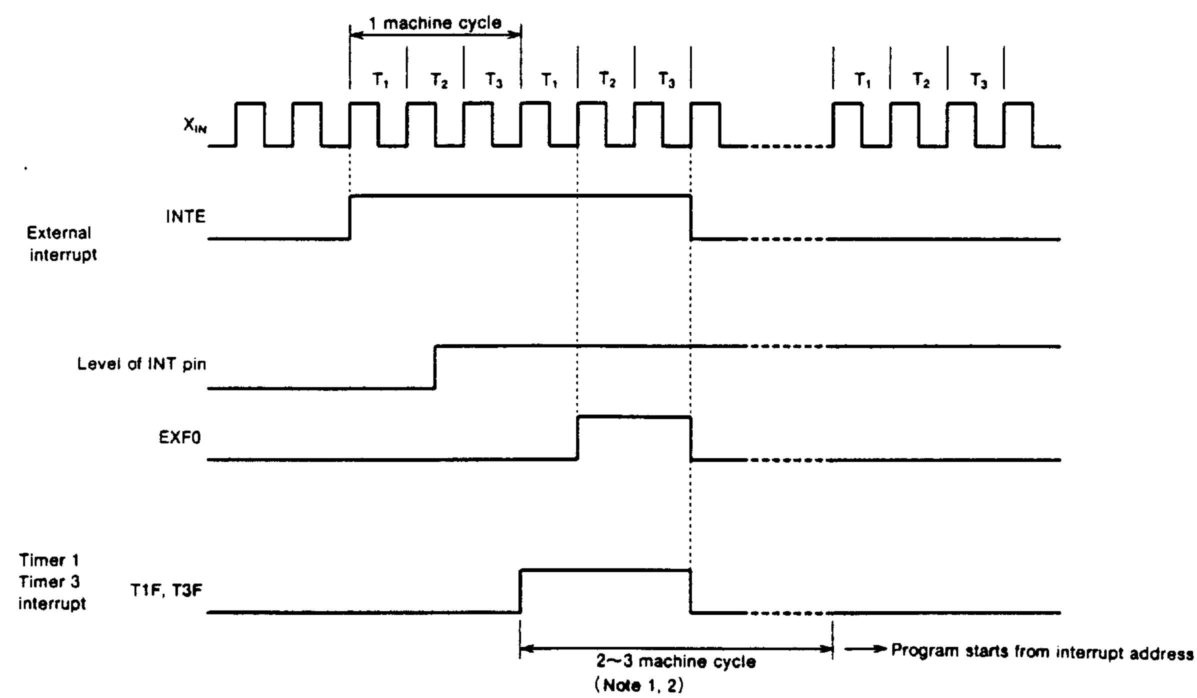
Fig. 13 Interrupt system diagram

(4) Internal state when an interrupt occurs
The internal state of the microcomputer is as follows when an interrupt occurs.

- Program counter (PC)
  The interrupt address is set. The address to be executed when returning to the main routine is automatically stored in the stack register (SK).
- Interrupt enable flag (INTE)
  INTE flag is reset to "0" and interrupt is disabled.
- Interrupt request flag
  Only the request flag for the interrupt source is reset to "0".
- Data pointer, carry flag, skip flag, registers A and B
  Data pointer, carry flag, skip flag, and registers A and B are stored to the stack register (SDP).

- Program counter(PC) .... Each interrupt address
- Stack register(SK) .... Executing address of main program
- Interrupt enable flag (INTE) .... 0 (Interrupt disabled)
- Interrupt request flag(The flag of interrupt source) 0
- Data pointer, carry flag, registers A and B .... Stored to stack register automatically
- Skip flag .... Stored to stack automatically

Fig. 14 Internal state when interrupt occurs



Notes 1. Depending on the instruction being executed when EXF0, T1F, and T3F become "1".
2. Address is stacked at the last cycle.

Fig. 15 Interrupt sequence

(5) Interrupt control register

• Interrupt control register (V1)

The interrupt enable bit is assigned to register V1. Set the contents of this register through register A with the TV1A instruction. The TAV1 instruction can be used to transfer the contents of register V1 to register A.

(6) Interrupt processing

When an interrupt occurs, the program at the interrupt address is executed after branching sequence to the interrupt address. When using an interrupt service routine, write the instruction to branch to the interrupt service routine at the interrupt address. Use the RTI instruction to return from an interrupt service routine. When the EI instruction and the RTI instruction are coded continuously at the end of an interrupt service routine, interrupts are enabled after executing the RTI instruction. (Refer to Fig. 16)

When using an interrupt service routine, the contents of the program counter at returning to the main routine is automatically stored to the stack register (SK). This uses 1 of the 8 stack stages. Therefore, 7 stages are left for subroutines.

When using the registers in the interrupt service routine, store the contents of the registers by program at the beginning of the interrupt service routine. And then, restore them before returning to the main routine. However, the data pointer (registers Z, X, Y), carry flag, skip flag, and registers A and B are automatically stored to the stack register (SDP) and restored.

```
INT :   ·       Interrupt service routine
        ·
        ·
        ·
        EI
        RTI
```

Fig. 16 Program example of interrupt processing

(7) External interrupt request flag (EXF0)

The EXF0 flag is set to "1" when a rising waveform ("L"→"H") or a falling waveform ("H"→"L") is input to $P3_0$/INT pin. However, both the level before the change and after must be retained at least 4 cycles (4.4μs at 910kHz oscillating frequency) of the signal selected as system clock in order for an interrupt activated condition to be satisfied.

The state of the EXF0 flag can be checked when an interrupt occurs or with a skip instruction (SNZ0). This flag is reset to "0" when an interrupt occurs or when the next instruction is skipped with a skip instruction.

The $P3_0$/INT pin need not be selected for an external interrupt input pin or normal port. However, the EXF0 flag is set when the condition for setting the EXF0 flag is satisfied even when this pin is used as input port $P3_0$.

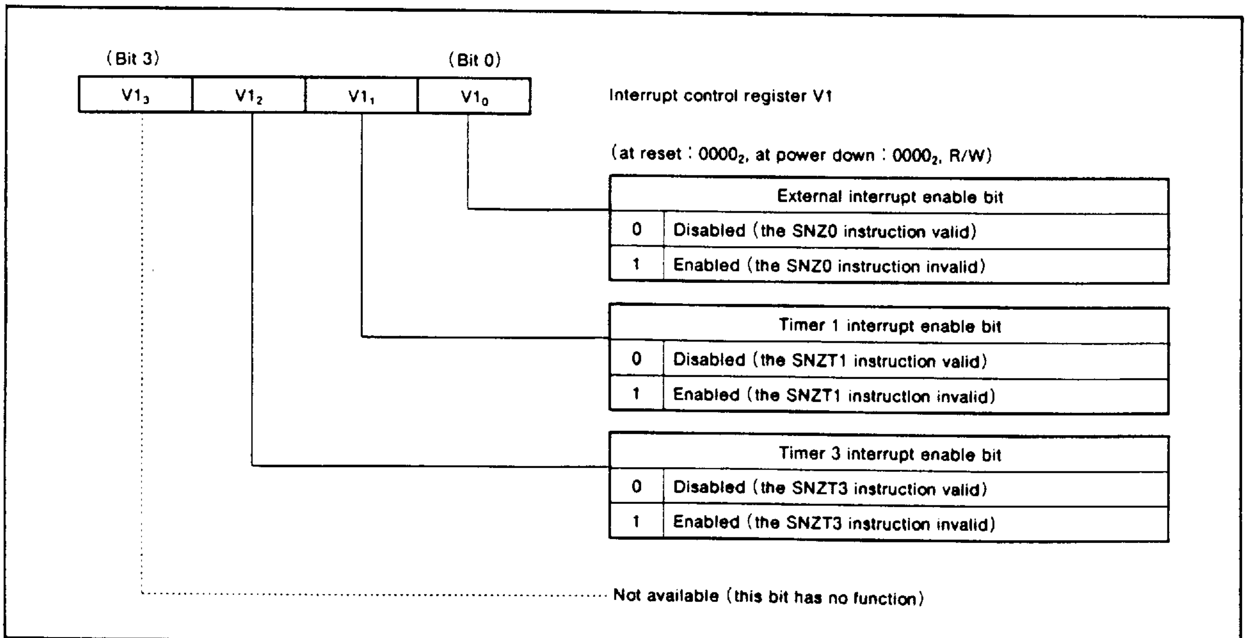


Fig. 17 Interrupt control register

TIMERS

The M34550Mx-XXXFP timer consists of the following circuits.

- Prescaler : frequency divider
- Timer 1 : 9-bit programmable timer (with interrupt function)
- Timer 2 : 8-bit fixed dividing frequency timer
- Timer 3 : 8-bit programmable timer (with interrupt function)
- Watchdog timer
- Frequency divider for LCD
- Buzzer drive output

These timers can be controlled with the timer control register (W1, W2, W3). Each function is described below.

Table 6 Function related timers

Circuit	Structure	Count source	Frequency dividing ratio	A use of output signal	control
Prescaler	Frequency divider	• $f(X_{IN})$ or $f(X_{CIN})$	2, 4, 8	• Timer 1, 3 count source • Multi-carrier generating circuit	W1
	(Frequency divider (divide by 8))		(8)	• Timer 2 count source	
Timer 1	9-bit programmable binary down counter	• Prescaler output (ORCLK) • Multi-carrier output (CARR)	1~512	• Multi-carrier generating circuit • Timer 1 interrupt	W1
Timer 2	8-bit fixed dividing frequency binary down counter	• $f(X_{CIN})$ • Prescaler output (Frequency divided by 8 output)	256	• Timer 3 count source	W2
	(Frequency divider (divide by 16))		(16)	• Buzzer drive output • Frequency divider for LCD	
Timer 3	8-bit programmable binary down counter	• Timer 2 overflow • Prescaler output (ORCLK)	1~256	• Watchdog timer • Power down 1 return • Timer 3 interrupt	W2
Watchdog timer	Timer 3	• Timer 3 overflow		• System reset	W3
Buzzer drive output	Frequency divider	• Timer 2 immediate overflow (Frequency divided by 16 output)	1, 2, 4		W3
Frequency divider for LCD	Frequency divider (divide by 1, 2, 4) +4-bit counter +frequency divider (divide by 2)	• Timer 2 immediate overflow (Frequency divided by 16 output)	2(n+1), 4(n+1), 8(n+1) [n=0~15]	• LCD controller/driver	W3

The MELPS 4500 has a programmable timer and a fixed dividing frequency timer.

- Programmable timer
  A programmable timer enables the frequency dividing ratio to be set and has a reload register. It is decremented from the setting value n. When it overflows (count to n+1), the overflow flag (interrupt request flag if equipped with interrupt function) is set to "1", a new data is set from the reload register, and count continues (auto-reload function).
- Fixed diviging frequency timer
  A fixed dividing frequency timer has a fixed frequency dividing ratio (n). The overflow flag (interrupt request flag if equipped with interrupt function) is set to "1" after every n count of the count pulse.

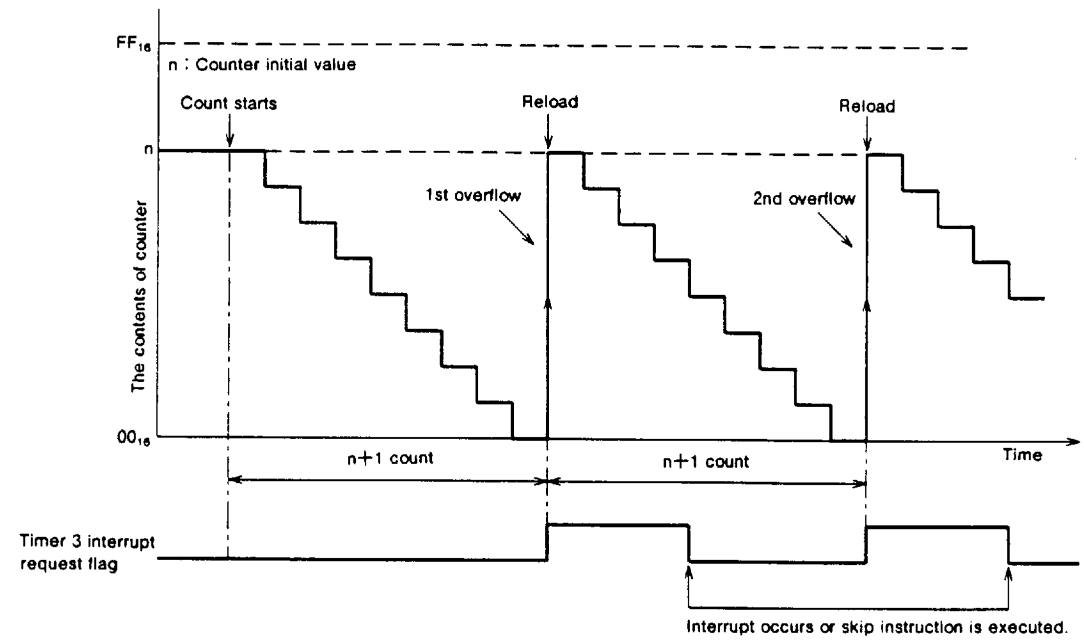


Fig. 18 Auto-reload function

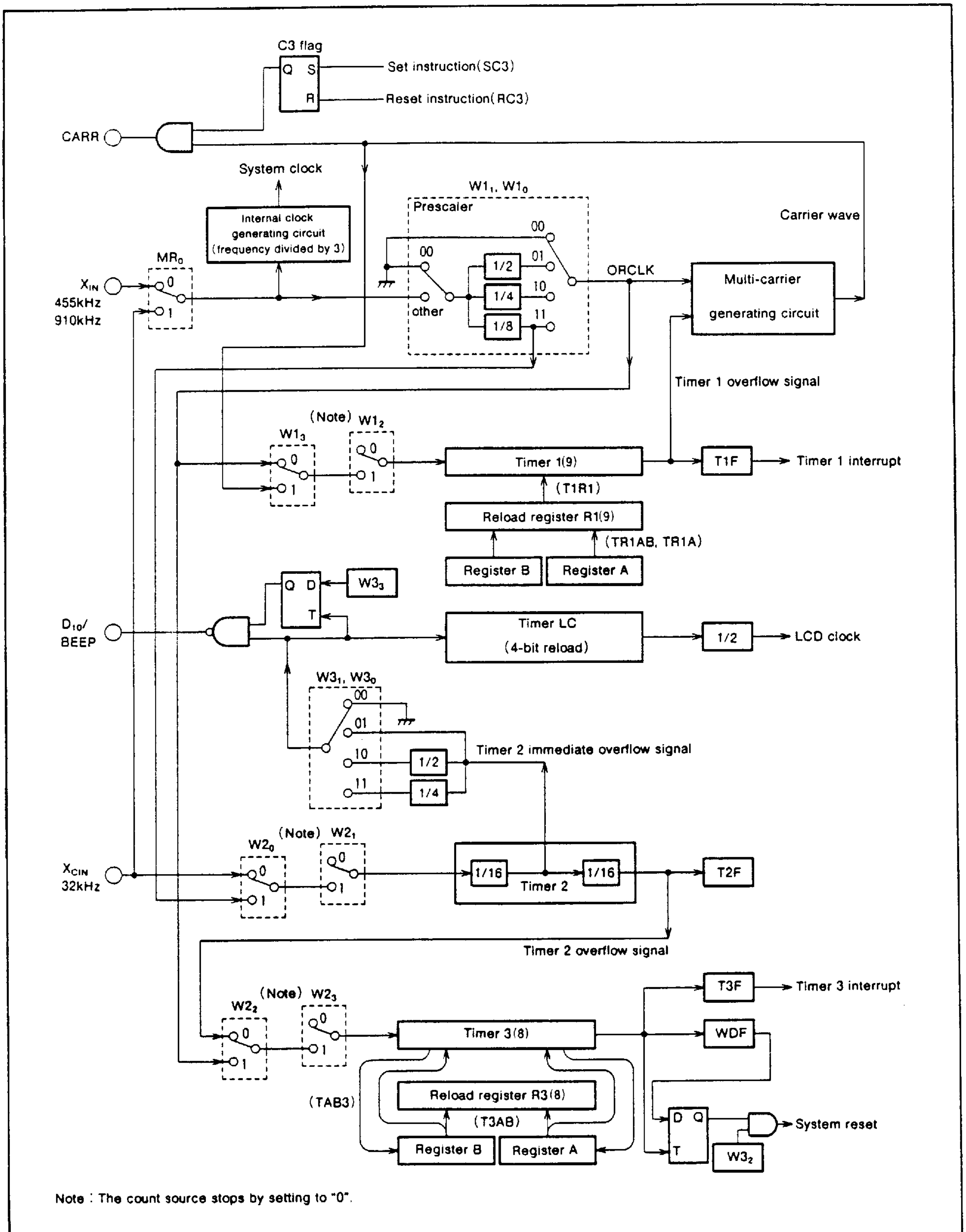


Fig. 19 Timers structure

(Bit 3) (Bit 0)

$W1_3$	$W1_2$	$W1_1$	$W1_0$

Timer control register W1

(at reset : 0000_2, at power down : 0000_2, R/W)

Prescaler frequency dividing ratio selection bit

$W1_1$	$W1_0$	Frequency dividing ratio
0	0	Prescaler stopped (reset state)
0	1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 2 (Note)
1	0	$f(X_{IN})$ or $f(X_{CIN})$ divided by 4 (Note)
1	1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 8 (Note)

Timer 1 control bit ($W1_2$)

0	Stop (retain state)
1	Operating

Timer 1 count source selection bit ($W1_3$)

0	Prescaler output (ORCLK)
1	Multi-carrier output (CARR)

Note : The signal in $f(X_{IN})$ or $f(X_{CIN})$ selected as system clock is used.

(Bit 3) (Bit 0)

$W2_3$	$W2_2$	$W2_1$	$W2_0$

Timer control register W2

(at reset : 0000_2, at power down : 0000_2, R/W)

Timer 2 count source selection bit ($W2_0$)

0	$f(X_{CIN})$
1	Prescaler output (frequency divided by 8 output)

Timer 2 control bit ($W2_1$)

0	Stop (retain state)
1	Operating

Timer 3 count source selection bit ($W2_2$)

0	Timer 2 overflow signal
1	Prescaler output (ORCLK)

Timer 3 control bit ($W2_3$)

0	Stop (retain state)
1	Operating

Fig. 20 Timer control register

(Bit 3)			(Bit 0)
$W3_3$	$W3_2$	$W3_1$	$W3_0$

Timer control register W3

(at reset : 0000_2, at power down : retain state, R/W)

BEEP, LCD clock frequency dividing circuit control bit ($W3_1$, $W3_0$)

$W3_1$	$W3_0$	Frequency dividing ratio
0	0	Stop
0	1	Timer 2 immediate overflow (frequency divided by 16 output)
1	0	Timer 2 immediate overflow (frequency divided by 16 output) divided by 2
1	1	Timer 2 immediate overflow (frequency divided by 16 output) divided by 4

Watchdog timer control bit ($W3_2$)

0	Not used
1	Used

BEEP output control bit ($W3_3$)

0	Output stopped
1	Output

Fig. 21 Timer control register (continued)

(1) Prescaler
The prescaler is a frequency divider with selectable frequency dividing ratio and it outputs 2 signals (ORCLK and frequency divided by 8 as signal). The prescaler count source is $f(X_{IN})$ or $f(X_{CIN})$ which is selected signal as system clock with the register MR.
Use bits 0 and 1 of the register W1 to select the prescaler dividing ratio and to start and stop its operation. The prescaler is reset state and the ORCLK and frequency divided by 8 as signal output stop when both bits 0 and 1 of the register W1 are set to "0".

(2) Timer 1
Timer 1 is a 9-bit binary down counter and has a timer 1 reload register (R1). To set data in timer 1, first set data in reload register R1 (TR1AB instruction, TR1A instruction) and then transfer it from the reload register R1 to timer 1 (T1R1 instruction). Timer 1 starts counting when data is set in timer 1, count source is selected with bit 3 of the register W1, and bit 2 is set to "1".
When timer 1 overflows (next count pulse is input after the contents of timer 1 becomes "0"), the timer 1 interrupt request flag (T1F) is set to "1", new data is loaded from the reload register R1, and count continues (auto-reload function). If the reload register R1 contains n, timer 1 divides the count source signal by n+1 (n=0~511).
When writing data to reload register R1, be sure the timing when timer 1 does not overflow.

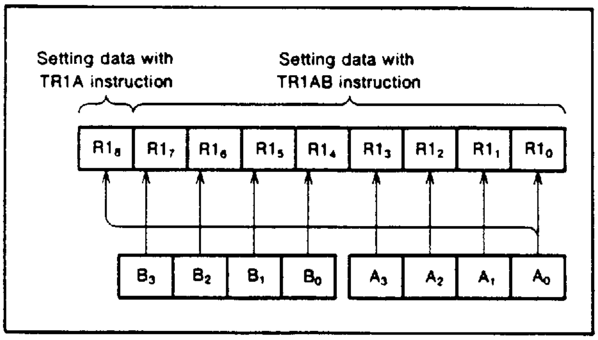


Fig. 22 Setting example of register R1

(3) Timer 2
Timer 2 is an 8-bit binary down counter. Timer 2 starts counting when the count source is selected with bit 0 of the register W2 and bit 1 is set to "1". The timer 2 overflow flag (T2F) is set to "1" at every 256 count of the count source.
Timer 2 outputs signals consisting of count source divided by 16 (intermediate overflow) as signal and count source divided by 256 (overflow) as signal. Timer 2 is reset and both frequency divided by 16 and 256 outputs stop when bit 1 of the register W2 is set to "0".
Timer 2 can be used as clock counter during power down 1 state (executing the POF instruction).

(4) Timer 3
Timer 3 is an 8-bit binary down counter with timer 3 reload register (R3). Data is set simultaneously in reload register R3 and timer 3 with the T3AB instruction. Timer 3 starts counting when data is set in timer 3, count source is selected with bit 2 of the register W2, and bit 3 is set to "1".
When timer 3 overflows (next count pulse is input after the contents of timer 3 becomes "0"), the timer 3 interrupt request flag (T3F) is set to "1", new data is loaded from the reload register R3, and count continues (auto-reload function). If the reload register R3 contains n, timer 3 divides the count source signal by n +1 (n=0~255).
The TAB3 instruction can be used to read the data in timer 3. Stop the counter before executing the TAB3 instruction to read the data. Timer 3 can be used as the clock counter during power down 1 state (executing the POF instruction).

(5) Watchdog timer

The watchdog timer consists of timer 3 and watchdog timer flag (WDF). When a timer 3 overflow signal is occurred, the WDF flag is set to "1". When the timer 3 overflows once more while the WDF flag is set, the watchdog timer forces a system reset (operationally equal to a power-on reset).

Whether to use the watchdog timer can be set with the bit 2 of the register W3.

When using the watchdog timer, be sure to reset the WDF flag to "0" with the WRST instruction by program once timer 3 overflows.

In order to effectively use the watchdog timer, do not execute the WRST instruction during timer 3 interrupt.

(6) Buzzer drive output

The D_{10}/BEEP pin has a buzzer drive output function. The output signal can be selected from the timer 2 intermediate overflow signal (frequency divided by 16 output) undivided, divided by 2 and 4. Select the frequency dividing ratio with bits 0 and 1 of the register W3. Signal start/stop can be controlled by bit 3 of the register W3.

When using the D_{10}/BEEP pin as buzzer drive output, set the D_{10} output latch to "1".

(7) Frequency divider for LCD

The frequency divider for the LCD consists of timer LC and frequency divider (divide by 2). Timer LC is a 4-bit programmable timer with reload latch. Data can be set simultaneously in the reload latch and timer LC with the TLCA instruction. The timer LC count source can be selected from the timer 2 intermediate overflow signal (frequency divided by 16 output) undivided, divided by 2 and 4.

Timer LC starts counting when data is set in timer LC and the count source is selected with bits 0 and 1 of the register W3. When it overflows, data is reloaded from the reload latch and count continues. If n is set in timer LC, the count source is divided by n+1 (n=0~15).

The timer LC overflow signal divided by 2 becomes the basic clock of the LCD.

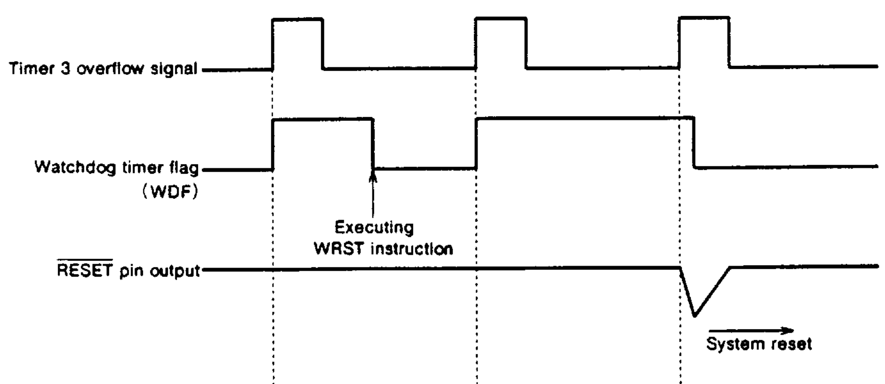


Fig. 23 Watchdog timer function

(8) Interrupt request flag (T1F, T3F)

The timer 1 interrupt request flag (T1F) is set to "1" when timer 1 overflows and the timer 3 interrupt request flag (T3F) is set to "1" when timer 3 overflows. The state of these flags can be checked when an interrupt occurs or with a skip instruction (SNZT1, SNZT3 instruction).

Use the interrupt control register (V1) to select between interrupt and skip instruction. The interrupt request flag is reset to "0" when an interrupt occurs or when the next instruction is skipped with a skip instruction.

(9) Overflow flag (T2F)

The timer 2 overflow flag (T2F) is set to "1" each time timer 2 overflows (every 256 count). The state of this flag can be checked when a skip instruction (SNZT2 instruction) is executed. The T2F flag is reset to "0" only when the next instruction is skipped with a skip instruction.

(10) Timer control register

- Timer control register (W1)

  Register W1 cotrols the prescaler and timer 1 count operation and the count source. Set this register with the TW1A instruction through register A. The TAW1 instruction can be used to transfer the contents of register W1 to register A.

- Timer control register (W2)

  Register W2 controls the timer 2 and timer 3 count operation and the count source. Set this register with the TW2A instruction through register A. The TAW2 instruction can be used to transfer the contents of register W2 to register A.

- Timer control register (W3)

  Register W3 controls the watchdog timer, BEEP drive output, and the frequency divider for the LCD. Set this register with the TW3A instruction through register A. The TAW3 instruction can be used to transfer the contents of register W3 to register A.

(11) Precautions

Note the following when using a timer.

- Prescaler precautions

  Be sure to stop the prescaler before changing the frequency dividing ratio of the prescaler.

- Timer precautions

  Be sure to stop counting of each timer before switching the timer 1, 2, or 3 count source.

  To read the data from timer 3, stop counting of the timer 3 and then execute the TAB3 instruction.

- D_{10}/BEEP pin precautions

  To start the buzzer drive output, set the frequency (bits 0 and 1 of the register W3) and then start output.

  When changing the buzzer drive output frequency or using this pin as port D_{10}, first stop the buzzer drive output, wait for 1 cycle of the buzzer drive output, and then set the frequency or start using as port D_{10}.

MULTI-CARRIER GENERATING CIRCUIT

The M34550Mx-XXXFP is equipped with multi-carrier generating circuit for generating transmission waves for remote control carrier wave. This circuit automatically generates a carrier wave compensated at constant period by setting data in the carrier wave data control register (C1), carrier wave compensation control register (C2), preset register (PA_0~PA_3), and compensation control timer (PT). If a waveform not obtainable with this method is necessary, the "H" or "L" interval of the carrier wave and the compensation can be controlled at your option by generating the wait interval until the set instruction and reset instruction (SC4, RC4) with software.

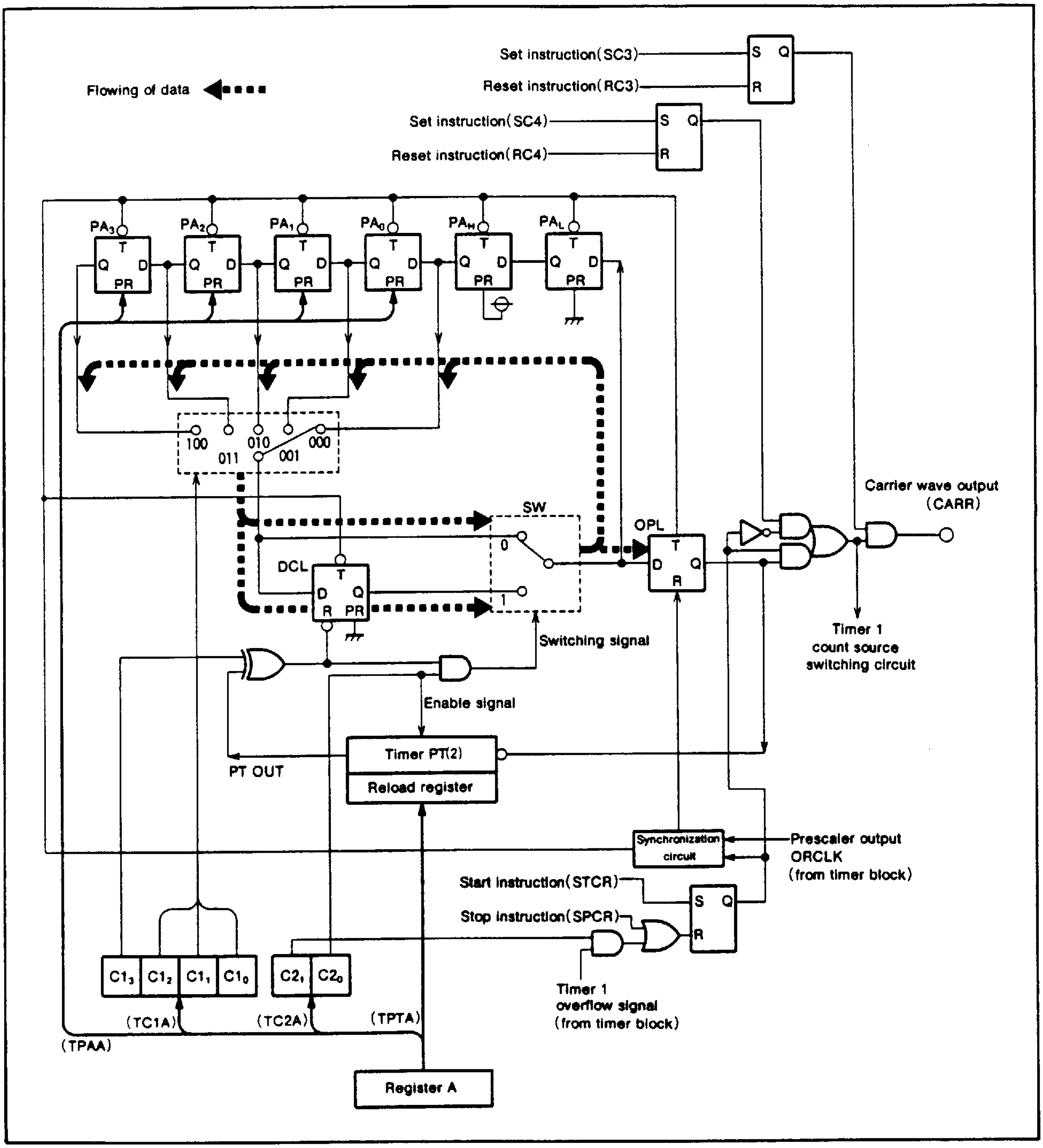


Fig. 24 Multi-carrier generating circuit

(Bit 3)			(Bit 0)
$C1_3$	$C1_2$	$C1_1$	$C1_0$

Carrier wave data control register C1

(at reset : 0000_2, at power down : 0000_2, W)

Carrier wave data register connection control bit			
$C1_2$	$C1_1$	$C1_0$	Number of connection bits
0	0	0	2 bits connection
0	0	1	3 bits connection
0	1	0	4 bits connection
0	1	1	5 bits connection
1	0	0	6 bits connection
Other combination			Not used

Carrier wave data compensation control bit	
0	−1 compensation
1	+1 compensation

(Bit 1)	(Bit 0)
$C2_1$	$C2_0$

Carrier wave compensation control register C2

(at reset : 00_2, at power down : 00_2, W)

Carrier wave compensation control bit	
0	Do not compensate
1	Compensate

Carrier wave automatic stop function control bit	
0	Automatic stop function not used
1	Automatic stop function used

C3	

Carrier wave output control flag C3

(at reset : 0_2, at power down : 0_2, W)

Carrier wave output control	
0	Carrier wave output disabled (execute RC3 instruction)
1	Carrier wave output (execute SC3 instruction)

Fig. 25 Multi-carrier generating circuit control register and control flag

(1) Multi-carrier generating circuit operation

The carrier wave is compensated by +1 compensation or −1 compensation. Assuming the interval between the rise of the reference clock (ORCLK) input through the synchronization circuit and the next rise is 1T :

+1 compensation : extends the "L" interval by 1T at constant period.

−1 compensation : reduces the "L" interval by 1T at constant period.

The operation of the multi-carrier generating circuit is described below with examples for +1 compensation and −1 compensation (refer to Fig. 24).

● +1 compensation example

[Output waveform]

- Basic waveform : "H" interval=2T
  "L" interval=2T
- Compensation period : once every 2 cycle (+1 compensation)

[Initial setting value]

- Carrier wave data control register
  $C1_3 \sim C1_0 = (1010)_2$
- Carrier wave compensation control register
  $C2_1$, $C2_0 = (XX01)_2$
- Preset register $PA_3 \sim PA_0$
  Initial value$=(XX01)_2$
- Compensation control timer PT
  Initial value $(1)_{16}$

In this case, the shift operation is $PA_L \rightarrow PA_H \rightarrow PA_0 \rightarrow PA_1$ because the carrier wave data register (PA) is set to 4 stages connection. In addition, the data compensation latch (DCL) stops at reset state when the timer PT output (PT OUT) is "H" and operates when it is "L" because $C1_3$ is set to "1". The ORCLK is input to the multi-carrier generating circuit with the STCR instruction and register PA shift operation starts. At this time, DCL stops at reset state and disconnected from register PA because timer PT outputs initial level "H". Therefore, PA_1 output is input to output latch (OPL) and output as carrier wave (CARR) after T/2. This is the basic waveform.

When timer PT overflows and PT OUT changes to "L", DCL reset is removed and connected to the last level of register PA. This causes the shift operation $PA_L \rightarrow PA_H \rightarrow PA_0 \rightarrow PA_1 \rightarrow$ DCL. Therefore, the DCL output is input to OPL and the "L" interval becomes longer than the basic waveform by 1T. This is the compensated waveform.

When the next fall of the carrier wave occurs, PT OUT returns to "H", DCL is disconnected, and a basic waveform is output. The carrier waveform is stopped with the SPCR instruction because $C2_1$ is set to "0".

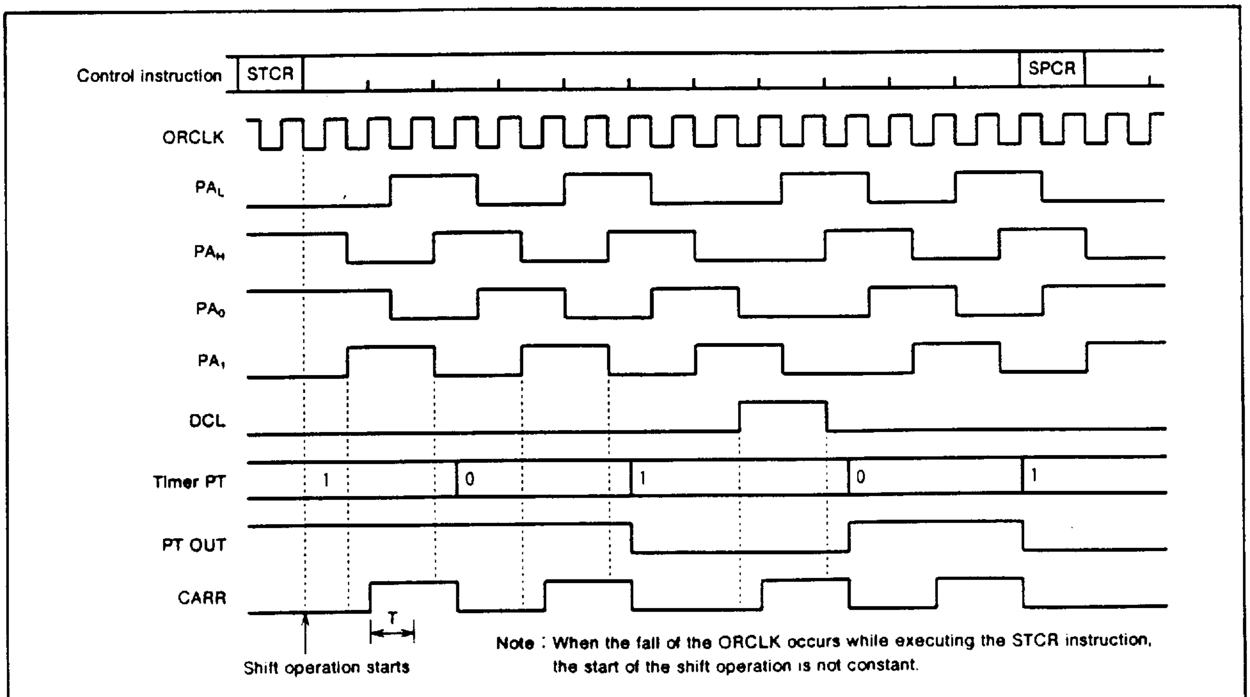


Fig. 26 Timing diagram at +1 compensation

● −1 compensation example

[Output waveform]

- Basic waveform : "H" interval=2T
  "L" interval=2T
- Compensation period : once every 2 cycle (+1 compensation)

[Initial setting value]

- Carrier wave data control register
  $C1_3 \sim C1_0 = (0001)_2$
- Carrier wave compensation control register
  $C2_1$, $C2_0 = (XX01)_2$
- Preset register $PA_3 \sim PA_0$
  Initial value=$(XXX1)_2$
- Compensation control timer PT
  Initial value $(1)_{16}$

In this case the shift operation is $PA_L \rightarrow PA_H \rightarrow PA_0$ because the carrier wave data register (PA) is set to 3 stages connection. In addition, the data compensation latch (DCL) operates when the timer PT output (PT OUT) is "H" and stops at reset state when it is "L" because $C1_3$ is set to "0". The ORCLK is input to the multi-carrier generating circuit with the STCR instruction and register PA shift operation starts. At this time, DCL operates and is connected to the last stage of register PA because timer PT outputs initial level "H". Therefore, DCL output is input to output latch (OPL) and output as carrier wave (CARR) after T/2 because shift operation $PA_L \rightarrow PA_H \rightarrow PA_0 \rightarrow$ DCL is performed. This is the basic waveform.

When timer PT overflows and PT OUT changes to "L", DCL stops at reset state and is disconnected from register PA opposite of +1 compensation. Therefore, the PA_0 output is input to OPL and the "L" interval becomes shorter than the basic waveform by 1T. This is the compensated waveform.

When the next fall of the carrier wave occurs, PT OUT becomes "H" and the basic waveform is output. The carrier waveform is stopped with the SPCR instruction because $C2_1$ is set to "0".

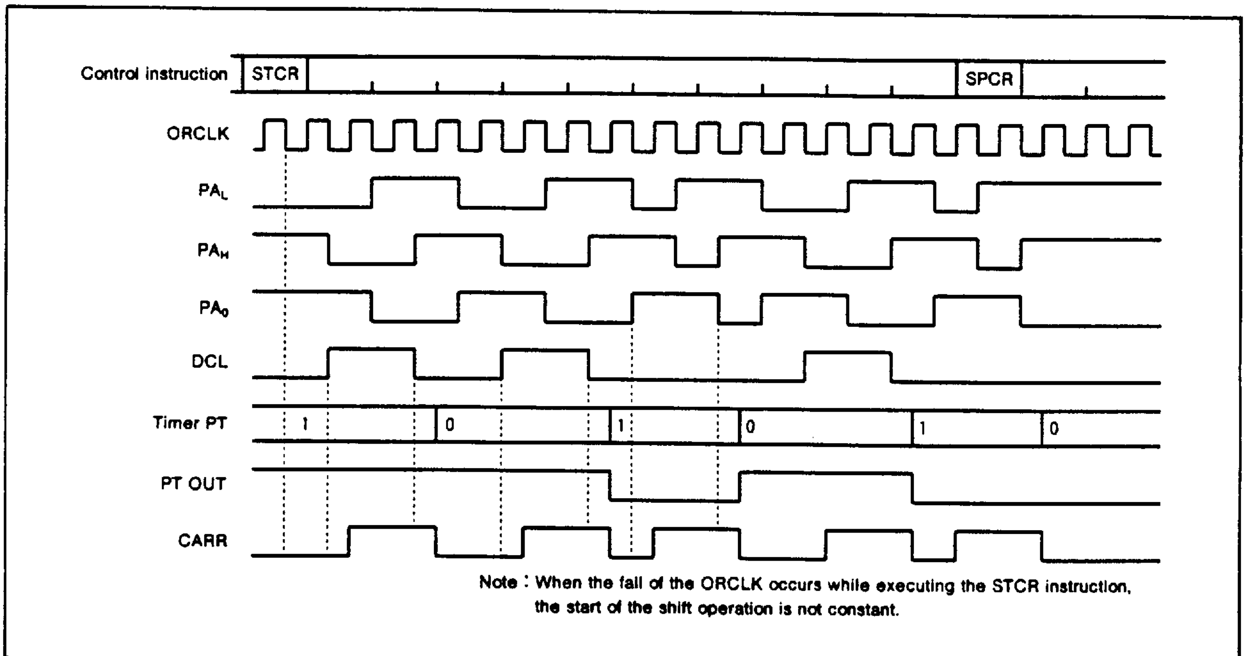


Fig. 27 Timing diagram at −1 compensation

(2) Preset register ($PA_0 \sim PA_3$)

The preset register is the high-order 4 bits of the carrier wave data register (PA) which consists of 6-bit shift register. The waveform of the carrier wave is determined by the connection levels of this register and the preset value.

Set the level number of preset register with bits 0 to 2 of the carrier wave data control register (C1) and the preset value with the TPAA instruction through register A. Set so that the waveform generated by the carrier wave data register (PA) is 1 period (both "H" and "L" are one interval).

(3) Compensation control timer (PT)

Timer PT is a 2-bit programmable timer and is used to determine the compensation period of the carrier wave. The initial level of the timer PT output (PT OUT) is "H". Timer PT down counts the fall of the carrier wave ("H" → "L"). An overflow occurs and PT OUT changes to "L" at the fall of the carrier wave after its becomes "0". Then the initial value is reloaded into timer PT and count continues. The output returns to "H" next time the carrier wave falls.

The carrier wave is compensated while this PT OUT is "L" (carrier wave compensation interval). Therefore, when n is set in timer PT, the carrier wave is compensated every n + 1 period. Data can be set simultaneously in timer PT and the reload register with the TPTA instruction.

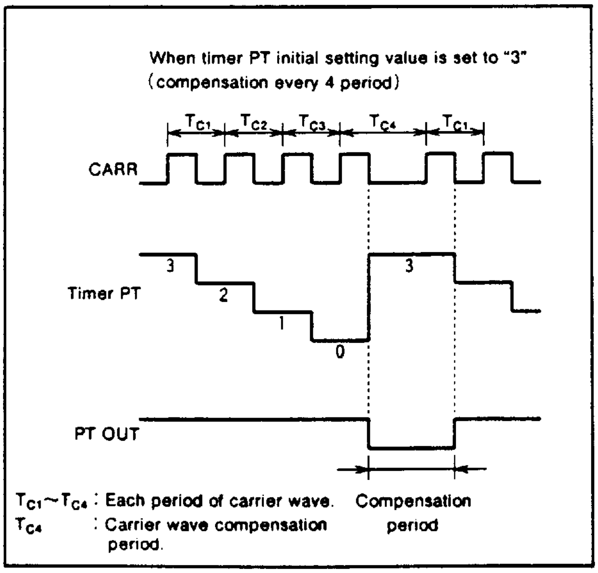


Fig. 28 Timer PT operation

(4) Data compensation latch (DCL)

The data compensation latch is a 1-bit latch with the preset value fixed to "0". The "L" interval of the carrier wave changes depending on whether or not this latch is connected to the last level of the shift register (register PA). The connection/disconnection of DCL is automatically controlled by timer PT output value (PT OUT).

Table 7 Timer PT output value and DCL connection state

		$C1_3$="0"	$C1_3$="1"
PT OUT	"H"	Connect	Disconnect
	"L"	Disconnect	Connect

Note : This table is at $C2_0$="1"

(5) Carrier wave control instruction

The carrier wave generation is controlled with the STCR instruction (generation start) and the SPCR instruction (generation stop). Whether to output the generated carrier wave from the CARR pin can be controlled by the SC3 instruction (output) and the RC3 instruction (disable output).

(6) Multi-carrier generating circuit control register and control flag

- Carrier wave data control register (C1)

  Register C1 controls the number of levels connected to the carrier wave data register (PA) and the carrier wave compensation method. Set this register with the TC1A instruction through register A.

- Carrier wave compensation control register (C2)

  Register C2 controls the carrier wave compensation function and the automatic stop function (stop with timer 1 overflow flag). Set this register with the TC2A instruction through register A.

- Carrier wave output control flag (C3)

  The C3 flag controls whether to output the generated carrier wave from the CARR pin. C3 becomes "0" and carrier wave output is disabled when the RC3 instruction is executed and C3 becomes "1" and carrier wave output is enabled when the SC3 instruction is executed.

  Even when output is disabled with this flag, carrier wave generation is possible and the carrier wave output stop interval can be counted using timer 1. This flag is set to "0" at system reset.

(7) Precautions

Take the following precautions when using the multi-carrier generating circuit.

- Precaution when starting carrier wave (CARR) generation

  The shift operation of the multi-carrier generating circuit starts in synchronization with the fall ("H"→"L") of ORCLK. However, the shift operation start timing after executing the carrier wave generation start instruction (STCR) is not constant because the instruction cycle does not match the ORCLK period.

  In addition, if the fall of ORCLK occurs during the STCR instruction execution cycle, whether register PA starts shift operation or not is undefined. If the shift operation is not started, it is started at the fall of the next ORCLK. The carrier wave output timing after starting shift operation depends on the initial setting value as described in the carrier wave compensation example.

- Precaution when stopping carrier wave (CARR) generation

  The carrier wave is stopped at the fall of the carrier wave. However, the carrier wave stop timing after executing the carrier wave stop instruction (SPCR) is not constant because the instruction cycle does not match the carrier wave period.

  In addition, if the fall of the carrier wave occurs during the SPCR instruction execution cycle, whether the carrier wave is stopped or not is undefined. If the carrier wave is not stopped, it is stopped at the fall of the next carrier wave. If the prescaler is to be stopped after stopping the carrier wave, wait one ORCLK period after the carrier wave has stopped and then stopping the prescaler.

- Precaution when restarting carrier wave (CARR) generation

  If carrier wave generation is restarted after stopping, timer PT retains the previous value without initializing. Therefore, be sure to set again timer PT (with the TPTA instruction) before restarting carrier wave generation (with the STCR instruction).

- Precaution when using the carrier wave (CARR) automatic stop function

  Carrier wave generation can be stopped ($C2_1$ = "1") with the timer 1 overflow signal using the carrier wave as the timer 1 count source ($W1_3$="1"). In this case, it is necessary to set again timer 1 (with the T1R1 instruction) if carrier wave generation is to be returned (with STCR instruction) after stopping it with a timer 1 ovreflow signal.

LCD FUNCTION

The M34550Mx-XXXFP has a built-in LCD (Liquid Crystal Display) controller/driver. When proper voltage is applied to the LCD power supply input pins and data are set in timer control register (W2, W3), timer LC, LCD control register (L1~L3), and LCD RAM, the controller/driver automatically reads the display data, controls duty and bias, and displays the data.

4 common signal output pins and 40 segment signal output pins can be used to drive the LCD to control the display of up to 160 segments (when 1/4 duty and 1/3 bias are selected). If the required number of segment pins is less than 40, SEG_{36}~SEG_{39} can be used as input ports $P4_0$~$P4_3$.

(1) Duty and bias control

There are three duty and bias combinations for displaying data on the LCD. Use bits 0 and 1 of the LCD control register (L1) to select the proper display method for the LCD panel being used.

- 1/2 duty, 1/2 bias
- 1/3 duty, 1/3 bias
- 1/4 duty, 1/3 bias

Table 8 Duty and maximum number of displayed pixels

Duty	Maximum number of displayed pixels	Used COM pins
1/2	80 segment	COM_0, COM_1 (Note)
1/3	120 segment	COM_0~COM_2 (Note)
1/4	160 segment	COM_0~COM_3

Note : Leave unused COM pins open.

(2) LCD clock control

The frame frequency for each display method can be obtained by the following formula :

$$\text{Frame frequency} = \frac{F}{n} \quad \left(\begin{array}{l} F: \text{LCD clock frequency} \\ 1/n: \text{Duty} \end{array}\right)$$

The LCD clock is determined by the setting value of the timer 2 count source selection bit ($W2_0$), LCD clock frequency divider circuit control bit ($W3_0$, $W3_1$), and timer LC. Therefore, the frequency (F) of the LCD clock is obtained by the following formula :

- When using the prescaler output (frequency divided by 8 output) as timer 2 count source ($W2_0$=1)

$$F = \frac{\text{Clock frequency}}{8} \times \frac{1}{16} \times \frac{1}{m} \times \frac{1}{LC+1} \times \frac{1}{2}$$

- When using $f(X_{CIN})$ as timer 2 count source ($W2_0$=0)

$$F = f(X_{CIN}) \times \frac{1}{16} \times \frac{1}{m} \times \frac{1}{LC+1} \times \frac{1}{2}$$

$$\left(\begin{array}{ll} \text{Clock frequency} : f(X_{IN}) \text{ or } f(X_{CIN}) & \\ m : 1, 2, 4 & LC : 0 \sim 15 \end{array}\right)$$

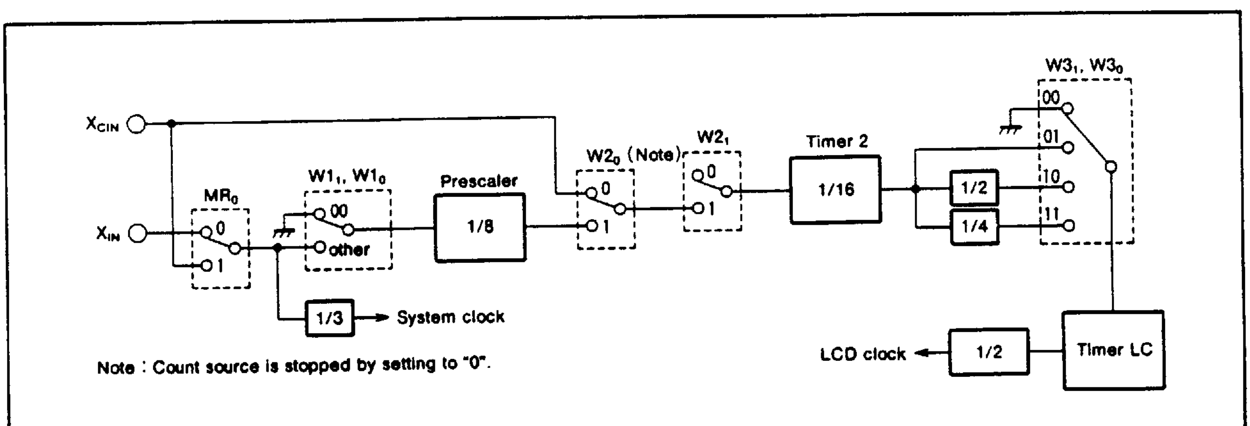


Fig. 29 LCD clock control circuit

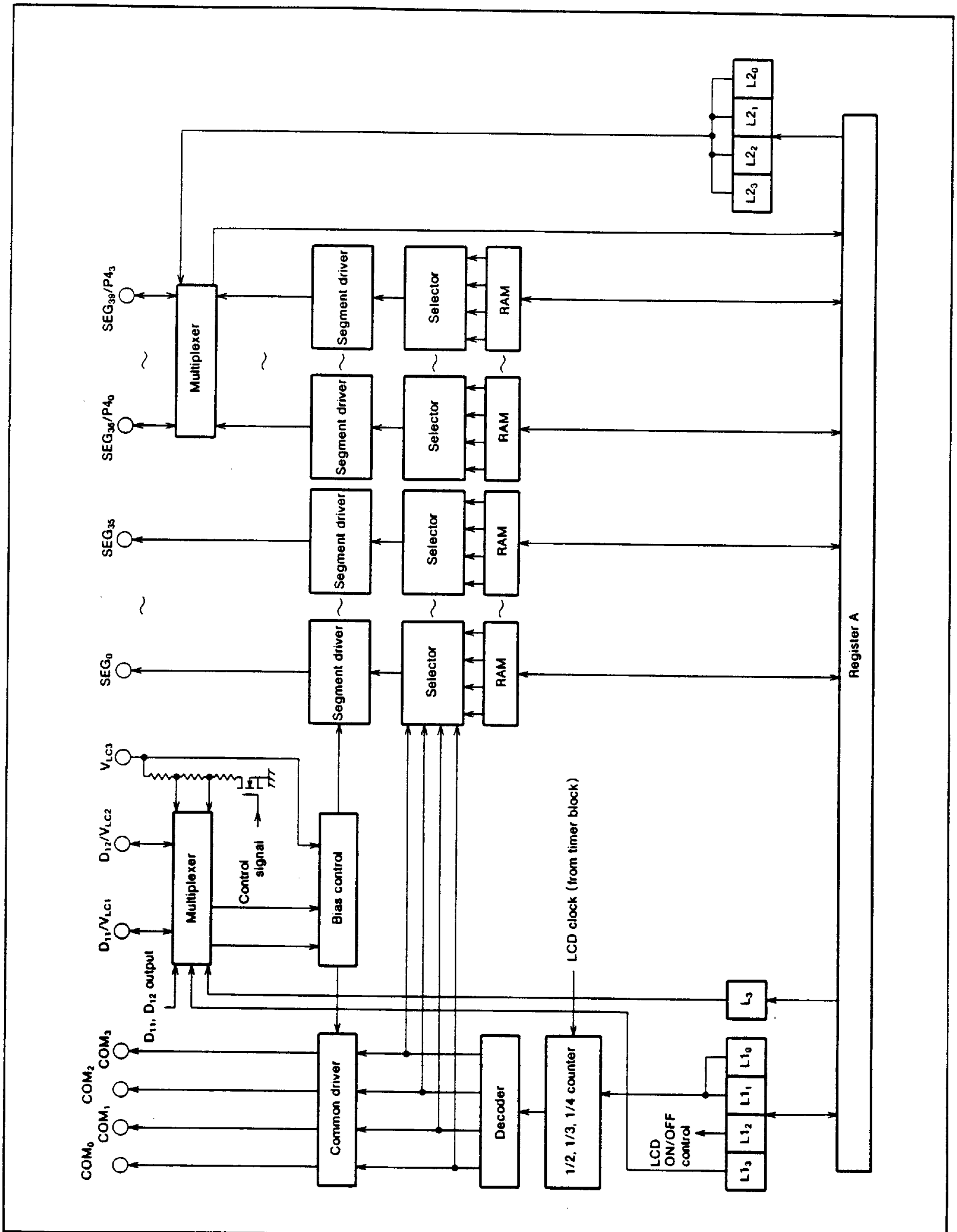


Fig. 30 LCD controller/driver structure

(Bit 3)			(Bit 0)
$L1_3$	$L1_2$	$L1_1$	$L1_0$

LCD control register L1

(at reset : 0000_2, at power down : retain state, R/W)

LCD duty and bias selection bit			
$L1_1$	$L1_0$	Duty	Bias
0	0	This is not available	
0	1	1/2	1/2
1	0	1/3	1/3
1	1	1/4	1/3

LCD ON/OFF bit	
0	Off
1	On

LCD power supply dividing resistance control bit	
0	Connecting internal dividing resistance to LCD power circuit
1	Disconnecting internal dividing resistance from LCD power circuit

(Bit 3)			(Bit 0)
$L2_3$	$L2_2$	$L2_1$	$L2_0$

LCD control register L2

(at reset : 0000_2, at power down : retain state, W)

$SEG_{36}/P4_0$ pin function switch bit	
0	SEG_{36}
1	$P4_0$

$SEG_{37}/P4_1$ pin function switch bit	
0	SEG_{37}
1	$P4_1$

$SEG_{38}/P4_2$ pin function switch bit	
0	SEG_{38}
1	$P4_2$

$SEG_{39}/P4_3$ pin function switch bit	
0	SEG_{39}
1	$P4_3$

L3

LCD control register L3

(at reset : 0_2, at power down : retain state, W)

D_{12}, D_{11}/V_{LC2}, V_{LC1} pin function switch bit	
0	D_{12}, D_{11}
1	V_{LC2}, V_{LC1}

Fig. 31 LCD control register

(3) LCD RAM

The RAM contains areas corresponding to the liquid crystal display. When "1" is written to this LCD RAM, the display pixel corresponding to the bit is displayed automatically.

Z	1											
X	4				5				6			
Y \ Bit	3	2	1	0	3	2	1	0	3	2	1	0
8	SEG_0	SEG_0	SEG_0	SEG_0	SEG_8	SEG_8	SEG_8	SEG_8	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}
9	SEG_1	SEG_1	SEG_1	SEG_1	SEG_9	SEG_9	SEG_9	SEG_9	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}
10	SEG_2	SEG_2	SEG_2	SEG_2	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}
11	SEG_3	SEG_3	SEG_3	SEG_3	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}
12	SEG_4	SEG_4	SEG_4	SEG_4	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}
13	SEG_5	SEG_5	SEG_5	SEG_5	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}
14	SEG_6	SEG_6	SEG_6	SEG_6	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}
15	SEG_7	SEG_7	SEG_7	SEG_7	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}
COM	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Z	1							
X	7				8			
Y \ Bit	3	2	1	0	3	2	1	0
8	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{32}
9	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{33}	SEG_{33}	SEG_{33}	SEG_{33}
10	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{34}	SEG_{34}	SEG_{34}	SEG_{34}
11	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{35}	SEG_{35}	SEG_{35}	SEG_{35}
12	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{36}	SEG_{36}	SEG_{36}	SEG_{36}
13	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{37}	SEG_{37}	SEG_{37}	SEG_{37}
14	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{38}	SEG_{38}	SEG_{38}	SEG_{38}
15	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{39}	SEG_{39}	SEG_{39}	SEG_{39}
COM	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Fig. 32 LCD RAM map

(4) LCD control register

- LCD control register (L1)

  Register L1 controls the combination of duty and bias, LCD on/off, and internal dividing resistance connection. Set this register with the TL1A instruction through register A. The TAL1 instruction can also be used to transfer the contents of register L1 to register A.

- LCD control register (L2)

  Register L2 controls pins $SEG_{36}/P4_0 \sim SEG_{39}/P4_3$ function. Set this register with the TL2A instruction through register A.

- LCD control register (L3)

  Register L3 controls pins D_{11}/V_{LC1} and D_{12}/V_{LC2} function. Set this register with the TL3A instruction through register A.

(5) LCD drive waveform

Fig. 33 shows the drive waveform example for each display method. When "1" is written in the LCD RAM, the voltage difference between the corresponding common pin and segment pin becomes | V_{LC3} | and the display pixel at the cross section turns on.

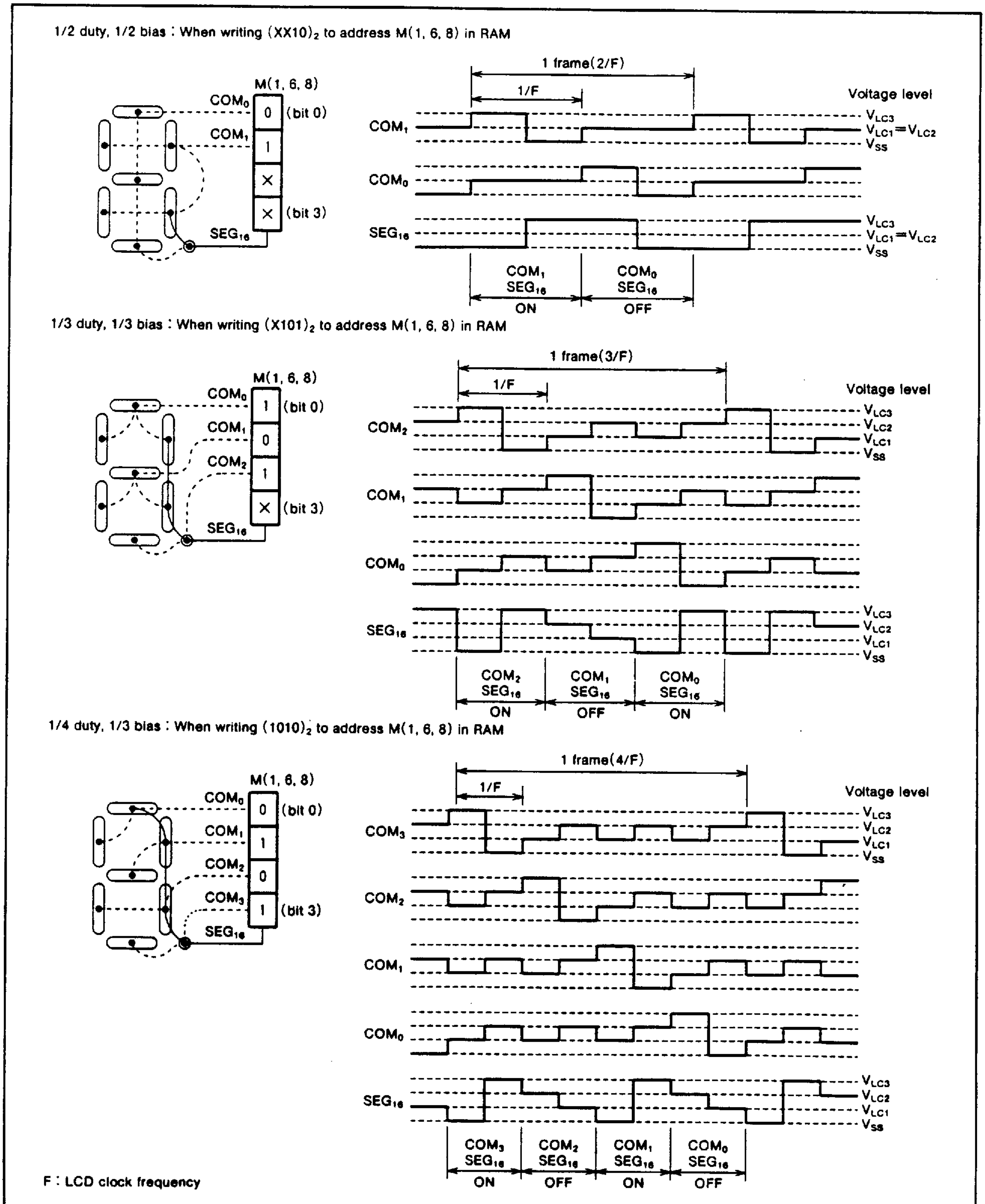


Fig. 33 Drive wave example

(6) LCD power supply
The M34550Mx-XXXFP has a built-in LCD dividing resistance that can be disconnected by software. Select whether to connect this internal dividing resistance or not and select the LCD power circuit appropriate for the LCD panel being used according to the combination of 3 items in the following Table 9. LCD power supply control.

Table 9 LCD power supply control

Control Item	Control Bit	
Connect/disconnect internal dividing resistance to LCD power supply.	$L1_3$	
	Connecting	0
	Disconnecting	1
Connect/disconnect pins D_{11}/V_{LC1} and D_{12}/V_{LC2} to LCD power supply.	L3	
	Disconnecting	0
	Connecting	1
Use 1/2 or 1/3 bias.	$L1_1$	
	1/2 bias	0
	1/3 bias	1

- When connecting the internal dividing resistance and disconnecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2} [$L1_3$=0, L3=0]
In this case, 0~V_{LC3} (V) voltage is applied to the LCD panel. Apply voltage between 2.2V and V_{DD} to the V_{LC3} pin. (circuit example a)

- When connecting the internal dividing resistance and connecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2} [$L1_3$=0, L3=1]
In this case, internally generated divided voltage is output from pins D_{11}/V_{LC1} and D_{12}/V_{LC2}. Therefore, the impedance of the LCD power can be reduced by externally connecting a capacitor between the pins D_{11}/V_{LC1} and D_{12}/V_{LC2}. Apply voltage between 2.2V and V_{DD} to the V_{LC3} pin.
(1/3 bias : circuit example b, 1/2 bias : circuit example c)

- When disconnecting the internal dividing resistance and connecting pins D_{11}/V_{LC1} and D_{12}/V_{LC2} [$L1_3$=1, L3=1]
This is the external power input mode. Apply the following voltage to each LCD power input pins.
When using 1/3 bias : ($2.2V \leq V_{LC3} \leq V_{DD}$)
$V_{LC2}=2/3\ V_{LC3}$, $V_{LC1}=1/3\ V_{LC3}$

When using 1/2 bias : ($2.2V \leq V_{LC3} \leq V_{DD}$)
$V_{LC2}=V_{LC1}=1/2\ V_{LC3}$

(1/3 bias : circuit example d, 1/2 bias : circuit example e)

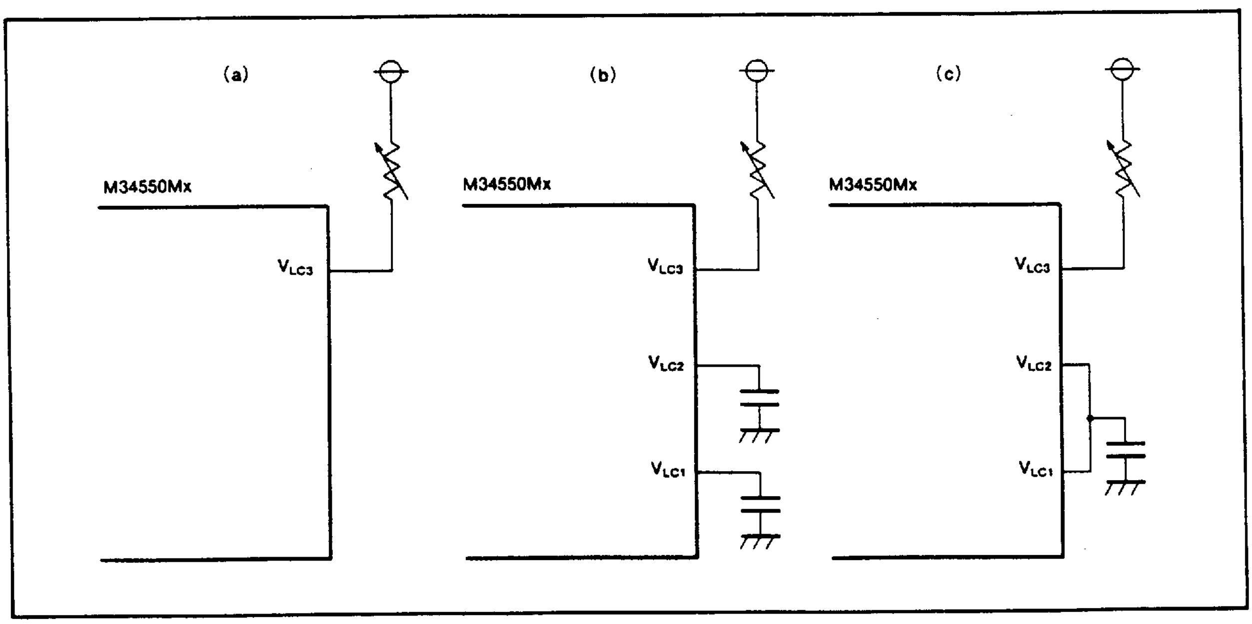


Fig. 34 LCD power circuit example

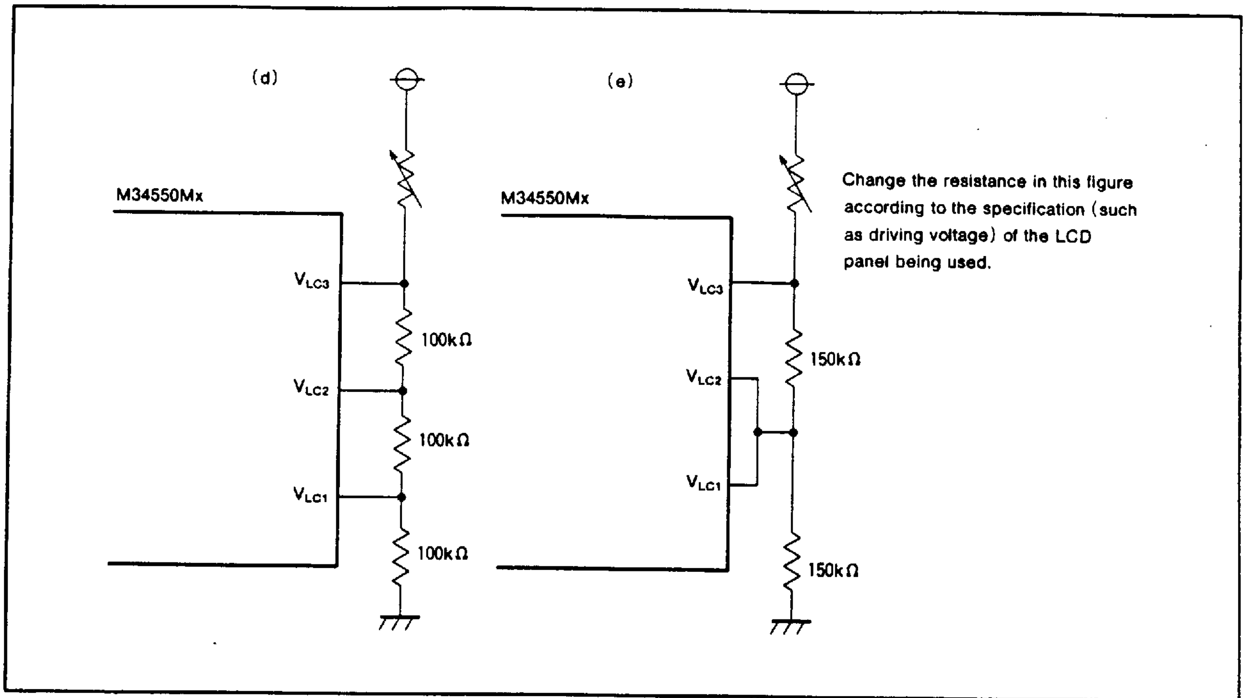


Fig. 35 LCD power circuit example (continued)

(7) LCD display method

The connection example in Fig. 36 shows how to set the LCD control register and the drive waveform when displaying the number "9".

1. Select the duty and bias combination with bits 0 and 1 of the register L1.
2. Set the built-in resistance with bit 3 of the register L1 and register L3.
3. Switch pins $SEG_{36}/P4_0$ and $SEG_{37}/P4_1$ to segment output ports with bits 0 and 1 of the register L2.
4. Write $(1011)_2$ and $(0111)_2$ in RAM addresses M (1, 8, 12) and M (1, 8, 13) as shown in Fig. 38.
5. Character "9" is displayed by setting bit 2 of the register L1 to "1".

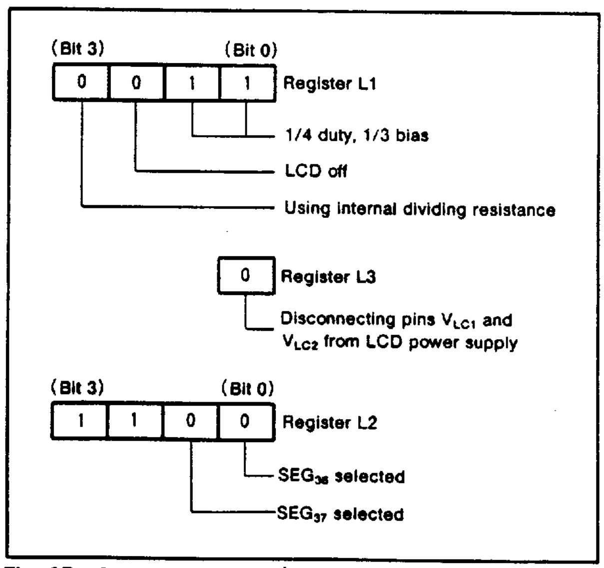


Fig. 37 Setting registers (before LCD on)

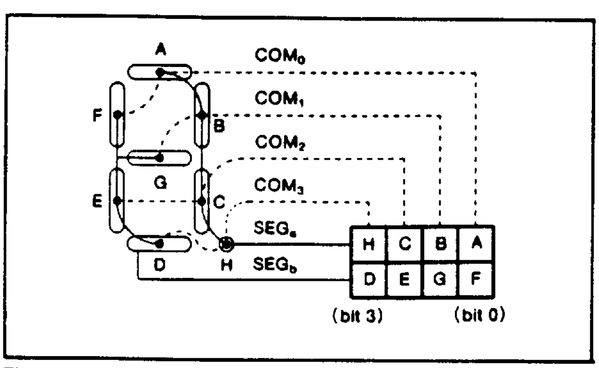


Fig. 36 LCD connection example

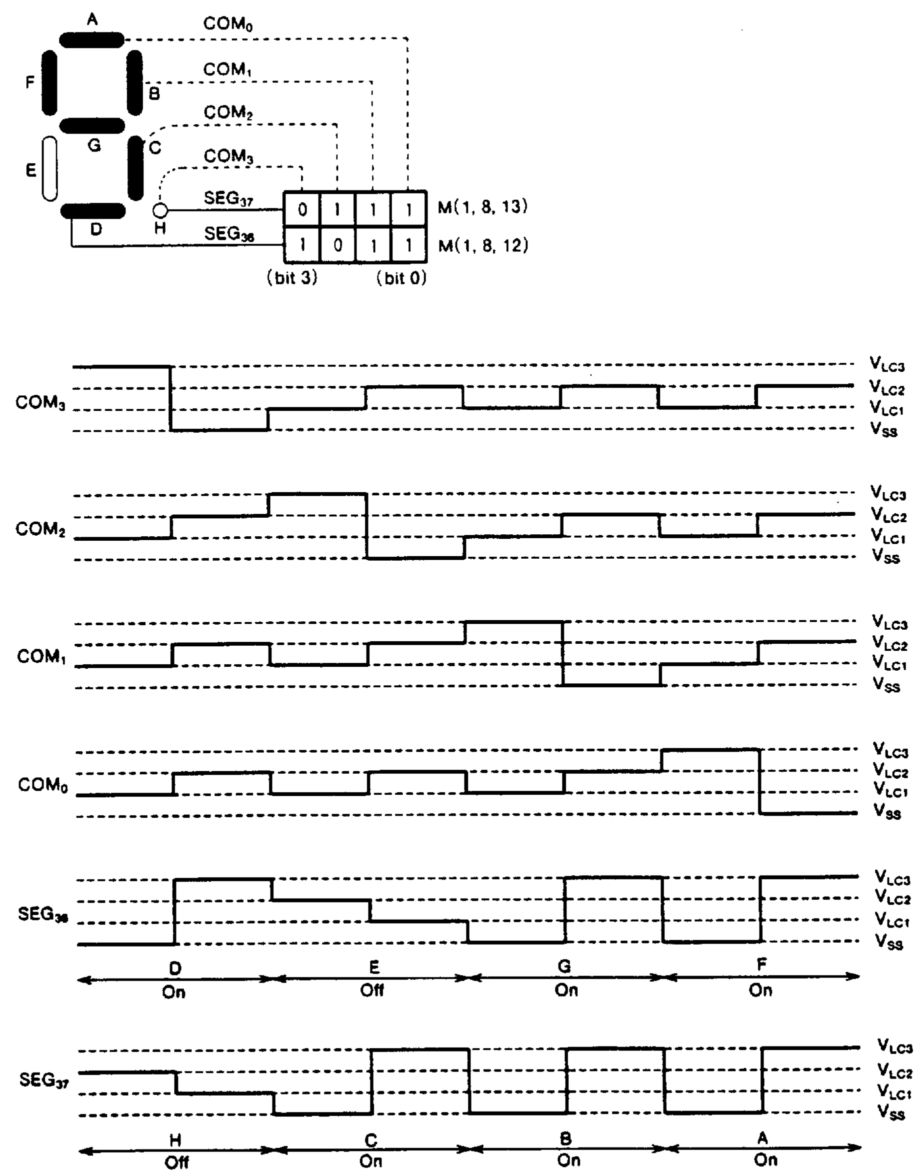


Fig. 38 Display pattern example and drive waveform example

RESET FUNCTION

System reset is performed regardless of the microcomputer state when "L" level is applied to the RESET pin for at least 1 machine cycle. Then when "H" level is applied to the RESET pin, program starts from address 0 in page 0.

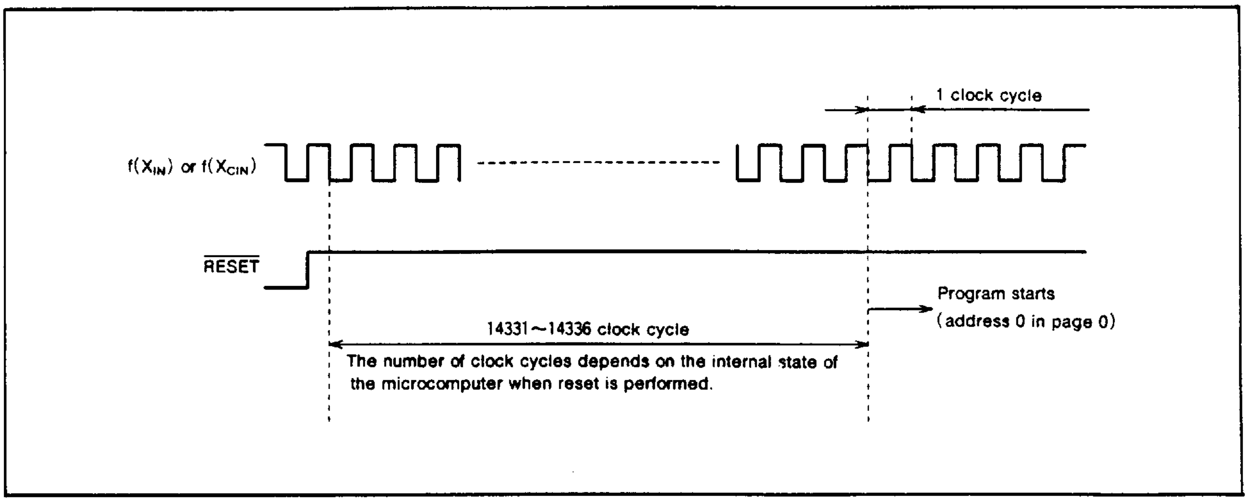


Fig. 39 Timing of reset removing

(1) Power-on reset

Reset can be performed automatically at power-on (power-on reset) by connecting a resistance, diode, and a capacitor to the RESET pin. Connect the RESET pin and the external circuit at the shortest distance.

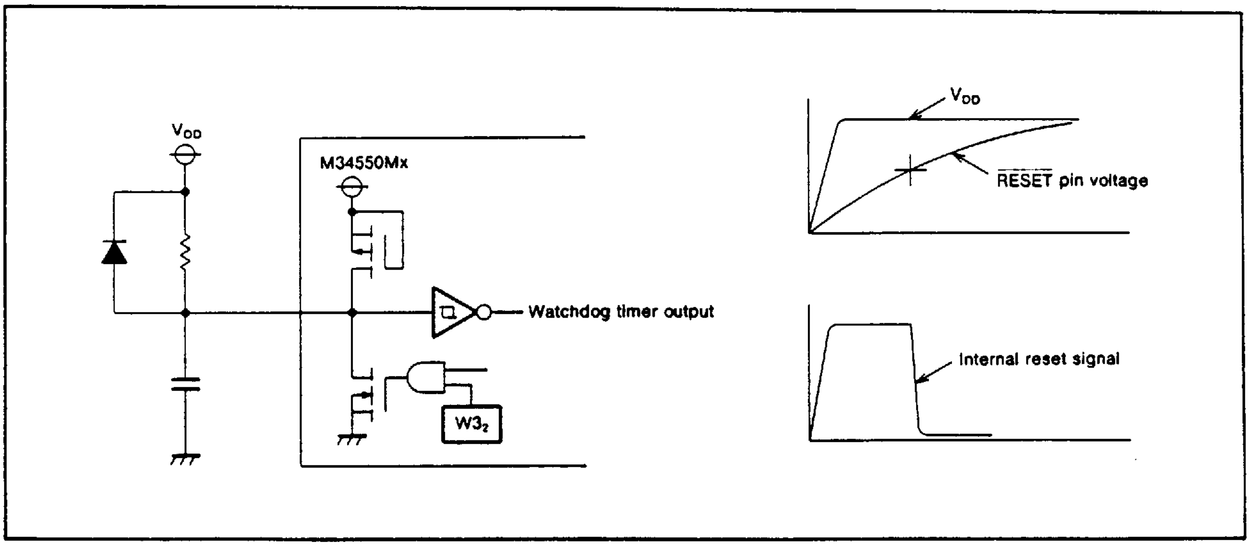


Fig. 40 Power-on reset circuit example

(2) Internal state at reset
Fig. 41 shows the internal state and port state at reset (they are the same after reset is removed).

• Program counter (PC)	0 0 0 0 0 0 0 0 0 0 0 0 0 0	Address 0 in page 0 is set.
• Interrupt enable flag (INTE)	0	(Interrupt disabled)
• Power down flag (P)	0	
• External interrupt request flag (EXF0)	0	
• Interrupt control register (V1)	0 0 0 0	(Interrupt disabled)
• Interrupt control register (I1)	0 0 0 0	(Pull-up transistor OFF)
• Clock control register (MR)	0 0 0	(X_{IN} selected)
• Timer 1 interrupt request flag (T1F)	0	
• Timer 2 overflow flag (T2F)	0	
• Timer 3 interrupt request flag (T3F)	0	
• Watchdog timer flag (WDF)	0	
• Timer control register (W1)	0 0 0 0	(Prescaler and timer 1 stop)
• Timer control register (W2)	0 0 0 0	(Timer 2 and timer 3 stop)
• Timer control register (W3)	0 0 0 0	(Watchdog timer disabled) (BEEP output disabled)
• Carrier wave data control register (C1)	0 0 0 0	
• Carrier wave compensation control register (C2)	0 0	
• Carrier wave output control flag (C3)	0	(Carrier wave output disabled)
• LCD control register (L1)	0 0 0 0	(LCD off)
• LCD control register (L2)	0 0 0 0	(Segment driver selected)
• LCD control register (L3)	0	
• Carry flag (CY)	0	
• Register A	0 0 0 0	
• Register B	0 0 0 0	
• Register D	× × ×	
• Register E	× × × × × × × ×	
• Data pointer X	0 0 0 0	
• Data pointer Y	0 0 0 0	
• Data pointer Z	× ×	
• Stack pointer (SP)	1 1 1	

"X" indicates undefined.

Fig. 41 Internal state at reset

Table 10 Port state at reset

Name	Function at reset	State at reset
$D_0 \sim D_7$	$D_0 \sim D_7$	High impedance state (Note 1)
D_8, D_9	D_8, D_9	High impedance state (Note 1)
D_{10}/BEEP	D_{10}/BEEP	High impedance state (Note 1)
D_{11}/V_{LC1}, D_{12}/V_{LC2}	D_{11}, D_{12}	High impedance state (Note 1)
$P0_0 \sim P0_3$	$P0_0 \sim P0_3$	"H" (V_{DD}) level (Note 1)
$P1_0 \sim P1_3$	$P1_0 \sim P1_3$	"H" (V_{DD}) level (Note 1)
$P2_0 \sim P2_3$	$P2_0 \sim P2_3$	High impedance state
$P3_0$/INT	$P3_0$	High impedance state (Note 2)
$P3_1$	$P3_1$	High impedance state (Note 2)
$SEG_{36}/P4_0 \sim SEG_{39}/P4_3$	$SEG_{36} \sim SEG_{39}$	V_{LC3} level
$SEG_0 \sim SEG_{35}$	$SEG_0 \sim SEG_{35}$	V_{LC3} level
$COM_0 \sim COM_3$	$COM_0 \sim COM_3$	V_{LC3} level
CARR	CARR	"L" (V_{SS}) level

Notes 1. Output latch is set to "1".
2. Pull-up transistor is turned OFF.

POWER DOWN FUNCTION

The M34550Mx-XXXFP has two power down functions.

- Power down 1 (clock operating mode)
  POF instruction
- Power down 2 (RAM back-up mode)
  POF2 instruction

Power down is performed by executing each instruction. The start condition is different between these power downs and normal reset.

- Return from power-down state
  Warm start condition
- Return from reset state
  Cold start codition

(1) Power down 1 (clock operating mode)
The following functions and states are retained after a power down with the POF instruction.
- RAM
- Reset circuit
- X_{CIN}~X_{COUT} oscillation
- LCD display
- Timer 2, timer 3

(2) Power down 2 (RAM back-up mode)
The following function and state are retained after a power down with the POF2 instruction.
- RAM
- Reset circuit

Unlike power down 1, all oscillations stop with power down 2.

(3) Warm start condition
The system returns from the power-down state when :
- external wakeup signal is input
- timer 3 interrupt request flag is set
  in power down 1 state or when :
- external wakeup signal is input
  in power down 2 state. In either case, the CPU starts from address 0 in page 0 after returning. In this case, the P flag is "1".

(4) Cold start condition
The CPU starts from address 0 in page 0 when :
- reset pulse is input
- reset by watchdog timer.

In this case, the P flag is "0".

Table 11 Functions and states retained at power down

Function	Power down	
	Mode 1	Mode 2
Registers A, B Program counter (PC) Stack pointer (SP)(Note 2) Carry flag (CY)	×	×
Contents of RAM	○	○
Port level	○	○
Clock control register (MR)	○	○
Timer control register (W1)	×	×
Timer control registers (W2, W3)	○	○
Interrupt control register (V1)	×	×
Interrupt control register (I1)	○	○
Multi-carrier generating circuit control registers and flag (C1, C2, C3)	×	×
LCD display function	○	(Note 3)
LCD control registers (L1, L2, L3)	○	○
Timer LC	○	(Note 4)
Timer 2 function	○	(Note 4)
Timer 3 function	○	(Note 4)
External interrupt request flag (EXF0)	×	×
Timer 2 overflow flag (T2F)	○	(Note 4)
Timer 3 interrupt request flag (T3F)	○	(Note 4)
Watchdog timer flag (WDF)	○	(Note 4) (Note 5)
Interrupt enable flag	×	×

Notes 1. "O" indicates that the function can be retained and "X" indicates that the function is initialized.
Registers and flags other than the above are undefined at power down and initialize after power up.
2. The stack pointer (SP) points to the stack register and is initialized to "7" at power down.
3. The LCD goes off.
4. The state of the timer is undefined.
5. Stop the watchdog timer by software and then execute the POF2 instruction.

(5) Identification of the start condition

The start condition (warm start or cold start) can be identified by checking the P flag with the SNZP instruction. The warm start condition (timer 3 or external wakeup signal) can be identified by checking the state of the T3F flag.

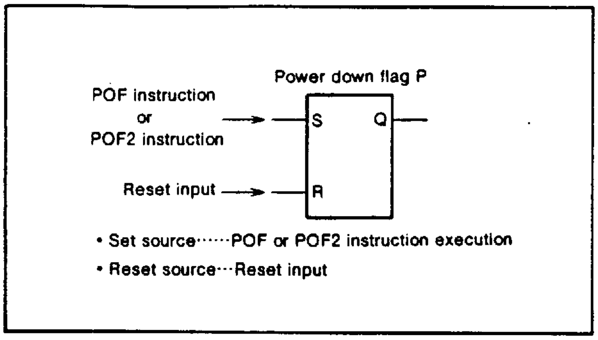


Fig. 42. Set source and reset source of P flag

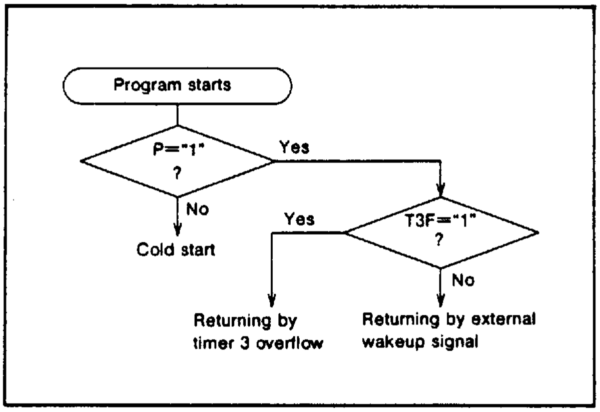


Fig. 43 Start condition identification example using the SNZP instruction

(6) State transition

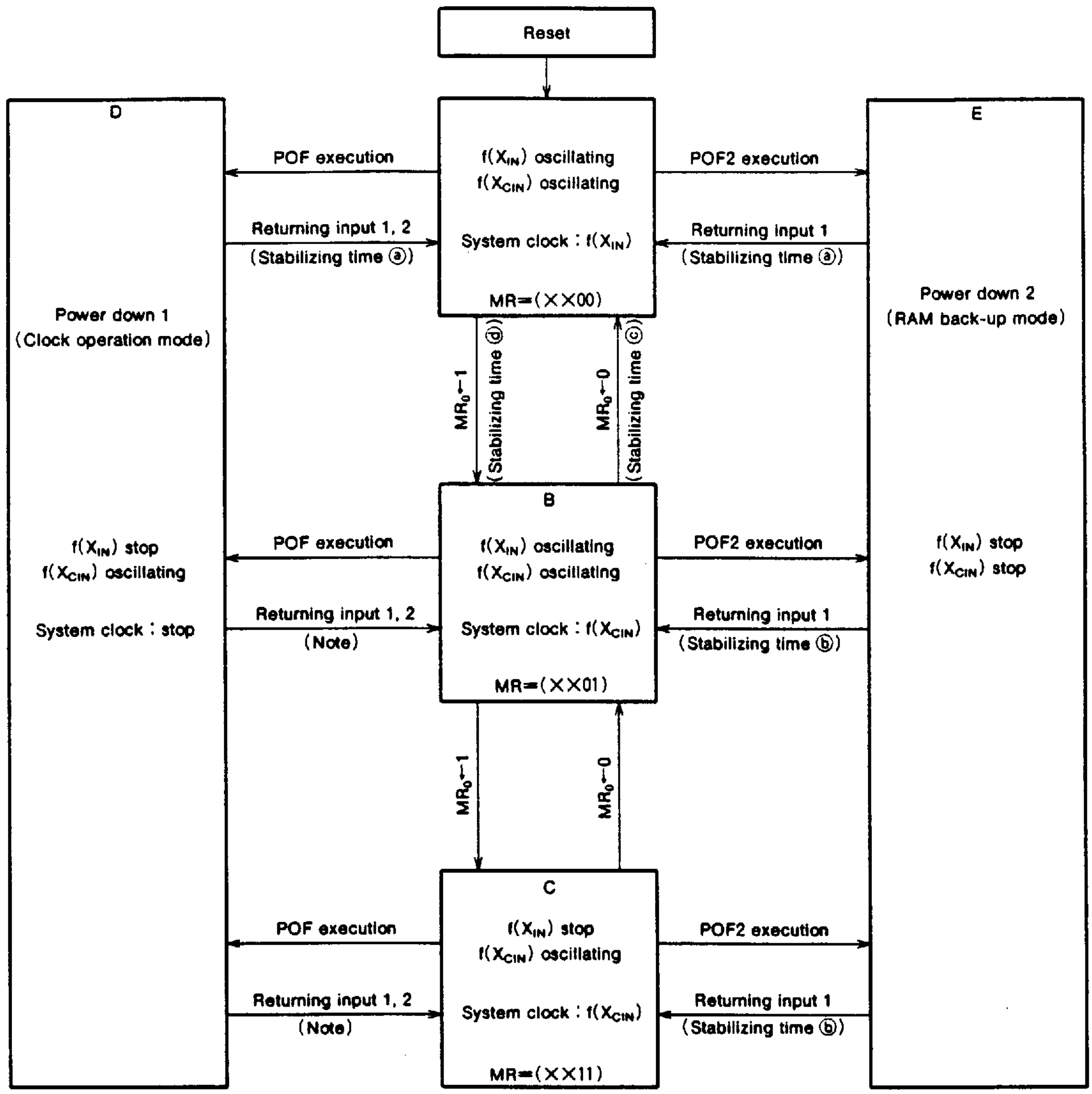
State transition is described using Fig. 44.

The state is A after a cold start from the reset state. In state A, bit 0 (MR_0) and bit 1 (MR_1) of the clock control register are both "0" and $f(X_{IN})$ is selected as the system clock.

To go from state A to low-speed mode state C, first set MR_0 to "1" (state B) to switch the system clock and then set MR_1 to "1" (state C) to stop $f(X_{IN})$ oscillation. However, after a cold start, do not use $f(X_{CIN})$ as system clock and count source until $f(X_{CIN})$ oscillation sufficiently stabilizes (same as when returning from state A with the POF2 instruction).

The power down 1 (state D) or power down 2 (state E) state can be entered from state A, B, C with the POF or POF2 instruction. When returning, the state returns to the state before executing the POF or POF2 instruction, but stabilizing time is generated automatically according to the state as shown in the figure because the oscillation stabilizing time depends on the state of $f(X_{IN})$ or $f(X_{CIN})$.

To go from state C to state A, first set MR_1 to "0" to go to state B, generate sufficient time for $f(X_{IN})$ oscillation to stabilize with software, and then set MR_0 to "0" to go to state A. Also generate sufficient time for $f(X_{IN})$ oscillation to stabilize with software, and then set MR_0 to "0" to go to state A after returning from state B with the POF instruction.



Stabilizing time a : Time required for $f(X_{IN})$ oscillation to stabilize is generated automatically by hardware.

Stabilizing time b : Time required for $f(X_{CIN})$ oscillation to stabilize is generated automatically by hardware.

Stabilizing time c : When switching state from C→B→A or D→B→A, generate the time for $f(X_{IN})$ oscillation to stabilize in state B by software.

Stabilizing time d : The $f(X_{CIN})$ oscillation may not be stable immediately after a cold start or immediately after returning from power down 2. Generate the time for $f(X_{CIN})$ oscillation to stabilize in state A by software.

Returning input 1 : External wakeup signal ($P0_0$~$P0_3$, $P1_0$~$P1_3$, $P2_0$, $P2_1$, $P3_0$)

Returning input 2 : Timer 3 interrupt request flag

Note : The microcomputer starts operation after counting $f(X_{CIN})$ 27 to 34 times.

Fig. 44 State transition diagram

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(7) Return signal
The external wakeup signal or the timer 3 interrupt request flag is used to return from power down 1. External wakeup signal is used to return from power down 2 because the oscillator is stopped. Table 12 shows the return condition each return source.

Table 12 Return source and condition

Return Source		Return Condition	Note
External wakeup signal	Ports P0, P1	Returning by external falling edge input ("H"→"L").	Set all ports P0 and P1 to "H" level before going into power down state because the falling edge detection circuit shares ports P0 and P1.
External wakeup signal	Ports $P2_0$, $P2_1$	Returning by external falling edge input ("H"→"L").	Set both ports $P2_0$ and $P2_1$ to "H" level before going into power down state because the falling edge detection circuit shares ports $P2_0$ and $P2_1$.
External wakeup signal	Ports $P3_0$/INT (Note)	Returning by external "H" level or "L" level input. In this case, EXF0 flag is not set.	Select the return level ("L" level or "H" level) with bit 2 of the interrupt control register (I1) before going into power down state according to the external state.
Timer 3 interrupt request flag		Returning when timer 3 overflows and T3F flag is set to "1".	Allowed only for return from power down 1 (POF instruction). However, if the POF or POF2 instruction is executed when T3F = "1", return condition is recognized and return is performed.

Note : The $P3_0$/INT pin has a built-in pull-up transistor that can be turned ON/OFF by program. When going into power down state with the $P3_0$/INT pin set to "L" level, current flows from the $P3_0$/INT pin if this pull-up transistor is ON. Therefore, systems that required power consumption to be kept low should turn off this pull-up transistor by program ($I1_0$ = "0") before going into power down state. However, when pull-up transistor is necessary to get the return level "H", pull-up transistor can be temporarily ON by using timer 2 output signal ($I1_0$ = "0", $I1_3$ = "1")

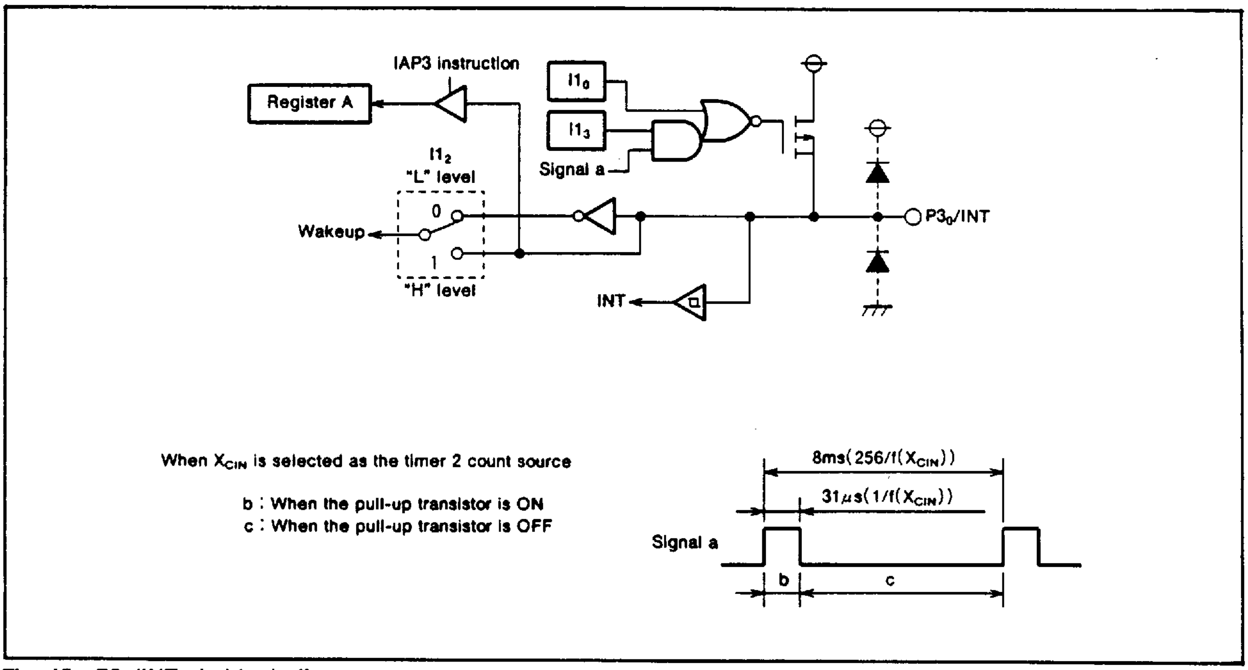


Fig. 45 $P3_0$/INT pin block diagram

(8) Power down function control register

- Interrupt control register (I1)

Register I1 turns pins $P3_0$/INT and $P3_1$ pull-up transistors ON/OFF and controls the return signal level of the $P3_0$/INT pin. Set the contents of this register with the TI1A instruction through register A. The TAI1 instruction can also be used to transfer the contents of register I1 to register A.

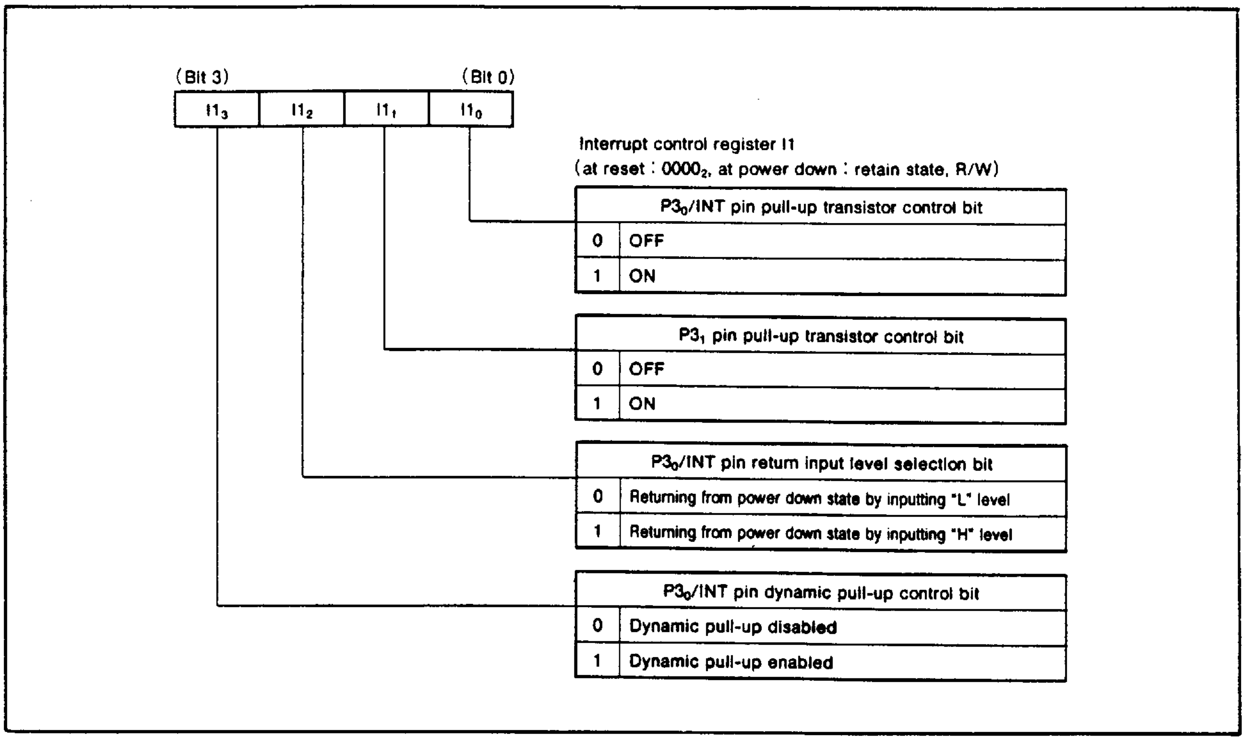


Fig. 46 Power down function control register

CLOCK CONTROL

The clock control circuit consists of the following circuits.

- $f(X_{IN})$ clock generating circuit
- $f(X_{CIN})$ clock generating circuit
- Clock generating termination control circuit
- Control circuit for return from power down state

System clock selection and clock oscillation start/stop are controlled with the clock control register (MR). The $f(X_{IN})$ clock is selected at cold start, but it can be switched to the $f(X_{CIN})$ clock with the system clock selection bit (MR_0). At warm start, the clock selected just before power down is used. The actual system clock is signal divided by 3 of the selected clock ($f(X_{IN})/3$ or $f(X_{CIN})/3$).

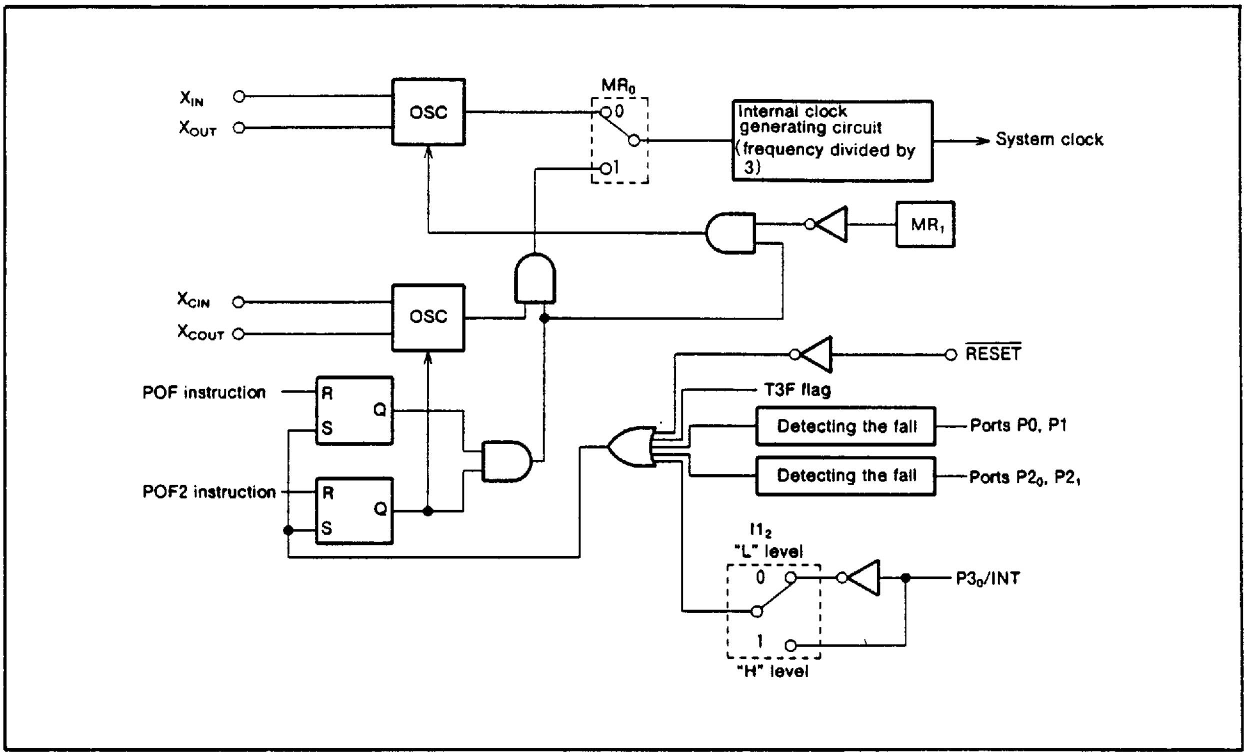


Fig. 47 Clock control circuit structure

(Bit 2) (Bit 0)

MR₂	MR₁	MR₀

Clock control register MR

(at reset : 000_2, at power down : retain state, R/W)

MR₀:

System clock selection bit	
0	$f(X_{IN})$
1	$f(X_{CIN})$

MR₁:

$f(X_{IN})$ clock oscillating circuit control bit	
0	Oscillation enabled
1	Oscillation disabled

MR₂: Not used (this bit has no function)

Fig. 48 Registers related clock control

(1) $f(X_{IN})$ clock generating circuit
Clock signal ($f(X_{IN})$) is obtained by externally connecting a ceramic oscillator. Connect this external circuit to pins X_{IN} and X_{OUT} at the shortest distance. A feedback resistance is built-in between pins X_{IN} and X_{OUT}.
When external clock signal is input, connect the clock source to X_{IN} and leave X_{OUT} open. When using an external clock, the maximum clock oscillating frequency is 500kHz. Use the external clock at 30 to 70% duty ratio.

(2) $f(X_{CIN})$ clock generating circuit
Clock signal ($f(X_{CIN})$) is obtained by externally connecting a crystal oscillator. Connect this external circuit to pins X_{CIN} and X_{COUT} at the shortest distance. A feedback resistance is built-in between pins X_{CIN} and X_{COUT}.
Unlike the $f(X_{IN})$ generating circuit, external clock signal cannot be used for this circuit.

ROM ordering method
Please submit the information described below when ordering Mask ROM.

(1) M34550M6-XXXFP ROM Order Confirmation Form or M34550M8-XXXFP ROM Order Confirmation Form ····· 1
(2) Data to be written into mask ROM ·················· EPROM (three sets containing the identical data)
(3) Mark Specification Form ·· 1

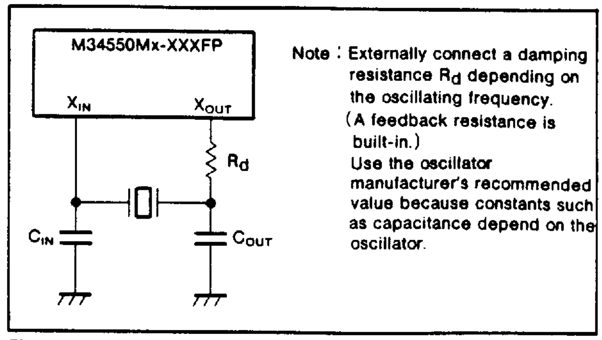


Fig. 49 Ceramic oscillator external circuit

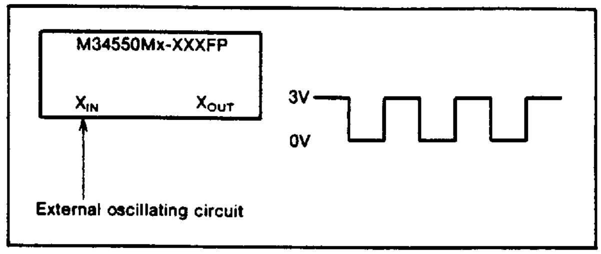


Fig. 50 External clock input circuit

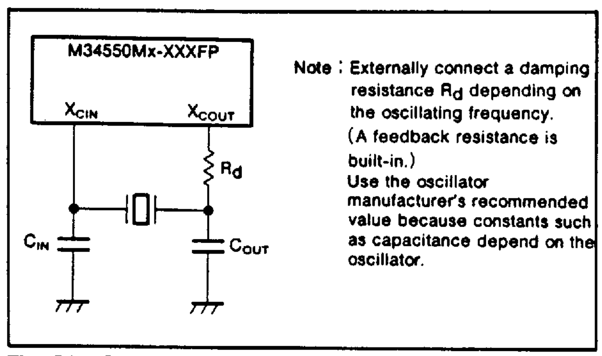


Fig. 51 Crystal oscillation external circuit

LIST OF PRECAUTIONS

(1) Noise and latch-up prevention
Connect a capacitor (approx. 0.1μF) between pins V_{DD} and V_{SS} at the shortest distance using relatively thick wire to prevent noise and latch up.

(2) Prescaler
Be sure to stop the prescaler before changing the frequency dividing ratio of the prescalar.

(3) Timer 1, 2, 3
Be sure to stop counting of each timer before switching the timer 1, 2, or 3 count source. To read the data from timer 3, stop counting of timer 3 and then execute the TAB3 instruction.

(4) D_{10}/BEEP pin
To start the buzzer drive output, set the frequency (bits 0 and 1 of the register W3) and then start output.
When changing the buzzer drive output frequency or using this pin as port D_{10}, first stop the buzzer drive output, wait for 1 cycle of the buzzer drive output, and then set the frequency or start using as port D_{10}.

(5) Multi-carrier generating circuit

- Precaution when starting carrier wave (CARR) generation
The shift operation of the multi-carrier generating circuit starts in synchronization with the fall ("H"→"L") of ORCLK. However, the shift operation start timing after executing the carrier wave generation start instruction (STCR) is not constant because the instruction cycle does not match the ORCLK period.
In addition, if the fall of ORCLK occurs during the STCR instruction execution cycle, whether register PA starts shift operation or not is undefined. If the shift operation is not started, it is started at the fall of the next ORCLK. The carrier wave output timing after starting shift operation depends on the initial setting value as described in the carrier wave compensation example.
- Precaution when stopping carrier wave (CARR) generation
The carrier wave is stopped at the fall of the carrier wave. However, the carrier wave stop timing after executing the carrier wave stop instruction (SPCR) is not constant because the instruction cycle does not match the carrier wave period.
In addition, if the fall of the carrier wave occurs during the SPCR instruction execution cycle, whether the carrier wave is stopped or not is undefined. If the carrier wave is not stopped, it is stopped at the fall of the next carrier wave.
If the prescaler is to be stopped after stopping the carrier wave, wait one ORCLK period after the carrier wave has stopped and then stop the prescaler.
- Precaution when restarting carrier wave (CARR) generation
If carrier wave generation is restarted after stopping, timer PT retains the previous value without initializing. Therefore, be sure to set again timer PT (with the TPTA instruction) before restarting carrier wave generation (with the STCR instruction).
- Precaution when using the carrier wave (CARR) automatic stop function
Carrier wave generation can be stopped ($C2_1$ = "1") with the timer 1 overflow signal using the carrier wave as the timer 1 count source ($W1_3$="1"). In this case, it is necessary to set again timer 1 (with the T1R1 instruction) if carrier wave generation is to be returned (with the STCR instruction) after stopping it with a timer 1 overflow signal.

(6) Built-in PROM version precautions
The operating power voltage of the built-in EPROM version (M34550E8FS) and the one-time programmable version (M34550E8-XXXFP) is 2.5 to 3.6V.

CONTROL REGISTERS

Interrupt control register V1		at reset : 0000_2	at power down : 0000_2	R/W
$V1_3$	Unused	0	This bit has no function	
		1		
$V1_2$	Timer 3 interrupt enable bit	0	Occurrence disabled (SNZT3 instruction is valid)	
		1	Occurrence enabled (SNZT3 instruction is invalid)	
$V1_1$	Timer 1 interrupt enable bit	0	Occurrence disabled (SNZT1 instruction is valid)	
		1	Occurrence enabled (SNZT1 instruction is invalid)	
$V1_0$	External interrupt enable bit	0	Occurrence disabled (SNZ0 instruction is valid)	
		1	Occurrence enabled (SNZ0 instruction is invalid)	

Interrupt control register I1		at reset : 0000_2	at power down : retain state	R/W
$I1_3$	$P3_0$/INT pin dynamic pull-up control bit	0	Dynamic pull-up disabled	
		1	Dynamic pull-up enabled	
$I1_2$	$P3_0$/INT pin return input level selection bit	0	Returning from power down state by inputting "L" level	
		1	Returning from power down state by inputting "H" level	
$I1_1$	$P3_1$ pin pull-up transistor control bit	0	OFF	
		1	ON	
$I1_0$	$P3_0$/INT pin pull-up transistor control bit	0	OFF	
		1	ON	

Clock control register MR		at reset : 0000_2	at power down : retain state	R/W
MR_2	Unused	0	This bit has no function	
		1		
MR_1	$f(X_{IN})$ oscillating circuit control bit	0	Oscillating enabled	
		1	Oscillating disabled	
MR_0	System clock selection bit	0	$f(X_{IN})$	
		1	$f(X_{CIN})$	

Timer control register W1		at reset : 0000_2	at power down : 0000_2	R/W
$W1_3$	Timer 1 count source selection bit	0	Prescaler output (ORCLK)	
		1	Multi-carrier output (CARR)	
$W1_2$	Timer 1 control bit	0	Stop (retain state)	
		1	Operating	
$W1_1$, $W1_0$	Prescaler frequency dividing ratio selection bit	$W1_1$ $W1_0$	Frequency dividing ratio	
		0 0	Prescaler stop (reset state)	
		0 1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 2 (Note 2)	
		1 0	$f(X_{IN})$ or $f(X_{CIN})$ divided by 4 (Note 2)	
		1 1	$f(X_{IN})$ or $f(X_{CIN})$ divided by 8 (Note 2)	

Notes 1. "R" indicates read enabled and "W" indicates write enabled.
2. The signal in $f(X_{IN})$ or $f(X_{CIN})$ selected as system clock is used.

Timer control register W2		at reset : 0000_2	at power down : retain state	R/W
$W2_3$	Timer 3 control bit	0	Stop (retain state)	
		1	Operating	
$W2_2$	Timer 3 count source selection bit	0	Timer 2 overflow signal	
		1	Prescaler output (ORCLK)	
$W2_1$	Timer 2 control bit	0	Stop (reset state)	
		1	Operating	
$W2_0$	Timer 2 count source selection bit	0	$f(X_{CIN})$	
		1	Prescaler output (frequency divided by 8 output)	

Timer control register W3		at reset : 0000_2	at power down : retain state	R/W
$W3_3$	BEEP output control bit	0	Output stop	
		1	Output	
$W3_2$	Watchdog timer control bit	0	Not used	
		1	Used	
$W3_1$	BEEP, LCD clock frequency dividing circuit control bit	$W3_1$ $W3_0$	Frequency dividing ratio	
		0 0	Stop	
		0 1	Timer 2 immediate overflow (frequency divided by 16 output)	
$W3_0$		1 0	Timer 2 immediate overflow (frequency divided by 16 output) divided by 2	
		1 1	Timer 2 immediate overflow (frequency divided by 16 output) divided by 4	

Carrier wave data control register C1		at reset : 0000_2	at power down : 0000_2	W
$C1_3$	Carrier wave data compensation control bit	0	−1 compensation	
		1	+1 compensation	
$C1_2$	Carrier wave data register connection control bit	$C1_2$ $C1_1$ $C1_0$	Number of connection bits	
		0 0 0	2 bits connection	
$C1_1$		0 0 1	3 bits connection	
		0 1 0	4 bits connection	
$C1_0$		0 1 1	5 bits connection	
		1 0 0	6 bits connection	
		Other	This is not available	

Carrier wave compensation control register C2		at reset : 00_2	at power down : 00_2	W
$C2_1$	Carrier wave automatic stop function control bit	0	Automatic stop function not used	
		1	Automatic stop function used	
$C2_0$	Carrier wave compensation control bit	0	Not compensated	
		1	Compensated	

Carrier wave output control flag C3		at reset : 0_2	at power down : 0_2	W
C3	(Carrier wave output control)	0	Carrier wave output disabled (RC3 instruction execution)	
		1	Carrier wave output (SC3 instruction execution)	

Note "R" indicates read enabled and "W" indicates write enabled.

LCD control register L1		at reset : 0000_2		at power down : (retain state)	R/W
$L1_3$	LCD power supply dividing resistance control bit	0	Connecting internal dividing resistance to LCD power circuit		
		1	Disconnecting internal dividing resistance from LCD power circuit		
$L1_2$	LCD ON/OFF bit	0	OFF		
		1	ON		
$L1_1$	LCD duty and bias selection bit	$L1_1$ $L1_0$	Duty	Bias	
		0 0	This is not available		
$L1_0$		0 1	1/2	1/2	
		1 0	1/3	1/3	
		1 1	1/4	1/3	

LCD control register L2		at reset : 0000_2		at power down : (retain state)	W
$L2_3$	$SEG_{39}/P4_3$ pin function switch bit	0	SEG_{39}		
		1	$P4_3$		
$L2_2$	$SEG_{38}/P4_2$ pin function switch bit	0	SEG_{38}		
		1	$P4_2$		
$L2_1$	$SEG_{37}/P4_1$ pin function switch bit	0	SEG_{37}		
		1	$P4_1$		
$L2_0$	$SEG_{36}/P4_0$ pin function switch bit	0	SEG_{36}		
		1	$P4_0$		

LCD control register L3		at reset : 0_2		at power down : (retain state)	W
L3	D_{12}, D_{11}/V_{LC2}, V_{LC1} pin function switch bit	0	D_{12}, D_{11}		
		1	V_{LC2}, V_{LC1}		

Note "R" indicates read enabled and "W" indicates write enabled.

SYMBOL

The symbols shown are used in the following instruction function table and instruction list.

Symbol	Contents	Symbol	Contents
A	Register A (4 bits)	T1F	Timer 1 interrupt request flag
B	Register B (4 bits)	T2F	Timer 2 overflow flag
D	Register D (3 bits)	T3F	Timer 3 interrupt request flag
E	Register E (8 bits)	INTE	Interrupt enable flag
C1	Carrier wave data control register C1 (4 bits)	EXF0	External interrupt request flag
C2	Carrier wave compensation control register C2 (2 bits)	P	Power down flag
C3	Carrier wave output control flag C3	WDF	Watchdog timer flag WDF
PA	Preset register PA (4 bits)		
L1	LCD control register L1 (4 bits)	D	Port D (13 bits)
L2	LCD control register L2 (4 bits)	P0	Port P0 (4 bits)
L3	LCD control register L3 (1 bit)	P1	Port P1 (4 bits)
MR	Clock control register MR (3 bits)	P2	Port P2 (4 bits)
V1	Interrupt control register V1 (4 bits)	P3	Port P3 (2 bits)
I1	Interrupt control register I1 (4 bits)	P4	Port P4 (4 bits)
W1	Timer control register W1 (4 bits)		
W2	Timer control register W2 (4 bits)	x	Hexadecimal variable
W3	Timer control register W3 (4 bits)	y	Hexadecimal variable
		z	Hexadecimal variable
X	Register X (4 bits)	p	Hexadecimal variable
Y	Register Y (4 bits)	n	Hexadecimal constant
Z	Register Z (2 bits)	i	Hexadecimal constant
DP	Data pointer (10 bits)	j	Hexadecimal constant
	(consisted of register X, Y and Z)	$A_3A_2A_1A_0$	Binary notanion of hexadecimal variable A
PC	Program counter (14 bits)		(same for others)
PC_H	High-order 7 bits of program counter		
PC_L	Low-order 7 bits of program counter	←	Direction of data movement
SK	Stack register (14 bits×8)	( )	Contents of registers and memories
SP	Stack pointer (3 bits)	—	Negate, Flag unchanged after executing instruction
CY	Carry flag	M(DP)	RAM address pointed by the data pointer
T1	Timer 1	a	Label indicating address $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$
T2	Timer 2	p, a	Label indicating address $a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$ in page $p_5\ p_4\ p_3\ p_2\ p_1\ p_0$
T3	Timer 3		
R1	Timer 1 reload register		
R2	Timer 2 reload register	C	Hex. C + Hex. number X (also same for others)
R3	Timer 3 reload register	+	
		X	

Note : The M34550Mx-XXXFP performs a skip by invalidating the next instruction. The program counter is not increased by 2. Therefore, the number of cycles does not change even if skip is not performed. However, the cycle count becomes "1" if the TABP p, RT, or RTS instruction is skipped.

LIST OF INSTRUCTION FUNCTION

Grouping	Mnemonic	Function
Register to register transfers	TAB	(A)←(B)
	TBA	(B)←(A)
	TAY	(A)←(Y)
	TYA	(Y)←(A)
	TEAB	$(E_7 \sim E_4)$←(B) $(E_3 \sim E_0)$←(A)
	TABE	(B)←$(E_7 \sim E_4)$ (A)←$(E_3 \sim E_0)$
	TDA	$(D_2 \sim D_0)$←$(A_2 \sim A_0)$
	TAD	$(A_2 \sim A_0)$←$(D_2 \sim D_0)$ (A_3)←0
	TAZ	(A_1, A_0)←(Z_1, D_0) (A_3, A_2)←0
	TAX	(A)←(X)
	TASP	$(A_2 \sim A_0)$←$(SP_2 \sim SP_0)$ (A_3)←0
RAM addresses	LXY x, y	(X)←x, x=0~15 (Y)←y, y=0~15
	LZ z	(Z)←z, z=0~3
	INY	(Y)←(Y)+1
	DEY	(Y)←(Y)−1
RAM to register transfers	TAM j	(A)←(M(DP)) (X)←(X)EXORj j=0~15
	XAM j	(A)←→(M(DP)) (X)←(X)EXORj j=0~15
	XAMD j	(A)←→(M(DP)) (X)←(X)EXORj j=0~15

Grouping	Mnemonic	Function
RAM to register transfers	XAMI j	(A)←→(M(DP)) (X)←(X)EXORj j=0~15 (Y)←(Y)+1
	TAM j	(M(DP))←(A) (X)←(X)EXORj j=0~15
Arithmetic operations	LA n	(A)←n, However, n=0~15
	TABP p	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←$(D_2 \sim D_0, A_3 \sim A_0)$ (B)←$(ROM(PC))_{7\sim4}$ (A)←$(ROM(PC))_{3\sim0}$ (PC)←(SK(SP)) (SP)←(SP)−1
	AM	(A)←(A)+(M(DP))
	AMC	(A)←(A)+(M(DP))+(CY) (CY)←Carry
	A n	(A)←(A)+n, However, n=0~15
	AND	(A)←(A)AND(M(DP))
	OR	(A)←(A)OR(M(DP))
	SC	(CY)←1
	RC	(CY)←0
	SZC	(CY)=0?
	CMA	(A)←$(\bar{A})$
	RAR	→CY→$A_3A_2A_1A_0$→
Bit operations	SB j	(Mj(DP))←1, However, j=0~3
	RB j	(Mj(DP))←0, However, j=0~3

Grouping	Mnemonic	Function
Bit operations	SZB j	(Mj(DP))=0?, However, j=0~3
Comparison operations	SEAM	(A)=(M(DP))?
	SEA n	(A)=n?, However, n=0~15
Branch operations	B a	(PC_L)←$a_6 \sim a_0$
	BL p, a	(PC_H)←p (PC_L)←$a_6 \sim a_0$
	BLA p	(PC_H)←p (PC_L)←$(D_2 \sim D_0, A_3 \sim A_0)$
Subroutine operations	BM a	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←2 (PC_L)←$a_6 \sim a_0$
	BML p, a	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←$a_6 \sim a_0$
	BMLA p	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p (PC_L)←$(D_2 \sim D_0, A_2 \sim A_0)$
Return operations	RTI	(PC)←(SK(SP)) (SP)←(SP)−1
	RT	(PC)←(SK(SP)) (SP)←(SP)−1
	RTS	(PC)←(SK(SP)) (SP)←(SP)−1

Grouping	Mnemonic	Function
Interrupt operations	DI	(INTE)←0
	EI	(INTE)←1
	SNZ0	(EXF0)=1?, After skipping, (EXF0)←0
	TV1A	(V1)←(A)
	TI1A	(I1)←(A)
	TAV1	(A)←(V1)
	TAI1	(A)←(I1)
Timer operations	TW1A	(W1)←(A)
	TW2A	(W2)←(A)
	TW3A	(W3)←(A)
	TAW1	(A)←(W1)
	TAW2	(A)←(W2)
	TAW3	(A)←(W3)
	T3AB	$(R3_7 \sim R3_4) \leftarrow (B)$ $(T3_7 \sim T3_4) \leftarrow (B)$ $(R3_3 \sim R3_0) \leftarrow (A)$ $(T3_3 \sim T3_0) \leftarrow (A)$
	T1R1	(T1)←(R1)
	TR1AB	$(R1_7 \sim R1_4) \leftarrow (B)$ $(R1_3 \sim R1_0) \leftarrow (A)$
	TR1A	$(R1_8) \leftarrow (A_0)$
	TAB3	$(B) \leftarrow (T3_7 \sim T3_4)$ $(A) \leftarrow (T3_3 \sim T3_0)$
	SNZT1	(T1F)=1?, After skipping, (T1F)←0
	SNZT2	(T2F)=1?, After skipping, (T2F)←0
Timer operations	SNZT3	(T3F)=1?,
Input/Output operations	IAP0	(A)←(P0)
	IAP1	(A)←(P1)
	IAP2	(A)←(P2)
	IAP3	$(A_1, A_0) \leftarrow (P3_1, P3_0)$ $(A_3, A_2) \leftarrow 0$
	IAP4	(A)←(P4)
	CLD	(D)←1
	RD	(D(Y))←0, However, Y=0~12
	SD	(D(Y))←1 However, Y=0~12
	SZD	(D(Y))=0?, However, Y=8~10
	OP0A	(P0)←(A)
	OP1A	(P1)←(A)
LCD control operations	TL1A	(L1)←(A)
	TAL1	(A)←(L1)
	TL2A	(L2)←(A)
	TL3A	$(L3) \leftarrow (A_0)$
	TLCA	(LC)←(A)
Multi-carrier generating circuit operations	TPTA	$(PT) \leftarrow (A_1, A_0)$
	TC1A	(C1)←(A)
	TPAA	(PA)←(A)
	RC3	(C3)←0
	SC3	(C3)←1
	RC4	(C4)←0
Multi-carrier generating circuit operations	SC4	(C4)←1
	STCR	Carrier wave generating starts
	SPCR	Carrier wave generating stops
	TC2A	$(C2) \leftarrow (A_1, A_0)$
Other operations	NOP	(PC)←(PC)+1
	POF	Power down 1
	POF2	Power down 2
	SNZP	(P)=1?
	TMRA	$(MP_2 \sim MR_0) \leftarrow (A_2 \sim A_0)$
	TAMR	$(A_2 \sim A_0) \leftarrow (MR_2 \sim MR_0)$ $(A_3) \leftarrow 0$
	WRST	(WDF)←0

INSTRUCTION CODE TABLE

$D_3 \sim D_0$ \ $D_9 \sim D_4$	Hexadecimal notation	000000 00	000001 01	000010 02	000011 03	000100 04	000101 05	000110 06	000111 07	001000 08	001001 09	001010 0A	001011 0B	001100 0C	001101 0D	001110 0E	001111 0F	010000 ~ 010110 10~17	011000 ~ 011111 18~1F
0000	0	NOP	BLA	SZB 0	BMLA	—	TASP	A 0	LA 0	TABP 0	TABP 16	TABP 32	TABP 48*	BML	BML	BL	BL	BM	B
0001	1	—	CLD	SZB 1	—	—	TAD	A 1	LA 1	TABP 1	TABP 17	TABP 33	TABP 49*	BML	BML	BL	BL	BM	B
0010	2	POF	—	SZB 2	—	—	TAX	A 2	LA 2	TABP 2	TABP 18	TABP 34	TABP 50*	BML	BML	BL	BL	BM	B
0011	3	SNZP	INY	SZB 3	—	—	TAZ	A 3	LA 3	TABP 3	TABP 19	TABP 35	TABP 51*	BML	BML	BL	BL	BM	B
0100	4	DI	RD	SZD	—	RT	TAV1	A 4	LA 4	TABP 4	TABP 20	TABP 36	TABP 52*	BML	BML	BL	BL	BM	B
0101	5	EI	SD	SEAn	—	RTS	—	A 5	LA 5	TABP 5	TABP 21	TABP 37	TABP 53*	BML	BML	BL	BL	BM	B
0110	6	RC	—	SEAM	—	RTI	—	A 6	LA 6	TABP 6	TABP 22	TABP 38	TABP 54*	BML	BML	BL	BL	BM	B
0111	7	SC	DEY	—	—	—	—	A 7	LA 7	TABP 7	TABP 23	TABP 39	TABP 55*	BML	BML	BL	BL	BM	B
1000	8	POF2	AND	—	SNZ0	LZ 0	—	A 8	LA 8	TABP 8	TABP 24	TABP 40	TABP 56*	BML	BML	BL	BL	BM	B
1001	9	—	OR	TDA	—	LZ 1	—	A 9	LA 9	TABP 9	TABP 25	TABP 41	TABP 57*	BML	BML	BL	BL	BM	B
1010	A	AM	TEAB	TABE	—	LZ 2	—	A 10	LA 10	TABP 10	TABP 26	TABP 42	TABP 58*	BML	BML	BL	BL	BM	B
1011	B	AMC	—	—	—	LZ 3	—	A 11	LA 11	TABP 11	TABP 27	TABP 43	TABP 59*	BML	BML	BL	BL	BM	B
1100	C	TYA	CMA	—	—	RB 0	SB 0	A 12	LA 12	TABP 12	TABP 28	TABP 44	TABP 60*	BML	BML	BL	BL	BM	B
1101	D	—	RAR	—	—	RB 1	SB 1	A 13	LA 13	TABP 13	TABP 29	TABP 45	TABP 61*	BML	BML	BL	BL	BM	B
1110	E	TBA	TAB	—	—	RB 2	SB 2	A 14	LA 14	TABP 14	TABP 30	TABP 46	TABP 62*	BML	BML	BL	BL	BM	B
1111	F	—	TAY	SZC	TV1A	RB 3	SB 3	A 15	LA 15	TABP 15	TABP 31	TABP 47	TABP 63*	BML	BML	BL	BL	BM	B

The above table shows the relationship between machine language codes and machine language instructions. $D_3 \sim D_0$ shows the low-order 4 bits of the machine language code and $D_9 \sim D_4$ shows the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use the code marked "—".

The codes for the second word of a two-word instruction are described below.

	The second word
BL	1 0 p a a a a a a a
BML	1 0 p a a a a a a a
BLA	1 0 p a 0 0 p p p p
BMLA	1 0 p a 0 0 p p p p
SEA	0 0 0 1 1 1 n n n n
SZD	0 0 0 0 1 0 1 0 1 1

* cannot be used at M34550M6-XXXFP.

$D_3 \sim D_0$ \ $D_9 \sim D_4$	Hexa-decimal notation	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111	110000 ~ 111111
		20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30~3F
0000	0	—	TW3A	OP0A	—	—	—	IAP0	—	SNZT 1	—	WRST	TMA 0	TAM 0	XAM 0	XAMI 0	XAMD 0	LXY
0001	1	—	—	OP1A	—	—	—	IAP1	—	SNZT 2	—	—	TMA 1	TAM 1	XAM 1	XAMI 1	XAMD 1	LXY
0010	2	—	—	—	T3AB	—	TAMR	IAP2	TAB3	SNZT 3	—	—	TMA 2	TAM 2	XAM 2	XAMI 2	XAMD 2	LXY
0011	3	—	—	—	—	—	TAI1	IAP3	—	—	—	—	TMA 3	TAM 3	XAM 3	XAMI 3	XAMD 3	LXY
0100	4	—	—	—	—	—	—	IAP4	—	—	—	—	TMA 4	TAM 4	XAM 4	XAMI 4	XAMD 4	LXY
0101	5	—	—	—	—	—	—	—	—	—	—	TPTA	TMA 5	TAM 5	XAM 5	XAMI 5	XAMD 5	LXY
0110	6	—	TMRA	—	—	—	—	—	—	—	—	TR1A	TMA 6	TAM 6	XAM 6	XAMI 6	XAMD 6	LXY
0111	7	—	TI1A	—	—	—	—	—	—	—	—	—	TMA 7	TAM 7	XAM 7	XAMI 7	XAMD 7	LXY
1000	8	—	—	—	—	—	—	—	—	—	STCR	TC1A	TMA 8	TAM 8	XAM 8	XAMI 8	XAMD 8	LXY
1001	9	—	—	—	—	—	—	—	—	—	SPCR	TC2A	TMA 9	TAM 9	XAM 9	XAMI 9	XAMD 9	LXY
1010	A	TL1A	—	—	—	TAL1	—	—	—	—	—	TPAA	TMA 10	TAM 10	XAM 10	XAMI 10	XAMD 10	LXY
1011	B	TL2A	—	—	—	TAW1	—	—	—	—	—	T1R1	TMA 11	TAM 11	XAM 11	XAMI 11	XAMD 11	LXY
1100	C	TL3A	—	—	—	TAW2	—	—	—	—	—	RC3	TMA 12	TAM 12	XAM 12	XAMI 12	XAMD 12	LXY
1101	D	TLCA	—	—	—	TAW3	—	—	—	—	—	SC3	TMA 13	TAM 13	XAM 13	XAMI 13	XAMD 13	LXY
1110	E	TW1A	—	—	—	—	—	—	—	—	—	RC4	TMA 14	TAM 14	XAM 14	XAMI 14	XAMD 14	LXY
1111	F	TW2A	—	—	TR1AB	—	—	—	—	—	—	SC4	TMA 15	TAM 15	XAM 15	XAMI 15	XAMD 15	LXY

The above table shows the relationship between machine language codes and machine language instructions. $D_3 \sim D_0$ shows the low-order 4 bits of the machine language code and $D_9 \sim D_4$ shows the high-order 6 bits of the machine language code. The hexadecimal representation of the code is also provided. There are one-word instructions and two-word instructions, but only the first word of each instruction is shown. Do not use the code marked "—".

The codes for the second word of a two-word instruction are described below.

	The second word
BL	1 0 p a a a a a a a
BML	1 0 p a a a a a a a
BLA	1 0 p a 0 0 p p p p
BMLA	1 0 p p 0 0 p p p p
SEA	0 0 0 1 1 1 n n n n
SZD	0 0 0 0 1 0 1 0 1 1

MACHINE INSTRUCTIONS

Type of instructions	Mnemonic	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Register to register transfers	TAB	0	0	0	0	0	1	1	1	1	0	0 1 E	1	1	$(A) \leftarrow (B)$
	TBA	0	0	0	0	0	0	1	1	1	0	0 0 E	1	1	$(B) \leftarrow (A)$
	TAY	0	0	0	0	0	1	1	1	1	1	0 1 F	1	1	$(A) \leftarrow (Y)$
	TYA	0	0	0	0	0	0	1	1	0	0	0 0 C	1	1	$(Y) \leftarrow (A)$
	TEAB	0	0	0	0	0	1	1	0	1	0	0 1 A	1	1	$(E_7 \sim E_4) \leftarrow (B)$, $(E_3 \sim E_0) \leftarrow (A)$
	TABE	0	0	0	0	1	0	1	0	1	0	0 2 A	1	1	$(B) \leftarrow (E_7 \sim E_4)$, $(A) \leftarrow (E_3 \sim E_0)$
	TDA	0	0	0	0	1	0	1	0	0	1	0 2 9	1	1	$(D_2 \sim D_0) \leftarrow (A_2 \sim A_0)$
	TAD	0	0	0	1	0	1	0	0	0	1	0 5 1	1	1	$(A_2 \sim A_0) \leftarrow (D_2 \sim D_0)$, $(A_3) \leftarrow 0$
	TAZ	0	0	0	1	0	1	0	0	1	1	0 5 3	1	1	$(A_1, A_0) \leftarrow (Z_1, Z_0)$ $(A_3, A_2) \leftarrow 0$
	TAX	0	0	0	1	0	1	0	0	1	0	0 5 2	1	1	$(A) \leftarrow (X)$
	TASP	0	0	0	1	0	1	0	0	0	0	0 5 0	1	1	$(A_2 \sim A_0) \leftarrow (SP_2 \sim SP_0)$ $(A_3) \leftarrow 0$
RAM addresses	LXY x, y	1	1	x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0	3 x y	1	1	$(X) \leftarrow x$, $x = 0 \sim 15$ $(Y) \leftarrow y$, $y = 0 \sim 15$
	LZ z	0	0	0	1	0	0	1	0	z_1	z_0	0 4 8+z	1	1	$(Z) \leftarrow z$, $z = 0 \sim 3$
	INY	0	0	0	0	0	1	0	0	1	1	0 1 3	1	1	$(Y) \leftarrow (Y)+1$
	DEY	0	0	0	0	0	1	0	1	1	1	0 1 7	1	1	$(Y) \leftarrow (Y)-1$
RAM to register transfers	TAM j	1	0	1	1	0	0	j	j	j	j	2 C j	1	1	$(A) \leftarrow (M(DP))$ $(X) \leftarrow (X)$EXORj, $j = 0 \sim 15$
	XAM j	1	0	1	1	0	1	j	j	j	j	2 D j	1	1	$(A) \longleftrightarrow (M(DP))$ $(X) \leftarrow (X)$EXORj, $j = 0 \sim 15$
	XAMD j	1	0	1	1	1	1	j	j	j	j	2 F j	1	1	$(A) \longleftrightarrow (M(DP))$ $(X) \leftarrow (X)$EXORj, $j = 0 \sim 15$ $(Y) \leftarrow (Y)-1$
	XAMI j	1	0	1	1	1	0	j	j	j	j	2 E j	1	1	$(A) \longleftrightarrow (M(DP))$ $(X) \leftarrow (X)$EXORj, $j = 0 \sim 15$ $(Y) \leftarrow (Y)+1$
	TMA j	1	0	1	0	1	1	j	j	j	j	2 B j	1	1	$(M(DP)) \leftarrow (A)$ $(X) \leftarrow (X)$EXORj, $j = 0 \sim 15$
Arithmetic operations	LA n	0	0	0	1	1	1	n	n	n	n	0 7 n	1	1	$(A) \leftarrow n$, However, $n = 0 \sim 15$
	TABP p	0	0	1	0	p_5	p_4	p_3	p_2	p_1	p_0	0 8+p	1	3	$(SP) \leftarrow (SP)+1$ $(SK(SP)) \leftarrow (PC)$ $(PC_H) \leftarrow p$ $(PC_L) \leftarrow (D_2 \sim D_0, A_3 \sim A_0)$ $(B) \leftarrow (ROM(PC))_{7 \sim 4}$ $(A) \leftarrow (ROM(PC))_{3 \sim 0}$ $(PC) \leftarrow (SK(SP))$ $(SP) \leftarrow (SP)-1$ Note
	AM	0	0	0	0	0	0	1	0	1	0	0 0 A	1	1	$(A) \leftarrow (A)+(M(DP))$

Note : p is 0-63 for M34550M8.
p is 0-47 for M34550M6.

Skip condition	Carry flag CY	Detailed description
—	—	Transfers the contents of register B to register A.
—	—	Transfers the contents of register A to register B.
—	—	Transfers the contents of register Y to register A.
—	—	Transfers the contents of register A to register Y.
—	—	Transfers the contents of register A and register B to register E.
—	—	Transfers the contents of register E to register A and register B.
—	—	Transfers the contents of register A to register D.
—	—	Transfers the contents of register D to register A.
—	—	Transfers the contents of register Z to register A.
—	—	Transfers the contents of register X to register A.
—	—	Transfers the contents of stack pointer (SP) to register A.
Continuous description	—	Loads the value x in the immediate field in register X and the value y in the immediate field in register Y. If the LXY instruction is continuously coded and executed, only the first LXY instruction is executed and other LXY instruction coded continuously are skipped.
—	—	Loads the value z in the immediate field in register Z.
(Y) = 0	—	Adds 1 to register Y. As a result, if the contents of register Y are 0, next instruction is skipped.
(Y) = 15	—	Subtracts 1 to register Y. As a result, if the contents of register Y are 15, next instruction is skipped.
—	—	After transferring the contents of M(DP) to register A, an exclusive logic OR is performed between register X and the immediate field value j, and stores the result to register X.
—	—	After exchanging the contents of M(DP) with register A, an exclusive logic OR is performed between register X and the immediate field value j, and stores the result to register X.
(Y) = 15	—	After exchanging the contents of M(DP) with register A, an exclusive logic OR is performed between register X and the immediate field value j, and stores the result to register X. Subtracts 1 to register Y. As a result, if the contents of register Y are 15, next instruction is skipped.
(Y) = 0	—	After exchanging the contents of M(DP) with register A, an exclusive logic OR is performed between register X and the immediate field value j, and stores the result to register X. Adds 1 to register Y. As a result, if the contents of register Y are 0, next instruction is skipped.
—	—	After transferring the contents of register A to M(DP), an exclusive logic OR is performed between register X and the immediate field value j, and stores the result to register X.
Continuous description	—	Loads the value n in the immediate field in the register A. If a continuous description of LA instructions are written and are being executed, only the first LA instruction is executed, the following LA instructions are all skipped.
—	—	Transfers bits 7~4 to register B and bits 3~0 to register A. These bits 7~0 are the ROM pattern in address (D_2 D_1 D_0 A_3 A_2 A_1 A_0) specified by register A and register D in page p. When this instruction is executed, 1 level of stack register is used.
—	—	Adds the contents of M(DP) to register A. Stores the result to register A. The contents of carry flag CY are not changed.

Type of instructions \ Parameter	Mnemonic	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation	Number of words	Number of cycles	Functions
Arithmetic operations	AMC	0	0	0	0	0	0	1	0	1	1	0 0 B	1	1	(A)←(A)+(M(DP))+(CY) (CY)←Carry
	An	0	0	0	1	1	0	n	n	n	n	0 6 n	1	1	(A)←(A)+n, However, n= 0 ~15
	AND	0	0	0	0	0	1	1	0	0	0	0 1 8	1	1	(A)←(A) AND (M(DP))
	OR	0	0	0	0	0	1	1	0	0	1	0 1 9	1	1	(A)←(A) OR (M(DP))
	SC	0	0	0	0	0	0	0	1	1	1	0 0 7	1	1	(CY)←1
	RC	0	0	0	0	0	0	0	1	1	0	0 0 6	1	1	(CY)←0
	SZC	0	0	0	0	1	0	1	1	1	1	0 2 F	1	1	(CY)=0 ?
	CMA	0	0	0	0	0	1	1	1	0	0	0 1 C	1	1	(A)←($\overline{A}$)
	RAR	0	0	0	0	0	1	1	1	0	1	0 1 D	1	1	→CY→$A_3A_2A_1A_0$→
Bit operations	SB j	0	0	0	1	0	1	1	1	j	j	0 5 C+j	1	1	(Mj(DP))←1, However, j= 0 ~ 3
	RB j	0	0	0	1	0	0	1	1	j	j	0 4 C+j	1	1	(Mj(DP))←0, However, j= 0 ~ 3
	SZB j	0	0	0	0	1	0	0	0	j	j	0 2 j	1	1	(Mj(DP))= 0 ?, However, j= 0 ~ 3
Comparison operations	SEAM	0	0	0	0	1	0	0	1	1	0	0 2 6	1	1	(A)=(M(DP)) ?
	SEA n	0	0	0	0	1	0	0	1	0	1	0 2 5	2	2	(A)=n ?, However, n= 0 ~15
		0	0	0	1	1	1	n	n	n	n	0 7 n			
Branch operations	Ba	0	1	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 8 a+a	1	1	(PC_L)←a_6~a_0
	BL p, a	0	0	1	1	1	p_4	p_3	p_2	p_1	p_0	0 E p+p	2	2	(PC_H)←p (PC_L)←a_6~a_0 Note
		1	0	p_5	a_6	a_5	a_4	a_3	a_2	a_1	a_0	2 p a+a			
	BLA p	0	0	0	0	0	1	0	0	0	0	0 1 0	2	2	(PC_H)←p (PC_L)←(D_2~D_0, A_3~A_0) Note
		1	0	p_6	p_4	0	0	p_3	p_2	p_1	p_0	2 p p			
Subroutine operations	BM a	0	1	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	1 a a	1	1	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←2, (PC_L)←a_6~a_0
	BML p, a	0	0	1	1	0	p_4	p_3	p_2	p_1	p_0	0 C p+p	2	2	(SP)←(SP)+1 (SK(SP))←(PC) (PC_H)←p, (PC_L)←a_6~a_0 Note
		1	0	p_5	a_6	a_5	a_4	a_3	a_2	a_1	a_0	2 p a+a			
	BMLA p	0	0	0	0	1	1	0	0	0	0	0 3 0	2	2	(SP)←(SP)+1 (SK(SP))←(PC)
		1	0	p_5	p_4	0	0	p_3	p_2	p_1	p_0	2 p p			(PC_H)←p (PC_L)←(D_2~D_0, A_2~A_0) Note

Note : p is 0-63 for M34550M8.
p is 0-47 for M34550M6.

MITSUBISHI ELECTRIC

Skip condition	Carry flag CY	Detailed description
—	0/1	Adds the contents of M(DP) and carry flag CY to register A. Stores the result to register A and carry flag CY.
Overflow= 0	—	Adds the value n in the immediate field to register A. The contents of carry flag CY are not changed. Skips the next instruction if there is no overflow as the result of operation.
—	—	Takes the AND of register A and M(DP) and stores the result in register A.
—	—	Takes the OR of register A and M(DP) and stores the result in register A.
—	1	Carry flag CY is set to 1.
—	0	Carry flag CY is reset to 0.
(CY)= 0	—	Skips the next instruction when the contents of carry flag CY is 0.
—	—	Stores the one's complement for register A's contents are stored into register A.
—	0/1	Rotates 1 bit of register A including the carry flag CY to the right.
—	—	Sets (1) the j bit (bit specified by the value j in the immediate field of M(DP).
—	—	Resets (0) the j bit (bit specified by the value j in the immediate field of M(DP).
(Mj(DP))= 0, However, j= 0 ~ 3	—	Resets (0) the next instruction when the j bit (bit speified by the value j in the immediate field) of M(DP) is "0".
(A)=(M(DP))	—	Skips the next instruction if the contents of register A are equal to the contents of M(DP).
(A)=n	—	Skips the next instruction if the contents of register A are equal to the value n in the immediate field.
—	—	Branch inside page : Branches to address a in identical page.
—	—	Branch outside page : Branches to address a in page p.
—	—	Branch outside page : Branches to address (address D_2 D_1 D_0 A_3 A_2 A_1 A_0) specified by registers D and A in page p.
—	—	Call the subroutine in page 2 : Calls the subroutine at address a in page 2.
—	—	Call the subroutine : Calls the subroutine at address a in page p.
—	—	Call the subroutine : Calls the subroutine at address (D_2 D_1 D_0 A_3 A_2 A_1 A_0) specified by register A and register D in page p.

Type of instructions \ Parameter	Mnemonic	Instruction code											Number of words	Number of cycles	Functions
		D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation			
Return operations	RTI	0	0	0	1	0	0	0	1	1	0	0 4 6	1	1	(PC)←(SK(SP)) (SP)←(SP)−1
	RT	0	0	0	1	0	0	0	1	0	0	0 4 4	1	2	(PC)←(SK(SP)) (SP)←(SP)−1
	RTS	0	0	0	1	0	0	0	1	0	1	0 4 5	1	2	(PC)←(SK(SP)) (SP)←(SP)−1
Interrupt operations	DI	0	0	0	0	0	0	0	1	0	0	0 0 4	1	1	(INTE)←0
	EI	0	0	0	0	0	0	0	1	0	1	0 0 5	1	1	(INTE)←1
	SNZ0	0	0	0	0	1	1	1	0	0	0	0 3 8	1	1	(EXF0)=1 ?, After skipping (EXF0)←0
	TV1A	0	0	0	0	1	1	1	1	1	1	0 3 F	1	1	(V1)←(A)
	TI1A	1	0	0	0	0	1	0	1	1	1	2 1 7	1	1	(I1)←(A)
	TAV1	0	0	0	1	0	1	0	1	0	0	0 5 4	1	1	(A)←(V1)
	TAI1	1	0	0	1	0	1	0	0	1	1	2 5 3	1	1	(A)←(I1)
Timer operations	TW1A	1	0	0	0	0	0	1	1	1	0	2 0 E	1	1	(W1)←(A)
	TW2A	1	0	0	0	0	0	1	1	1	1	2 0 F	1	1	(W2)←(A)
	TW3A	1	0	0	0	0	1	0	0	0	0	2 1 0	1	1	(W3)←(A)
	TAW1	1	0	0	1	0	0	1	0	1	1	2 4 B	1	1	(A)←(W1)
	TAW2	1	0	0	1	0	0	1	1	0	0	2 4 C	1	1	(A)←(W2)
	TAW3	1	0	0	1	0	0	1	1	0	1	2 4 D	1	1	(A)←(W3)
	T3AB	1	0	0	0	1	1	0	0	1	0	2 3 2	1	1	$(R3_7 \sim R3_4) \leftarrow (B)$, $(T3_7 \sim T3_4) \leftarrow (B)$ $(R3_3 \sim R3_0) \leftarrow (A)$, $(T3_3 \sim T3_0) \leftarrow (A)$
	T1R1	1	0	1	0	1	0	1	0	1	1	2 A B	1	1	(T1)←(R1)
	TR1AB	1	0	0	0	1	1	1	1	1	1	2 3 F	1	1	$(R1_7 \sim R1_4) \leftarrow (B)$, $(R1_3 \sim R1_0) \leftarrow (A)$
	TR1A	1	0	1	0	1	0	0	1	1	0	2 A 6	1	1	$(R1_8) \sim (A_0)$
	TAB3	1	0	0	1	1	1	0	0	1	0	2 7 2	1	1	$(B) \leftarrow (T3_7 \sim T3_4)$, $(A) \leftarrow (T3_3 \sim T3_0)$
	SNZT1	1	0	1	0	0	0	0	0	0	0	2 8 0	1	1	(T1F)=1 ?, After skipping (T1F)←0
	SNZT2	1	0	1	0	0	0	0	0	0	1	2 8 1	1	1	(T2F)=1 ?, After skipping (T2F)←0
	SNZT3	1	0	1	0	0	0	0	0	1	0	2 8 2	1	1	(T3F)=1 ?, After skipping (T3F)←0
Input/Output operations	IAP0	1	0	0	1	1	0	0	0	0	0	2 6 0	1	1	(A)←(P0)
	IAP1	1	0	0	1	1	0	0	0	0	1	2 6 1	1	1	(A)←(P1)
	IAP2	1	0	0	1	1	0	0	0	1	0	2 6 2	1	1	(A)←(P2)
	IAP3	1	0	0	1	1	0	0	0	1	1	2 6 3	1	1	$(A_1, A_0) \leftarrow (P3_1, P3_0)$ $(A_3, A_2) \leftarrow 0$
	IAP4	1	0	0	1	1	0	0	1	0	0	2 6 4	1	1	(A)←(P4)
	CLD	0	0	0	0	0	1	0	0	0	1	0 1 1	1	1	(D)←1
	RD	0	0	0	0	0	1	0	1	0	0	0 1 4	1	1	(D(Y))←0, However, Y=0~12
	SD	0	0	0	0	0	1	0	1	0	1	0 1 5	1	1	(D(Y))←1, However, Y=0~12
	SZD	0	0	0	0	1	0	0	1	0	0	0 2 4	2	2	(D(Y))=0 ?, However, Y=8~10
		0	0	0	0	1	0	1	0	1	1	0 2 B			
	OP0A	1	0	0	0	1	0	0	0	0	0	2 2 0	1	1	(P0)←(A)
	OP1A	1	0	0	0	1	0	0	0	0	1	2 2 1	1	1	(P1)←(A)

Skip condition	Carry flag CY	Detailed description
—	—	Returns from interrupt service routine to main routine. Returns the value of data pointer (X, Y, Z), carry flag, skip status, NOP mode status by LA/LXY continuous description, register A and register B to the states before interrupt.
—	—	Returns from subroutine to the routine called this subroutine.
Skip at uncondition	—	Returns from subroutine to the routine called this subroutine and skips the next instruction at uncondition.
—	—	Resets (0) to the interrupt enable flag INTE, and disables the interrupt.
—	—	Sets (1) to the interrupt enable flag INTE, and enables the interrupt.
(EXF0) = 1	—	Skips the next instruction when EXF0 flag is "1". After skipping, resets the EXF0 flag.
—	—	Transfers the contents of register A to interrupt control register V1.
—	—	Transfers the contents of register A to interrupt control register I1.
—	—	Transfers the contents of interrupt control register V1 to register A.
—	—	Transfers the contents of interrupt control register I1 to register A.
—	—	Transfers the contents of register A to timer control register W1.
—	—	Transfers the contents of register A to timer control register W2.
—	—	Transfers the contents of register A to timer control register W3.
—	—	Transfers the contents of timer control register W1 to register A.
—	—	Transfers the contents of timer control register W2 to register A.
—	—	Transfers the contents of timer control register W3 to register A.
—	—	Transfers the contents of register A and register B to timer 3 and the reload register of timer 3.
—	—	Transfers the reload register value of timer 1 to timer 1.
—	—	Transfers the contents of register A and register B to reload register R1 of timer 1.
—	—	Transfers the contents of register A to reload register R1 of timer 1.
—	—	Transfers the contents of timer 3 to register A and register B.
(T1F) = 1	—	Skips the next instruction when the T1F flag is "1". Resets the T1F flag after skipping.
(T2F) = 1	—	Skips the next instruction when the T2F flag is "1". Resets the T2F flag after skipping.
(T3F) = 1	—	Skips the next instruction when the T3F flag is "1". Resets the T3F flag after skipping.
—	—	Transfers input to Port P0 to register A.
—	—	Transfers input to Port P1 to register A.
—	—	Transfers input to Port P2 to register A.
—	—	Transfers input to Port P3 to register A.
—	—	Transfers input to Port P4 to register A.
—	—	Sets (1) port D.
—	—	Resets (0) a bit of port D specified by register Y.
—	—	Sets (1) a bit of port D specified by register Y.
(D(Y)) = 0, However, Y = 8 ~ 10	—	When the contents of a bit of port D specified by register Y is "0", skips the next instruction.
—	—	Outputs the contents of register A to port P0.
—	—	Outputs the contents of register A to port P1.

Type of instructions \ Parameter	Mnemonic	Instruction code											Number of words	Number of cycles	Functions
		D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hexadecimal notation			
LCD control operations	TL1A	1	0	0	0	0	0	1	0	1	0	2 0 A	1	1	(L1)←(A)
	TAL1	1	0	0	1	0	0	1	0	1	0	2 4 A	1	1	(A)←(L1)
	TL2A	1	0	0	0	0	0	1	0	1	1	2 0 B	1	1	(L2)←(A)
	TL3A	1	0	0	0	0	0	1	1	0	0	2 0 C	1	1	(L3)←(A_0)
	TLCA	1	0	0	0	0	0	1	1	0	1	2 0 D	1	1	(LC)←(A)
Multi-carrier generating circuit operations	TPTA	1	0	1	0	1	0	0	1	0	1	2 A 5	1	1	(PT)←(A_1, A_0)
	TC1A	1	0	1	0	1	0	1	0	0	0	2 A 8	1	1	(C1)←(A)
	TPAA	1	0	1	0	1	0	1	0	1	0	2 A A	1	1	(PA)←(A)
	RC3	1	0	1	0	1	0	1	1	0	0	2 A C	1	1	(C3)←0
	SC3	1	0	1	0	1	0	1	1	0	1	2 A D	1	1	(C3)←1
	RC4	1	0	1	0	1	0	1	1	1	0	2 A E	1	1	(C4)←0
	SC4	1	0	1	0	1	0	1	1	1	1	2 A F	1	1	(C4)←1
	STCR	1	0	1	0	0	1	1	0	0	0	2 9 8	1	1	Carrier wave generating start
	SPCR	1	0	1	0	0	1	1	0	0	1	2 9 9	1	1	Carrier wave generating stop
	TC2A	1	0	1	0	1	0	1	0	0	1	2 A 9	1	1	(C2)←(A_1, A_0)
Other operations	NOP	0	0	0	0	0	0	0	0	0	0	0 0 0	1	1	(PC)←(PC)+1
	POF	0	0	0	0	0	0	0	0	1	0	0 0 2	1	1	Power down 1
	POF2	0	0	0	0	0	0	1	0	0	0	0 0 8	1	1	Power down 2
	SNZP	0	0	0	0	0	0	0	0	1	1	0 0 3	1	1	(P)=1 ?
	TMRA	1	0	0	0	0	1	0	1	1	0	2 1 6	1	1	(MR_2~MR_0)←(A_2~A_0)
	TAMR	1	0	0	1	0	1	0	0	1	0	2 5 2	1	1	(A_2~A_0)←(MR_2~MR_0), (A_3)←0
	WRST	1	0	1	0	1	0	0	0	0	0	2 A 0	1	1	(WDF)←0

Skip condition	Carry flag CY	Detailed description
—	—	Transfers the contents of register A to LCD control register L1.
—	—	Transfers the contents of LCD control register L1 to register A.
—	—	Transfers the contents of register A to LCD control register L2.
—	—	Transfers the contents of register A to LCD control register L3.
—	—	Transfers the contents of register A to LC counter and reload register.
—	—	Transfers the contents of register A to compensation control timer PT.
—	—	Transfers the contents of register A to data control register C1.
—	—	Transfers the contents of register A to preset register PA.
—	—	Resets (0) the output control flag C3 and disables carrier wave output.
—	—	Sets (1) the output control flag C3 and enables carrier wave output.
—	—	Resets (0) to C4 flag.
—	—	Sets (1) to C4 flag.
—	—	Starts generating of carrier wave.
—	—	Stops generating of carrier wave.
—	—	Transfers the contents of register A to compensation control register C2.
—	—	No operation
—	—	Puts the system in power down 1 state (clock operation mode) $f(X_{CIN})$ oscillation, LCD, timer 2 and timer 3 can be used.
—	—	Puts the system in power down 2 state (RAM back-up mode). Oscillations are all stopped.
(P) = 1	—	Skips the next instruction when p flag is "1". After skipping, p flag is not changed.
—	—	Transfers the contents of register A to clock control register MR.
—	—	Transfers the contents of clock control register MR to register A.
—	—	Resets watchdog flag WDF.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		−0.3~7	V
V_I	Input voltage P0, P1, P2, D_8~D_{10}, P3, P4, $\overline{RESET}$, X_{IN}		−0.3~V_{DD}+0.3	V
V_I	Input voltage V_{LC1}, V_{LC2}, V_{LC3}		−0.3~V_{DD}+0.3	V
V_O	Output voltage P0, P1, D, $\overline{RESET}$	Output transistors cut-off	−0.3~V_{DD}+0.3	V
V_O	Output voltage X_{OUT}, CARR		−0.3~V_{DD}+0.3	V
V_O	Output voltage SEG, COM		−0.3~V_{LC3}+0.3	V
Pd	Power dissipation		300	mW
Topr	Operating temperature range		−20~70	℃
Tstg	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20~70℃, V_{DD}=2.2~3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{DD}	Supply voltage	f(X_{IN})=1MHz	2.2		3.6	V
V_{RAM}	RAM ratain voltage (at RAM back-up mode)		2.0		3.6	V
V_{SS}	Supply voltage			0		V
V_{LC3}	Supply voltage for LCD (Note 1)		2.2		3.6	V
V_{IH}	"H" level input voltage P0, P1, P2, P3, P4, D_8~D_{10}	V_{DD}=3.0V	0.8V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage X_{IN}	V_{DD}=3.0V	0.7V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage $\overline{RESET}$	V_{DD}=3.0V	0.85V_{DD}		V_{DD}	V
V_{IH}	"H" level input voltage INT	V_{DD}=3.0V	0.8V_{DD}		V_{DD}	V
V_{IL}	"L" level input voltage P0, P1, P2, P3, P4, D_8~D_{10}	V_{DD}=3.0V	0		0.3V_{DD}	V
V_{IL}	"L" level input voltage X_{IN}	V_{DD}=3.0V	0		0.3V_{DD}	V
V_{IL}	"L" level input voltage $\overline{RESET}$	V_{DD}=3.0V	0		0.3V_{DD}	V
V_{IL}	"L" level input voltage INT	V_{DD}=3.0V	0		0.2V_{DD}	V
I_{OL}(peak)	"L" level peak output current P0, P1, D_0~D_7, D_{10}~D_{12}, CARR, $\overline{RESET}$				4	mA
I_{OL}(peak)	"L" level peak output current D_8, D_9				24	mA
I_{OL}(avg)	"L" level average output current P0, P1, D_0~D_7, D_{10}~D_{12}, CARR, $\overline{RESET}$				2	mA
I_{OL}(avg)	"L" level average output current D_8, D_9				12	mA
I_{OH}(peak)	"H" level peak output current CARR		−30			mA
I_{OH}(avg)	"H" level average output current CARR		−15			mA
f(X_{IN})	f(X_{IN}) clock frequency	at ceramic oscillation			1	kHz
f(X_{IN})	f(X_{IN}) clock frequency (Note 2)	at external clock			500	kHz
f(X_{CIN})	f(X_{CIN}) clock frequency	Crystal oscillation	32		50	kHz

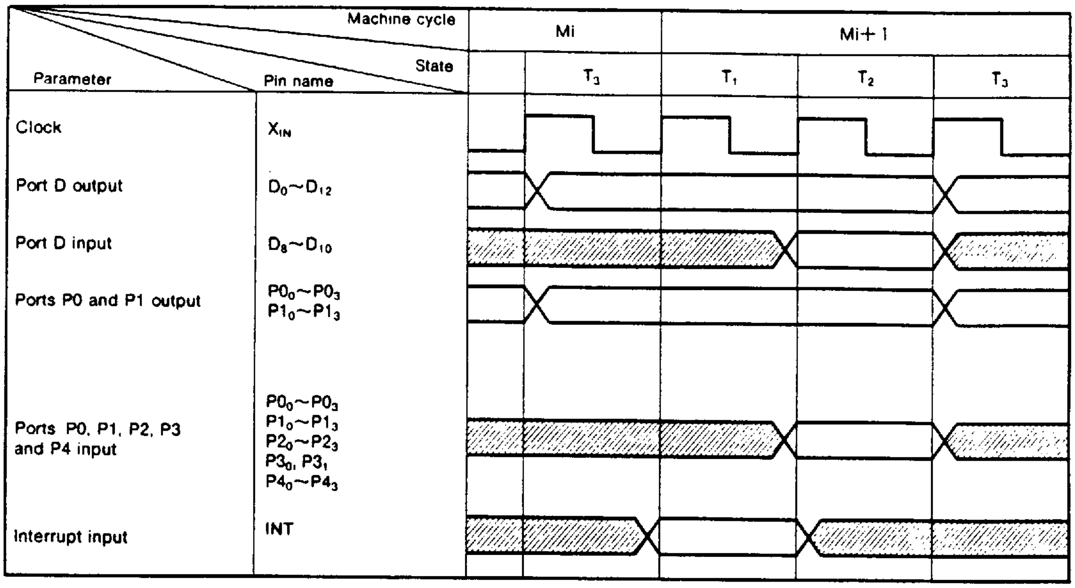
Note 1. at 1/2 bias : V_{LC1}=V_{LC2}=1/2 · V_{LC3}
at 1/3 bias : V_{LC1}=1/3 · V_{LC3}, V_{LC2}=2/3 · V_{LC3}
2. External clock duty is 30~70%.

ELECTRICAL CHARACTERISTICS (T_a=−20~70℃, V_{DD}=3V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OL}	"L" level output voltage P0, P1, D_0~D_7, D_{10}~D_{12}, CARR, $\overline{RESET}$		I_{OL}=2mA			0.9	V
V_{OL}	"L" level output voltage D_8, D_9		I_{OL}=12mA			1.5	V
V_{OH}	"H" level output voltage CARR		I_{OH}=−7mA	1.0			V
I_{IH}	"H" level input current P0, P1, P2, P3, P4, D_8~D_{10}, $\overline{RESET}$		V_I=V_{DD} (Note 1)			1	μA
I_{IL}	"L" level input current P2, P3, P4, D_8~D_{10}, $\overline{RESET}$		V_I=0V (Note 1)	−1			μA
I_{OZ}	OFF-state output current D_0~D_7		V_O=V_{DD}			1	μA
I_{DD}	Supply current	at CPU high-speed operation	f(X_{IN})=1MHz f(X_{CIN})=32kHz		1	2	mA
			f(X_{IN})=500kHz f(X_{CIN})=32kHz		0.5	1.0	mA
		at CPU low-speed operation	f(X_{IN})=Stop f(X_{CIN})=32kHz		20	50	μA
		Clock operating mode at LCD operation	f(X_{IN})=Stop f(X_{CIN})=32kHz T_a=25℃		4	10	μA
			f(X_{IN})=Stop f(X_{CIN})=32kHz			15	μA
		at RAM back-up mode	f(X_{IN})=Stop f(X_{CIN})=Stop T_a=25℃		0.1	1.0	μA
			f(X_{IN})=Stop f(X_{CIN})=Stop			10	μA
R_{PH}	Pull-up resistance value		V_{DD}=3V V_I=0V	40	100	250	kΩ
V_+ V_-	Hysteresis INT				0.4		V
V_+ V_-	Hysteresis $\overline{RESET}$				0.7		V
R_{COM}	COM output impedance		(Note 2)		2	10	kΩ
R_{SEG}	SEG output impedance		(Note 2)		3	15	kΩ
R_{VLC}	Internal resistance value for LCD power (Impedance between V_{LC3} and V_{SS})		T_a=25℃	300	600	1200	kΩ

Note : In this case, port P4 is selected as input port by software.
External power is used for LCD power and measurement is performed with all pins freed except the measurement pin.

BASIC TIMING DIAGRAM



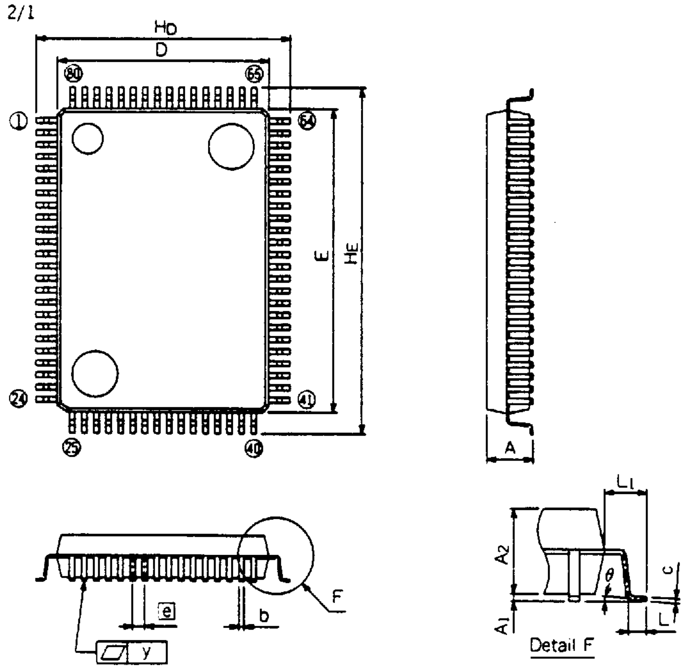
PACKAGE OUTLINE

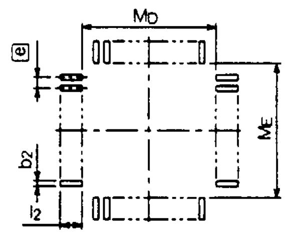
80P6N−A

Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
＊QFP080-P-1420	−	1.58

Scale : 2/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	−	−	3.05
A1	0	0.1	0.2
A2	−	2.8	−
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	−	0.8	−
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	−	1.4	−
y	−	−	0.1
θ	0°	−	10°
b2	−	0.5	−
l2	−	1.3	−
MD	−	14.6	−
ME	−	20.6	−

All values shown in this catalogue are subject to change for product improvement.
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