

**Precision Waveform Generator/Voltage Controlled Oscillator**

The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

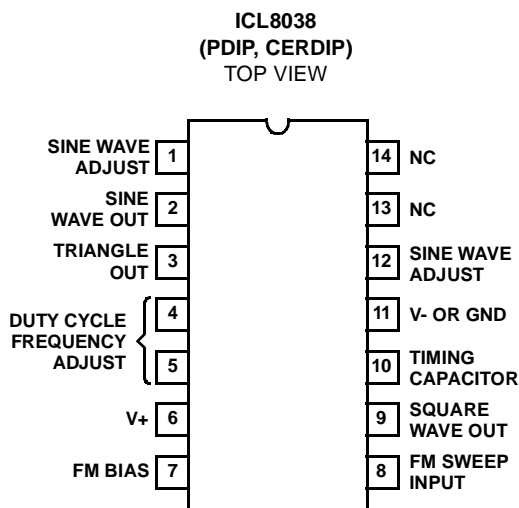
**Features**

- Low Frequency Drift with Temperature. . . . . 250ppm/°C
- Low Distortion . . . . . 1% (Sine Wave Output)
- High Linearity . . . . . 0.1% (Triangle Wave Output)
- Wide Frequency Range . . . . . 0.001Hz to 300kHz
- Variable Duty Cycle . . . . . 2% to 98%
- High Level Outputs. . . . . TTL to 28V
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Easy to Use - Just a Handful of External Components Required

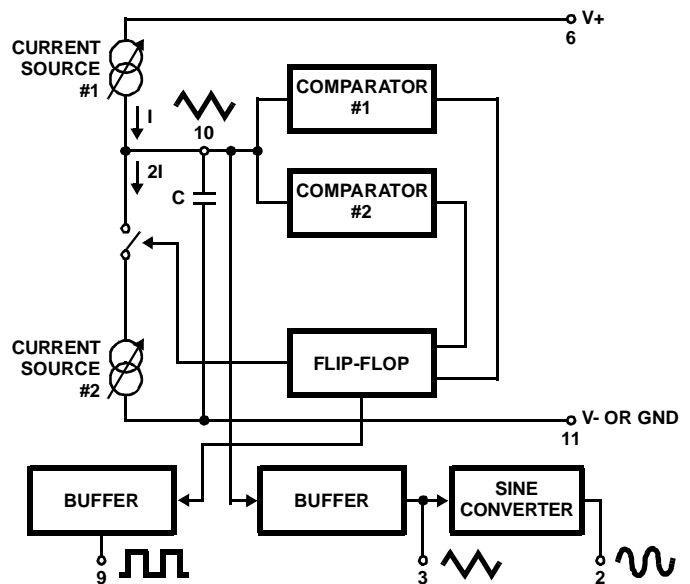
**Ordering Information**

PART NUMBER	STABILITY	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL8038CCPD	250ppm/°C (Typ)	0 to 70	14 Ld PDIP	E14.3
ICL8038CCJD	250ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
ICL8038BCJD	180ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
ICL8038ACJD	120ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3

**Pinout**



**Functional Diagram**



**Absolute Maximum Ratings**

Supply Voltage (V- to V+) . . . . . 36V  
 Input Voltage (Any Pin) . . . . . V- to V+  
 Input Current (Pins 4 and 5) . . . . . 25mA  
 Output Sink Current (Pins 3 and 9) . . . . . 25mA

**Operating Conditions**

Temperature Range  
 ICL8038AC, ICL8038BC, ICL8038CC . . . . . 0°C to 70°C

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  $\theta_{JC}$  (°C/W)  
 CERDIP Package . . . . . 75 20  
 PDIP Package . . . . . 115 N/A  
 Maximum Junction Temperature (Ceramic Package) . . . . . 175°C  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

**Die Characteristics**

Back Side Potential . . . . . V-

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $V_{SUPPLY} = \pm 10V$  or  $+20V$ ,  $T_A = 25^\circ C$ ,  $R_L = 10k\Omega$ , Test Circuit Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC			ICL8038AC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Operating Range	$V_{SUPPLY}$ V+	Single Supply	+10	-	+30	+10	-	+30	+10	-	+30	V
	V+, V-	Dual Supplies	±5	-	±15	±5	-	±15	±5	-	±15	V
Supply Current	$I_{SUPPLY}$	$V_{SUPPLY} = \pm 10V$ (Note 2)		12	20	-	12	20	-	12	20	mA

**FREQUENCY CHARACTERISTICS** (All Waveforms)

Max. Frequency of Oscillation	$f_{MAX}$		100	-	-	100	-	-	100	-	-	kHz
Sweep Frequency of FM Input	$f_{SWEEP}$		-	10	-	-	10	-	-	10	-	kHz
Sweep FM Range		(Note 3)	-	35:1	-	-	35:1	-	-	35:1	-	
FM Linearity		10:1 Ratio	-	0.5	-	-	0.2	-	-	0.2	-	%
Frequency Drift with Temperature (Note 5)	$\Delta f/\Delta T$	0°C to 70°C	-	250	-	-	180	-	-	120		ppm/°C
Frequency Drift with Supply Voltage	$\Delta f/\Delta V$	Over Supply Voltage Range	-	0.05	-	-	0.05		-	0.05	-	%/V

**OUTPUT CHARACTERISTICS**

Square Wave												
Leakage Current	$I_{OLK}$	$V_G = 30V$	-	-	1	-	-	1	-	-	1	µA
Saturation Voltage	$V_{SAT}$	$I_{SINK} = 2mA$	-	0.2	0.5	-	0.2	0.4	-	0.2	0.4	V
Rise Time	$t_R$	$R_L = 4.7k\Omega$	-	180	-	-	180	-	-	180	-	ns
Fall Time	$t_F$	$R_L = 4.7k\Omega$	-	40	-	-	40	-	-	40	-	ns
Typical Duty Cycle Adjust (Note 6)	$\Delta D$		2		98	2	-	98	2	-	98	%
Triangle/Sawtooth/Ramp												
Amplitude	$V_{TRIANGLE}$	$R_{TRI} = 100k\Omega$	0.30	0.33	-	0.30	0.33	-	0.30	0.33	-	x $V_{SUPPLY}$
Linearity			-	0.1	-	-	0.05	-	-	0.05	-	%
Output Impedance	$Z_{OUT}$	$I_{OUT} = 5mA$	-	200	-	-	200	-	-	200	-	Ω

# ICL8038

## Electrical Specifications $V_{SUPPLY} = \pm 10V$ or $+20V$ , $T_A = 25^\circ C$ , $R_L = 10k\Omega$ , Test Circuit Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC			ICL8038AC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Sine Wave												
Amplitude	$V_{SINE}$	$R_{SINE} = 100k\Omega$	0.2	0.22	-	0.2	0.22	-	0.2	0.22	-	$xV_{SUPPLY}$
THD	THD	$R_S = 1M\Omega$ (Note 4)	-	2.0	5	-	1.5	3	-	1.0	1.5	%
THD Adjusted	THD	Use Figure 4	-	1.5	-	-	1.0	-	-	0.8	-	%

### NOTES:

2.  $R_A$  and  $R_B$  currents not included.
3.  $V_{SUPPLY} = 20V$ ;  $R_A$  and  $R_B = 10k\Omega$ ,  $f \cong 10kHz$  nominal; can be extended 1000 to 1. See Figures 5A and 5B.
4.  $82k\Omega$  connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use  $R_A$  and  $R_B$ .)
5. Figure 1, pins 7 and 8 connected,  $V_{SUPPLY} = \pm 10V$ . See Typical Curves for T.C. vs  $V_{SUPPLY}$ .
6. Not tested, typical value for design purposes only.

### Test Conditions

PARAMETER	$R_A$	$R_B$	$R_L$	C	$SW_1$	MEASURE
Supply Current	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Current Into Pin 6
Sweep FM Range (Note 7)	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage (Note 8)	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Frequency at Pin 9
Output Amplitude (Note 10)						
Sine	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Pk-Pk Output at Pin 2
Triangle	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Pk-Pk Output at Pin 3
Leakage Current (Off) (Note 9)	10k $\Omega$	10k $\Omega$		3.3nF	Closed	Current into Pin 9
Saturation Voltage (On) (Note 9)	10k $\Omega$	10k $\Omega$		3.3nF	Closed	Output (Low) at Pin 9
Rise and Fall Times (Note 11)	10k $\Omega$	10k $\Omega$	4.7k $\Omega$	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust (Note 11)						
Max	50k $\Omega$	~1.6k $\Omega$	10k $\Omega$	3.3nF	Closed	Waveform at Pin 9
Min	~25k $\Omega$	50k $\Omega$	10k $\Omega$	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10k $\Omega$	10k $\Omega$	10k $\Omega$	3.3nF	Closed	Waveform at Pin 2

### NOTES:

7. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 ( $f_{HI}$ ) and then connecting pin 8 to pin 6 ( $f_{LO}$ ). Otherwise apply Sweep Voltage at pin 8 ( $\frac{2}{3} V_{SUPPLY} + 2V$ )  $\leq V_{SWEEP} \leq V_{SUPPLY}$  where  $V_{SUPPLY}$  is the total supply voltage. In Figure 5B, pin 8 should vary between 5.3V and 10V with respect to ground.
8.  $10V \leq V+ \leq 30V$ , or  $\pm 5V \leq V_{SUPPLY} \leq \pm 15V$ .
9. Oscillation can be halted by forcing pin 10 to +5V or -5V.
10. Output Amplitude is tested under static conditions by forcing pin 10 to 5V then to -5V.
11. Not tested; for design purposes only.

Test Circuit

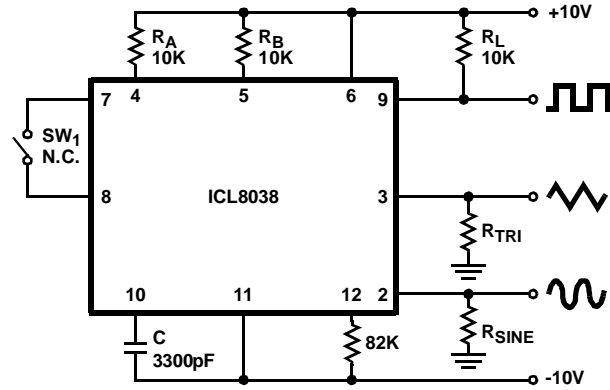
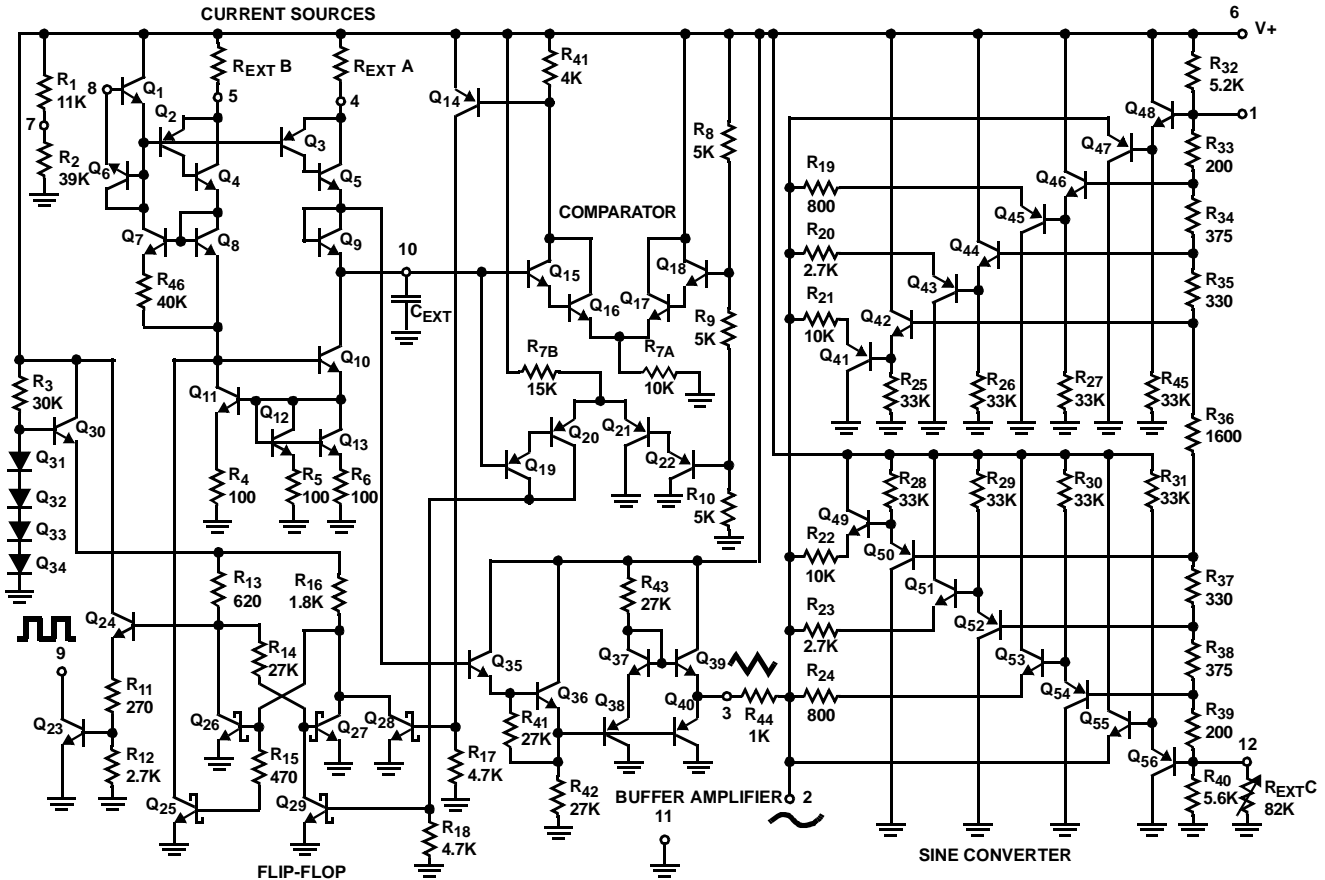


FIGURE 1. TEST CIRCUIT

Detailed Schematic



Application Information (See Functional Diagram)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a

net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at Terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at Terminal 9.

The sine wave is created by feeding the triangle wave into a nonlinear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves toward the two extremes.

**Waveform Timing**

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 3. Best results are obtained by keeping the timing resistors  $R_A$  and  $R_B$  separate (A).  $R_A$  controls the rising portion of the triangle and sine wave and the 1 state of the square wave.

The magnitude of the triangle waveform is set at  $1/3 V_{SUPPLY}$ ; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{1} = \frac{C \times 1/3 V_{SUPPLY}}{2(0.22) \frac{V_{SUPPLY}}{R_B} - 0.22 \frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when  $R_A = R_B$ .

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 3B is slightly more convenient. A 1kΩ potentiometer may not allow the duty cycle to be adjusted through 50% on all devices. If a 50% duty cycle is required, a 2kΩ or 5kΩ potentiometer should be used.

With two separate timing resistors, the frequency is given by:

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66} \left( 1 + \frac{R_B}{2R_A - R_B} \right)}$$

or, if  $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 3A)}$$

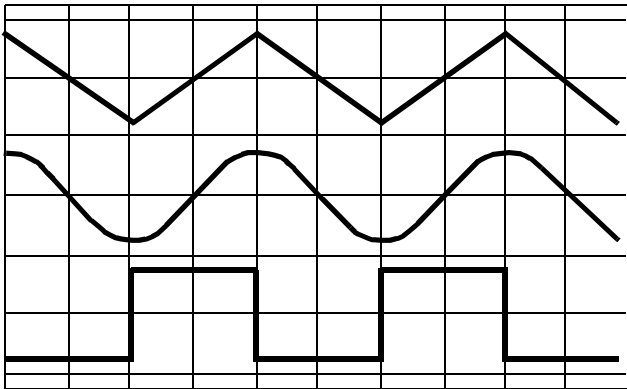


FIGURE 2A. SQUARE WAVE DUTY CYCLE - 50%

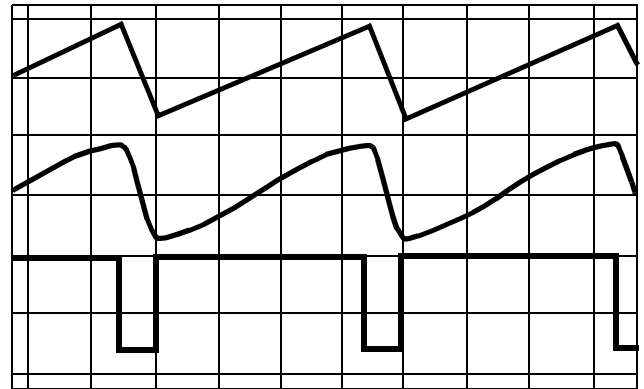


FIGURE 2B. SQUARE WAVE DUTY CYCLE - 80%

FIGURE 2. PHASE RELATIONSHIP OF WAVEFORMS

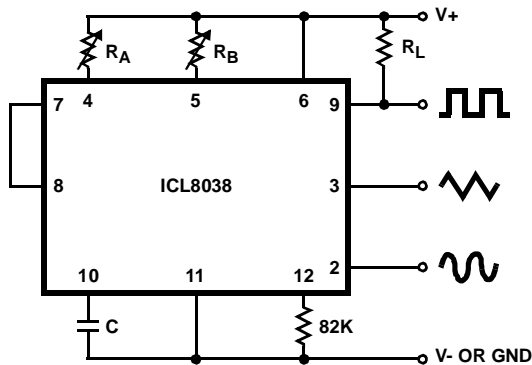


FIGURE 3A.

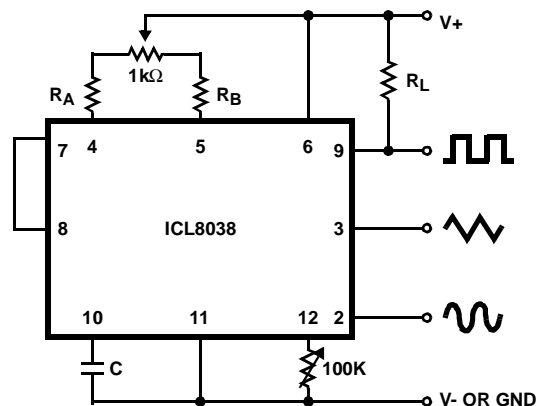


FIGURE 3B.

FIGURE 3. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents and thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

**Reducing Distortion**

To minimize sine wave distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 4; this configuration allows a typical reduction of sine wave distortion close to 0.5%.

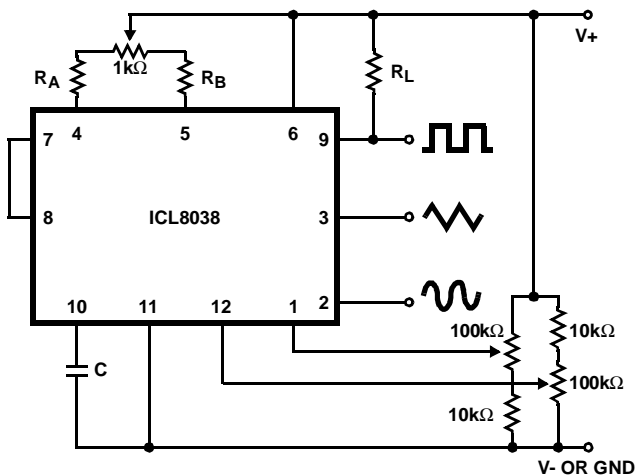


FIGURE 4. CONNECTION TO ACHIEVE MINIMUM SINE WAVE DISTORTION

**Selecting RA, RB and C**

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to RA can be calculated from:

$$I = \frac{R_1 \times (V+ - V-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V+ - V-)}{R_A}$$

R1 and R2 are shown in the Detailed Schematic.

A similar calculation holds for RB.

The capacitor value should be chosen at the upper end of its possible range.

**Waveform Out Level Control and Power Supplies**

The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (±5V to ±15V). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

**Frequency Modulation and Sweeping**

The frequency of the waveform generator is a direct function of the DC voltage at Terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 5A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 5B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = Minimum at VSWEPT = 0, i.e., Pin 8 = V+). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by (1/3 VSUPPLY - 2V).

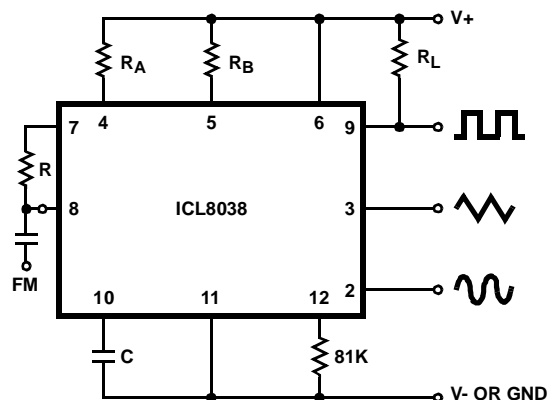


FIGURE 5A. CONNECTIONS FOR FREQUENCY MODULATION

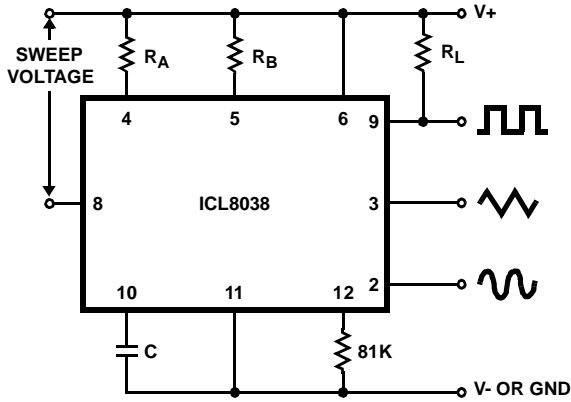


FIGURE 5B. CONNECTIONS FOR FREQUENCY SWEEP  
FIGURE 5.

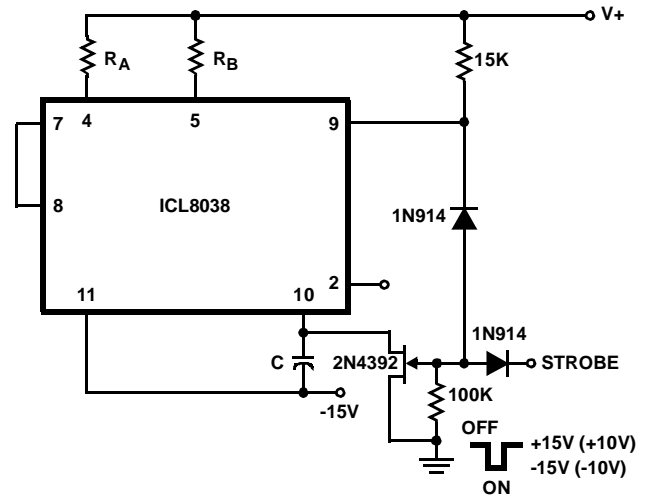


FIGURE 7. STROBE TONE BURST GENERATOR

**Typical Applications**

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 6 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

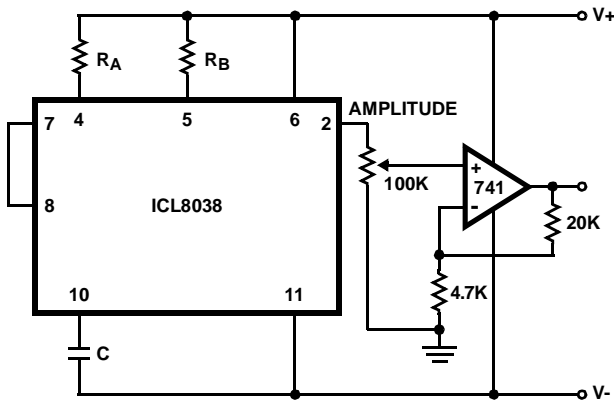


FIGURE 6. SINE WAVE OUTPUT BUFFER AMPLIFIERS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 7 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors  $R_A$  and  $R_B$  must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of  $R_A$  and  $R_B$  by a few hundred mV. The Circuit of Figure 8 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 10.

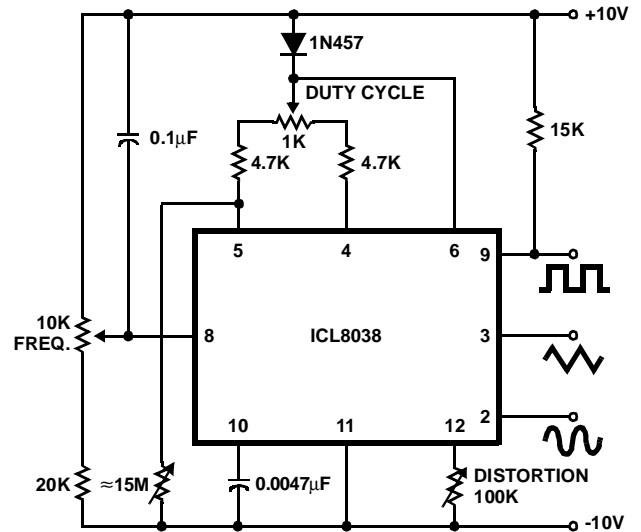


FIGURE 8. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHzY

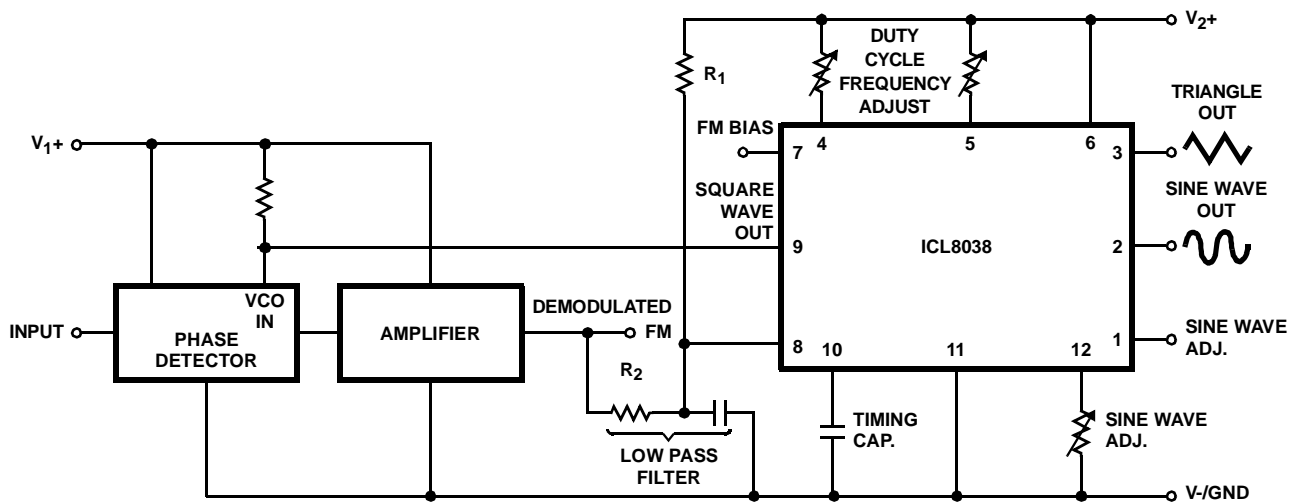


FIGURE 9. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP

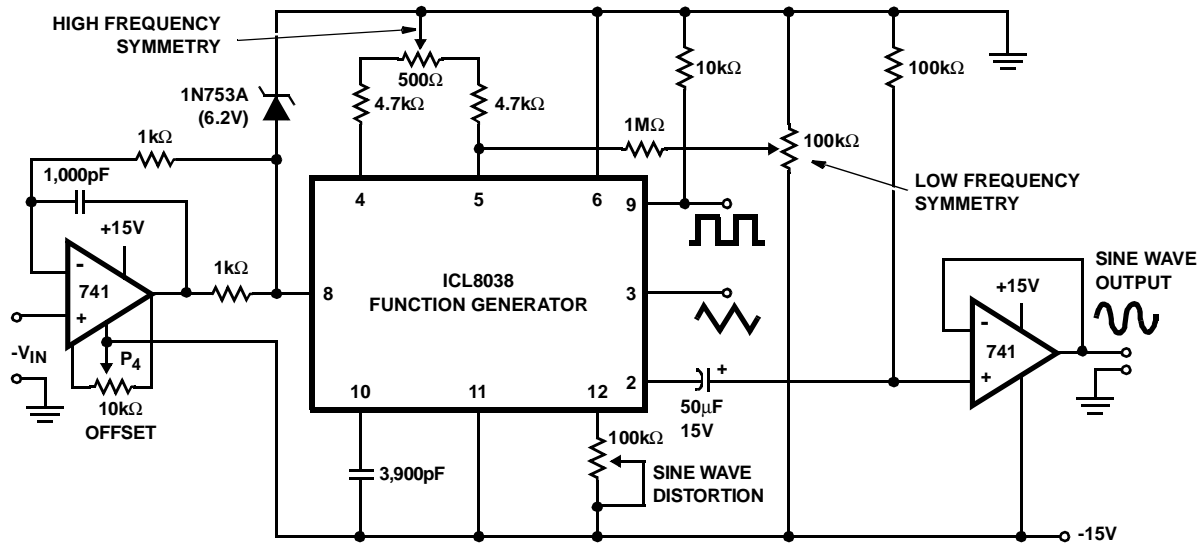


FIGURE 10. LINEAR VOLTAGE CONTROLLED OSCILLATOR

### Use in Phase Locked Loops

Its high frequency stability makes the ICL8038 an ideal building block for a phase locked loop as shown in Figure 9. In this application the remaining functional blocks, the phase detector and the amplifier, can be formed by a number of available ICs (e.g., MC4344, NE562).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to  $V_+$  ( $R_1$ ,  $R_2$  as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note AN013, "Everything You Always Wanted to Know About the ICL8038".



**Definition of Terms**

**Supply Voltage** ( $V_{SUPPLY}$ ). The total supply voltage from  $V+$  to  $V-$ .

**Supply Current.** The supply current required from the power supply to operate the device, excluding load currents and the currents through  $R_A$  and  $R_B$ .

**Frequency Range.** The frequency range at the square wave output through which circuit operation is guaranteed.

**Sweep FM Range.** The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range:

$$(\frac{2}{3} V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

**FM Linearity.** The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

**Output Amplitude.** The peak-to-peak signal amplitude appearing at the outputs.

**Saturation Voltage.** The output voltage at the collector of  $Q_{23}$  when this transistor is turned on. It is measured for a sink current of 2mA.

**Rise and Fall Times.** The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

**Triangle Waveform Linearity.** The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

**Total Harmonic Distortion.** The total harmonic distortion at the sine wave output.

**Typical Performance Curves**

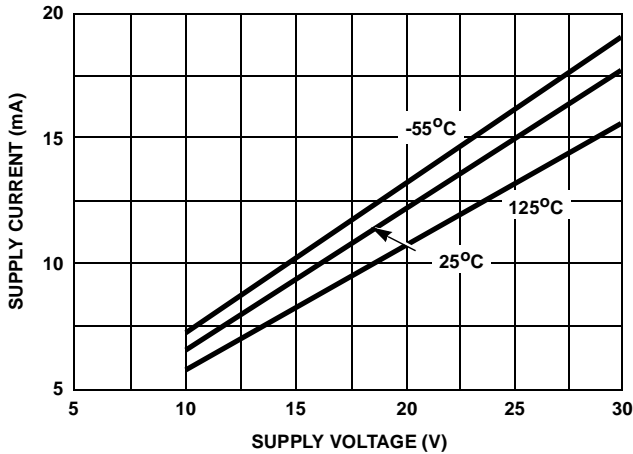


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

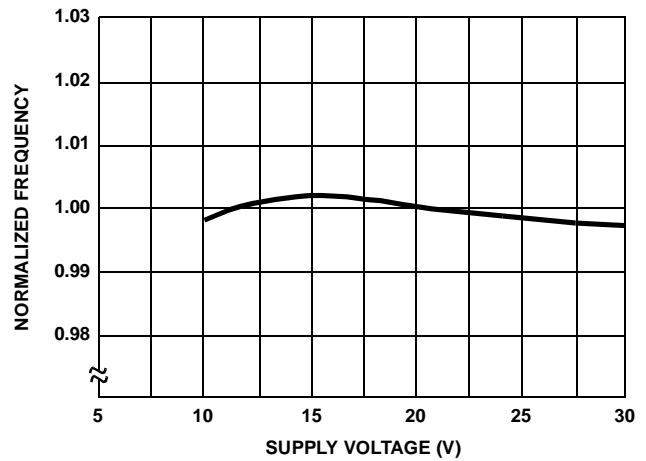


FIGURE 12. FREQUENCY vs SUPPLY VOLTAGE

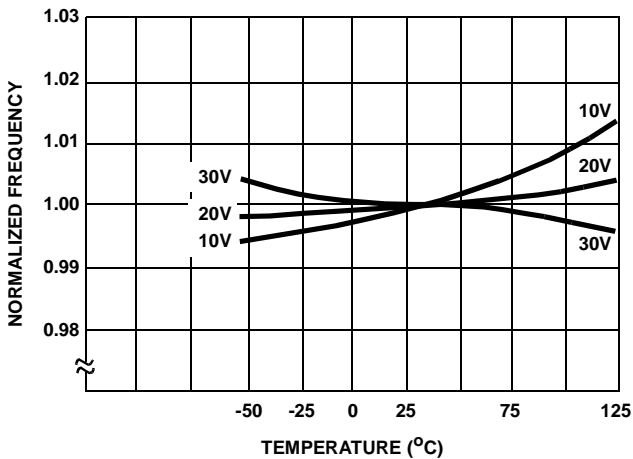


FIGURE 13. FREQUENCY vs TEMPERATURE

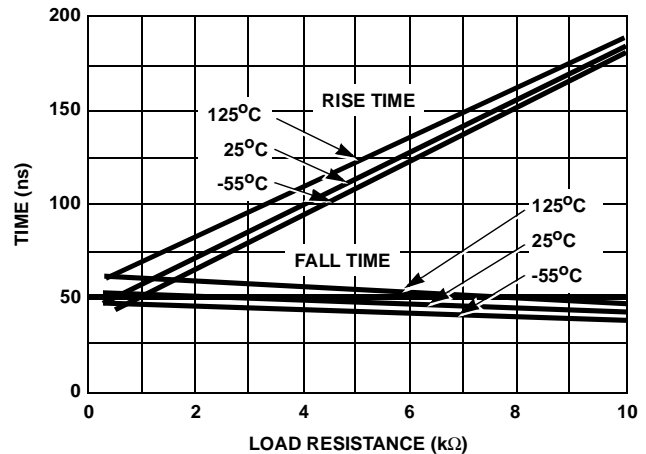


FIGURE 14. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE

Typical Performance Curves (Continued)

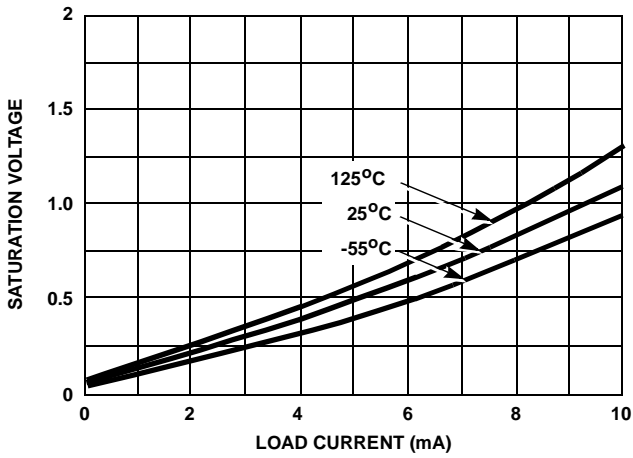


FIGURE 15. SQUARE WAVE SATURATION VOLTAGE vs LOAD CURRENT

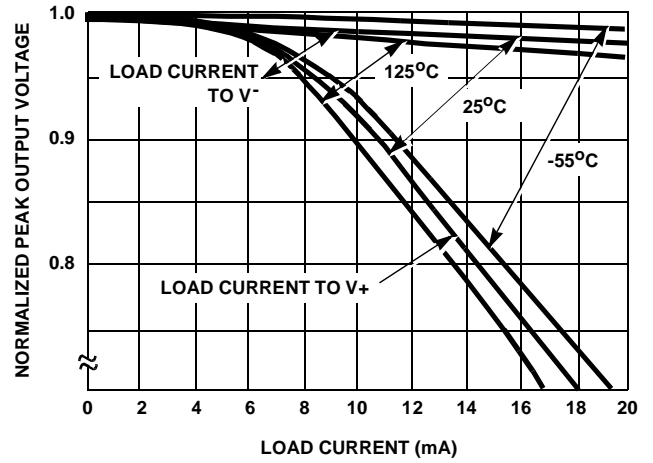


FIGURE 16. TRIANGLE WAVE OUTPUT VOLTAGE vs LOAD CURRENT

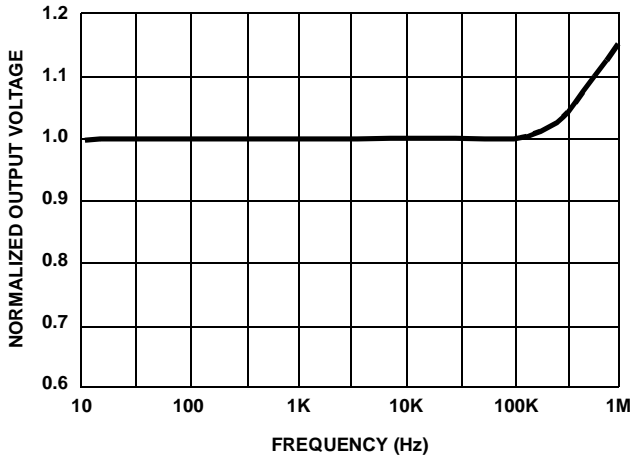


FIGURE 17. TRIANGLE WAVE OUTPUT VOLTAGE vs FREQUENCY

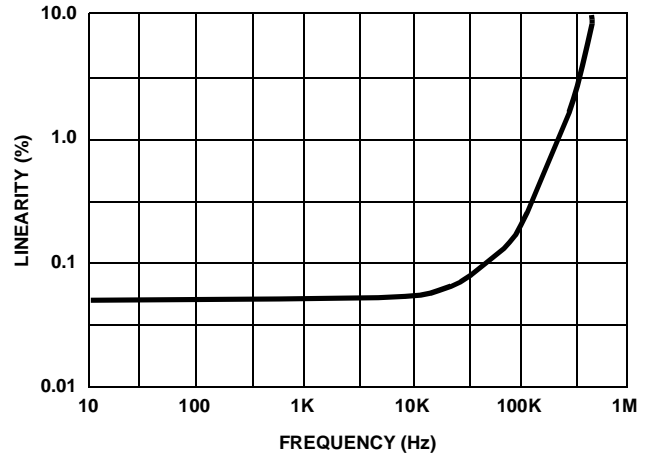


FIGURE 18. TRIANGLE WAVE LINEARITY vs FREQUENCY

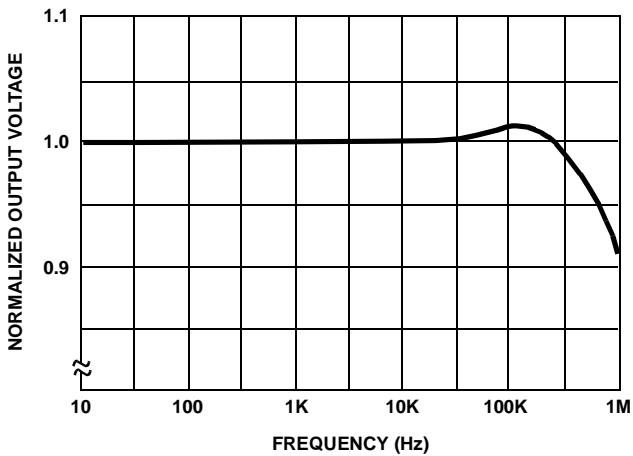


FIGURE 19. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

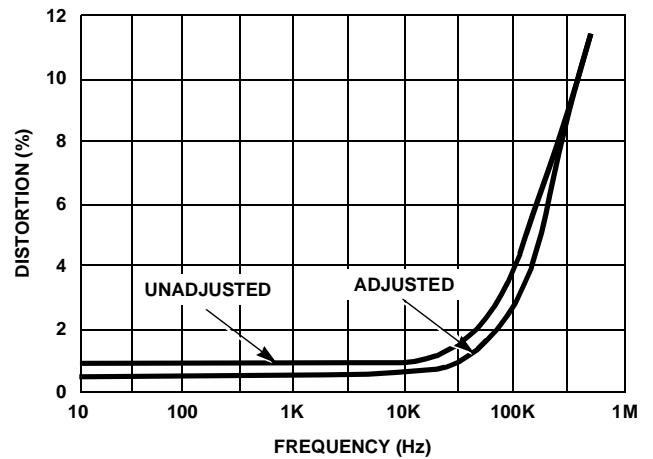
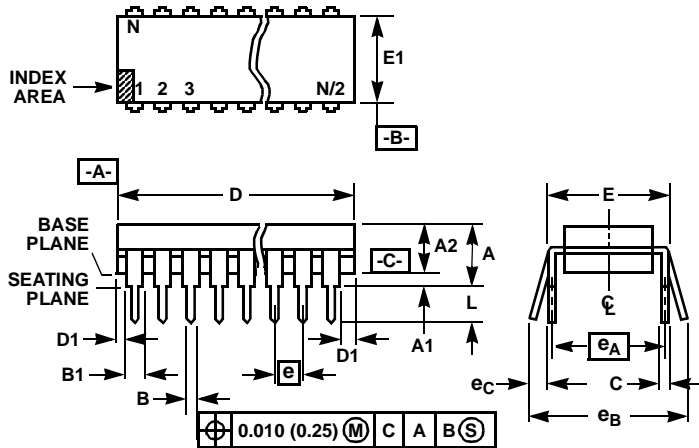


FIGURE 20. SINE WAVE DISTORTION vs FREQUENCY

Dual-In-Line Plastic Packages (PDIP)



NOTES:

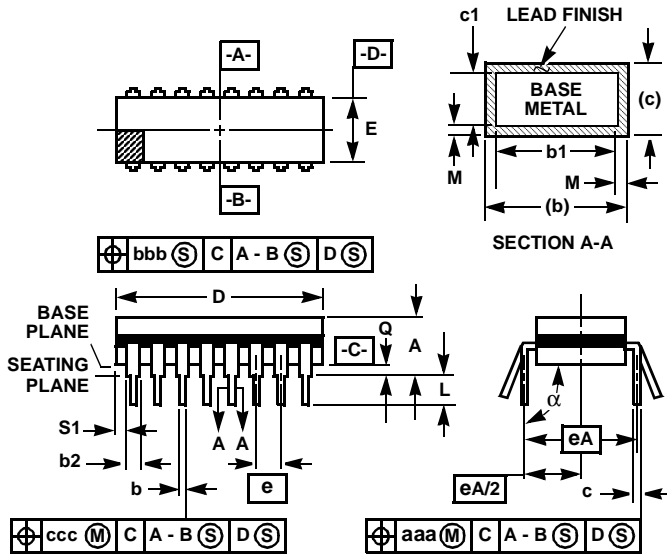
- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum [-C-].
- e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)  
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.300 BSC		7.62 BSC		6
e <sub>B</sub>	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

**Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)  
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
$\alpha$	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

All Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at website [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)

**Sales Office Headquarters**

**NORTH AMERICA**

Intersil Corporation  
2401 Palm Bay Rd., Mail Stop 53-204  
Palm Bay, FL 32905  
TEL: (321) 724-7000  
FAX: (321) 724-7240

**EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**

Intersil Ltd.  
8F-2, 96, Sec. 1, Chien-kuo North,  
Taipei, Taiwan 104  
Republic of China  
TEL: 886-2-2515-8508  
FAX: 886-2-2515-8369