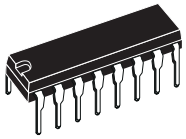
HCF40105B

FIFO REGISTER

- INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS
- 3-STATE OUTPUTS
- EXPANDABLE IN EITHER DIRECTION
- STATUS INDICATORS ON INPUT AND OUTPUT
- RESET CAPABILITY
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

ORDER CODES

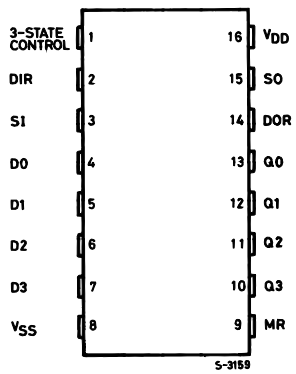
PACKAGE	TUBE	T & R
DIP	HCF40105BEY	

DESCRIPTION

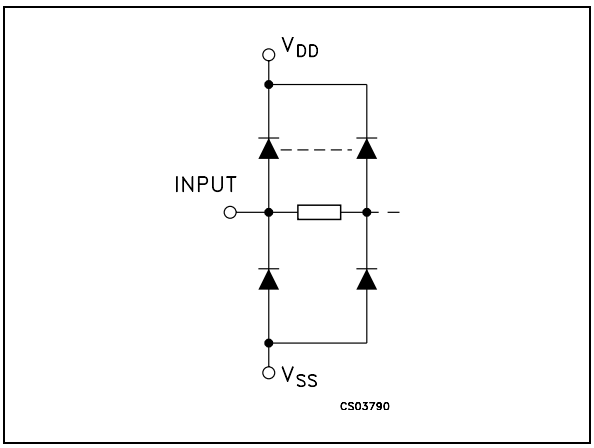
HCF40105B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP packages.

HCF40105B is a low power first-in-first-out (FIFO) "elastic" storage register that can store 164-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. "1" signifies that the position's data is filled and "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data is removed from the bottom of the data stack (the output and), all data entered later will automatically propagate (ripple) toward the output.

PIN CONNECTION



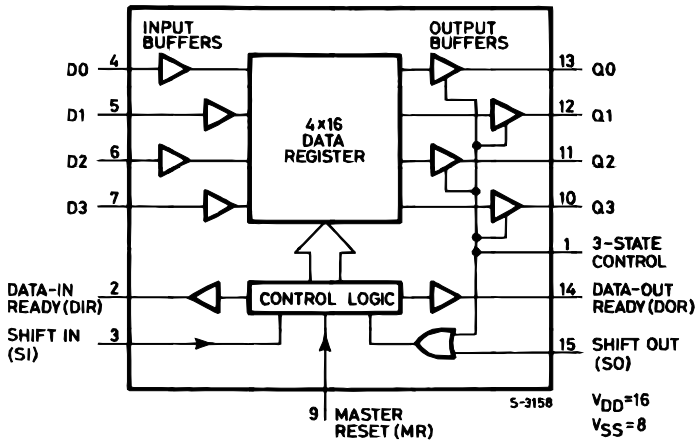
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	3-STATE CONTROL	3-State Control
2	DIR	Data-In Ready
3	SI	Shift In
15	SO	Shift Out
14	DOR	Data-Out Ready
4, 5, 6, 7	D0 to D3	Input Buffers
13, 12, 11, 10	Q0 to Q3	Output Buffers
9	MR	Master Reset
8	VSS	Negative Supply Voltage
16	VDD	Positive Supply Voltage

FUNCTIONAL DIAGRAM

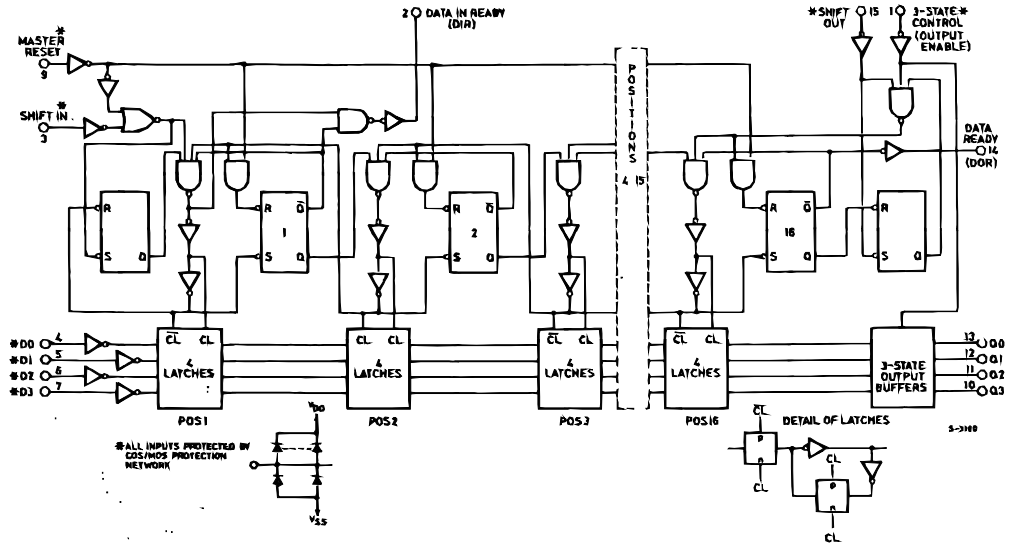


TRUTH TABLE

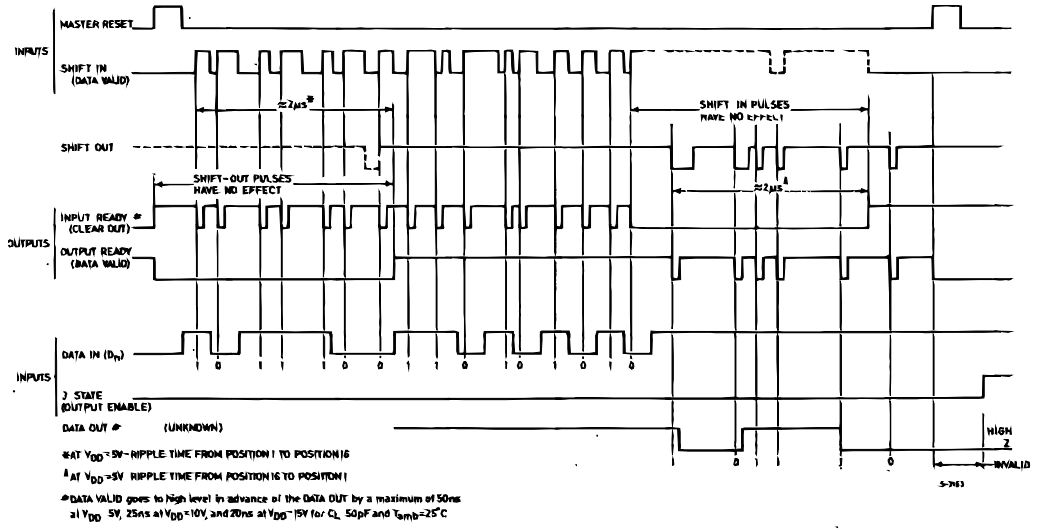
CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Synchronous	Inhibit Counter
H	H	H	L		Count Down
H	H	L	X		Preset on Next Positive Clock Transition
H	L	X	X	Asynchronous	Preset Asynchronously
L	X	X	X		Clear to Maximum Count

X : Don't Care
Clock connected to Clock input
Synchronous Operation : changes occur on negative to positive clock transitions.

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

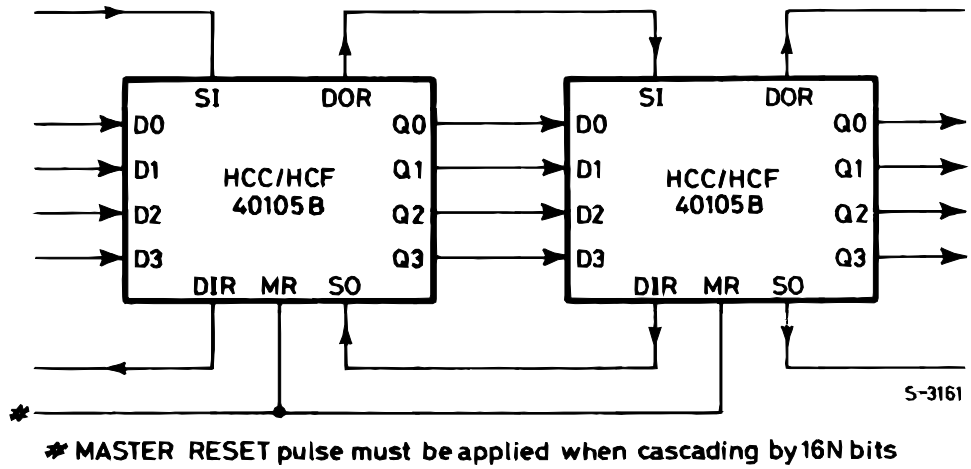
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL}	Propagation Delay Time Shift-out or Reset to Data out Ready	5			185	370	ns
		10			90	180	
		15			65	130	
t_{PHL}	Propagation Delay Time Shift-in to Data-in Ready	5			160	320	ns
		10			65	130	
		15			45	90	
t_{PZH} t_{PLZ}	Propagation Delay Time 3-State Control to Data-out	5			140	280	ns
		10			60	120	
		15			40	80	
t_{PHZ} t_{PLZ}	Propagation Delay Time 3-State Control to data-out	5			100	200	ns
		10			50	100	
		15			40	80	
t_{PLH}	Ripple-trough Delay Input to Output	5			2	4	µs
		10			1	2	
		15			0.7	1.4	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_I	Shift-in or Shift-out Rate	5			1.5	3	MHz
		10			3	6	
		15			4	8	
t_{WH}	Shift-in Pulse Width	5		200	100		ns
		10		80	40		
		15		60	30		
t_{WL}	Shift-out Pulse Width	5		360	180		ns
		10		160	80		
		15		100	50		
t_r	Shift-in or Shift-out Rise Time	5				15	µs
		10				15	
		15				15	
t_f	Shift-in Fall Time	5				15	µs
		10				15	
		15				15	
t_f	Shift-out Fall Time	5				15	µs
		10				5	
		15				5	
t_{setup}	Data Setup Time	5		0			ns
		10		0			
		15		0			
t_{hold}	Data Hold Time	5		350	175		ns
		10		150	75		
		15		120	60		
t_{WL}	Data-in Ready Pulse Width	5			260	520	ns
		10			100	120	
		15			70	140	

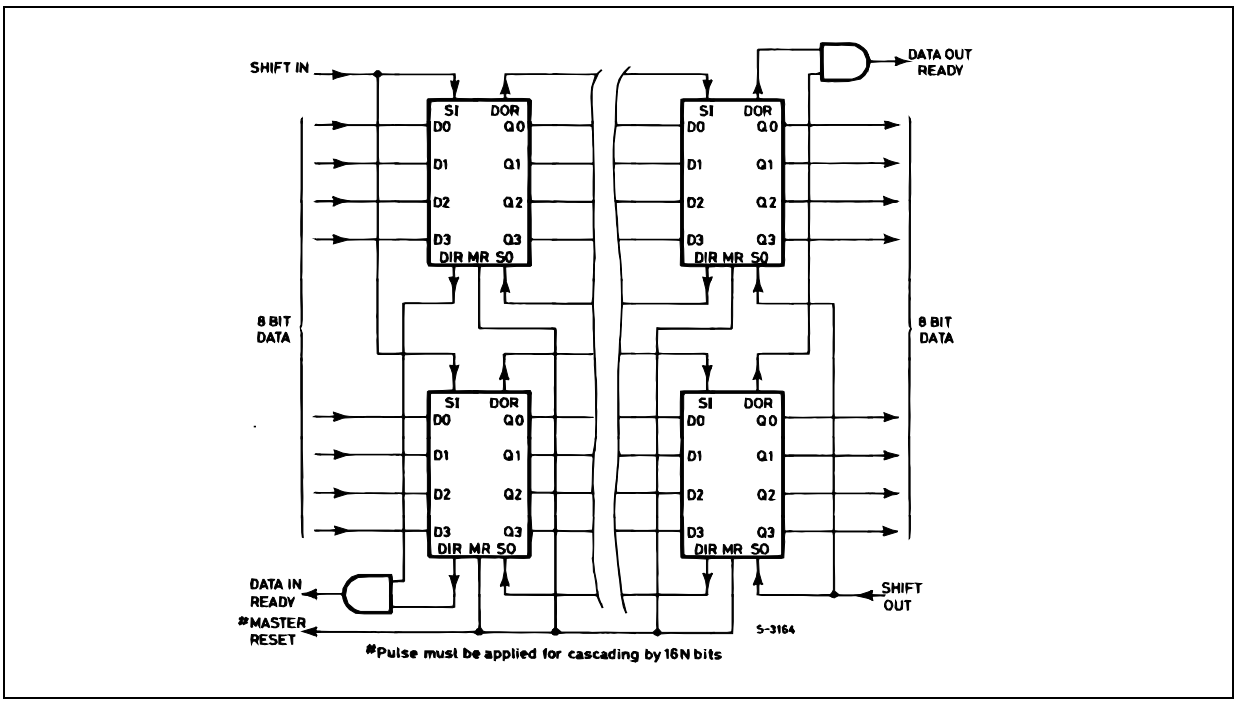
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{WL}	Data-out Ready Pulse Width	5			220	440	ns
		10			90	180	
		15			665	130	
t_{WH}	Master Reset Pulse Width	5		200	100		ns
		10		90	45		
		15		60	30		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TYPICAL APPLICATION: EXPANSION, 4 BIT-WIDE-BY-16 N-BITS LONG.



TYPICAL APPLICATION: EXPANSION, 8 BITS-WIDE-BY-16 N-BITS LONG.



APPLICATION INFORMATION

LOADING DATA

Data can be entered whenever the DATA-IN READY (DIR) flag is high by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily until the data has been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

UNLOADING DATA

As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic "0". This level change causes the first word to be shifted out (unloaded) immediately and the data to be lost.

CASCADING

HCF40105B can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4-bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions.

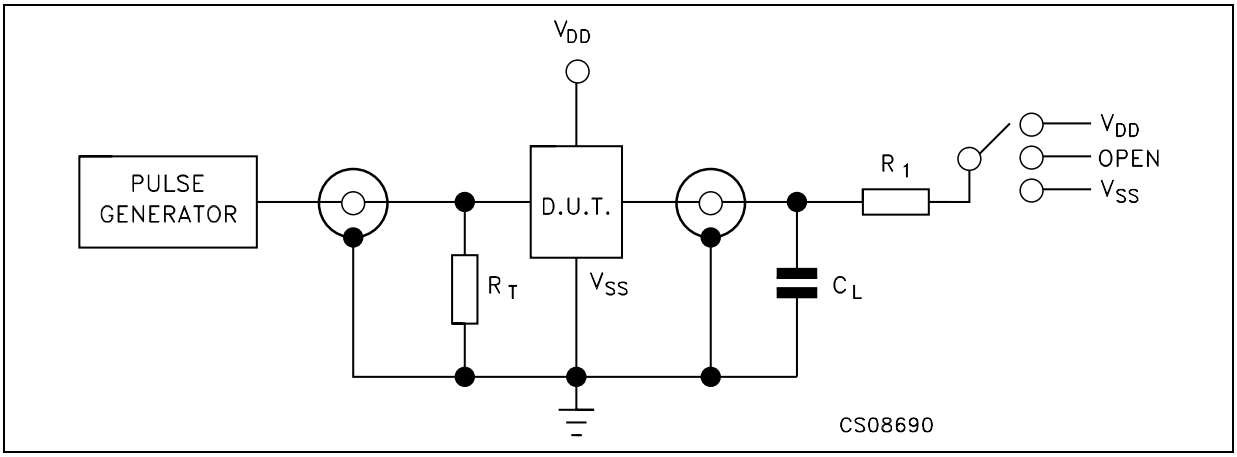
3-STATE OUTPUTS

In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

MASTER RESET

A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register do not change, only declared invalid, and will be superseded when the first word is loaded.

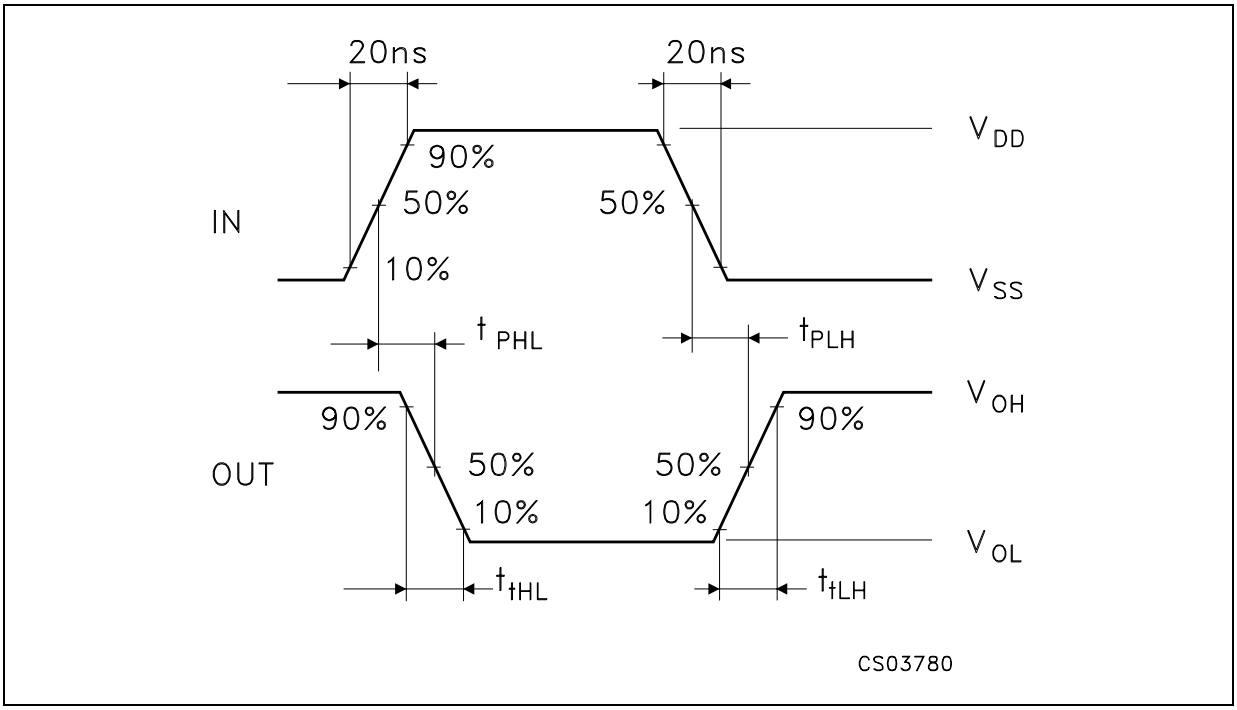
TEST CIRCUIT



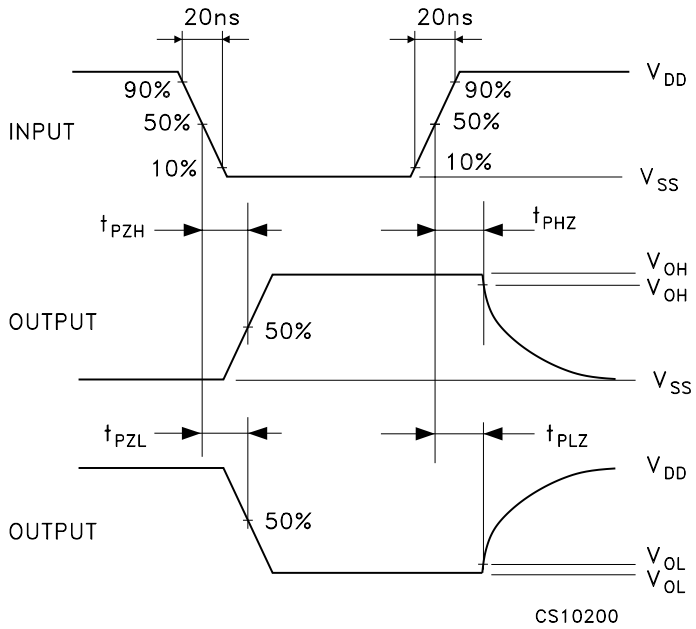
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{DD}
t_{PZH}, t_{PHZ}	V_{SS}

C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

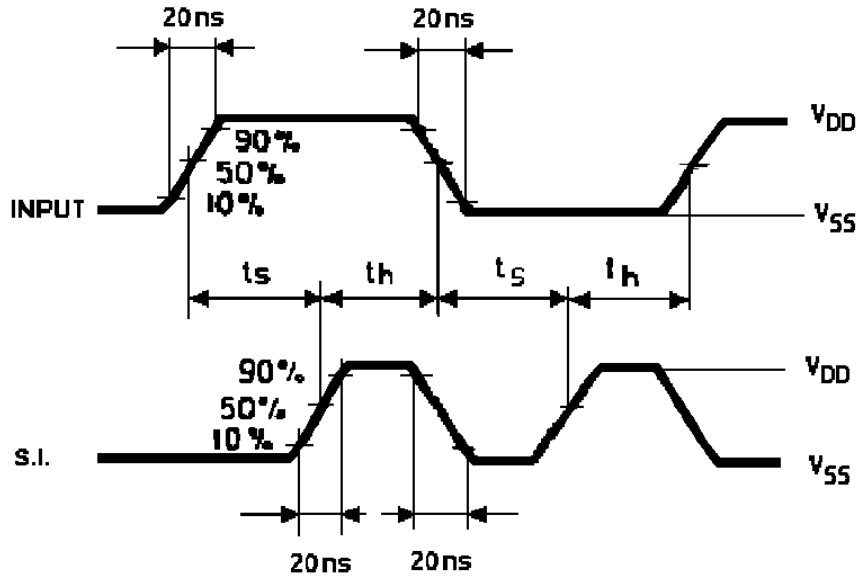
WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

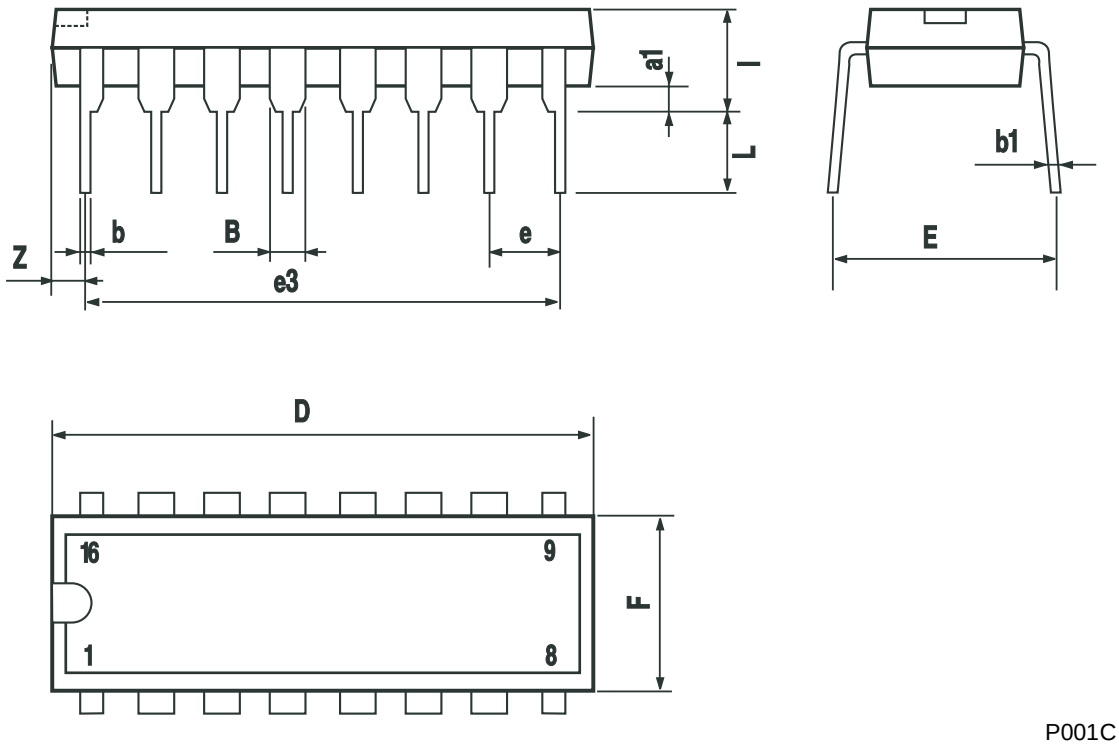


WAVEFORM 3 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



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