3.3V Zero-Delay Buffer

General Features

- Zero input - output propagation delay, adjustable by capacitive load on FBK input.
- Zero input - output propagation delay, adjustable by capacitive load on FBK input.
- Multiple configurations - Refer “ASM5P2308A Configurations Table”.
- Input frequency range: 10MHz to 133MHz
- Multiple low-skew outputs.
  - Output-output skew less than 200 ps.
  - Device-device skew less than 700 ps.
  - Two banks of four outputs, three-stateable by two select inputs.
- Less than 200 ps cycle-to-cycle jitter (-1, -1H, -4, -5H).
- Available in 16-pin SOIC and TSSOP packages.
- 3.3V operation.
- Advanced 0.35µ CMOS technology.
- Industrial temperature available.

Functional Description

ASM5P2308A is a versatile, 3.3V zero-delay buffer designed to distribute high-speed clocks. It is available in a 16-pin package. The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input-to-input propagation delay is guaranteed to be less than 350ps, and the output-to-output skew is guaranteed to be less than 250ps.

The ASM5P2308A has two banks of four outputs each, which can be controlled by the select inputs as shown in the Select Input Decoding Table. If all the output clocks are not required, Bank B can be three-stated. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

Multiple ASM5P2308A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700ps.

The ASM5P2308A is available in five different configurations (Refer “ASM5P2308A Configurations Table). The ASM5P2308A-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The ASM5P2308A-1H is the high-drive version of the -1 and the rise and fall times on this device are much faster.

The ASM5P2308A-2 allows the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. The ASM5P2308A-3 allows the user to obtain 4X and 2X frequencies on the outputs.

The ASM5P2308A-4 enables the user to obtain 2X clocks on all outputs. Thus, the part is extremely versatile, and can be used in a variety of applications.

The ASM5P2308A-5H is a high-drive version with REF/2 on both banks.

PRELIMINARY

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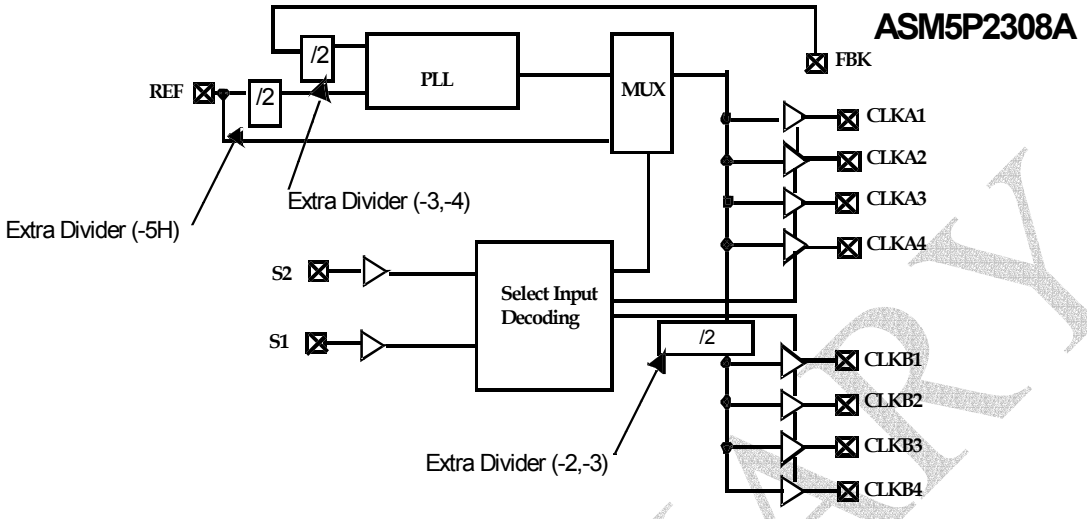
Block Diagram



Select Input Decoding for ASM5P2308A

S2	S1	Clock A1 - A4	Clock B1 - B4	Output Source	PLL Shut-Down
0	0	Three-state	Three-state	PLL	Y
0	1	Driven	Three-state	PLL	N
1	0	Driven[1]	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

ASM5P2308A Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
ASM5P2308A-1	Bank A or Bank B	Reference	Reference
ASM5P2308A-1H	Bank A or Bank B	Reference	Reference
ASM5P2308A-2	Bank A	Reference	Reference /2
ASM5P2308A-2	Bank B	2 X Reference	Reference
ASM5P2308A-3	Bank A	2 X Reference	Reference or Reference[2]
ASM5P2308A-3	Bank B	4 X Reference	2 X Reference
ASM5P2308A-4	Bank A or Bank B	2 X Reference	2 X Reference
ASM5P2308A-5H	Bank A or Bank B	Reference /2	Reference /2

Note:

1. Outputs inverted on 2308-2 and 2308-3 in bypass mode, S2 = 1 and S1 = 0.

2. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the ASM5P2308A-2.

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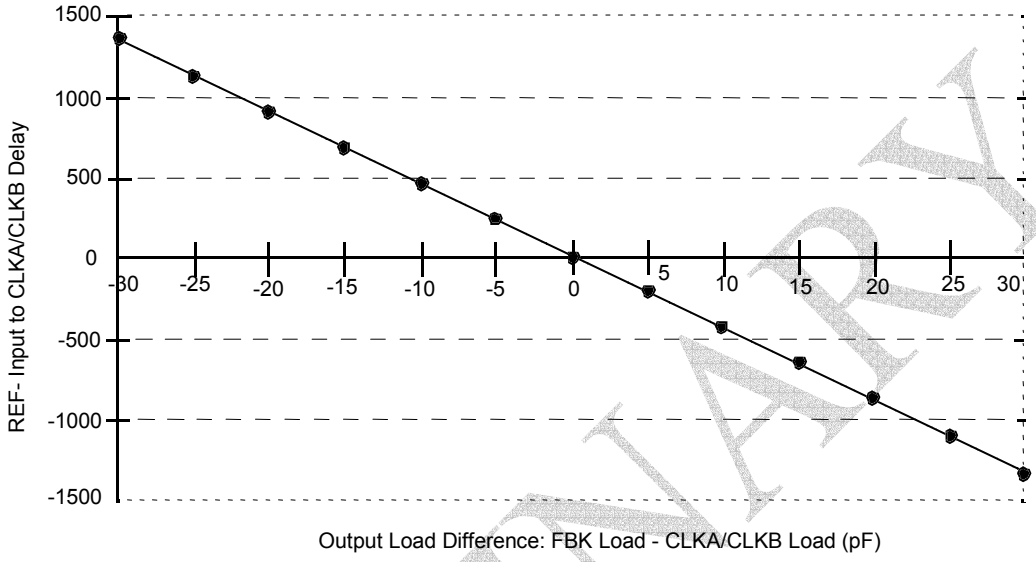
Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output.



To close the feedback loop of the ASM5P2308A, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output-output skew, be sure to load outputs equally.

PRELIMINARY

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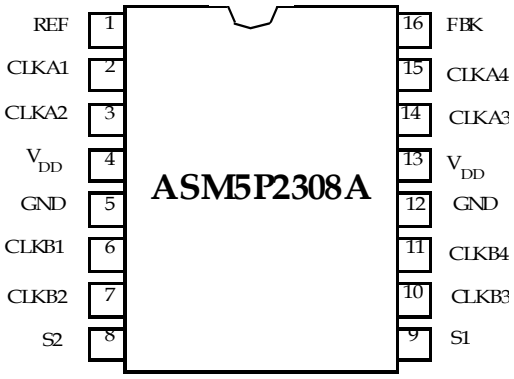
Pin Configuration



Pin Description for ASM5P2308A

Pin #	Pin Name	Description
1	REF[3]	Input reference frequency, 5V tolerant input
2	CLKA1[4]	Buffered clock output, bank A
3	CLKA2[4]	Buffered clock output, bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[4]	Buffered clock output, bank B
7	CLKB2 [4]	Buffered clock output, bank B
8	S2 [5]	Select input, bit 2
9	S1 [5]	Select input, bit 1
10	CLKB3 [4]	Buffered clock output, bank B
11	CLKB4 [4]	Buffered clock output, bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3 [4]	Buffered clock output, bank A
15	CLKA4 [4]	Buffered clock output, bank A
16	FBK	PLL feedback input

Notes:

3. Weak pull-down.

4. Weak pull-down on all outputs.

5. Weak pull-up on these inputs.

PRELIMINARY

Notice: The information in this document is subject to change without notice.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	VDD + 0.5	V
DC Input Voltage (REF)	-0.5	7	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		>2000	V
Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.			

Operating Conditions for ASM5P2308A Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance[6]		7	pF

Note:

6. Applies to both Ref Clock and FBK.

Electrical Characteristics for ASM5P2308A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage [7]	I_{OL} = 8mA (-1, -2, -3, -4) I_{OH} = 12mA (-1H, -5H)		0.4	V
V_{OH}	Output HIGH Voltage [7]	I_{OL} = -8mA (-1, -2, -3, -4) I_{OH} = -12mA (-1H, -5H)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100MHz REF		TBD	mA
		Select inputs at V_{DD} or GND		TBD	
		Unloaded outputs, 66MHz REF (-1, -2, -3, -4)		TBD	
		Unloaded outputs, 33MHz REF (-1, -2, -3, -4)		TBD	

Note:

7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Notice: The information in this document is subject to change without notice.

Switching Characteristics for ASM5P2308A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	20-pF load, -1H, -5H devices [8]	10		133.3	MHz
t_1	Output Frequency	15-pF load, -1, -2, -3, -4 devices	10		133.3	MHz
	Duty Cycle [7]= (t_2 / t_1) * 100 (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT} = <66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle [7] = (t_2 / t_1) * 100 (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT} = <50 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 30-pF load			2.20	ns
t_3	Output Rise Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_3	Output Rise Time [7] (-1H, -5H)	Measured between 0.8V and 2.0V 30-pF load			1.50	ns
t_4	Output Fall Time [7] (-1, -2, -3, -4)	Measured between 2.0V and 0.8V 30-pF load			2.20	ns
t_4	Output Fall Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_4	Output Fall Time [7] (-1H, -5H)	Measured between 2.0V and 0.8V 30-pF load			1.25	ns
t_5	Output-to-output skew on same bank (-1, -2, -3, -4) [7]	All outputs equally loaded			200	ps
	Output-to-output skew (-1H, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -4, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-2, -3)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [6]	Measured at V_{DD} /2		0	±250	ps
t_7	Device-to-Device Skew [7]	Measured at V_{DD}/2 on the FBK pins of the device		0	700	ps
t_J	Cycle-to-cycle jitter [7] (-1, -1H, -4, -5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [7] (-2, -3)	Measured at 66.67 MHz, loaded outputs, 30pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load			400	
t_{LOCK}	PLL Lock Time [7]	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

PRELIMINARY

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Switching Characteristics for ASM5I2308A - Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	20-pF load, -1H, -5H devices [8]	10		133.3	MHz
t_1	Output Frequency	15-pF load, -1, -2, -3, -4 devices	10		133.3	MHz
	Duty Cycle [7] = (t_2 / t_1) * 100 (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT} = <66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle [7]= (t_2 / t_1) * 100 (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT} = <50 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 30-pF load			2.50	ns
t_3	Output Rise Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_3	Output Rise Time [7] (-1H, -5H)	Measured between 0.8V and 2.0V 30-pF load			1.50	ns
t_4	Output Fall Time [7] (-1, -2, -3, -4)	Measured between 2.0V and 0.8V 30-pF load			2.50	ns
t_4	Output Fall Time [7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_4	Output Fall Time [7] (-1H, -5H)	Measured between 2.0V and 0.8V 30-pF load			1.25	ns
t_5	Output-to-output skew on same bank (-1, -2, -3, -4) [7]	All outputs equally loaded			200	ps
	Output-to-output skew (-1H, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -4, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-2, -3)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [7]	Measured at V_{DD} /2		0	±250	ps
t_7	Device-to-Device Skew [7]	Measured at V_{DD}/2 on the FBK pins of the device		0	700	ps
t_J	Cycle-to-cycle jitter [7] (-1, -1H, -4, -5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [7] (-2, -3)	Measured at 66.67 MHz, loaded outputs, 30pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load			400	
t_{LOCK}	PLL Lock Time [7]	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

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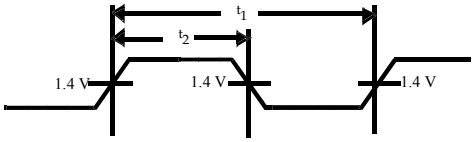
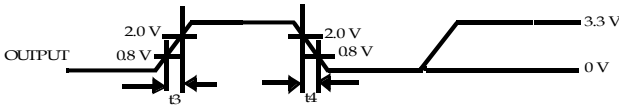
Switching Waveforms

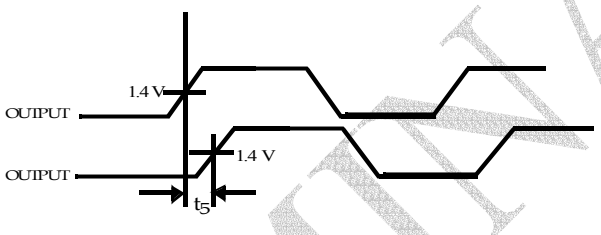
Duty Cycle Timing



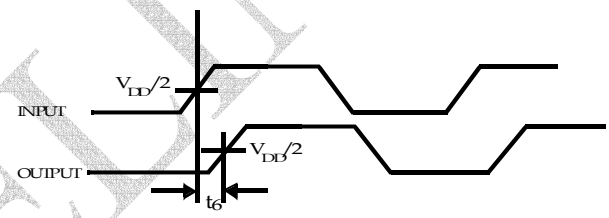
All Outputs Rise/Fall Time



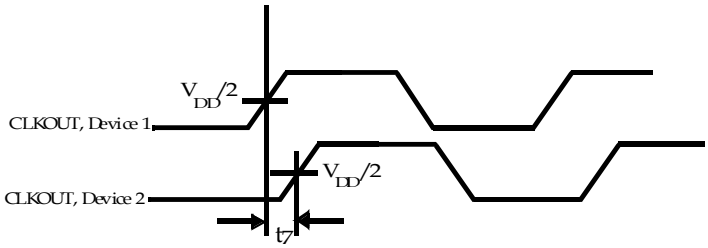
Output - Output Skew



Input - Output Propagation Delay



Device - Device Skew



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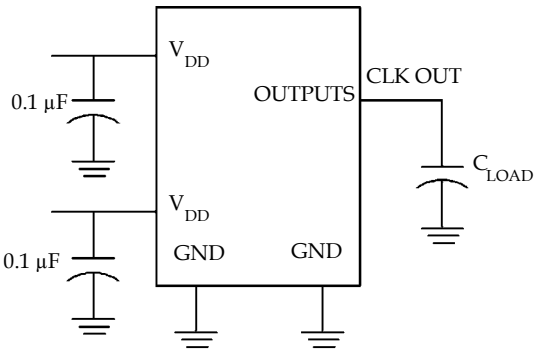
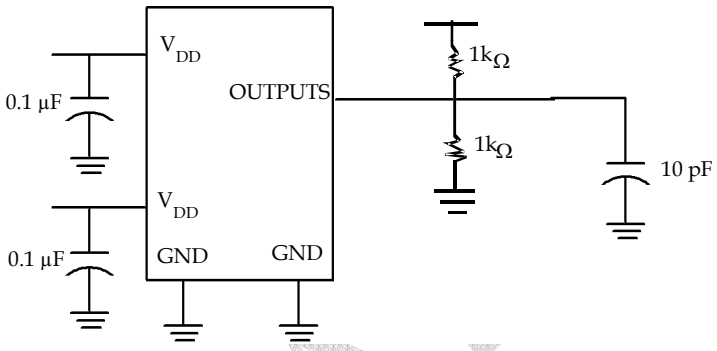
Test Circuits

Test Circuit #1



Test Circuit #2



For parameter t_8 (output slew rate) on -1H devices

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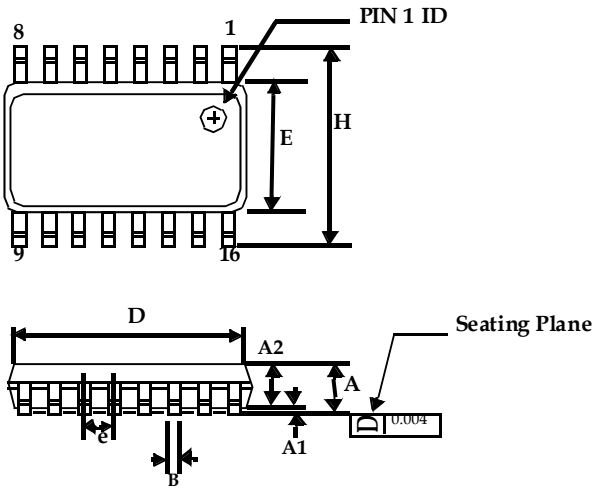
Package Information: 16-lead (150 Mil) Molded SOIC



Symbol	Dimensions (inches)		Dimensions (millimeters)	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
θ	0°	8°	0°	8°

PRELIMINARY

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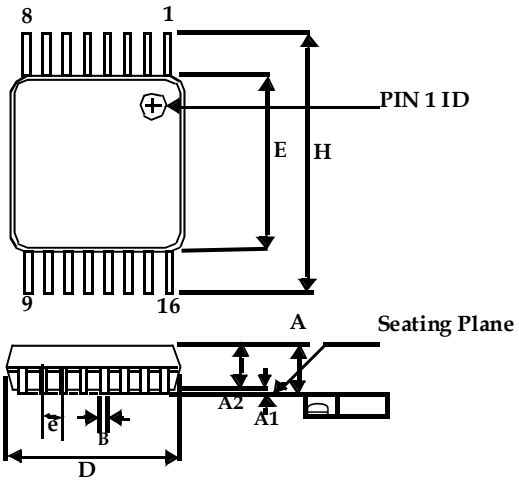
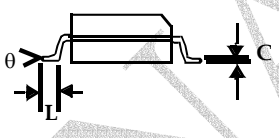
Package Information: 16-lead Thin Shrunk Small Outline Package (4.40-MM Body)





Symbol	Dimensions (inches)		Dimensions (mm)	
	MIN	MAX	MIN	MAX
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.003	0.37	0.85	0.95
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	2.008	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.246	0.256	6.25	6.50
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

PRELIMINARY

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Ordering Codes

Ordering Code	Package Type	Operating Range
ASM5P2308A-1-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-1-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-1-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-1-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-1-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-1-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-1-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-1-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial
ASM5P2308A-1H-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-1H-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-1H-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-1H-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-1H-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-1H-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-1H-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-1H-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial
ASM5P2308A-2-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-2-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-2-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-2-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-2-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-2-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-2-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-2-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial
ASM5P2308A-3-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-3-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-3-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-3-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-3-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-3-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-3-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-3-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial

PRELIMINARY

Notice: The information in this document is subject to change without notice.

Ordering Codes (contd)

Ordering Code	Package Type	Operating Range
ASM5P2308A-4-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-4-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-4-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-4-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-4-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-4-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-4-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-4-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial
ASM5P2308A-5H-16-ST	16-pin 150-mil SOIC-TUBE	Commercial
ASM5I2308A-5H-16-ST	16-pin 150-mil SOIC- TUBE	Industrial
ASM5P2308A-5H-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5I2308A-5H-16-SR	16-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5P2308A-5H-16-TT	16-PIN 150-mil TSSOP - TUBE	Commercial
ASM5I2308A-5H-16-TT	16-PIN 150-mil TSSOP - TUBE	Industrial
ASM5P2308A-5H-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Commercial
ASM5I2308A-5H-16-TR	16-PIN 150-mil TSSOP - TAPE & REEL	Industrial

PRELIMINARY

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

Notice: The information in this document is subject to change without notice.

PRELIMINARY

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Preliminary Information
Part Number: ASM5P2308A
Document Version: v1.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Dan Hariton / Alliance Semiconductor, dated 11-11-2003

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