PM5315

SPECTRA-2488

SPECTRA-2488 WITH TBS QUAD OC-12 LINE CARD

REFERENCE DESIGN

RELEASED

ISSUE 2: MARCH 2001

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	June 2000	Document created.
2	March 2001	Document revised to reflect changes made to schematic for revision of reference design. The following changes were made to the schematic: • LEDs 4, 5, and 6 on page 17 no longer connect to the CPLD (U7). These LEDS now connect to test points. The circuitry associated with pins 23 and 24 of the Triquint TQ8106s devices has been modified to include a 1N4148 diode, 1.5K resistor, and a 2.0 K resistor. These components are necessary to prevent the CDR PLL in TQ8106 from locking up. • Updated configuration register description • Added manufactures to BOM • Updated figures 1,2, and 7 • Updated CPLD Block Diagram

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1 DEFINITIONS

ADM	Add Drop Multiplexer
SERDES	Serializer/Deserializer
CHESS	Channelizer Engine for SONET/SDH
CPLD	Complex Programmable Logic Device
LVDS	Low Voltage Differential Signals
RWSEL	Read Working Link Select
xCMP	Grouped Connection Memory Page signals

2 FEATURES

- Provides four OC-12 rate 622.08 Mbits/s SONET/SDH physical layer channels.
- On the system side, provides four working 777.76 Mbps LVDS serial telecombus (STCB) links, four protect 777.76 Mbps LVDS STCB links, and four auxiliary 777.76 Mbps LVDS STCB links.
- System side interface connects through TBS Serializer device to SONET/SDH cross connect devices (eg. TSE).
- External system timing sources for multiple line-card applications, or local timing generation for stand-alone evaluation.
- Transmit line side timing can use either on board 77.76 MHz clock as reference or recovered clock as reference (Loop-Timing)
- System and line side loopback modes for diagnostics.
- CompactPCI interface allows the user to control and monitor the SPECTRA-2488 and on board CPLD.

3 APPLICATIONS

- SONET/SDH Multiservice ADMs
- SONET/SDH Cross Connects
- SONET/SDH Terminal Multiplexers

4 REFERENCES

- Bell Communications Research - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2 Revision 2, January 1999.
- Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996.
- IEEE – P1596.3 “Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)”, November 1995
- PLX Technology PCI9054 PCI Bridge Device, Data Sheet, Issue 1, January, 1999.
- PMC-1990821, PM5315 SPECTRA-2488 SONET/SDH Payload Extractor/Aligner Data Sheet, Issue 2, June, 2000.
- PMC-1991257, PM5310 Telecombus Serializer Data Sheet, Issue 4, September, 2000.
- PCI Industrial Computers Manufacturers Group (PICMG), “CompactPCI Specification 2.0 R 2.1”, Wakefield MA, September 1997.
- TriQuint Seminconductor, Inc., TQ8106 SONET/SDH Transceiver Data Sheet, Revision 0.3.A, July 1998.
- PMC-2000299, “777.6 MHz LVDS Serial Telecombus Design Considerations”, Issue 1, March 2000
- PMC-1991797, CHESS Users Guide, Issue 2, May 2000.
- PMC-2000021,CHESS Reference Design Hardware Manual, Issue 1, Dec 2000

5 APPLICATION EXAMPLES

The following example () demonstrates an implementation of a small North-South (STS-12 x 4) Add/Drop Multiplexer, using the SPECTRA-2488 With TBS Quad OC-12 Line Card and the S/UNI MACH48 Card (PMC-2000207). Aside from the serializing and backplane driving functions, the TBS can provide STS-1 switching and with use of its auxiliary port, drop/ add traffic to the S/UNI-MACH48 where ATM/POS processing can be done.

Figure 1 - Add/Drop MUX With SPECTRA-2488, TBS and S/UNI MACH48.

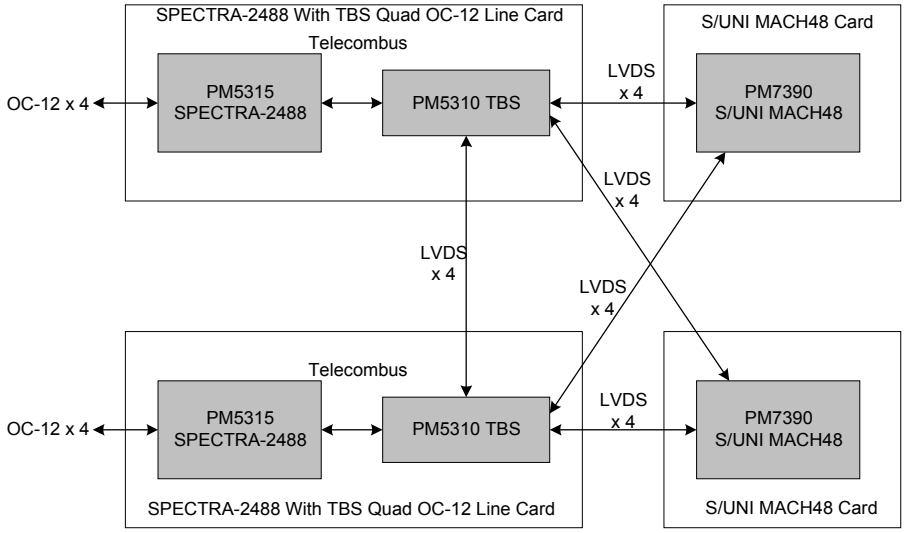
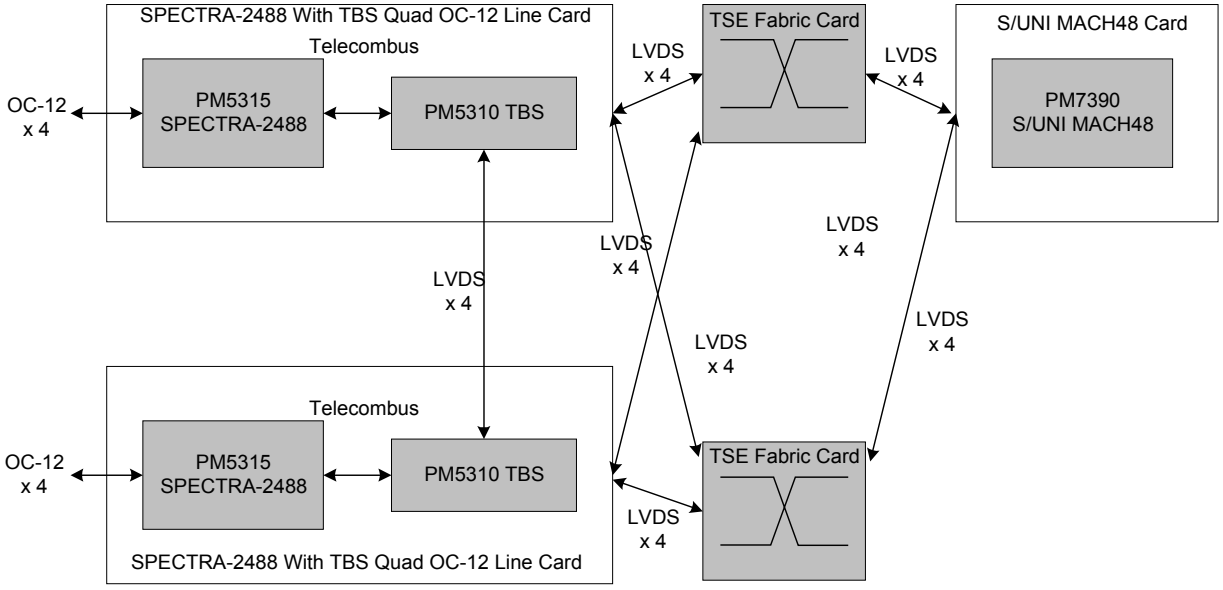


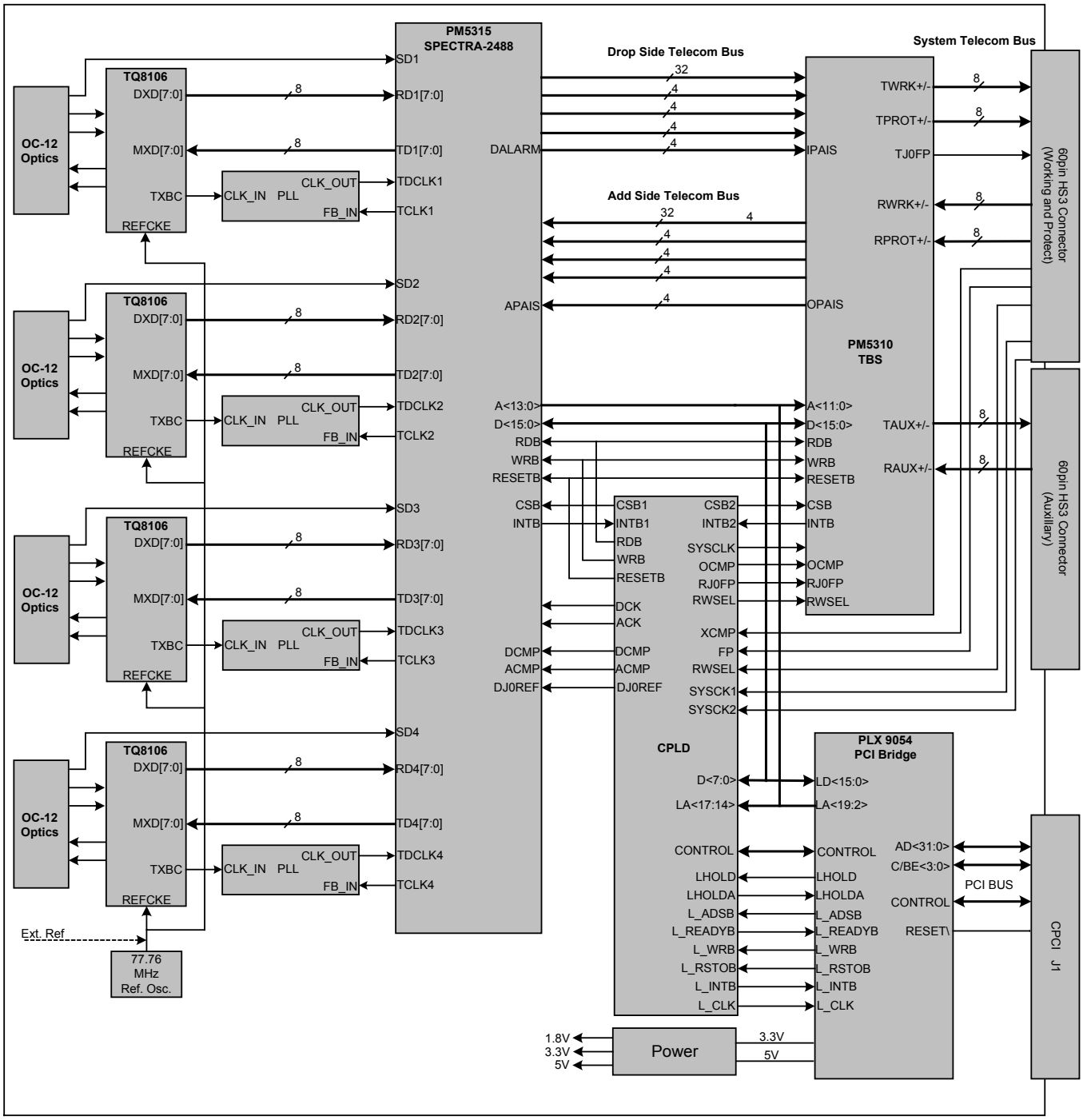
Figure 3 below shows an example of a multiservice Add/Drop Multiplexer (ADM). The SPECTRA-2488 With TBS Quad OC-12 Line Cards provide line-side interface to the SONET OC-12 x 4 traffic. The TSE Fabric Cards (PMC-1991247) route the different traffic types the SONET line may contain such as POS, voice, or video, to the appropriate service cards. In this way, the TSE decouples line-side PHY devices of SONET rings from multi-service system cards.

Figure 3 - Multiservice STS 12 x 4 ADM With TSE



6 BLOCK DIAGRAM

Figure 4 - SPECTRA-2488 With TBS Quad OC-12 Block Diagram



7 FUNCTIONAL DESCRIPTION

The QUAD OC-12 Reference Design receives 622Mbps serial data via the Siemens V23826-H18-C363 622 Mbps single mode fiber optic transceivers. Each incoming STS-12 data signal is fed into a TQ8106 Serdes, which recovers clock and data and outputs the data in parallel (8 bit byte serial) format at 77.76MHz to the SPECTRA-2488. The SPECTRA-2488 terminates the transport and path overhead of each of the incoming STS-12 streams. The STS-12 frames are transmitted to the system side via four 8 bit byte serial Telecombus interfaces operating at 77.76MHz.

The byte serial Telecombus interface connects seamlessly to the TBS device which takes the four input 77.76MHz byte serial data streams and serializes them for output onto the system backplane. The system side data stream is 8B/10B encoded LVDS at 777.6MHz.

Frames received at the system side are processed similarly (but in reverse) and are output on the line side OC-12 channels at 622Mbps.

7.1 PM5315 SPECTRA-2488

The PM5315 SONET/SDH PAYLOAD EXTRACTOR ALIGNER (SPECTRA-2488) is capable of terminating the transport and path overhead of a single STS-48 (STM-16/AU4-4c/AU4/AU3/TU3), a single STS-48c (STM-16/AU4-16c), a quad STS-12 (STM-4/ AU4/AU3/TU3) or a quad STS-12c (STM-4-4c) data stream at 2488 Mbit/sec. The SPECTRA-2488 implements significant functions for a SONET/SDH compliant line interface.

For this reference design, the SPECTRA-2488 is operating in quad STS-12/STM-4 mode. The device transmits four independent OC-12 SONET/SDH frames via four 8 bit serial interfaces at 77.76MHz. The SPECTRA-2488 formats the SONET section, line and path or the SDH regenerator section, multiplexer section, and high order path overhead. It performs framing pattern insertion (A1, A2), scrambling, section and line alarm insertion, and section and line BIPs (B1, B2) calculation as required to allow performance monitoring at the far end. Line remote error indicators (M1) are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the SPECTRA-2488 generates the transmit payload pointers (H1, H2), creates and inserts the path BIPs (B3), optionally inserts a 16 or 64 byte path trace message (J1), and optionally inserts the path status byte (G1). As well as basic processing of the transmit SONET/SDH overhead, the SPECTRA-2488 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing

additional external sourcing of overhead, if desired. The SPE is inserted from the 32 bit Telecom ADD bus operating at 77.76MHz.

The SPECTRA-2488 receives SONET/SDH frames via four 8 bit serial interfaces at 77.76MHz. The device terminates the SONET section, line and path or the SDH regenerator section, multiplexer section and line alarm conditions, and monitors section and line BIPs (B1, B2), accumulating error counts at each level for performance monitoring. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-2488 interprets the received payload, monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result and extracts the SPE. The SPE is made available on the 32 bit Telecom DROP bus operating at 77.76MHz.

The SPECTRA-2488 is implemented in low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital I/O. It is packaged in a 520 pin SBGA.

7.2 PM5310 TBS

The TBS implements conversion between byte-serial parallel Telecombus and bit serial 8B/10B encoded serial Telecombus formats. The TBS can be used to connect SONET/SDH framer devices (e.g. PM5315 SPECTRA-2488) to ATM/POS processors (PM7390 S/UNI MACH48) or to SONET/SDH cross-connects (PM5372 TSE). It can also be used to connect SONET/SDH tributary unit processors (PM5363 TUPP+622) to PDH mapper devices (PM8315 TEMUX).

On the ingress side, the TBS converts an incoming parallel Telecombus stream to a set of three serial LVDS Telecombus links (3 sets of 4 links called working, protect and auxiliary). Most users will use one of the three ports as the main port for grooming to the TSE switch fabric or connecting to a layer 2 processing card. The second port may be used for connecting to a redundant fabric or layer 2 processing card. The incoming parallel streams can carry a single STS-48/STM-16 stream or four STS-12/STM-4 streams that share a common clock. Incoming data is encoded into an extended set of 8B/10B characters and transferred onto three independent sets of 777.6Mbps LVDS serial links. Transport and payload frame boundaries, pointer justification events and alarm conditions are marked by 8B/10B control characters. A pseudo random bit sequence (PRBS) generator is provided to monitor the incoming payload for the $X^{23}+X^{18}+1$ pattern. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the incoming Telecombus stream. A time-slot interchange block is provided to allow arbitrary mapping of streams on the incoming parallel Telecombus to each of the three sets of LVDS serial Telecombus links at STS-1/AU-3 granularity. Multi-cast is also supported.

In the egress direction, the TBS connects three independent sets of four 777.6 Mbps serial LVDS Telecombus links to an outgoing parallel Telecombus stream. Each link contains a constituent STS-12/STM-4 of an STS-48/STM-16 stream. Bytes on the links are carried as 8B/10B characters. The TBS decodes the characters into Telecombus data and control signals. A PRBS processor is provided to monitor the decoded payload for the $X^{23}+X^{18}+1$ pattern. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the LVDS links.

The TBS is implemented in low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital I/O. It is packaged in a 352 pin UBGA.

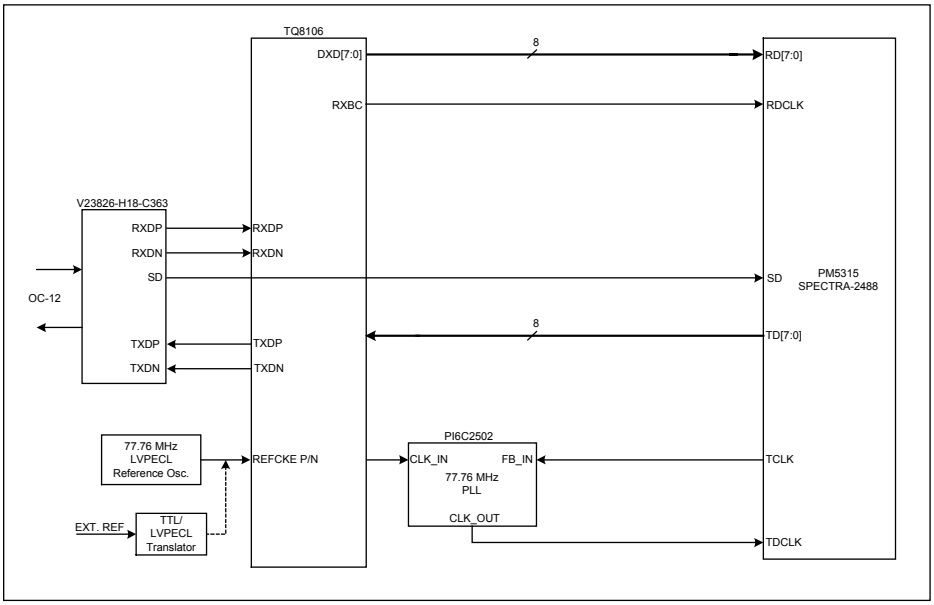
7.3 Serial LVDS Telecombus Interface

The Telecombus interface on the SPECTRA-2488 With TBS OC-48 Reference Design Card supports four STS-12/STM-4 serial 777.6 Mbps LVDS links (8B/10B encoded). The Telecom bus signals comprise the majority of the signals on the system interface connector. The complete connector pinout is shown below in Table 9 and Table 9.

7.4 Quad 622 Mbps Line Interface

Figure 5 below outlines the functionality of the Quad 622 Mbps Serial Line Interface on the SPECTRA-2488 with TBS Quad OC-12 Line Card.

Figure 5 - 622 Mbs Line Interface



The TQ8106 Transceiver performs serialization, deserialization and clock and data recovery for a single OC-12 channel. The device takes a single serial STS-12 PECL input stream, recovers clock and data and outputs it on an 8 bit byte serial bus. In the transmit direction, the TQ8106 takes incoming byte serial data at 77.76MHz and bit serializes it for transmission over optical fiber at 622.08 MBps.

Parallel data from the TQ8106 SERDES is clocked out of the device on the falling edge of the recovered clock, RXBC. The SPECTRA-2488 will use the rising edge of RXBC to clock the data in. See Figure 6 for timing diagrams and Table 1 and Table 2 for timing parameters.

Figure 6 - TQ8106 to SPECTRA-2488 Rx Input Timing Diagram

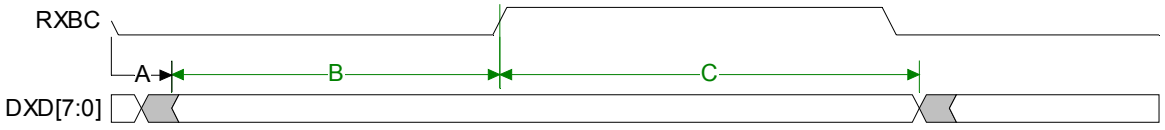


Table 1: TQ8106 to SPECTRA-2488 Rx Input Timing

	Description	Min	Max	Units
A	RXBC falling edge to DXD[7:0] valid	500	1000	ps
B	DXD[7:0] Set-up time to RXBC rising edge	5.43	5.93	ns
C	DXD[7:0] Hold time to RXBC rising edge	6.93	7.43	ns

Table 2: SPECTRA-2488 Rx Input Timing Specs.

Description	Min	Max	Units
RD1-4$_{[7:0]}$ Set-up time to RDCLK1-4 rising edge	2		ns
RD1-4$_{[7:0]}$ Hold time to RDCLK1-4 rising edge	0		ns

The outgoing parallel data from the SPECTRA-2488 is clocked out of the device on the rising edge of TCLK and clocked into the TQ8106 using the rising edge of TXBC + 270 degrees. The delay between the TDCLK input of the SPECTRA and the TCLK output of the SPETCRA is not specified and therefore the

relationship between the SPECTRA TX data TD[7:0] and the TQ8106 TX input clock TXBC would unknown. The 77.76 MHz PLL ensures that TCLK and TXBC are in phase. With the TXBC now phase locked to the TXLCK the timing between the TXBC and the SPECTRA TX data can be determined. See Figure 7 for timing diagram and Table 3 and Table 4 for timing parameters.

Figure 7 - SPECTRA-2488 to TQ8106 TX Input Timing Diagram

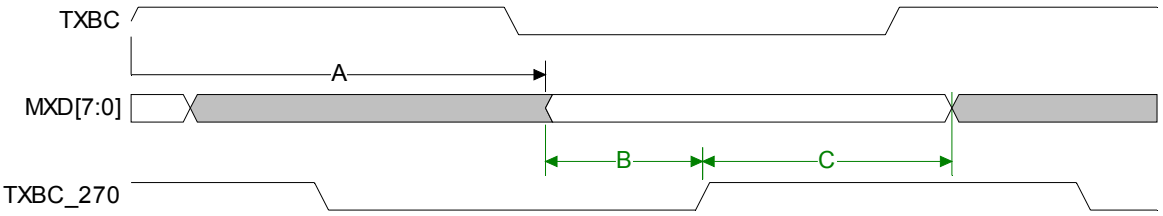


Table 3: SPECTRA-2488 to TQ8106 Tx Input Timing

	Description	Min	Max	Units
A	TXBC rising edge to MXD[7:0] valid	1	7	ns
B	MXD[7:0] Set-up time to TXBC rising edge	2.65	8.65	ns
C	MXD[7:0] Hold time to TXBC rising edge	4.21	10.21	ns

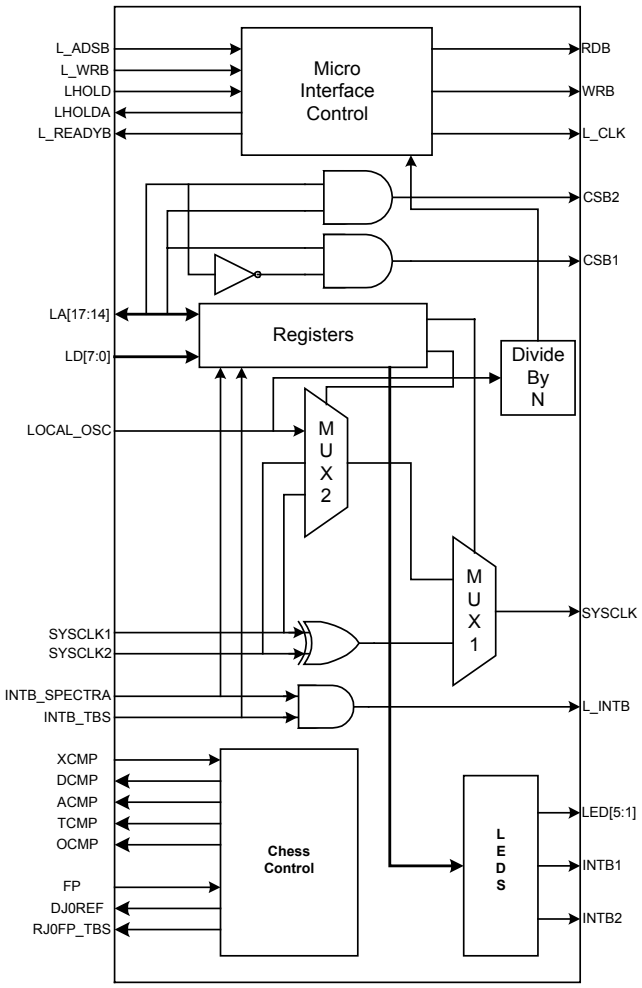
Table 4: TQ8106 TX Input Timing Specs.

Description	Min	Max	Units
MXD[7:0] Set-up time to TXBC rising edge	600	-	ps
MXD[7:0] Hold time to TXBC rising edge	600	-	ps

7.5 CPLD

The main function of the CPLD is to implement the glue logic and address decoding for interfacing the cPCI bus to the SPECTRA-2488 and TBS devices. Additionally, the 77.76MHz system clocks distributed via the backplane are buffered and output to the Telecombus clocks on the SPECTRA-2488 and to the SYSCLK input on the TBS. Overhead signals from the SPECTRA-2488 device have been routed to the CPLD for future design considerations. R/W registers have been included in the CPLD for TBS and SPECTRA interrupt status as well as 77.76 MHz system clock control.

Figure 8 - CPLD Functional Block Diagram



7.5.1 cPCI Interface

The interface to the cPCI interface chip can be summarized as follows: added signaling (LHOLD, LHOLDA#, ADS#, READY#) not support by the microprocessor interface and decoding for interface signals (RDB, WRB and CSB). Timing for the signals to the SPECTRA-2488 and TBS devices are achieved using counts of SYSCLK.

7.5.1.1 Address Space Allocation of Card

The LA<32:2> address space is allocated according to Table 5.

Table 5: Address Bit Allocation

LA<32:2> bits	Offset	Function
14:2	0x0000	SPECTRA-2488 Normal Registers
15:2	0x0000	SPECTRA-2488 Test Registers
12:2	0x4000	TBS Normal Registers
13:2	0x4000	TBS Test Registers
17:16	0x8000	CPLD Configuration Register
32:18		Unused bits

7.5.2 Configuration and Status Registers

The CPLD provides a register for control of system clock MUX1, MUX2, and interrupt status register. ALL registers are R/W registers.

CPLD Configuration Register 0x00: CONFIG_REG (LA[17:16]=10)

Bit	Type	Function	Default
Bit 7	R/W	unused	0
Bit 6	R/W	LED_3	0
Bit 5	R/W	Fpenable	0
Bit 4	R/W	MUX2[1]	0
Bit 3	R/W	MUX2[0]	0

Bit 2	R/W	MUX1	0
Bit 1	R/W	LBM[1]	0
Bit 0	R/W	LBM[0]	0

LBM[1:0]

The LBM[1:0] bits select the loop-back modes for the TQ8106 device as show below in Table 6:

Table 6: TQ8106 Loop-back Modes

LBM[1:0]	System clock
00	Loopback
01	Normal
10	Equipment
11	Facility

MUX1

The MUX1 bit controls the CPLD MUX1. This bit selects the source for the 77.76Mhz system clock. When MUX1=0 the output of MUX2 is selected. When MUX1=1 the logical XOR of SYSCLK1 and SYSCLK2 is selected. See Table 7.

MUX2[1:0]

The MUX2[1:0] bits control the CPLD MUX2. These bits combine with MUX1 select the source for the 77.76 MHz system clock. When MUX2[1:0]=00 or 11 the output of MUX2 is the 77.76 MHz clock from the on board oscillator. When MUX2[1:0]=01 the output of MUX2 is SYSCLK1 from backplane, and when MUX2[1:0]=10 the output of MUX2 is SYSCLK2 from the backplane. See Table 7.

Table 7: System Clock Truth Table

MUX1	MUX[1:0]	System clock
0	00	On board oscillator
0	01	SYSCLK1
0	10	SYSCLK2
0	11	On board oscillator
1	XX	SYSCLK1 xor SYSCLK2

CPLD Configuration Register 0x01: CMP_REG (LA[17:16]=11)

Bit	Type	Function	Default
Bit 7	R/W	OCMP selection	0
Bit 6	R/W	PGMOCMP	0
Bit 5	R/W	TCMP selection	0
Bit 4	R/W	PGMTCMP	0
Bit 3	R/W	ACMP selection	0
Bit 2	R/W	PGMACMP	0
Bit 1	R/W	DCMP selection	0
Bit 0	R/W	PGMDCMP	0

PGMDCMP:

The PGMDCMP bit is the alternative programmable source for the DCMP signal.

DCMP Selection:

DCMP_SEL determines the source of the DCMP signal. When DCMP_SEL = ‘0’, the XCMP signal is the source, otherwise, PGMDCMP is the source.

PGMACMP:

The PGMACMP bit is the alternative programmable source for the ACMP signal.

ACMP Selection:

ACMP_SEL determines the source of the ACMP signal. When ACMP_SEL = ‘0’, the XCMP signal is the source, otherwise, PGMACMP is the source.

PGMTCMP:

The PGMTCMP bit is the alternative programmable source for the TCMP signal.

TCMP Selection:

TCMP_SEL determines the source of the TCMP signal. When TCMP_SEL = ‘0’, the XCMP signal is the source, otherwise, PGMTCMP is the source.

PGMTCMP:

The PGMTCMP bit is the alternative programmable source for the TCMP signal.

OCMP Selection:

OCMP_SEL determines the source of the OCMP signal. When OCMP_SEL = '0', the XCMP signal is the source, otherwise, PGMOCMP is the source.

7.6 Clocks

The 77.76 MHz system clock signal for the TBS and ACK and DCK Telecom bus clocks for the SPECTRA-2488 can be configured in two ways. The clock is supplied from an on-board 77.76 MHz HCMOS crystal oscillator or from the backplane. This clock source should have a frequency stability of ± 100 ppm.

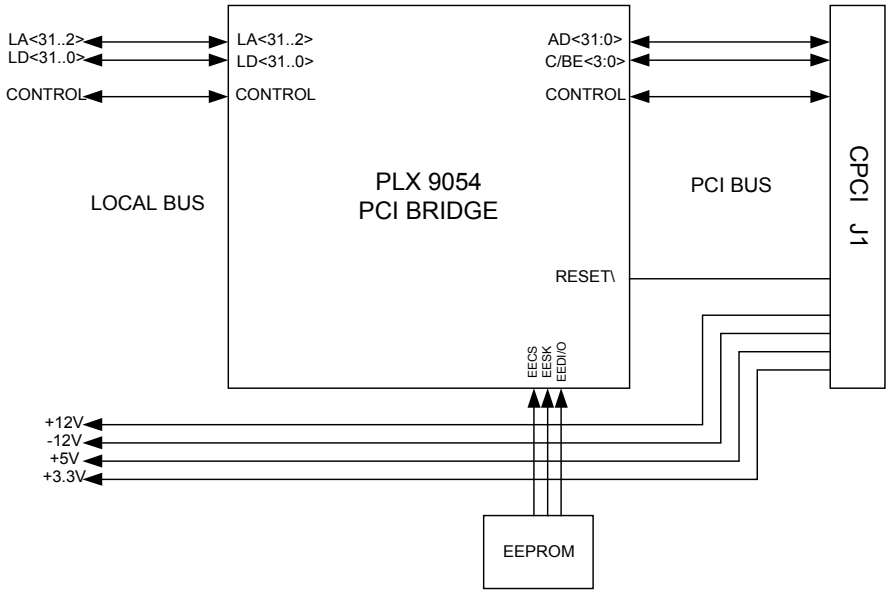
The 77.76 MHz reference clock for the MAXIM 3880 deserializer can be supplied by an on board LVPECL crystal oscillator or from the front panel through a SMA connector. This clock should be from a low phase noise source with a frequency stability ± 20 ppm.

7.7 CompactPCI Interface

The microprocessor interface provides read/write access to normal and test mode registers as described within the SPECTRA-2488 and TBS Data Sheet. This design connects a CompactPCI bus to this microprocessor interface.

A block diagram of the cPCI interface and bridge is shown below in Figure 9.

Figure 9 - cPCI Block Diagram.



7.7.1 Interface and Bridge Hardware

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1 connector to the PLC PCI9054 bridge device. The bus and control lines are terminated with 10 ohm stub resistance that should be placed close to the J1 connector pins.

For this reference design the PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. Address lines LA<31...2> provide 32-bit word addressing. The lower two bits of the address lines are used for 16 or 8 bit

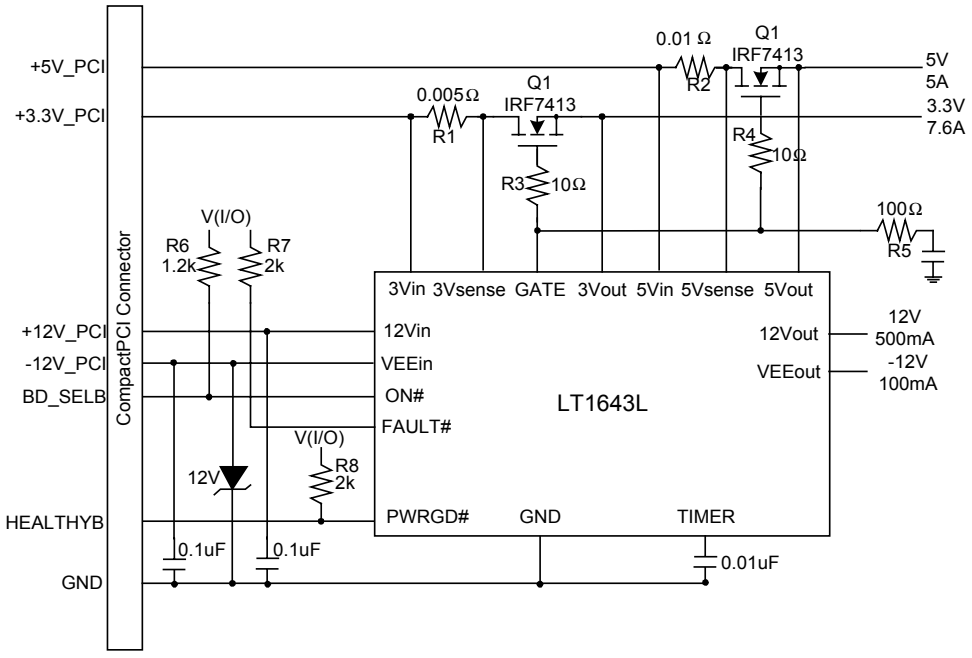
byte access but are unused in this application. The CPLD (Section **7.5.1**) implements the local bus glue logic.

A serial EEPROM is required for device configuration after reset or upon power-up. PLX recommends Fairchild Semiconductor the 93CSX6L family serial EEPROMs. The PCI9054 can also be configured by an on board microprocessor/controller if desired.

7.7.2 Hot Swap Features

The Hot Swap Controller is used to allow a board to be safely inserted or removed from a live cPCI slot. External N-channel MOSFETS control the 3.3V and 5V supplies, while the +12V and –12V supplies are controlled with on-chip switches. The supply voltages are ramped up at a programmable rate. The hot swap controller is implemented using the Linear Technology LTC1643L. A typical cPCI Hot Swap circuit is shown below in Figure 10. Note that only the hot swap controller is implemented in the power block. Additional Hot Swap circuitry including the precharge circuitry for the cPCI bus is included in the CompactPCI block.

Figure 10 - cPCI Hot Swap Circuit



The 3.3V, 5V, +12V, and –12V power supplies are generated from the medium length power pins on the PCI connector (+5V_PCI, +3.3V_PCI, etc). The long power pins which make the first connections are used to generate a 1V precharge voltage on the cPCI bus pins.

In the circuit above, the 3.3V and 5V power supplies are controlled by the N-channel pass transistors Q1 and Q2. Internal circuitry controls the +/-12V rails. R1 and R2 control overcurrent conditions. R5 and C1 provide current control loop compensation. R3 and R4 prevent high frequency oscillations in the pass transistors. Finally, the 12V Zener diode protects against power surges on the –12V rail.

During an insertion and power-up sequence, the BD_SEL# pin is the final pin to connect to the board. This pin is connected to the ON# pin of the Hot Swap Controller. When the ON# pin is pulled low, the pass transistors are turned on by pulling the GATE pin high, and the current in each pass transistor rises at a rate of dv/dt = 50μA/C1, until reaching the preset limit. If there is a high load capacitance, the rate of increase will be controlled by this value. Once the supply voltages stabilize the PWRGD# signal is pulled low.

The current limit for the 5V and 3.3V supplies is set by the sense resistors R1 and R2 in Figure 10 above, and is governed by the following equation:

$$I_{\lim} = 53mV / R_{sense}$$

In the circuit shown above, the 3.3V current limit will be 10.6A, and the 5V limit will be 7.6A.

Upon removal, the /ON pin will be pulled high, and the GATE pin on the pass transistors is pulled low to prevent load currents on the 3.3V and 5V rails from instantaneously going to zero and glitching the power supply. The /PWRGD pin is pulled high if any of the supply voltages moves below its threshold.

Refer to the LT1643 datasheets for additional operation and applications information.

7.8 Power

The SPECTRA-2488 With TBS Quad OC-12 reference design requires 5V, 3.3V and 1.8V supplies. Power on 3.3V and 5V is distributed via the cPCI backplane from a centralized power supply. A 1.8V switching regulator has been implemented to lower the supply current requirements in the system to meet cPCI specifications and reduce overall power dissipation.

Table 8: Card Maximum Estimated Power Consumption

PART	SUPPLY	CURRENT	QUANTITY	POWER
SPECTRA-2488	1.8	2163mA	1	3893 mW
TBS	1.8	1535 mA	1	2763 mW
1.8V MAX TOTAL		**3698mA**		**6656 mW**
SPECTRA-2488	3.3	682 mA	1	2251 mW
TBS	3.3	365 mA	1	1205 mW
V23826-H18-C363	3.3	920 mA	4	3036 mW
TQ8106	3.3	64 mA	1	211 mW
PI6C2502	3.3	400mA	4	1320 mW
PI49FCT3805	3.3	25 mA	1	82.5mW
MB3100H OSCILATOR	3.3	90 mA	1	297mW
XC9572XL	3.3	50 mA	1	165mW
PLX9054	3.3	250 mA	1	825 mW
3.3V MAX TOTAL		**2846mA**		**9393mW**
TQ8106	5.0	1292 mA	4	6460 mW
MC100EL14	5.0	42 mA	1	210 mW
MC100ELT22	5.0	22 mA	1	110 mW
PECL OSC.	5.0	85 mA	1	425 mW
5.0V MAX TOTAL		**1441 mA**		**7205mW**

7.9 Mechanical Form Factor

This board is based on the cPCI 6U (233.35mm by 160mm) board size. The J1 connections have standard cPCI pinouts carrying 32 standard cPCI signals. The other connectors implemented in this reference design are the AMP Z-Pack HS3 60 Mbps pin connectors. These connectors are used to connect the 777.6 Mbps LVDS and control signals to the backplane. Note that the columns of the connector are separated by ground planes. Column 10 of the HS3 connector does not have ground shielding on it's outer side, therefore low speed signals are placed in this column. The pin assignments are made in the low-noise configuration as specified by AMP. Table 9 and Table 10 on the following page outlines the HS3 pinout.

Table 9: Working and Protect HS3 Connector Pinout (J6)

Column	A	B	C	D	E	F
1	GND	SYSCLK1P	SYSCLK1N	SYSCLK2P	SYSCLK2N	GND
2	GND	RPPROT4	RNPROT4	TPPROT4	TNPROT4	GND
3	GND	RPPROT3	RNPROT3	TPPROT 3	TNPROT3	GND
4	GND	RPPROT2	RNPROT2	TPPROT2	TNPROT2	GND
5	GND	RPPROT1	RNPROT1	TPPROT1	TNPROT1	GND
6	GND	RPWRK4	RNWRK4	TPWRK4	TNWRK4	GND
7	GND	RPWRK3	RNWRK3	TPWRK3	TNWRK3	GND
8	GND	RPWRK2	RNWRK2	TPWRK2	TNWRK2	GND
9	GND	RPWRK1	RNWRK1	TPWRK1	TNWRK1	GND
10-	GND	TJ0FP_OUT	RJ0FP_IN	RWSEL_IN	XCMP_IN	GND

Table 10: Auxiliary HS3 Connector Pinout (J5)

Column	A	B	C	D	E	F
1	GND	GND	GND	GND	GND	GND

Column	A	B	C	D	E	F
2	GND	GND	GND	TNAUX4	TPAUX4	GND
3	GND	GND	GND	TNAUX3	TPAUX3	GND
4	GND	GND	GND	TNAUX2	TPAUX2	GND
5	GND	GND	GND	TNAUX1	TPAUX1	GND
6	GND	GND	GND	GND	GND	GND
7	GND	GND	GND	RNAUX4	RPAUX4	GND
8	GND	GND	GND	RNAUX3	RPAUX3	GND
9	GND	GND	GND	RNAUX2	RPAUX2	GND
10	GND	GND	GND	RNAUX1	RPAUX1	GND

8 TABLE IMPLEMENTATION DESCRIPTION

This section describes the hardware implementation of the SPECTRA-2488 With TBS Quad OC-12 Line Card Reference Design

8.1 Root Drawing (Schematic Page 1)

This sheet shows the interconnection between the functional blocks of the design. The design is comprised of eight functional blocks: OPTICS_BLOCK, SERDES_BLOCK, SPECTRA_2488_BLOCK, TBS_BLOCK, CPLD_BLOCK, SYSTEM_INTERFACE_BLOCK, CPCI_BLOCK, and POWER_BLOCK

8.2 Optics Block (Schematic Page 2)

This page shows the four fiber optic transceivers and their associated circuitry.

The four Seimens V23826-H18-C363 Optical Data Links (ODLs) provides the optical to electrical (O/E) function for the SPECTRA-2488 device. The V23826-H18-C363 transceiver is a 3.3V LVPECL device in a 1 x 9-pin package with a duplex SC receptacle. The PECL signals connect to the TQ8106 SERDES using differential, 50 Ω controlled impedance signal lines. The transmit signals are terminated at the ODL with an internal 100 Ω resistor. The transceivers have internal 390 Ω pull-down resistors on the receive outputs as well as AC coupling capacitors on both transmit and receive interfaces. The signal detect (SD) signal is a 3.3 V TTL level signal and can interface directly to the SD input of the SPECTRA-2488. Ferrite beads and their associated 0.1 µF bypass capacitors should be located as close as possible to the power pins of the fiber optic module. The 4.7 µF bulk decoupling capacitors can be located conveniently around the optical modules.

8.3 SERDES Block (Schematic Pages 3, 4, 5, 6)

The SERDES_BLOCK contains four Triqint TQ8106 8 bit OC-12 Serializer Deserializer chips, four 77.76 MHz PLLs, and power circuitry.

Schematic page 3 shows the TQ8106 Serializer deserializer, 77.76 MHz PECL clock source Y1, 100ELT22 PECL clock buffer, power supply circuitry and the connections to the SPECTRA_2488 Block. PECL oscillator Y1 provides a 77.76 MHz reference clock for the TQ8106 CSU. The MC100EL buffers the 77.76 MHz PECL clock and distributes it to the other three TQ8106s. The MC100ELT22 provides TTL/PECL conversion for an external reference source. The Pericom PI6C2502 and its' associated components provide a 77.76 MHz PLL that is

locked to the 77.76 MHz clock (TXBC) from the TQ8106 parallel interface and the TDCLK clock from the SPECTRA-2488 TX line side interface. This circuit ensures that the timing requirements between the TQ8106 and the SPECTRA-2488 are met. The parallel input TX data to the TQ8106 (MXD[7:0]) is clocked into the device with respect to its' output clock TXBC. The parallel data bus signals should be routed such that they are less than four inches in length and the difference from trace to trace is less than .5 inches. The resistors attached to pins 72 and 73 can be configured to adjust the phase of the TXBC clock in 90 degree increments to ensure setup and hold times are met.

All 0.1 μF bypass capacitors should be placed as close as possible to the power pins as well as 10 μF bulk capacitors located conveniently around the device. 100 Ω differential and Thevenin terminations should be located as close to the input pins of the TQ8106 and the MC100EL14 devices as possible. 50 Ω Thevenin terminations should be located as close as possible to input pin and have a 0.1 μF bypass capacitor associated with it. Analog loop filters connected to pins FP1, FP2, CDRFP1, and CDRFP2 should have a good ground plane directly below them.

Sheets 4, 5, and 6 are the same as sheet 3 except they have no PECL clock source, PECL clock buffer and TTL to PECL converter.

8.4 SPECTRA 2488 Block (Schematic Pages 7, 8, 9, 10, 11)

The SPECTRA_2488_BLOCK shows the SPECTRA-2488 signals and power circuitry.

Schematic page 7 contains the line interface section of the SPECTRA-2488 device. This interface consists of 32 TX data signals (TD4-1[7:0]), 32 RX data signals (RD4-1[7:0]), and their respective clocks (RCLK[4:1], RDCLK[4:1]). These signals are clocked at 77.76 MHz and should be 65 Ohm controlled impedance traces. Note although no source terminations have been shown, If trace lengths cannot be kept under 4 inches, it is recommended that 51 Ω source terminations be used.

Schematic page 8 contains power block section of the SPECTRA-2488 device. The power block shows all of the power and ground pins for the SPECTRA-2488 device. It is required that the 3.3 VDC I/O be powered before or at the same time as the 1.8 VDC core supply to prevent damage to the ESD protection structures within the SPECTRA-2488 device. The 1.8 V (RAVDL[3:0], TAVDL[3:0]) and 3.3 V (RAVDH[3:0], TAVDH[3:0]) analog power supplies are filtered with a RC network attached to each pin. Digital power pins have 0.1 μF bypass capacitors placed as close as possible to the pins as well as 10 μF bulk capacitors located conveniently around the device.

Schematic page 9 shows the SPECTRA-2488 incoming and outgoing Telecom Bus signals. These signals are clocked at 77.76 MHz and should be 65 Ohm controlled impedance traces. Note although no source terminations have been shown, If trace lengths cannot be kept under 4 inches, it is recommended that 51 Ω source terminations be used.

Schematic page 10 contains the SPECTRA-2488 Overhead, Ring Control Port, and Alarm signals. Some of the signals have been connected to the CPLD for future design considerations. The Ring Control Port signals have been connected to a 16 pin header (J2) for access when APS is implemented.

Schematic page 11 contains the micro interface of the SPECTRA-2488 device. JTAG is not implemented in this design and the pins are left unconnected. Internal JTAG pull-up resistors maintain appropriate level.

8.5 TBS Block (Schematic Pages 12, 13, 14,15, 16)

The TBS_BLOCK shows the TBS signals and power circuitry.

Schematic page 12 contains S-TCB signaling and CHESS system signaling of the TBS device. The S-TCB signals connect directly to the HS3 connector and system backplane with 50 ohm controlled impedance lines. No end terminations are needed as all receive channels are internally 100 Ω differentially terminated.

Schematic page 13 contains the incoming and outgoing parallel Telecombus signals of the TBS device. All OPAIS<1..4>, OTV5<1..4>, OTPL<1..4>, OTAIS<1..4>, OCOUT<1..4>, and IPAIS<1..4>, ITV5<1..4>, ITPL<1..4> and ITAIS<1..4> signals are routed to a header.

Schematic page 14 contains the micro interface of the TBS device. JTAG is not implemented in this design and the pins are left unconnected. Internal JTAG pull-up resistors maintain appropriate signal state.

Schematic page 15 contains the power section of the TBS device. The digital 1.8V pins and 3.3V pins are connected to the supplies generated in the Power Block. All 3.3 V and the 1.8 V supply pins are decoupled with 0.1 μF capacitors. The 1.8 V (AVDL[5:0]) and 3.3 V (AVDH[6:0]) analog power supplies are filtered with a RC network attached to each pin. The supply to the CSU_AVDH pin is passed through an RC filter to provide a clean voltage to the pin. The RES and RESK pins are externally attached via a 3.16 kΩ resistor.

8.6 System Interface Block (Schematic Page 16)

The System Interface Block contains the AMP HS3 connectors for connection to the system backplane. The transmit and receive differential pairs are grouped together on the connector. The top HS3 connector contains the LVDS working and protect differential signals and the differential SYSCLK signals from a timing card. The bottom connector is used strictly for the LVDS auxiliary channels and has space for additional signals. This connector is optional and can be populated depending on the application requirements. All of the LVDS signal traces and the differential SYSCLK traces are 50 Ω controlled impedance lines. More detailed information regarding layout of 777.76 MHz LVDS signals can be found in the “777.6 MHz LVDS DESIGN CONSIDERATIONS” document (PMC-2000299).

8.7 CPLD Block (Schematic Page 17)

The CPLD Block shows the signal connections of the Xilinx XC9572XL CPLD. The CPLD is used for address decoding, microprocessor access control, signal conversion, and clock distribution. Additionally, ring control and alarm signaling are connected for host processor access.

The PECL differential clock signals, SYSCLK1(P,N) and SYSCLK2(P,N), are translated into single-ended TTL signals using the Motorola MC100EPT23 device. A 77.76 MHz local oscillator signal is also input to the CPLD for use in standalone testing or other configurations where a timing card is not available. Through software control, the CPLD can select which of the clock sources is to be used and the Pericom 49FCT3805 clock driver device is used to buffer this signal to the TBS (SYSCLK) and SPECTRA-2488 (ACK and DCK) devices.

The Maxim MAX811T power supply monitor device with reset provides manual reset capability with a push-button switch attached to the master reset input. The Motorola MC74HC244 driver/buffer chip is used to drive the Lumex LXH5147 LED arrays. The microprocessor interrupt lines are routed to the LED’s for device interrupt status.

A header provides an interface to the CPLD JTAG pins for programming via an Xchecker cable.

The CPLD code is currently under development and will be available at a future date.

8.8 CPCI Block (Schematic Pages 18, 19)

The CPCI_BLOCK shows the PLX 9054 signal and power circuitry connections.

The PCI9054 is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The 32 bit multiplexed address/data bus and associated control lines connect directly from the CPCI J1 connector to the PLC PCI9054 interface device. The bus and control lines are terminated with 10 ohm stub resistance that should be placed close to the J1 connector pins.

The PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. Address lines LA<31...2> provide 32 bit word addressing. The lower two bits of the address lines are used for 16 or 8 bit byte access but are unused in this application.

A serial EEPROM is required for device configuration after reset or upon power-up. The Fairchild Semiconductor NM93CS46 serial EEPROM is used to program the 9054.

The Compact PCI specification outlines a number of layout requirements for the cPCI design. These include:

- All 10 ohm stub termination resistors must be placed within 0.6” of the J1 pins,
- All PCI signal traces must be less than 1.5” except P_CLK,
- P_CLK trace must be 2.5” +/- 0.1”,
- CPCI bus traces impedance is 65 Ω,
- 39 ohm stub resistor on REQ# should be placed near its source on the PCI9054.

8.9 Power Block (Schematic Page 20)

The Power Block shows the power signal connections, the hot-swap controller, and voltage regulator for 1.8V requirements.

The Power Block provides stable voltage supplies delivered over the CompactPCI backplane from a centralized power supply. Voltage levels of +5V, +3.3V, +12V, -12V and a regulated 1.8V are provided.

All 3.3V power requirements for the board are sourced directly from the hot swap control circuitry. A switching regulator module is used to provide the 1.8V supply

for digital pins of the SPECTRA-2488 and TBS devices. A 182 Ω resistor at its output draws 10 mA to ensure stability in all load conditions.

9 SCHEMATICS

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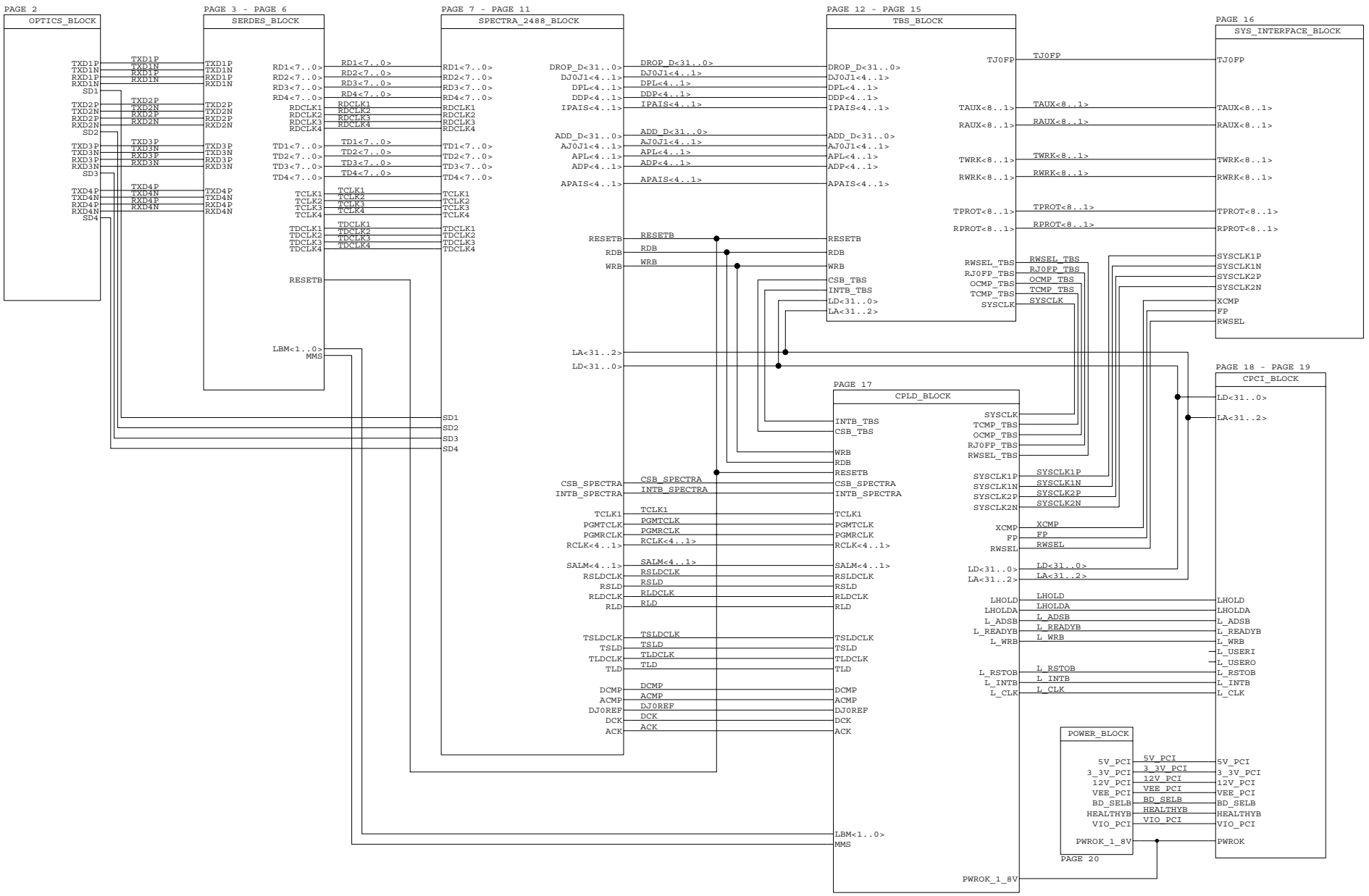

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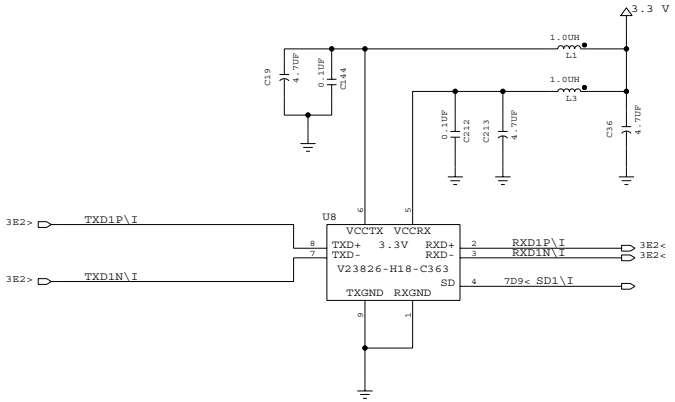

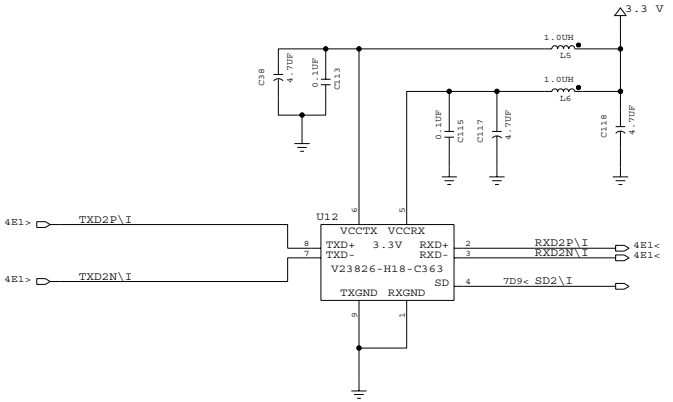

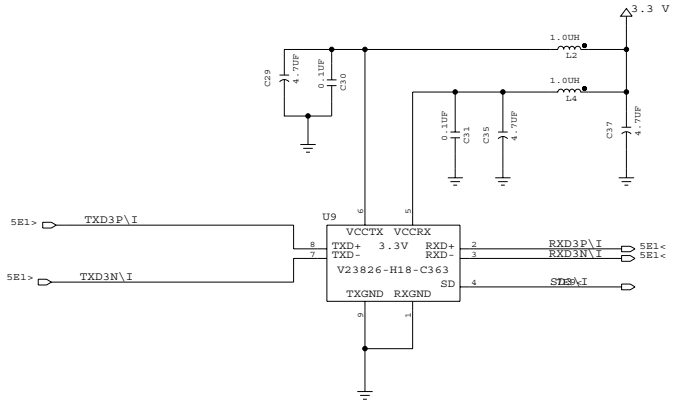

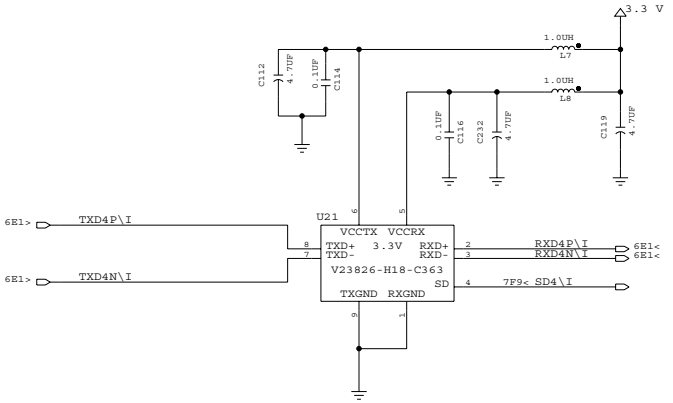

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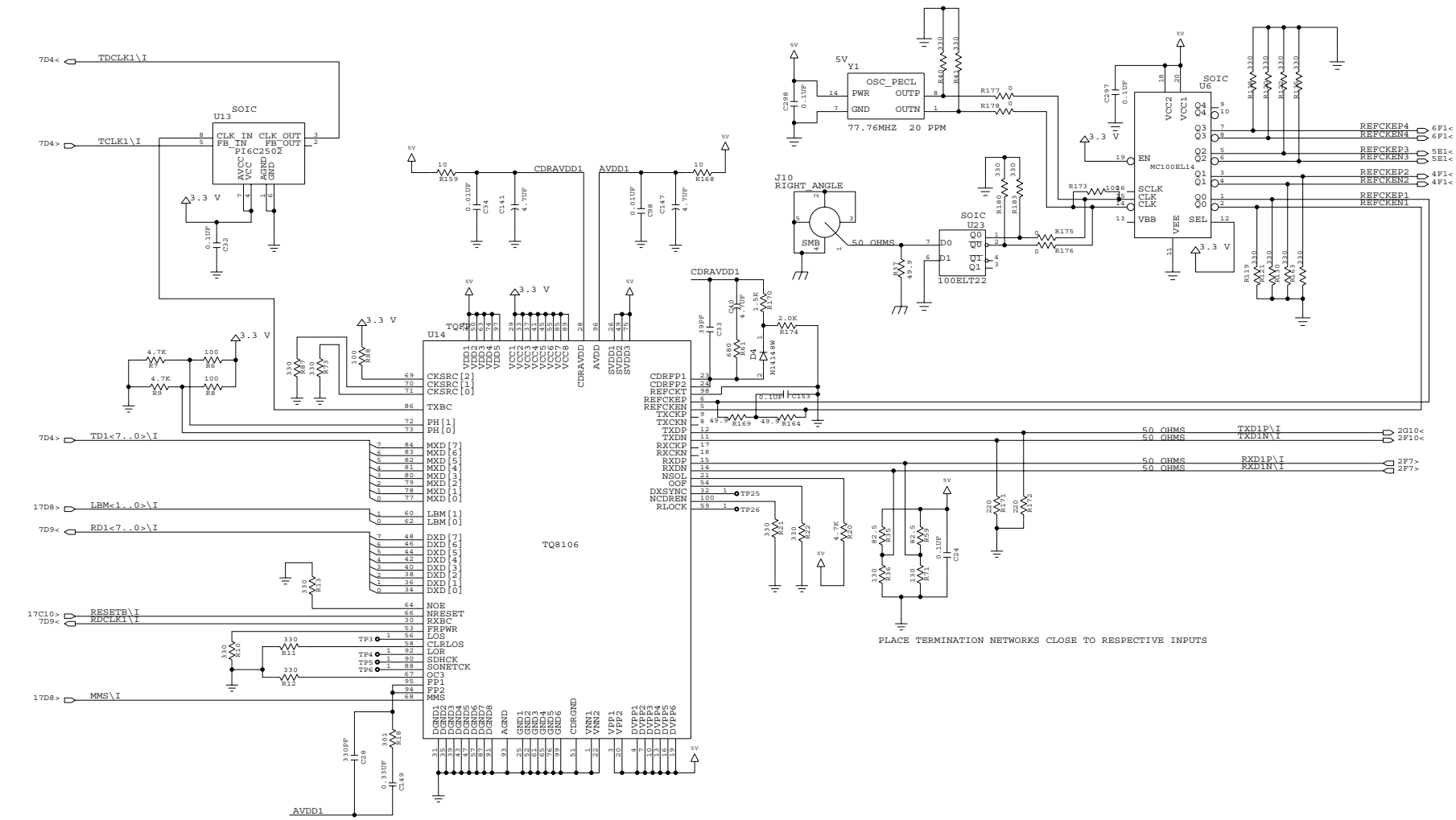

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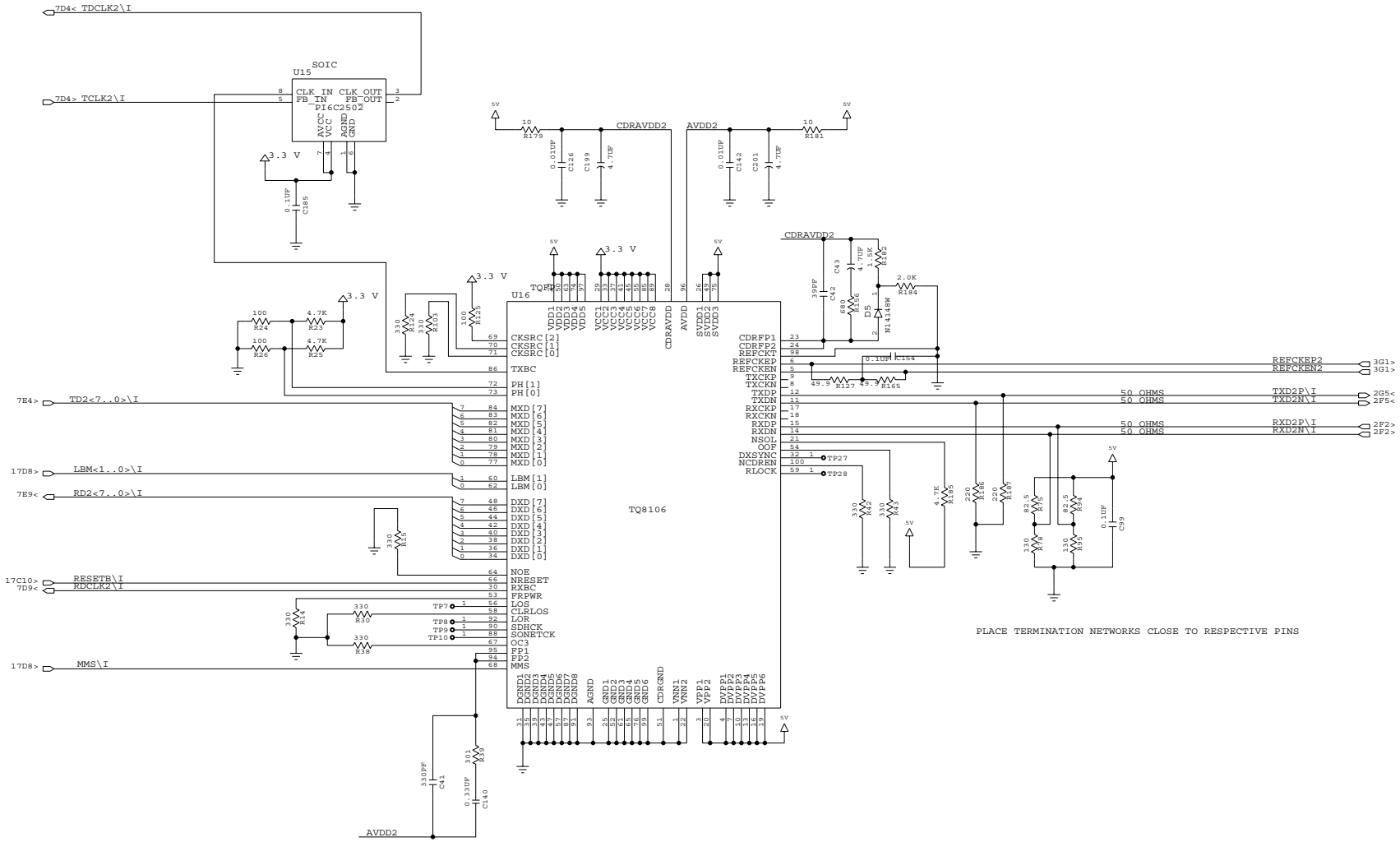

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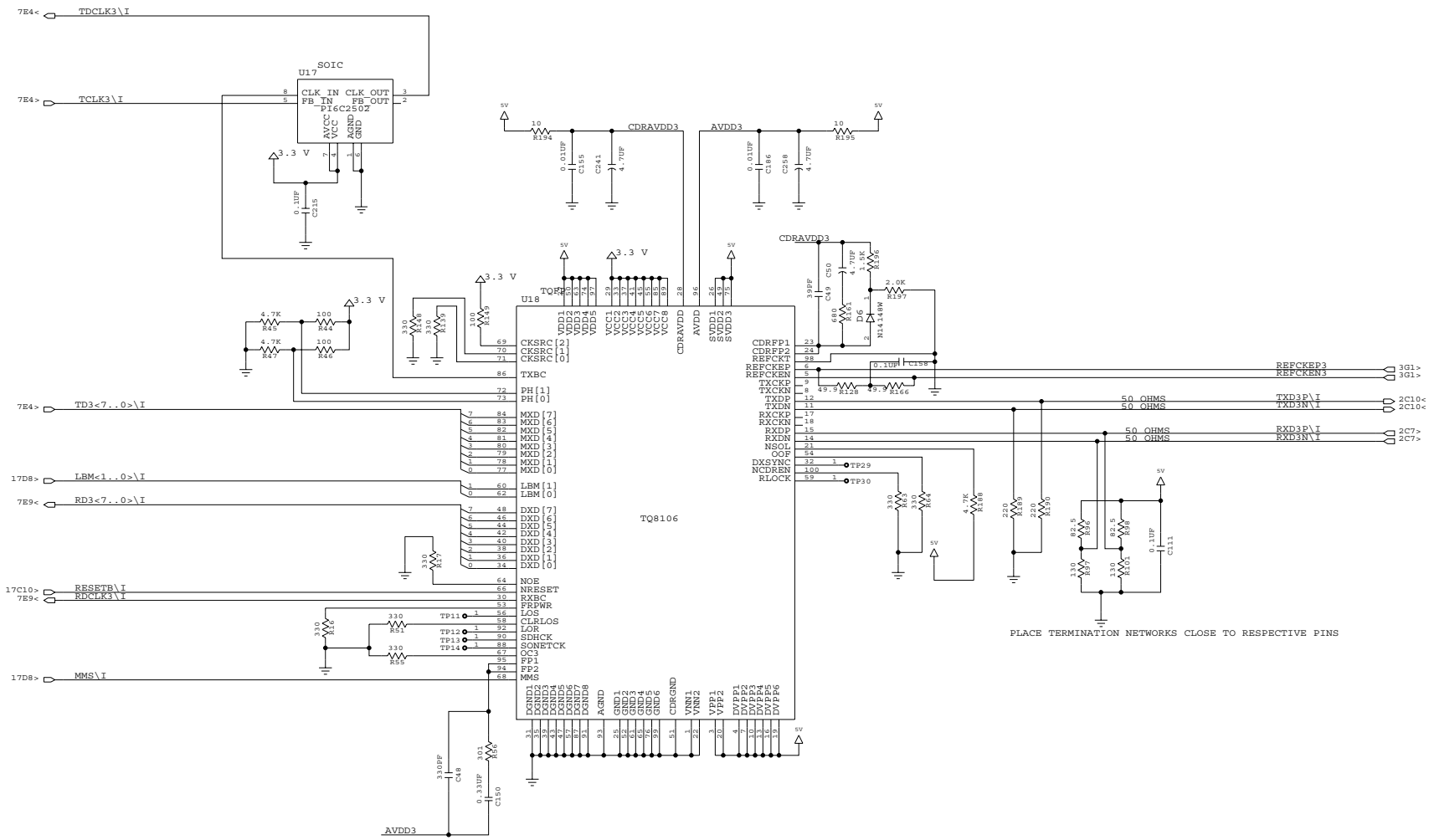

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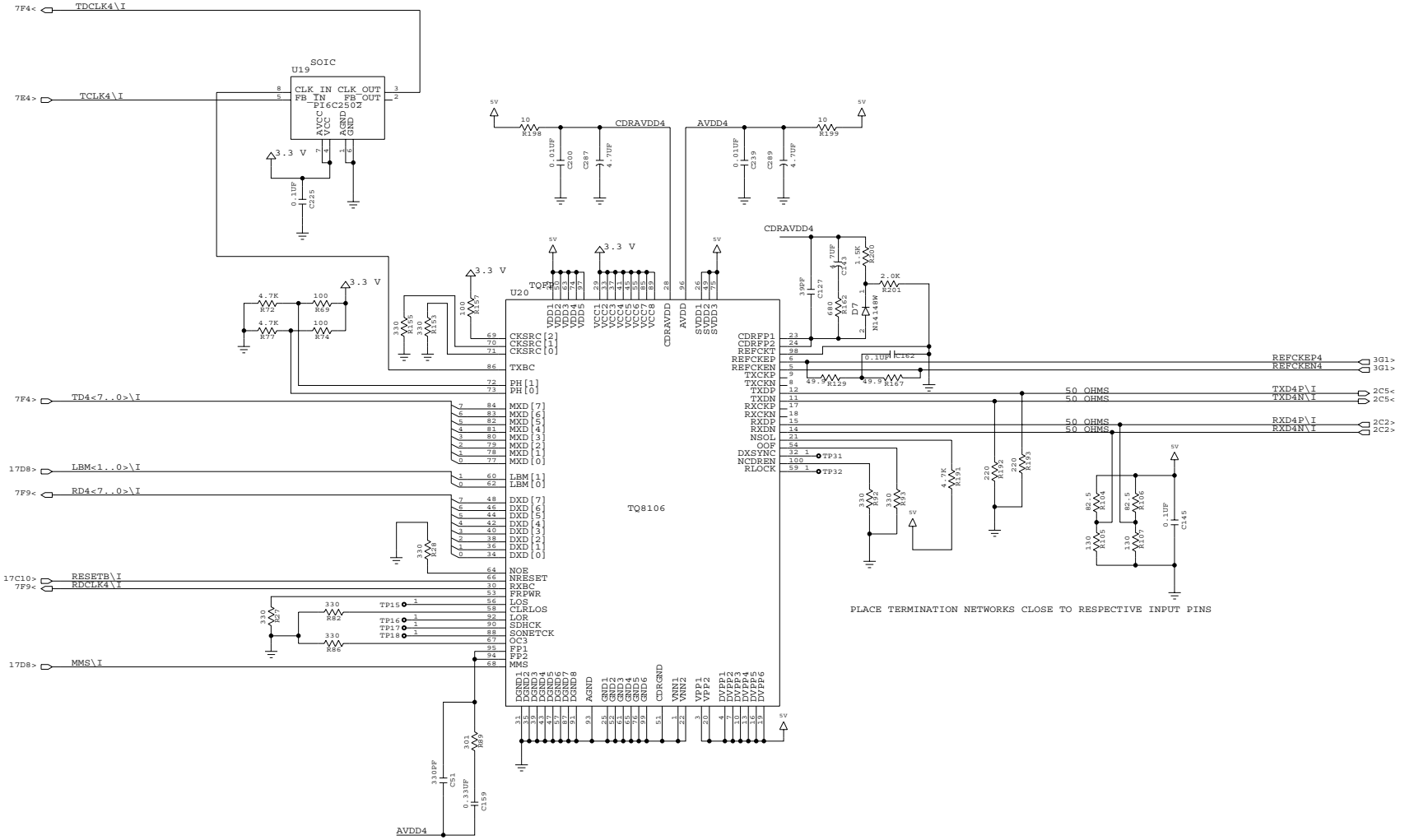

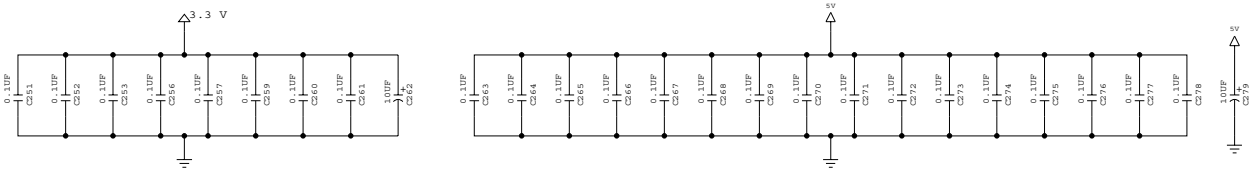

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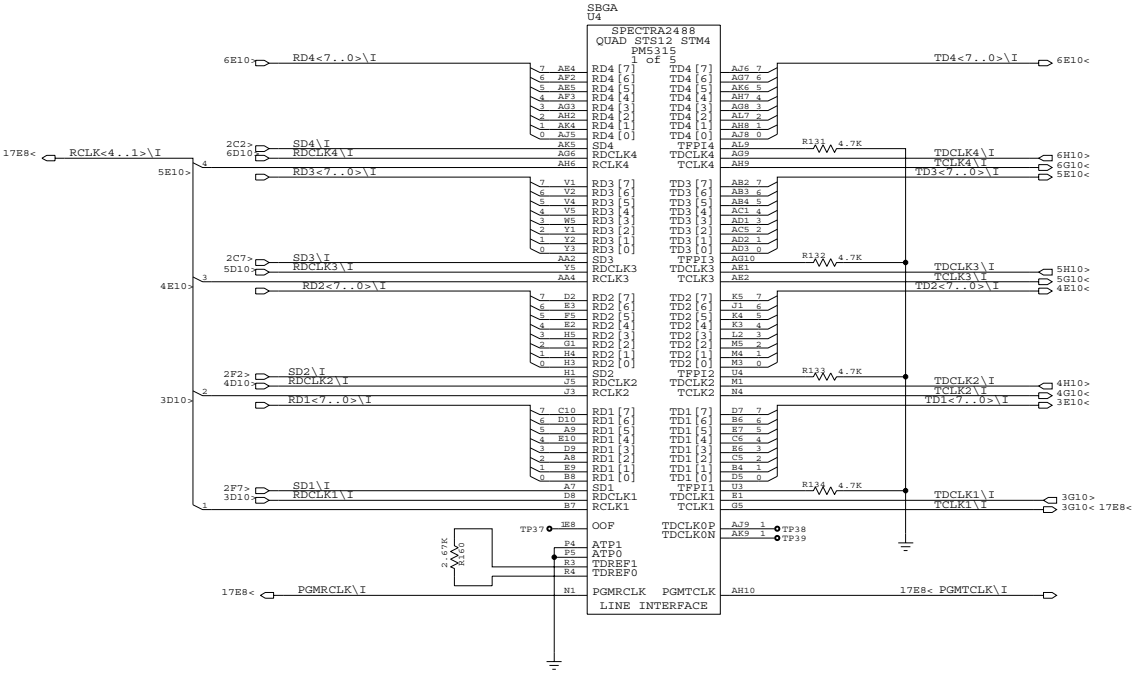

NOTE:WHEN THE SPECTRA-2488 IS USED IN THE QUAD STS-12/STM4 MODE, THE FOLLOWING SIGNALS CAN BE TREATED AS N/CS: RDCLK+/-, RFP+/-, TFPI+/- AND TDCLK+/-.

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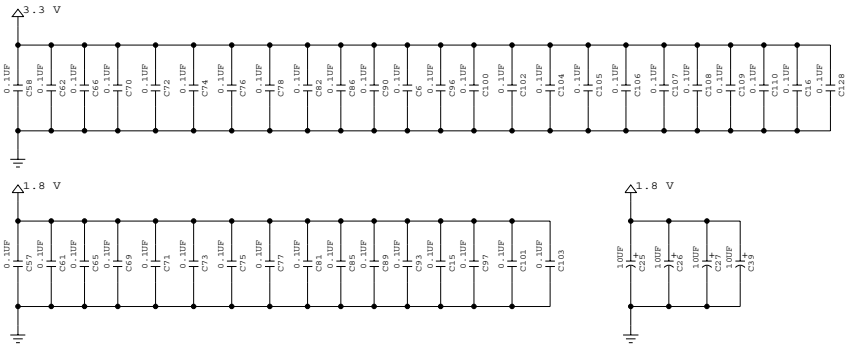

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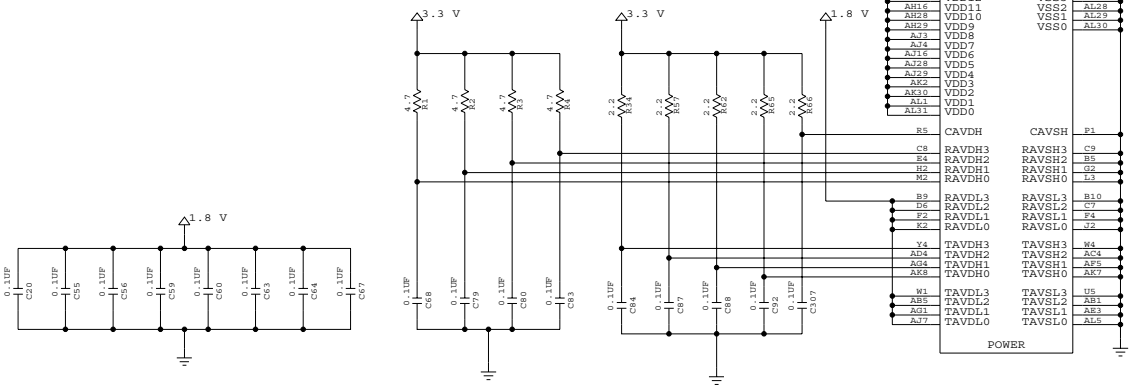

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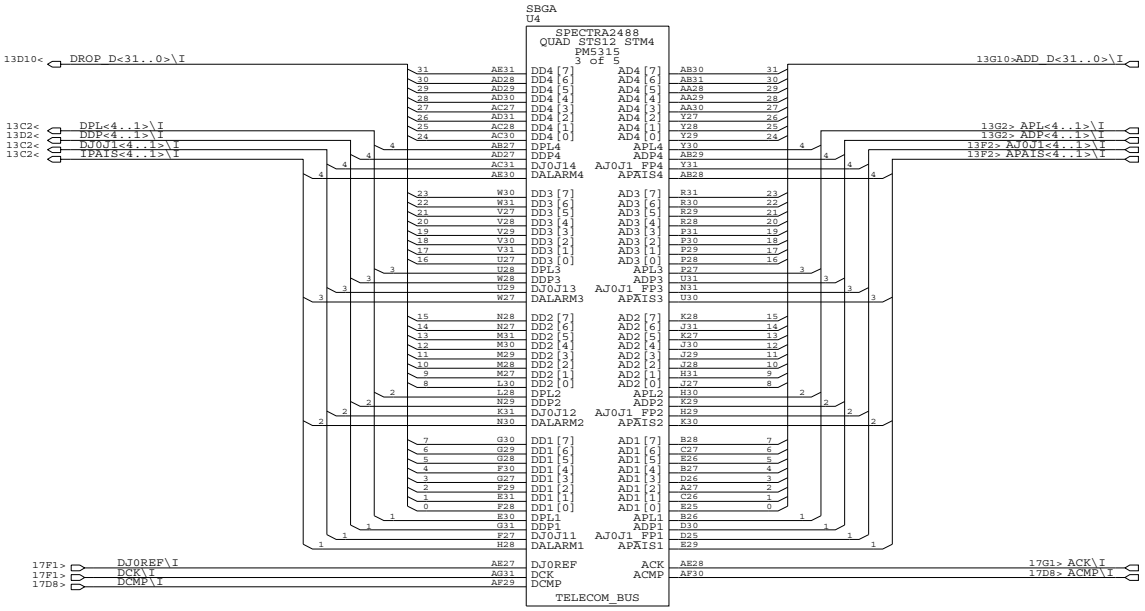

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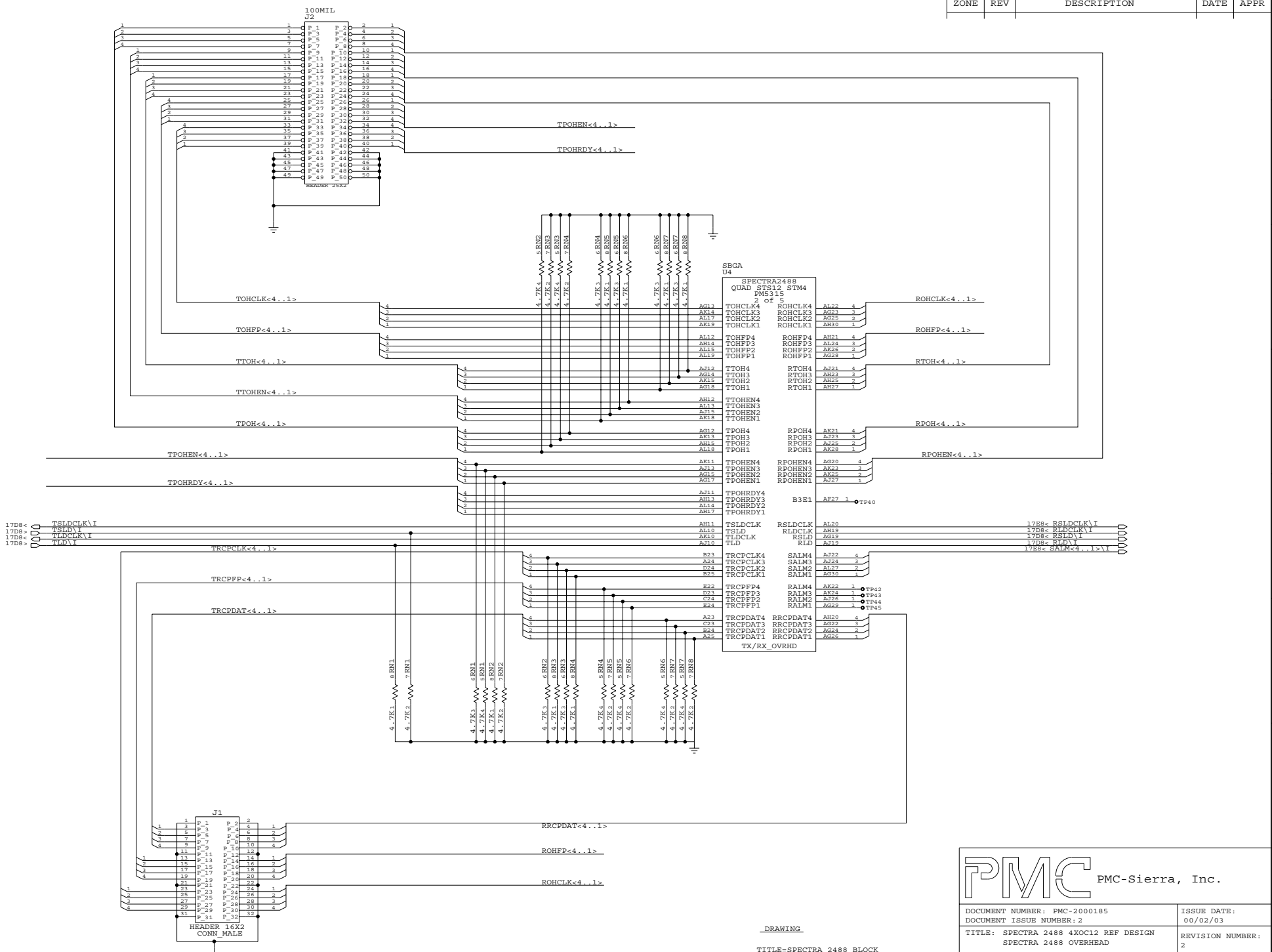

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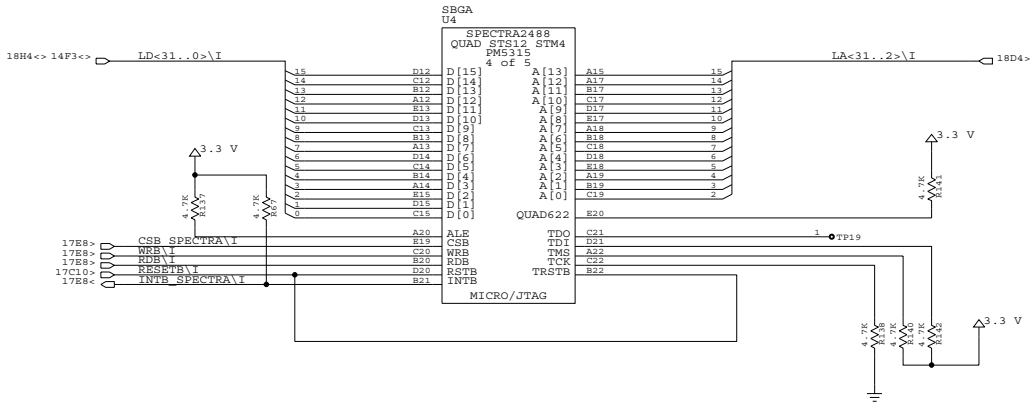

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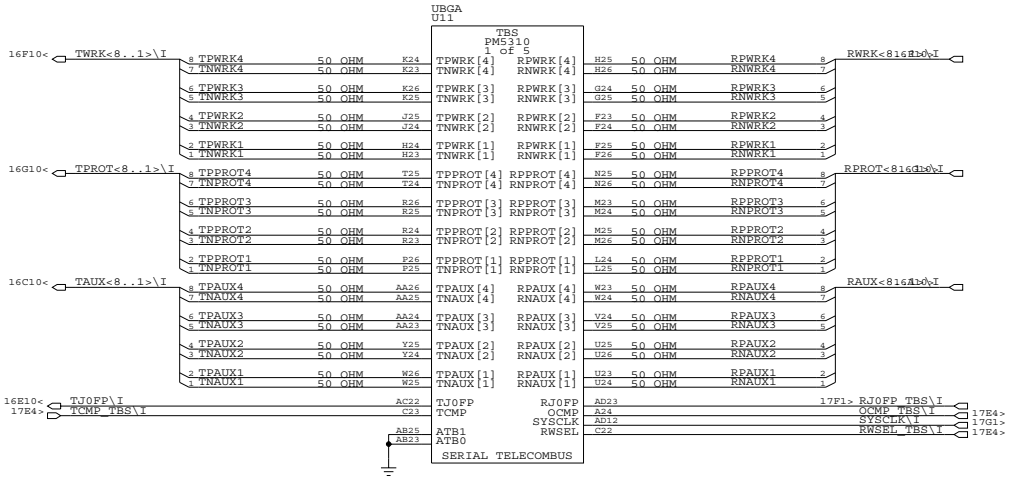

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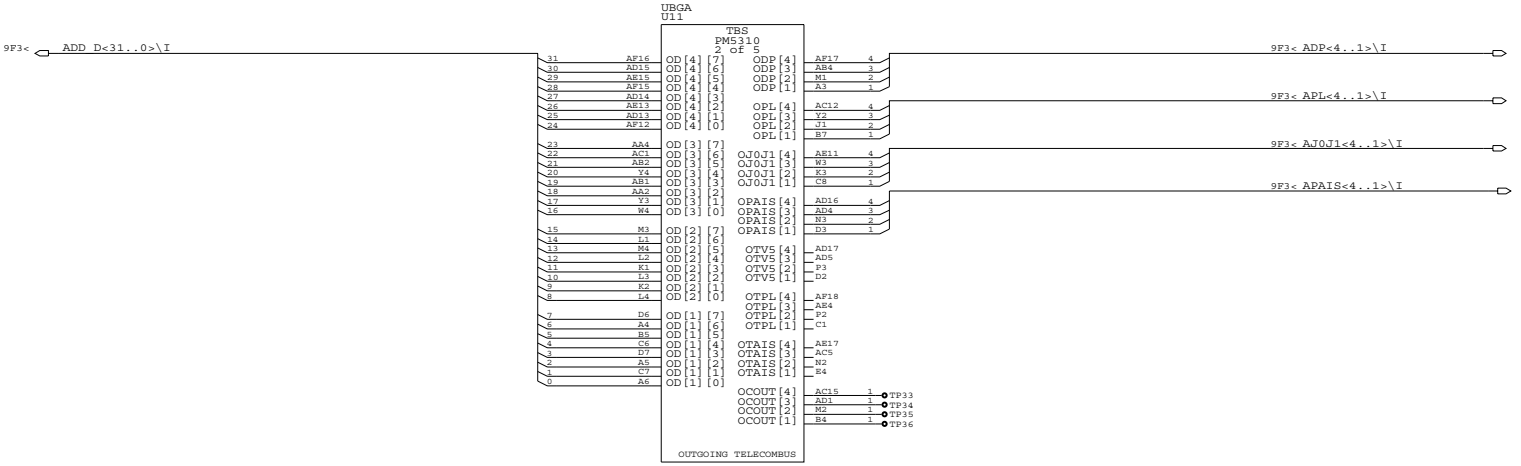

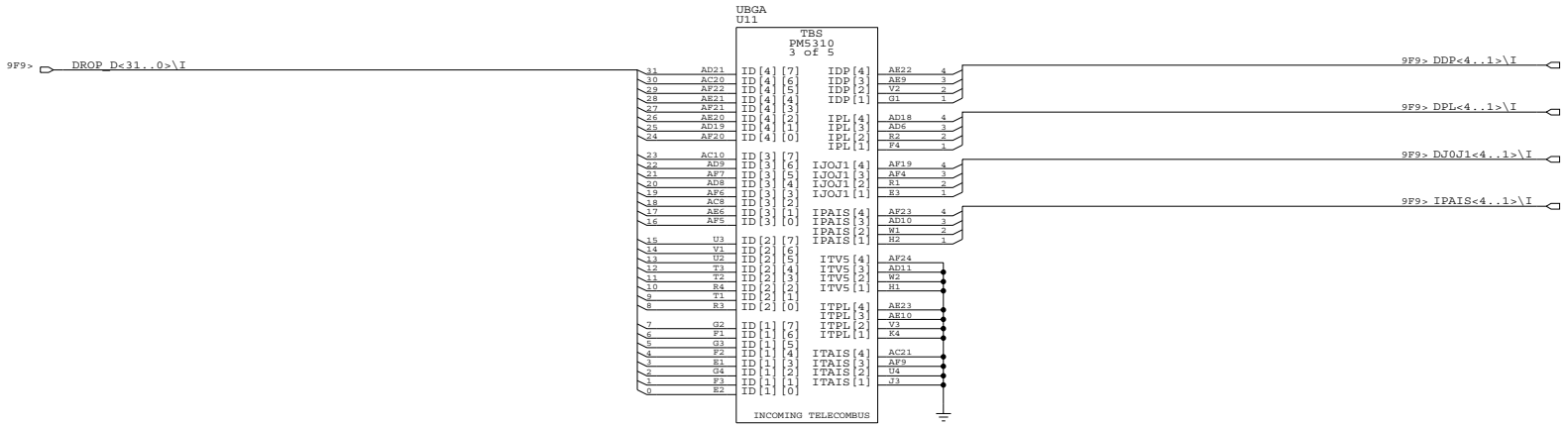

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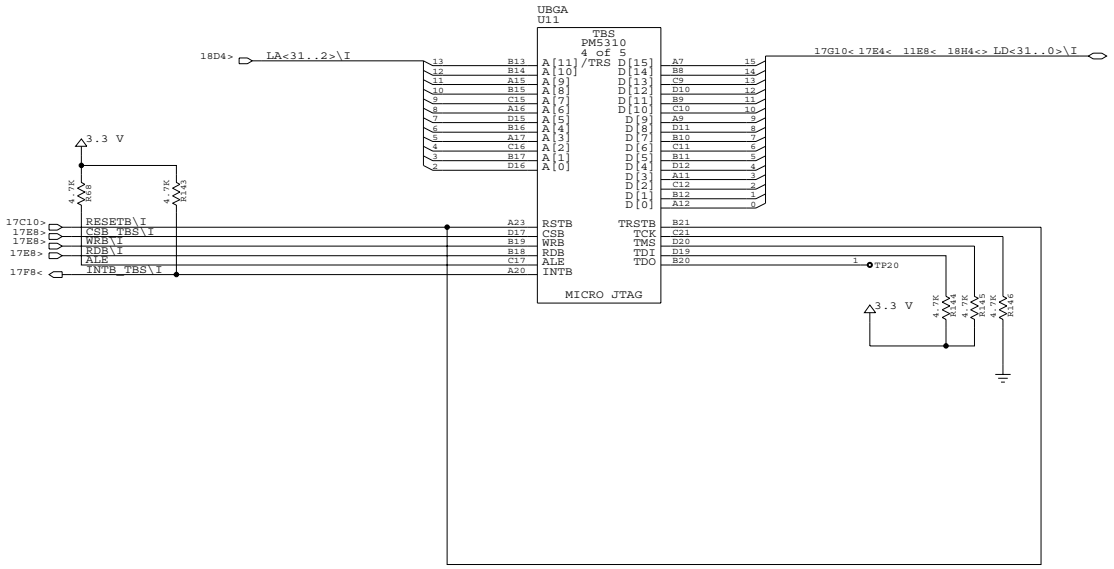
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/02/03
TITLE: SPECTRA 2488 4XOC12 REF DESIGN TBS_BLOCK OUTGOING/INCOMING	REVISION NUMBER: 2
ENGINEER: MK	PAGE:13 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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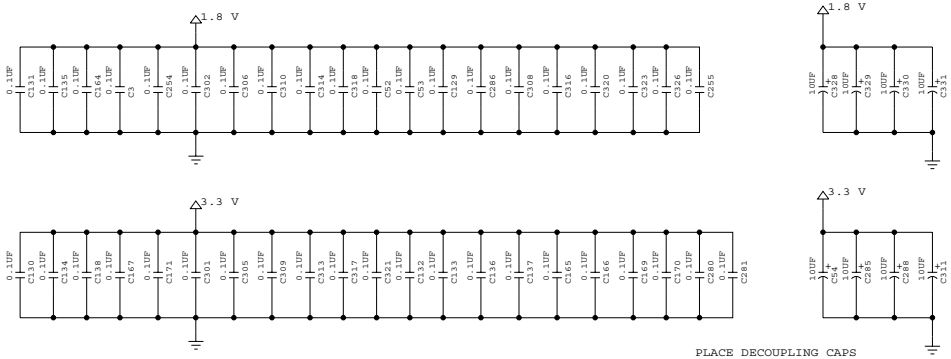
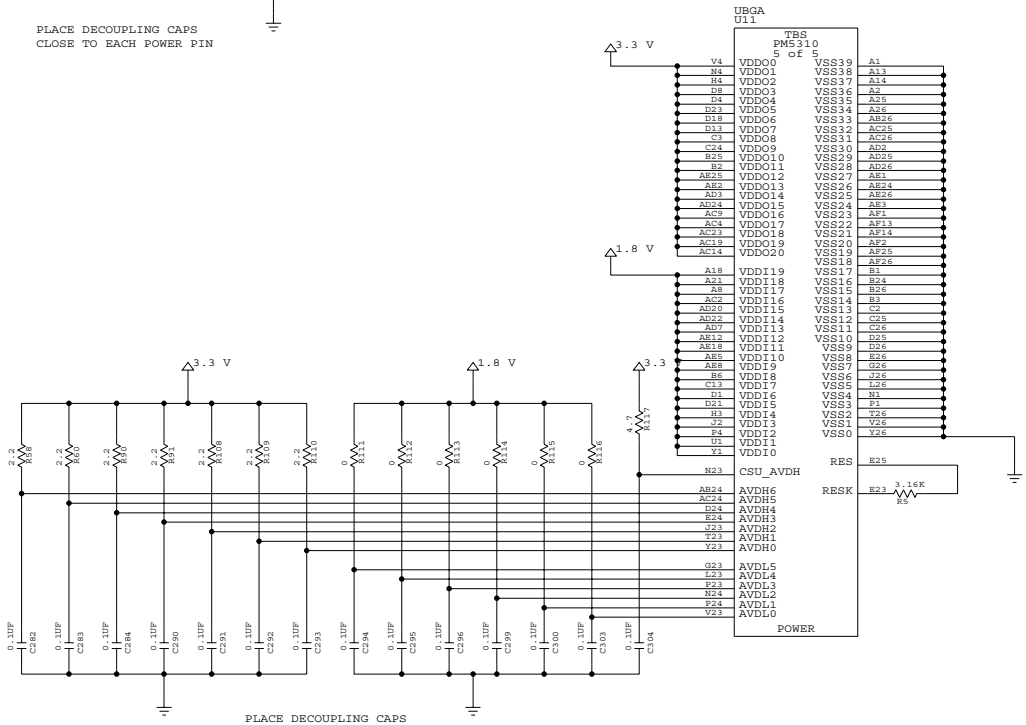
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/02/03
TITLE: SPECTRA 2488 4XOC12 REF DESIGN TBS BLOCK MICRO/JTAG	REVISION NUMBER: 2
ENGINEER: MK	PAGE:14 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





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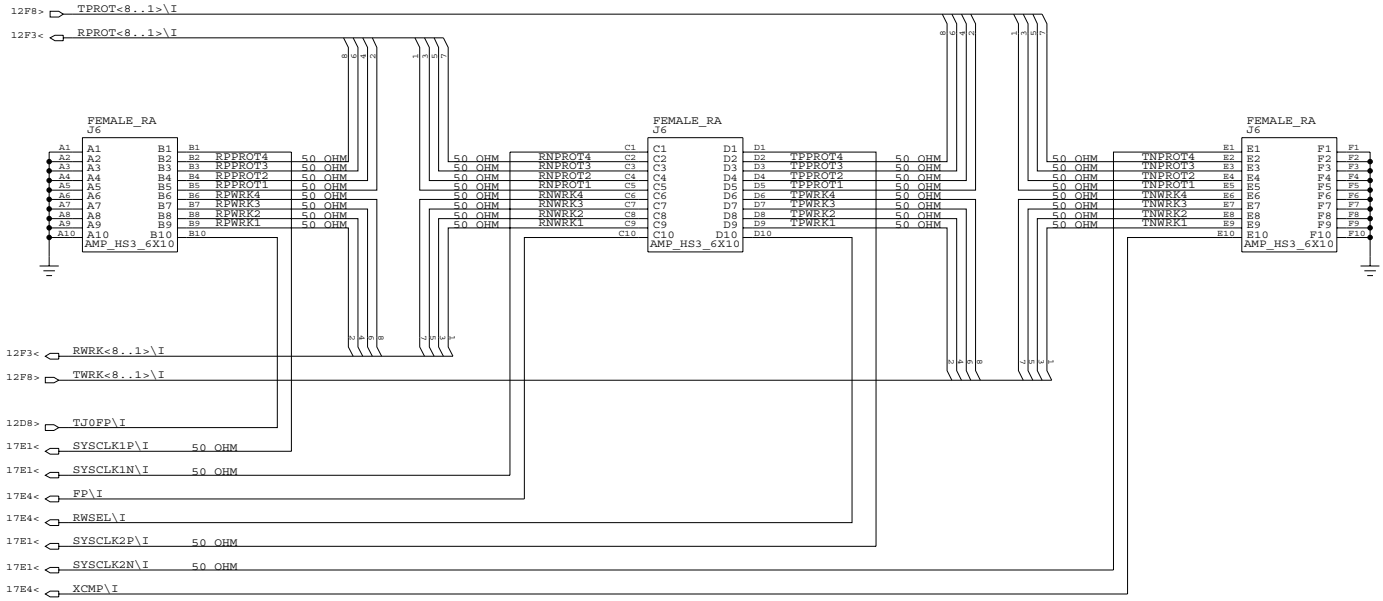
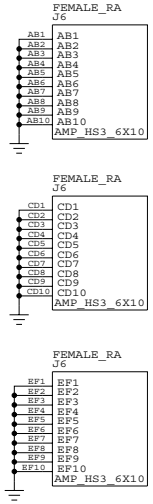
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/02/03
TITLE: SPECTRA 2488 4XOC12 REF DESIGN TBS BLOCK POWER	REVISION NUMBER: 2
ENGINEER: AS	PAGE:15 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

WORKING AND PROTECT LVDS LINKS

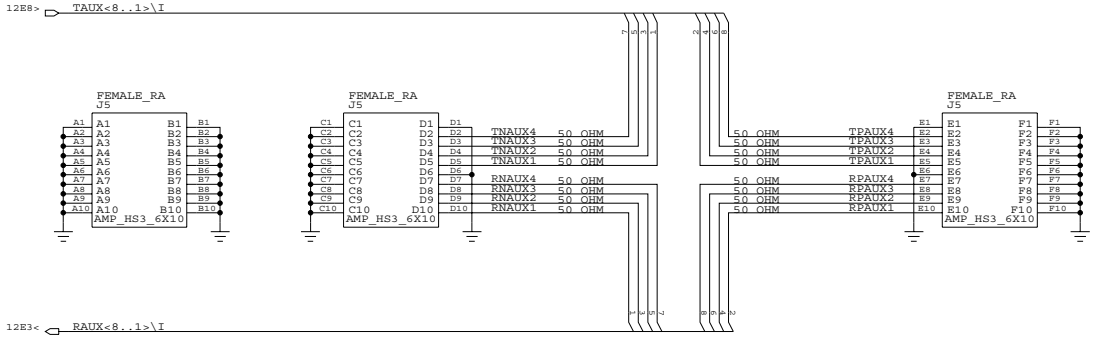


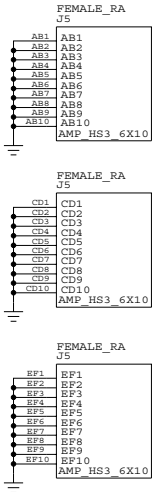


TPROT<8..1>, TWRK<8..1>, RWRK<8..1>, RPROT<8..1>, TAUX<8..1> AND RAUX<8..1>
CONSIST OF DIFFERENTIAL LVDS PAIRS. EACH PAIR SHOULD BE ROUTED TOGETHER ON
THE SAME LAYER AND HAVE THE SAME LENGTH. ALL LVDS TRACES SHOULD BE 50 OHM.

AUXILLARY LVDS LINKS

DO NOT POPULATE CONNECTOR IF AUXILLARY LVDS LINKS NOT REQUIRED





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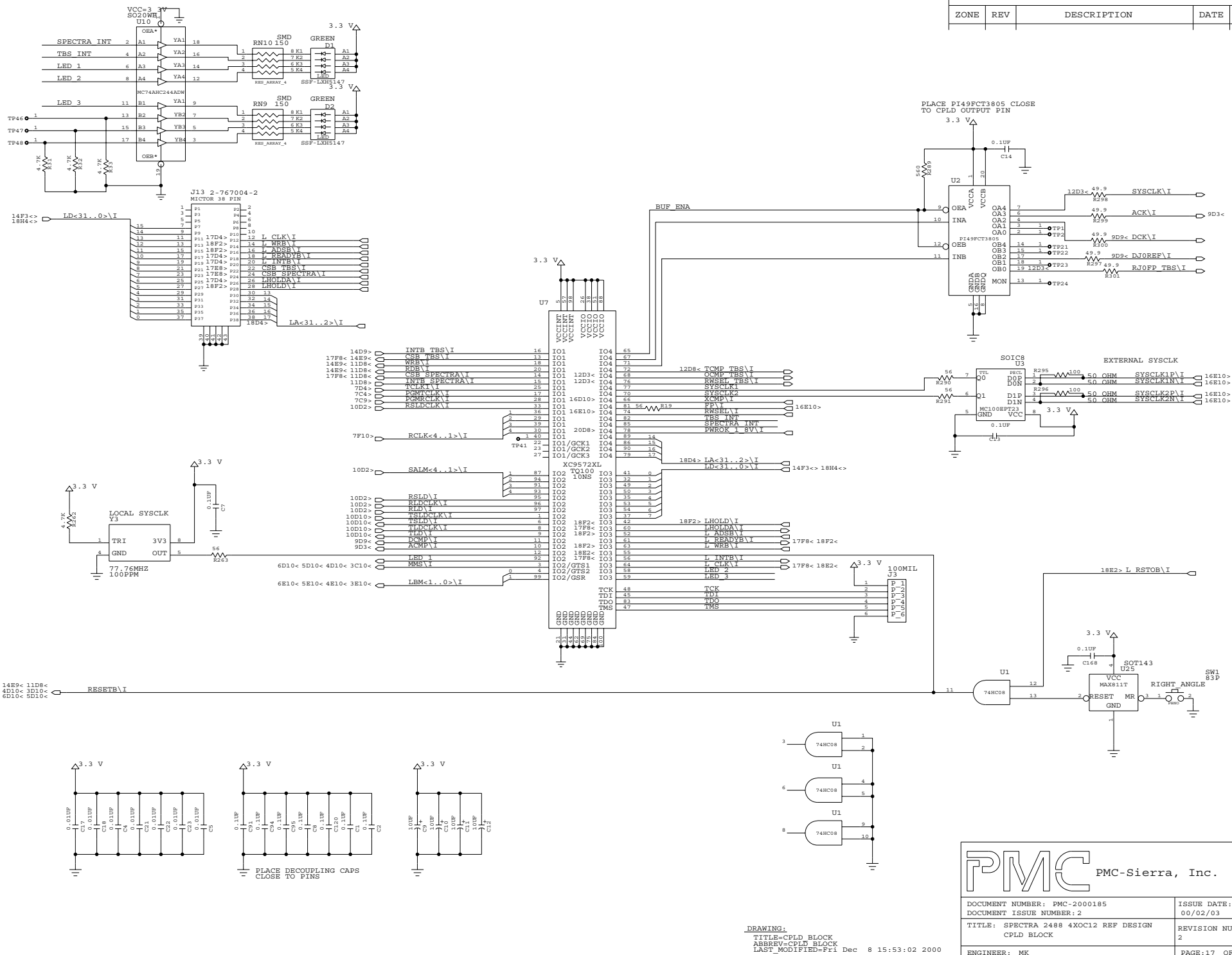
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/03/22
TITLE: SPECTRA 2488 4XOC12 REF DESIGN SYSTEM_INTERFACE_BLOCK	REVISION NUMBER: 2
ENGINEER: MK	PAGE:16 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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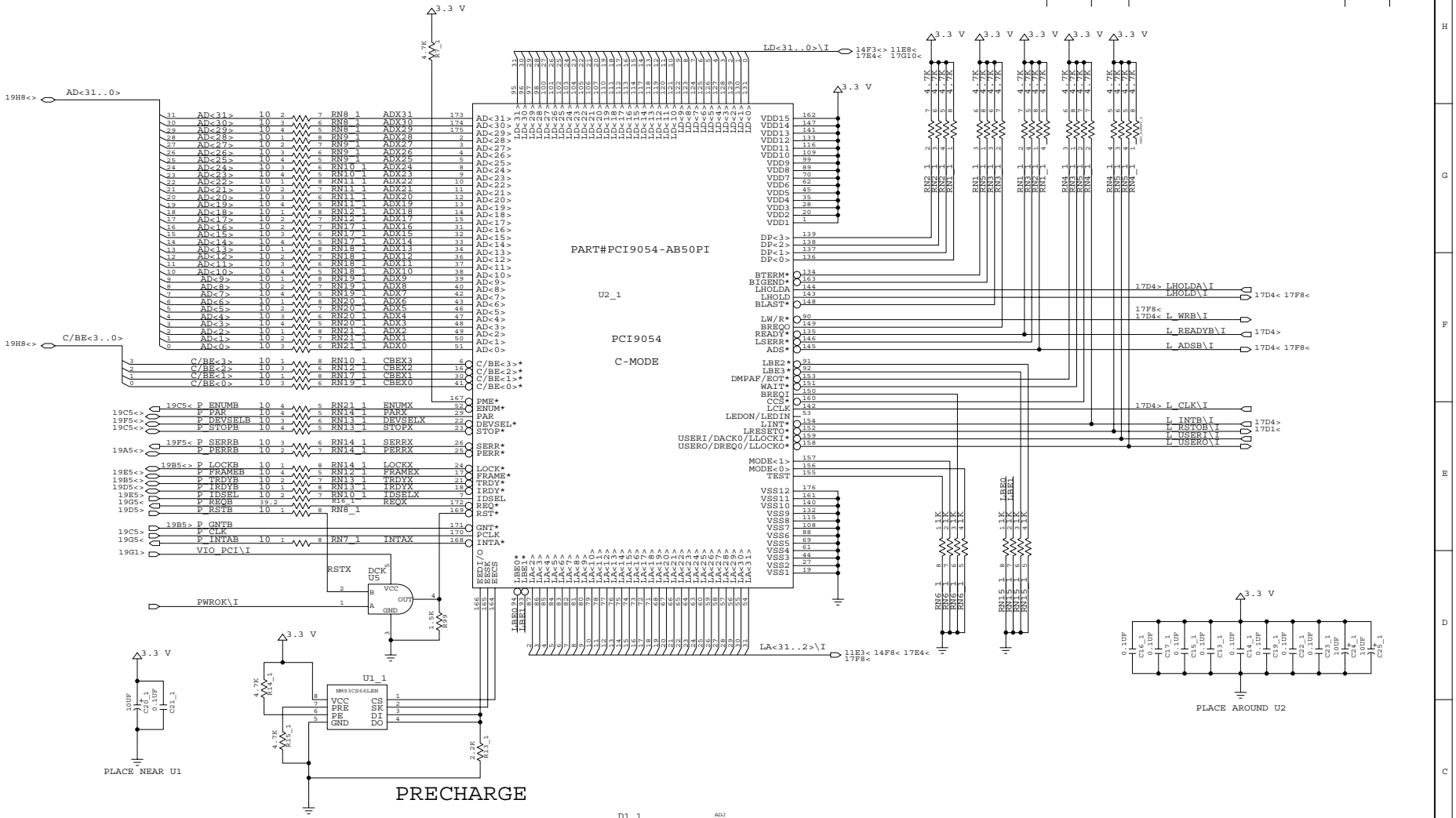
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/02/03
TITLE: SPECTRA 2488 4XOC12 REF DESIGN CPLD BLOCK	REVISION NUMBER: 2
ENGINEER: MK	PAGE:17 OF 20

CPCI BRIDGE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



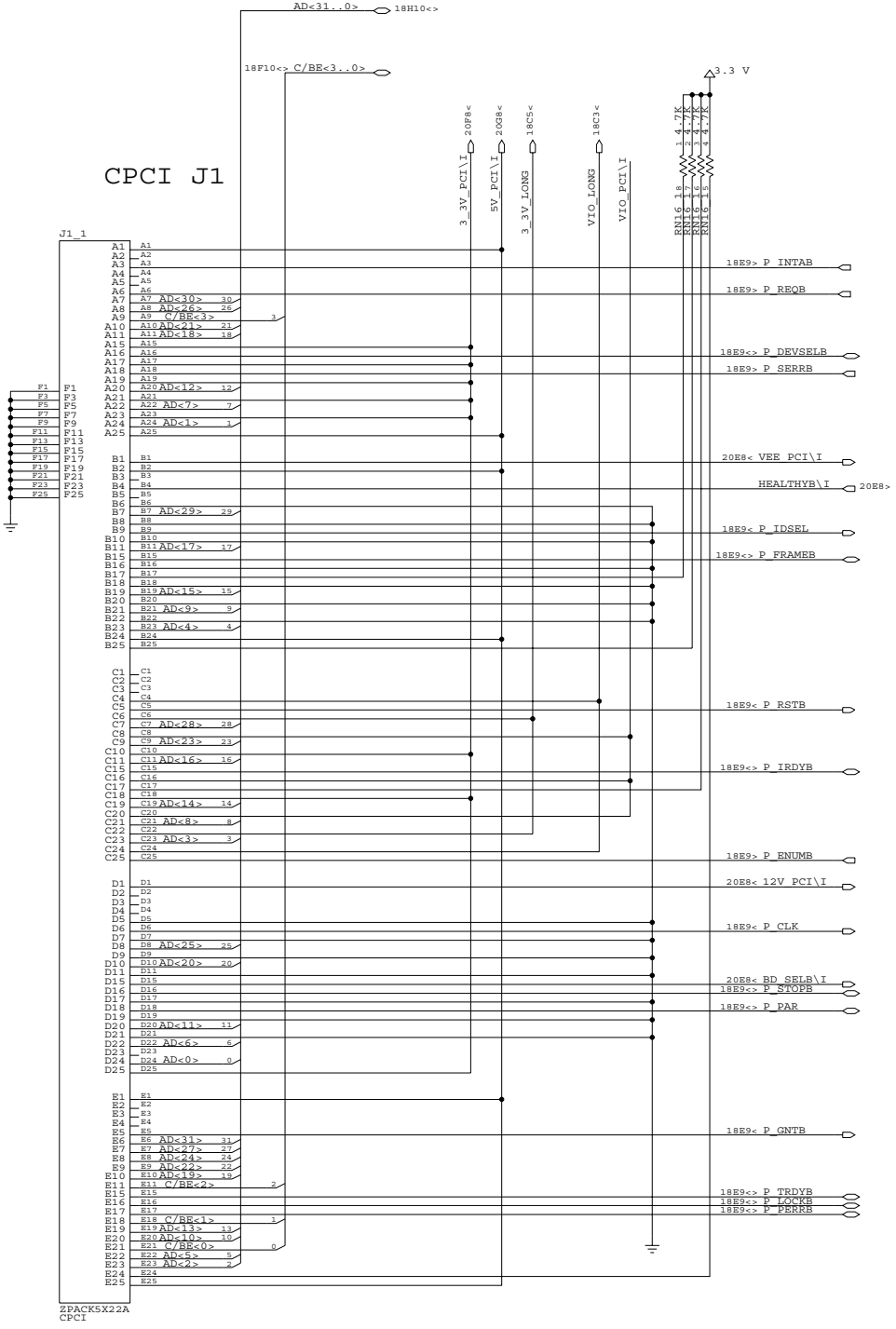
NOTES:
1. ALL 10 OHM STUBS WITHIN 0.6" OF J1
2. ALL PCI SIGNAL TRACES < 1.5" EXCEPT P_CLK
3. P_CLK TRACE MUST BE 2.5" +/- 0.1"
4. CPCI BUS TRACES ARE 65 OHM.
5. 39 OHM STUB RESISTOR ON REQB PLACED NEAR BRIDGE PIN

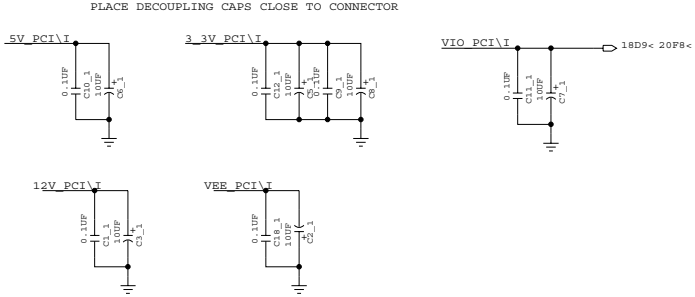
DRAWING:
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Fri Dec 8 15:52:50 2000

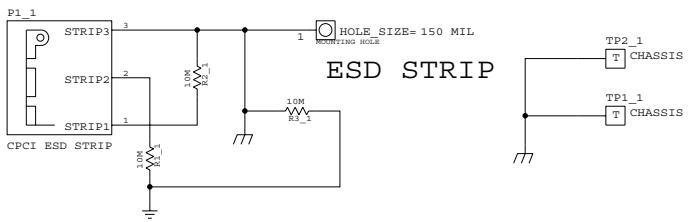
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/04/19
TITLE: SPECTRA 2488 4XOC12 REF DESIGN CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: MK	PAGE:18 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







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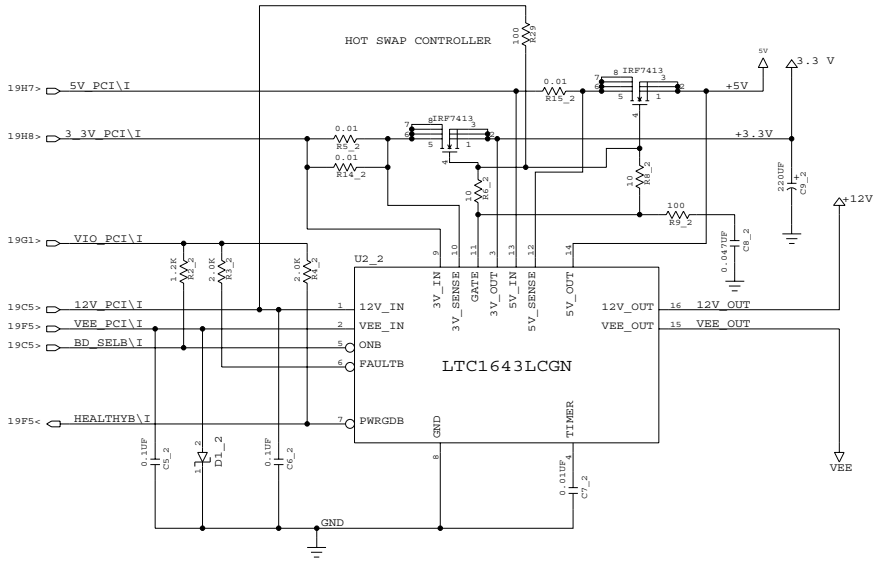
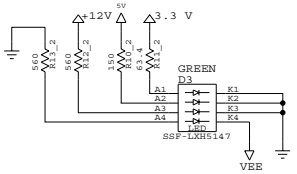
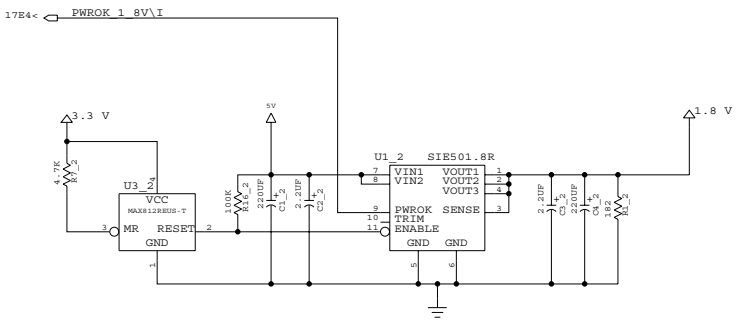
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER:2	ISSUE DATE: 00/04/19
TITLE: SPECTRA 2488 4XOC12 REF DESIGN CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: MK	PAGE:19 OF 20

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







DRAWING:
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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000185 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: 00/04/19
TITLE: SPECTRA 2488 4XOC12 REF DESIGN POWER_BLOCK	REVISION NUMBER: 2
ENGINEER: MK	PAGE:20 OF 20

10 BILL OF MATERIALS

Table 11 : Major Components List

NO.	Manufacturer Part Number	Ref Des	Qty	Descriptions
1	PANASONIC ECJ-1VB1C104K	C1, C10_1, C11_1, C12_1, C13, C13_1, C14, C14_1, C15, C15_1, C2, C3, C6-C8, C16, C20, C24, C30-C32, C52, C53, C55-C97, C99-C111, C113-C116, C120-C125, C128-C139, C144-C146, C148, C152-C154, C156-C158, C160-C162, C164-C169, C16_1, C170-C179, C17_1, C180-C182, C184, C185, C187-C189, C18_1, C190-C193, C195-C198, C19_1, C1_1, C202-C212, C214-C216, C218, C219, C21_1, C220-C226, C228, C229, C22_1, C230, C231, C233-C235, C23_1, C240, C242-C249, C251-C257, C259-C261, C263-C278, C280-C284, C286, C290-C310, C313-C318, C320, C321, C323, C326, C4_1, C5_2, C6_2, C9_1	260	CAP-0.1UF, 16V, CERAMIC X7R_603
2	PANASONIC ECE-V1AA221P	C1_2, C4_2, C9_2	3	CAP-220UF, 10V, ELECTROLYTIC
3	NEWARK -- 52F023	C140, C149, C150, C159	4	CAP-0.33UF, 16V, MURATA NICKEL INNER ELECTRODE TYPE, Y5V_805
4	DIGI-KEY -- PCT2475CT-ND	C19, C29, C35-C38, C40, C43, C50, C112, C117-C119, C141, C143, C147, C199, C201, C213, C232, C241, C258, C287, C289	24	CAP-4.7UF, 10V, TANT TEH
5	PANASONIC ECS-H1VC225R	C2_2, C3_2	2	CAP_POL-2.2UF, 35V, TANCAPC
6	PANASONIC ECS-H1CC106R	C20_1, C24_1, C25_1, C2_1, C3_1, C5_1, C6_1, C7_1, C8_1	9	CAP_POL-10UF, 16V, TANCAPC
7	PANASONIC ECU-V1H331KBN	C28, C41, C48, C51	4	CAP-330PF, 50V, CERAMIC, X7R_805
8	PANASONIC ECU-V1H390JCG	C33, C42, C49, C127	4	CAP-39PF, 50V, CERAMIC, NPO_805
9	PANASONIC ECU-V1H103KBV	C4, C5, C17, C18, C21-C23, C34, C98, C126, C142, C155, C186, C200, C239, C7_2	16	CAP-0.01UF, 50V, CERAMIC, X7R_603
10	PANASONIC ECU-V1H473KBW	C8_2	1	CAP-0.047UF, 50V, CERAMIC, X7R_1206

NO.	Manufacturer Part Number	Ref Des	Qty	Descriptions
11	PANASONIC ECS-T0JY106R	C9-C12, C25-C27, C39, C44-C47, C54, C151, C183, C194, C217, C227, C250, C262, C279, C285, C288, C311, C328-C331	28	CAP_POL-10UF, 6.3V, TANCAPA
12	MICROSEMI DL4148MS	D1_1	1	DIODE RECT 150MA 75V SMT MINIMELF
13	DIODES INC ZM4742A	D1_2	1	ZENER DIODE 12.0V 5% 1.0W SURFACE MOUNT
14	LUMEX SSF-LXH5147LGD	D1-D3	3	LED QUAD GREEN HORIZONTAL
15	VISHAY/LITE- ON 1N4148W	D4-D7	4	SURFACE MOUNT SWITCHING DIODE
16	SULLINS PZC36DAAN	J1	1	CONN HEADER 2 ROW 0.1"X0.1" 2X16
17	AMP 352068-1	J1_1	1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD
18	JOHNSON COMPONENTS 131-3701-341	J10	1	50 OHM RIGHT ANGLE BULKHEAD JACK RECEPTACLE
19	AMP 2-767004-2	J13	1	CONNECTOR 38 POS VERTICAL .025" TO .64" SMD MICTOR
20	SULLINS PZC36DAAN X 25/36	J2	1	HEADER 25X2 GOLD 0.1" SPACING
21	SULLINS ELECTRONICS PZC36SAAN	J3	1	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW
22	AMP 120673-1	J5, J6	2	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE
23	PANASONIC ELJ-FD1R0KF	L1-L8	8	INDUCTOR 1.0UH 10% TYPE FD 0805
24	MOUNTING HOLE	M1_1	1	MOUNTING_HOLE_150MIL - BASE
25	PART OF PCB	P1_1	1	PART OF PCB COMPACT PCI ESD STRIP
26	INTERNATIONA L RECTIFIER IRF7413	Q1_2, Q2_2	2	IC POWER MOSFET, SOIC-BASE
27	PANASONIC ERJ-8GEYJ106V	R1_1, R2_1, R3_1	3	RES-10M, 5%, 1206
28	PANASONIC ERJ-3EKF1820V	R1_2	1	RES-182, 1%, 603
29	PANASONIC ERJ-3EKF1000V	R10_1, R173, R295, R296, R9_2	5	RES-100, 1%, 603
30	PANASONIC ERJ-3GSYJ151V	R10_2	1	RES-150, 5%, 603
31	PANASONIC ERJ-3GSYJ331V	R10-R17, R21, R22, R27, R28, R30, R38, R40-R43, R51, R55, R63, R64, R73, R82, R86, R87, R92, R93, R103, R118-R122, R124, R130,	44	RES-330, 5%, 603

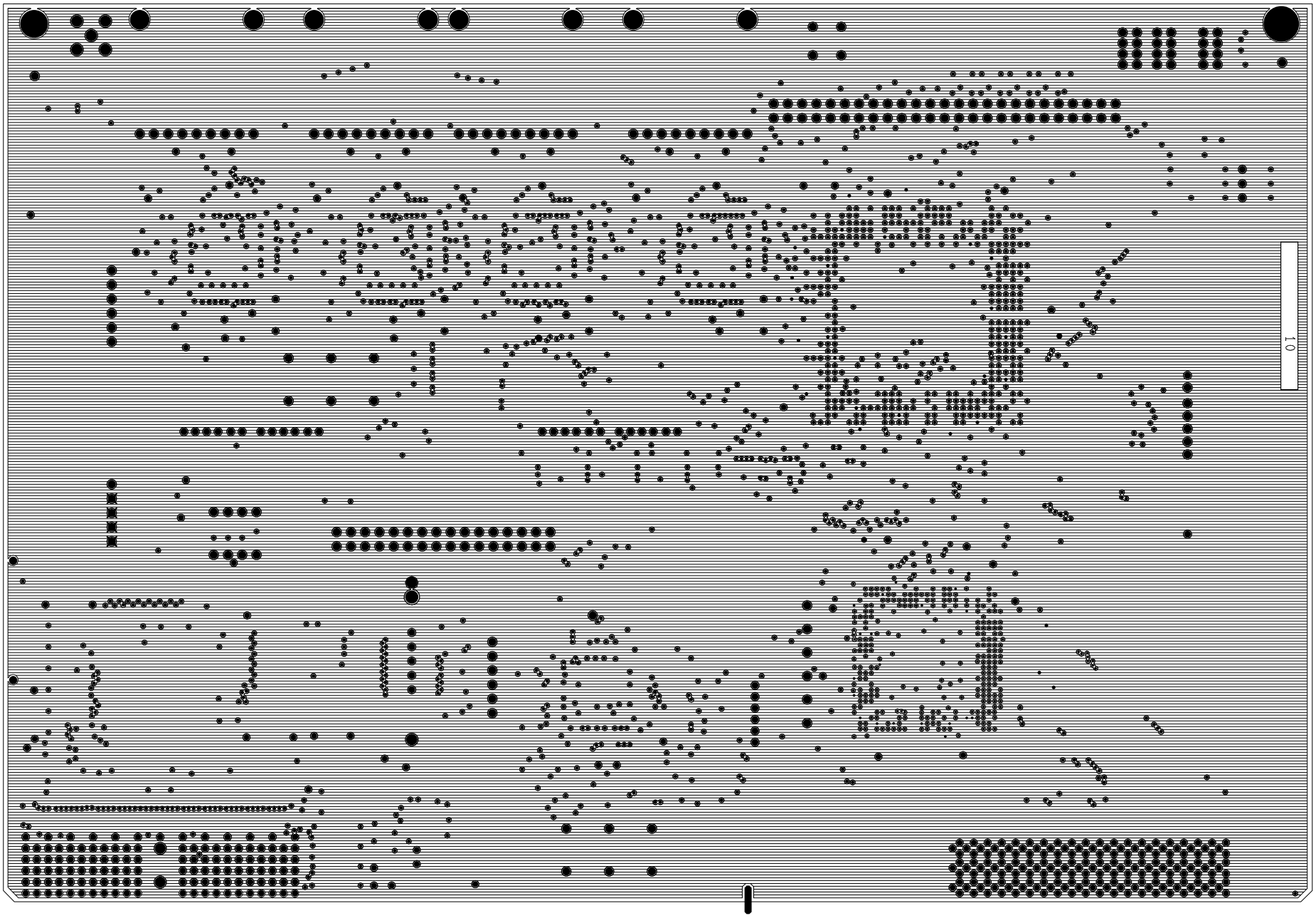
NO.	Manufacturer Part Number	Ref Des	Qty	Descriptions
		R135, R139, R148, R153, R155, R163, R180, R183		
32	PANASONIC ERJ-6GEYJ240V	R11_1	1	RES-24, 5%, 805
33	PANASONIC ERJ-3EKF63R4V	R11_2	1	RES-63.4, 1%, 603
34	PANASONIC ERJ-3GSY0R00V	R111-R116, R175-R178	10	RES-0, 5%, 603
35	PANASONIC ERJ-3EKF1500V	R12_1	1	RES-150, 1%, 603
36	PANASONIC ERJ-3GSYJ561V	R12_2, R13_2, R289	3	RES-560, 5%, 603
37	PANASONIC ERJ-3GSYJ222V	R13_1	1	RES-2.2K, 5%, 603
38	PANASONIC ERJ-3GSYJ472V	R14_1, R15_1, R7, R9, R20, R23, R25, R45, R47, R67, R68, R72, R77, R131-R134, R137, R138, R140-R146, R262, R7_1, R7_2	29	RES-4.7K, 5%, 603
39	VISHAY WSL2512-R01-1	R14_2, R15_2, R5_2	3	RES-0.01, 1%, 2512
40	PANASONIC ERJ-3GSYJ681V	R156, R161, R162	3	RES-680, 5%, 603
41	PANASONIC ERJ-3GSYJ100V	R159, R168, R179, R181, R194, R195, R198, R199, R6_2, R8_2	10	RES-10, 5%, 603
42	PANASONIC ERJ-3EKF39R2V	R16_1	1	RES-39.2, 1%, 603
43	PANASONIC ERJ-3GSYJ104V	R16_2, R8_1	2	RES-100K, 5%, 603
44	PANASONIC ERJ-3EKF2671V	R160	1	RES-2.67K, 1%, 603
45	PANASONIC ERJ-3GSYJ221V	R171, R172, R186, R187, R189, R190, R192, R193	8	RES-220, 5%, 603
46	PANASONIC ERJ-3GSYJ202V	R174, R184, R197, R201, R3_2, R4_2	6	RES-2.0K, 5%, 603
47	PANASONIC ERJ-3EKF3010V	R18, R39, R56, R89	4	RES-301, 1%, 603
48	DIGI-KEY -- P<VALUE>GCT-ND	R185, R188, R191	3	RES-4.7K, 5%, 603
49	PANASONIC ERJ-3GSYJ560V	R19	1	RES-56, 5%, 603
50	PANASONIC ERJ-3GSYJ4R7V	R1-R4, R117	5	RES-4.7, 5%, 603
51	PANASONIC ERJ-3GSYJ122V	R2_2	1	RES-1.2K, 5%, 603
52	DIGI-KEY -- P<VALUE>GCT-ND	R263, R290, R291	3	RES-56, 5%, 603
53	PANASONIC ERJ-3GSYJ2R2V	R34, R57, R58, R60, R62, R65, R66, R90, R91, R108-R110, R150	13	RES-2.2, 5%, 603
54	PANASONIC ERJ-3EKF82R5V	R35, R59, R75, R94, R96, R98, R104, R106	8	RES-82.5, 1%, 603
55	PANASONIC ERJ-3EKF1300V	R36, R71, R78, R95, R97, R101, R105, R107	8	RES-130, 1%, 603
56	PANASONIC ERJ-3EKF49R9V	R37, R127-R129, R164-R167, R169, R297-R301	14	RES-49.9, 1%, 603
57	PANASONIC ERJ-3EKF3161V	R5	1	RES-3.16K, 1%, 603
58	PANASONIC ERJ-3GSYJ101V	R6, R8, R24, R26, R29, R44, R46, R69, R74, R88, R125, R149, R157	13	RES-100, 5%, 603
59	DIGI-KEY -- P<VALUE>ACT-ND	R61	1	RES-680, 5%, 805

NO.	Manufacturer Part Number	Ref Des	Qty	Descriptions
60	PANASONIC ERJ-3GSYJ152V	R99, R170, R182, R196, R200	5	RES-1.5K, 5%, 603
61	PANASONIC -- EXB-V8V472JV	RN1, RN16_1, RN1_1, RN2, RN2_1, RN3, RN3_1, RN4, RN4_1, RN5, RN5_1, RN6-RN8	14	RES_ARRAY_4_SMD-4.7K
62	PANASONIC -- EXB-V8V100JV	RN10_1, RN11_1, RN12_1, RN13_1, RN14_1, RN17_1, RN18_1, RN19_1, RN20_1, RN21_1, RN7_1, RN8_1, RN9_1	13	RES_ARRAY_4_SMD-10
63	PANASONIC -- EXB-V8V102JV	RN15_1, RN6_1	2	RES_ARRAY_4_SMD-1K
64	PANASONIC -- EXB-V8V103JV	RN22_1, RN23_1, RN24_1, RN25_1, RN26_1, RN27_1, RN28_1, RN29_1, RN30_1, RN31_1, RN32_1, RN33_1, RN34_1	13	RES_ARRAY_4_SMD-10K
65	DIGI-KEY -- Y4<VALUE CODE>-ND	RN9, RN10	2	RES_ARRAY_4_SMD-150
66	DIGIKEY -- CKN4002-ND	SW1	1	RIGHT ANGLE PCB MOUNT SPST PUSH BUTTOM, CK_TP11
67	TEST POINT	TP1-TP32	32	TEST POINT THRU-HOLE PAD50CIR32D
68	TEST POINT	TP33-TP45	13	TEST POINT THRU-HOLE PAD60CIR36D
69	FAIRCHILD SEMI MM74HC08M	U1	1	IC QUAD 2 IN AND GATE SOIC14 NARROW BODY, VCC =3_3V
70	MILL MAX 614-93-308-31-012	U1_1	1	SOCKET FOR PART# NM93CS66LEN, DIP8_SOCKET
71	IPD CONVERTERS SIE501.8R	U1_2	1	REGULATOR 5.0V TO 1.8V 6A, 100MV MAX RIPPLE CONVERTER, SIP_DC_DC_90 -1
72	MOTOROLA MC74HC244ADW	U10	1	IC OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER SO20WB 3V
73	PMC SIERRA PM5310	U11	1	IC TELECOMBUS SERIALIZER, PBGA352
74	PERICOM PI6C2502W	U13, U15, U17, U19	4	IC PHASE LOCKED LOOP CLOCK DRIVER, SOIC8
75	TRIQUINT SEMICONDUCTO R TQ8106	U14, U16, U18, U20	4	IC SONET/SDH TRANSCEIVER W/ CDR, TQFP100
76	PERICOM PI49FCT3805CQ	U2	1	IC 3.3V 2X1:5 CMOS CLOCK DRIVER SPEED-GRADE-C QSOP20
77	PLX TECHNOLOGY PCI9054-AB50PI	U2_1	1	IC PCI-TO-LOCAL BUS, QFP176

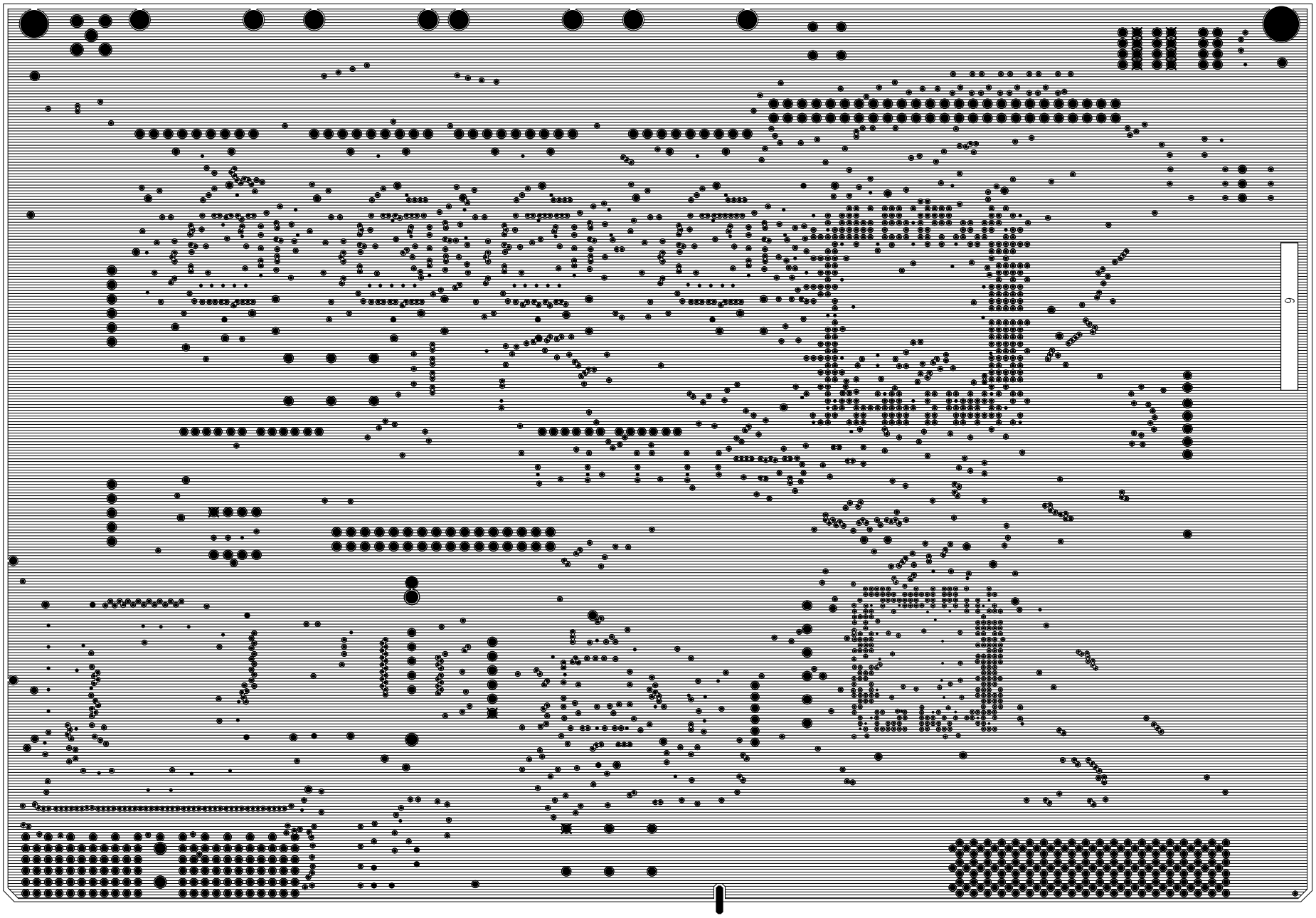
NO.	Manufacturer Part Number	Ref Des	Qty	Descriptions
78	LINEAR TECHNOLOGY LTC1643LCGN	U2_2	1	IC CPCI HOT SWAP CONTROLLER, SSOP16
79	MC100ELT22	U23	1	100ELT22_SOIC-BASE-V CC=5V
80	MAXIM MAX811TEUS-T	U25	1	IC 4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.08V SOT143
81	MOTOROLA SEMICONDUCTO R MC100EPT23D	U3	1	IC DUAL PECL/TTL TRNSLTR. 3.3V, SOIC8
82	LINEAR TECHNOLOGIES LT1117CST	U3_1	1	REGULATOR ADJUSTABLE SOT223 800MA OUTPUT
83	MAXIM MAX812REUS-T	U3_2	1	IC VOLTAGE MONITOR WITH MANUAL RESET INPUT 2.63V SOT143
84	PMC SIERRA PM5315	U4	1	IC SONET/SDH PAYLOAD EXTRACTOR/ALIGNER FOR 2488 MBIT/SEC, QUAD-STS 12-STM4, SBGA520
85	TI SN74AHC1G08DCKR	U5	1	IC SINGLE 2-INPUT POSITIVE AND GATE, MO-203
86	MOTOROLA MC100EL14DW	U6	1	MC100EL14_SOIC-BASE, IC LOW SKEW 1:5 CLOCK DISTRIBUTION CHIP, SO20WB
87	XILINX XC9572XL-10TQ100I	U7	1	XC9572XL-TQ10- CPLD, 10NS, 3.3V, TQFP100
88	SIEMENS V23826-H18-C363	U8, U9, U12, U21	4	3.3V DC/DC SINGLE MODE 1300NM 622MBD 1X9 TRANSCEIVER, LCD-PMD-SOCK ET
89	CONNOR WINFIELD -- EE13-541	Y1	1	77.76 MHZ, LVPECL OSCILLATOR, 20 PPM, 5V
90	MMD COMPONENTS MB3100H-77.76MHZ	Y3	1	OSC HCMOS/TTL HALF SIZE 8 PIN 77.76MHZ 100PPM

11 LAYOUT

1V8_PLANE

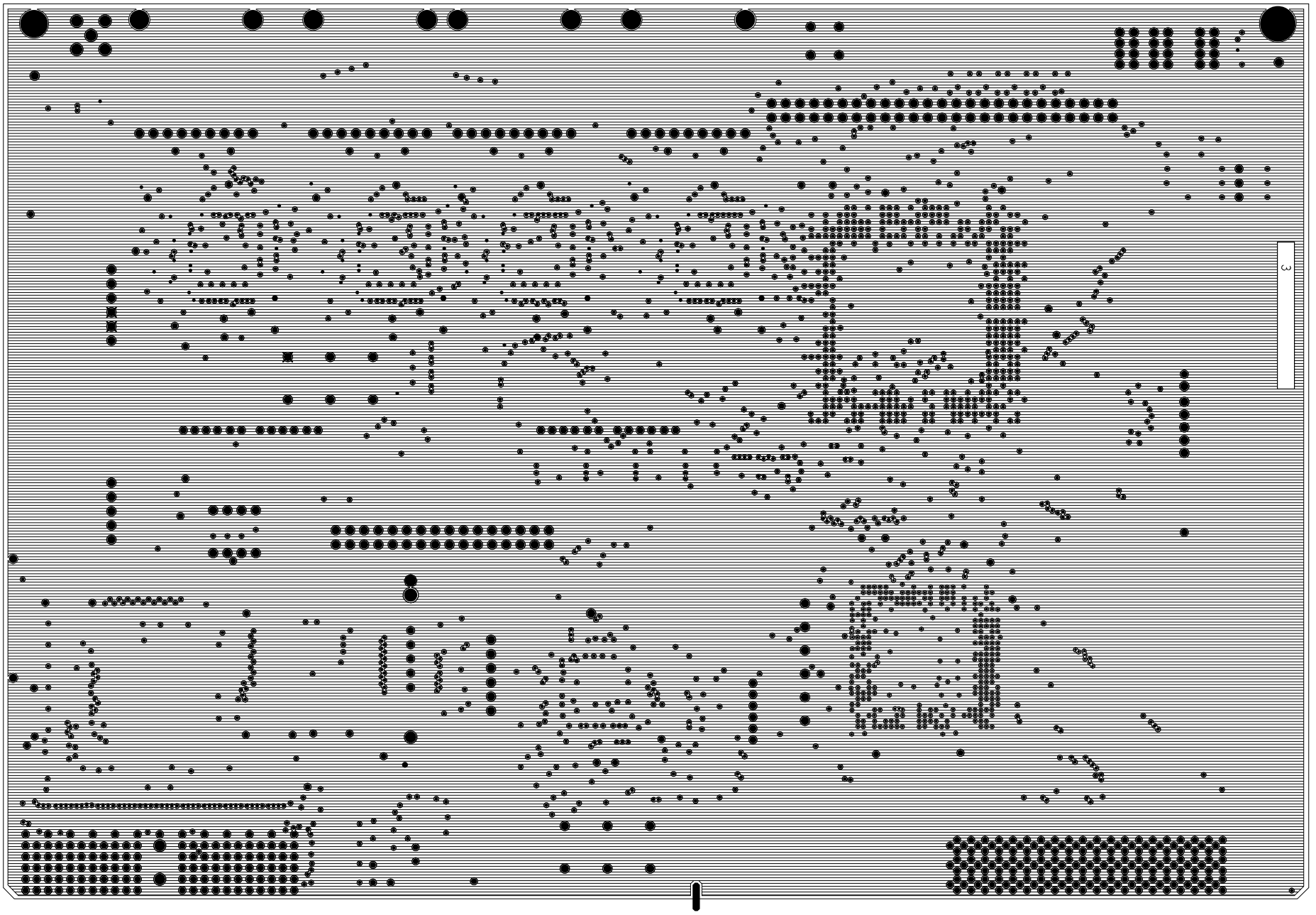


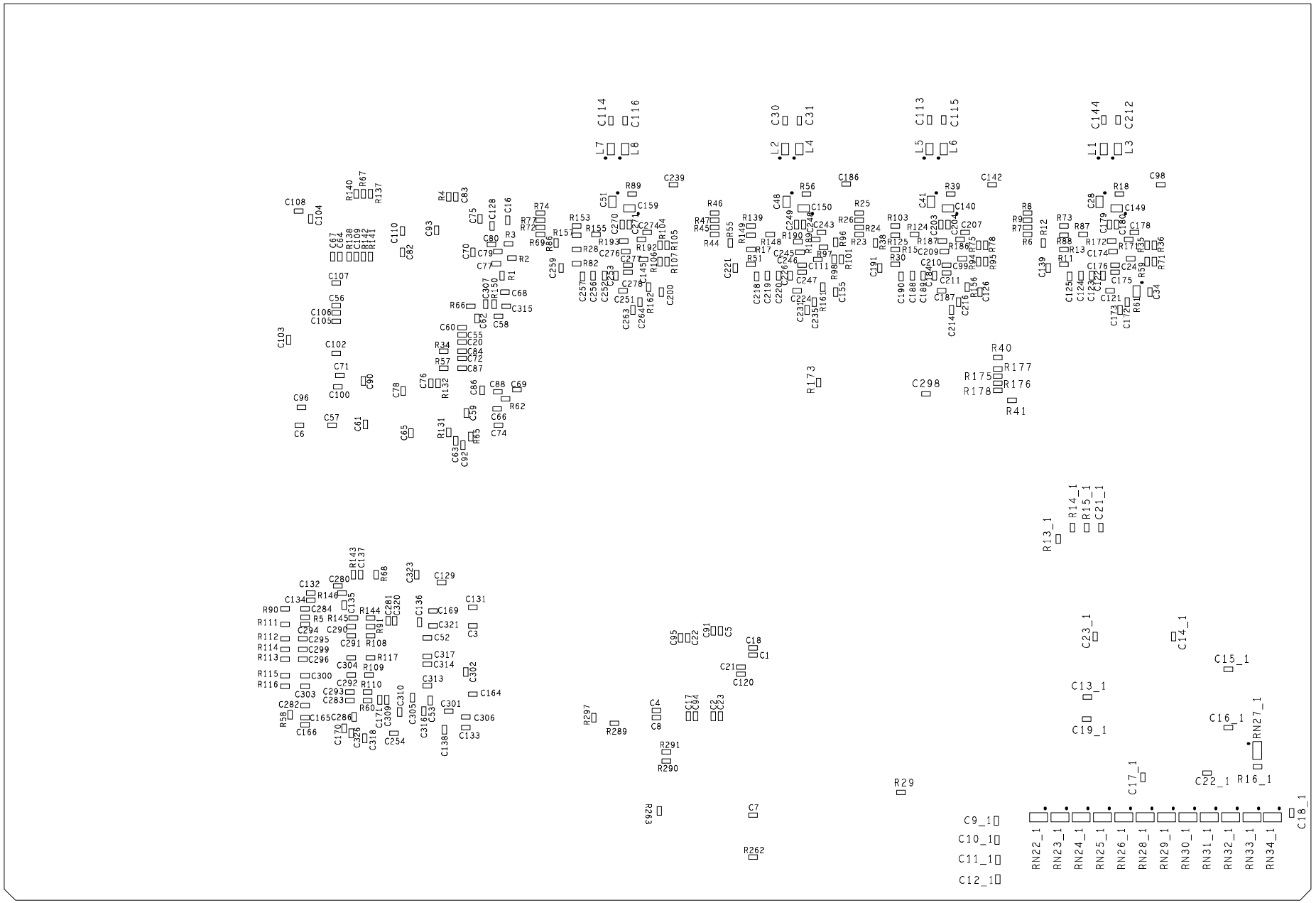
3V3_PLANE

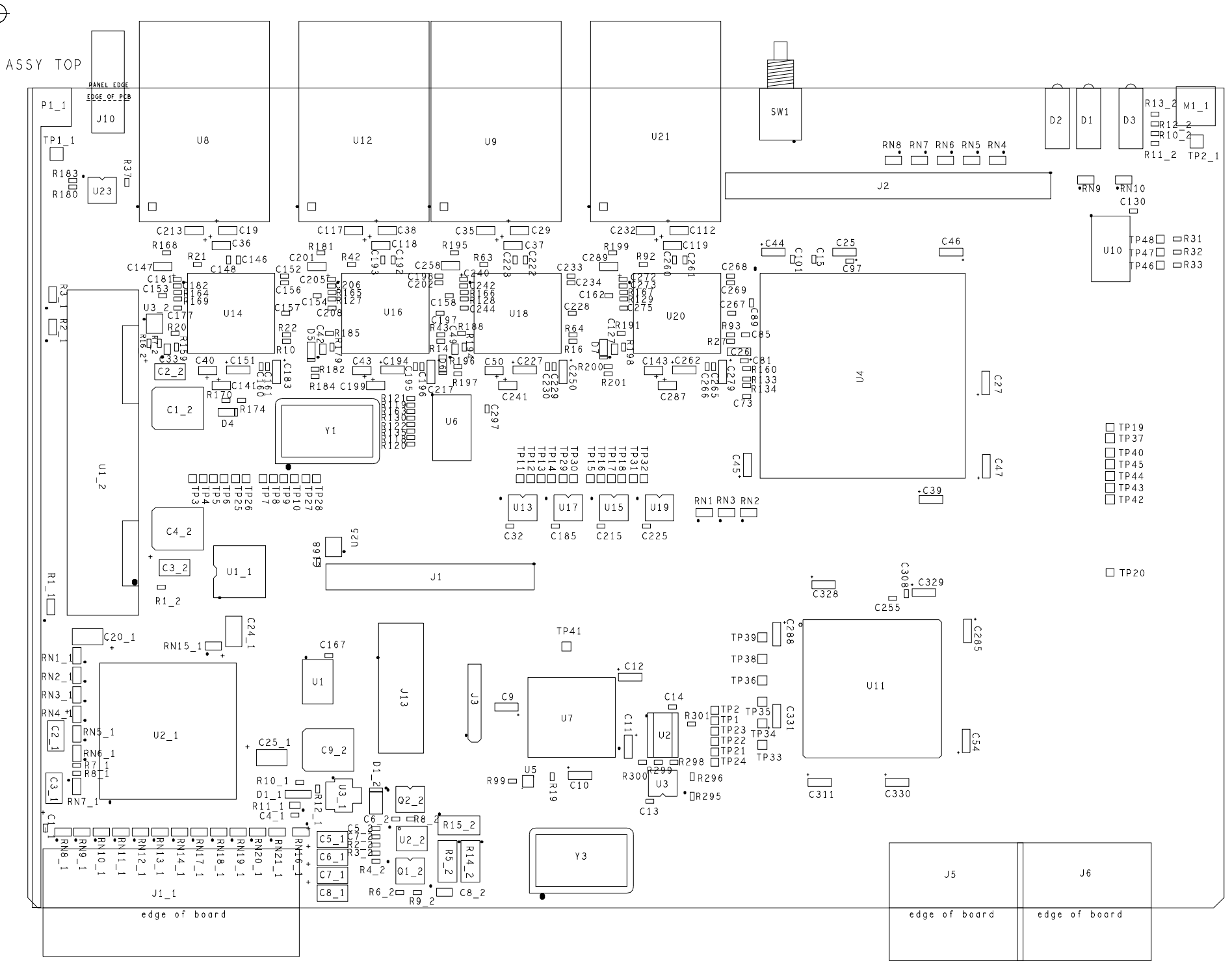


PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000

5V_PLANE







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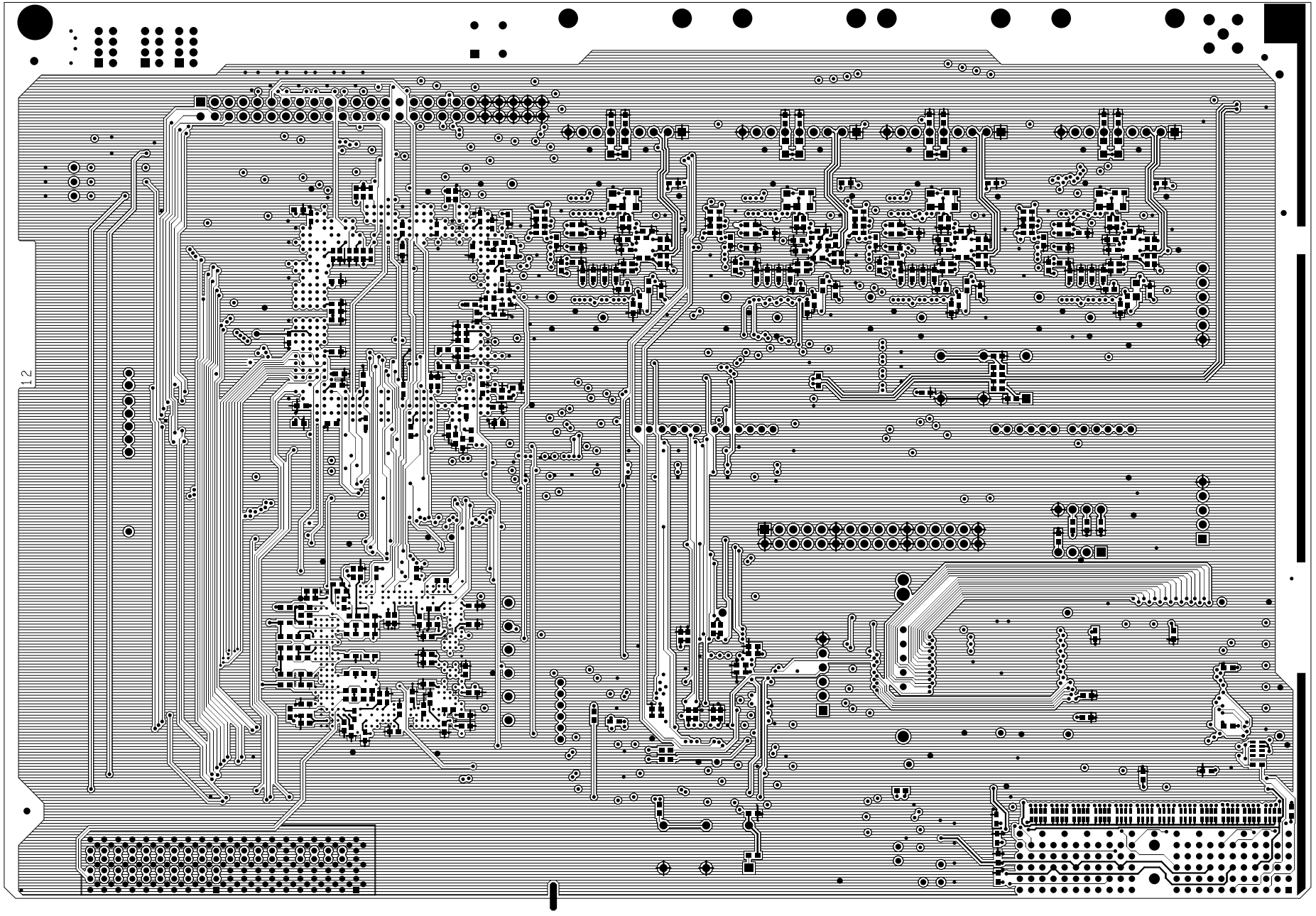
BOTTOM LAYER



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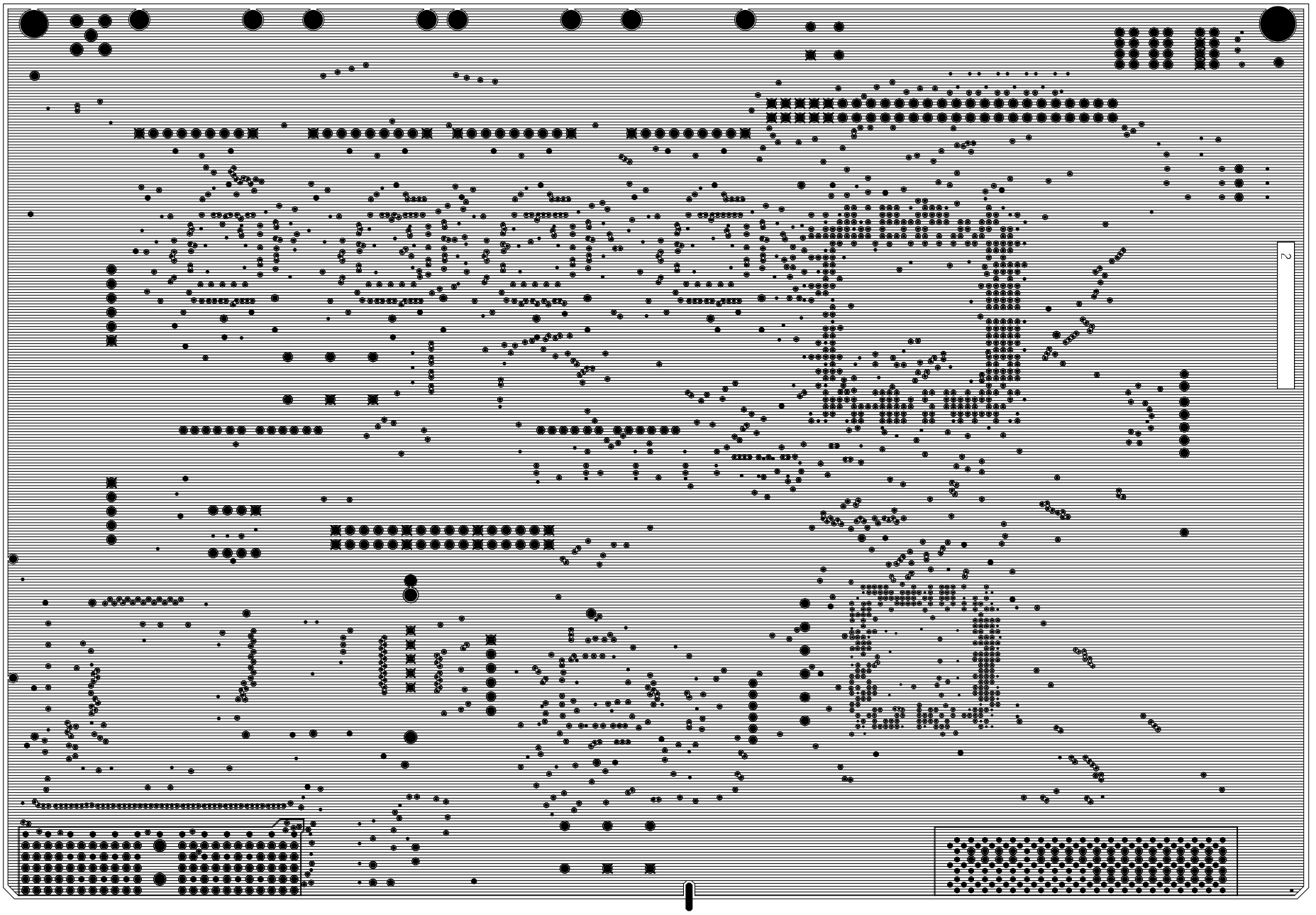
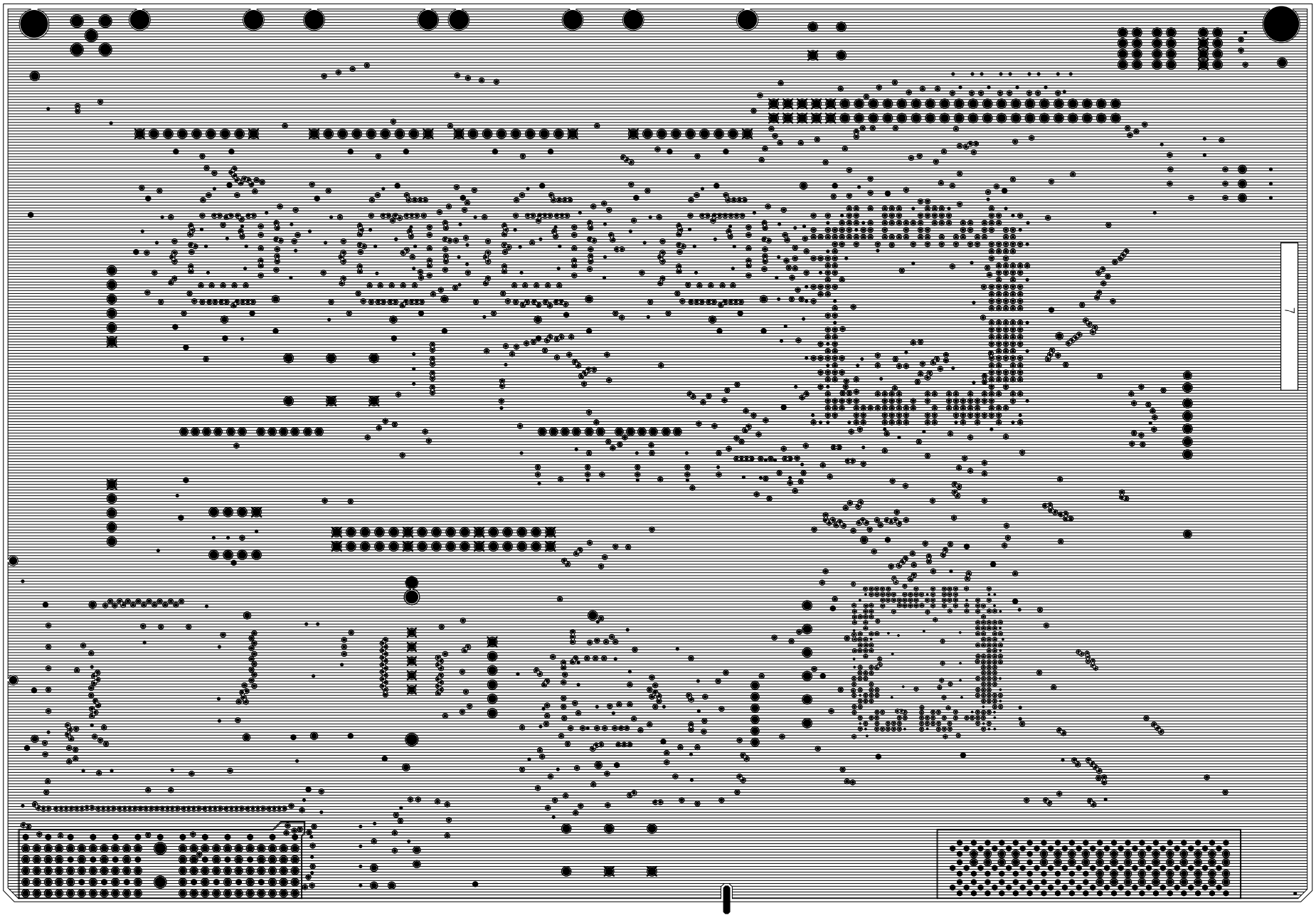
GND_PLANE

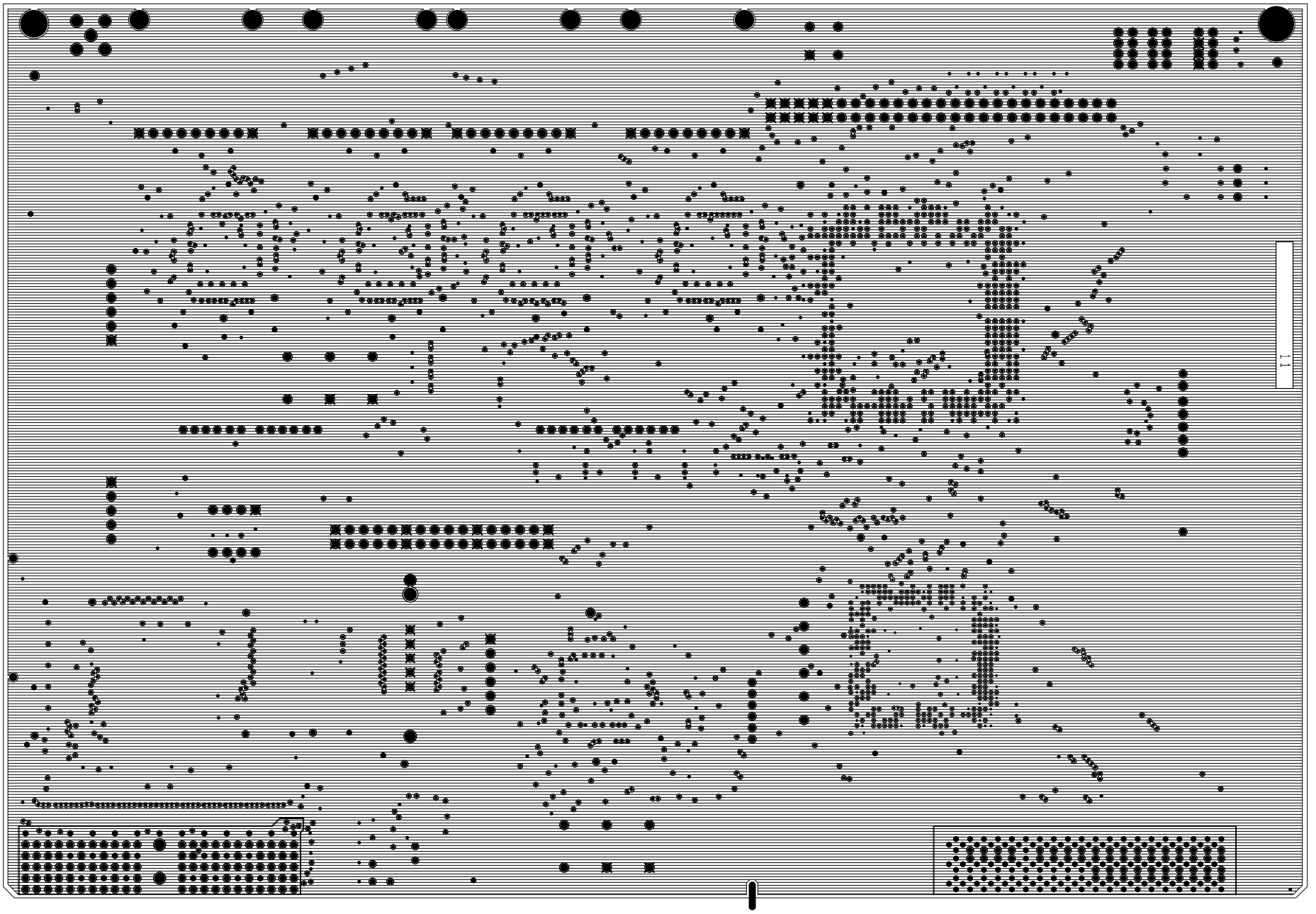


PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000

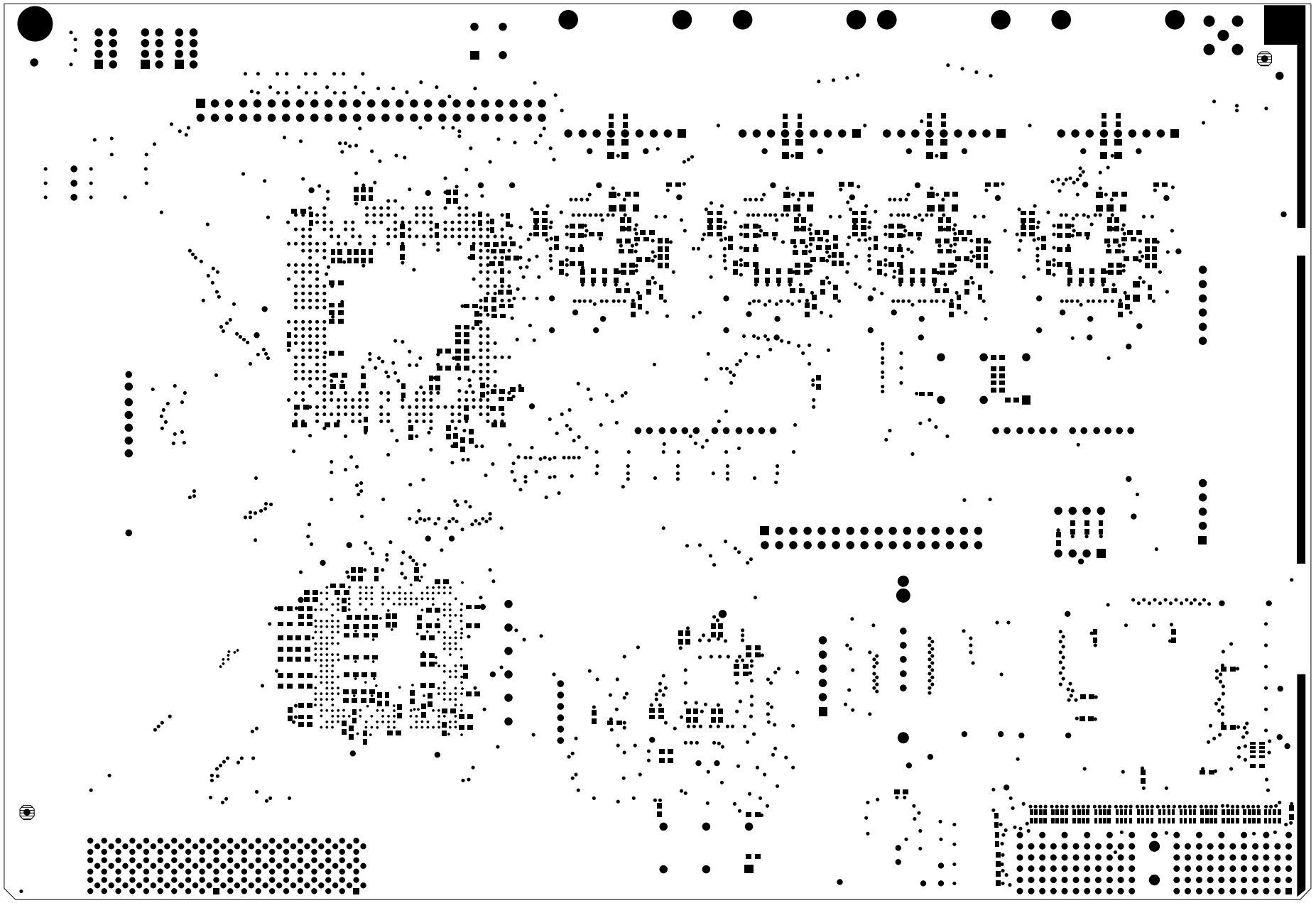
GND2_ PLANE



PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000



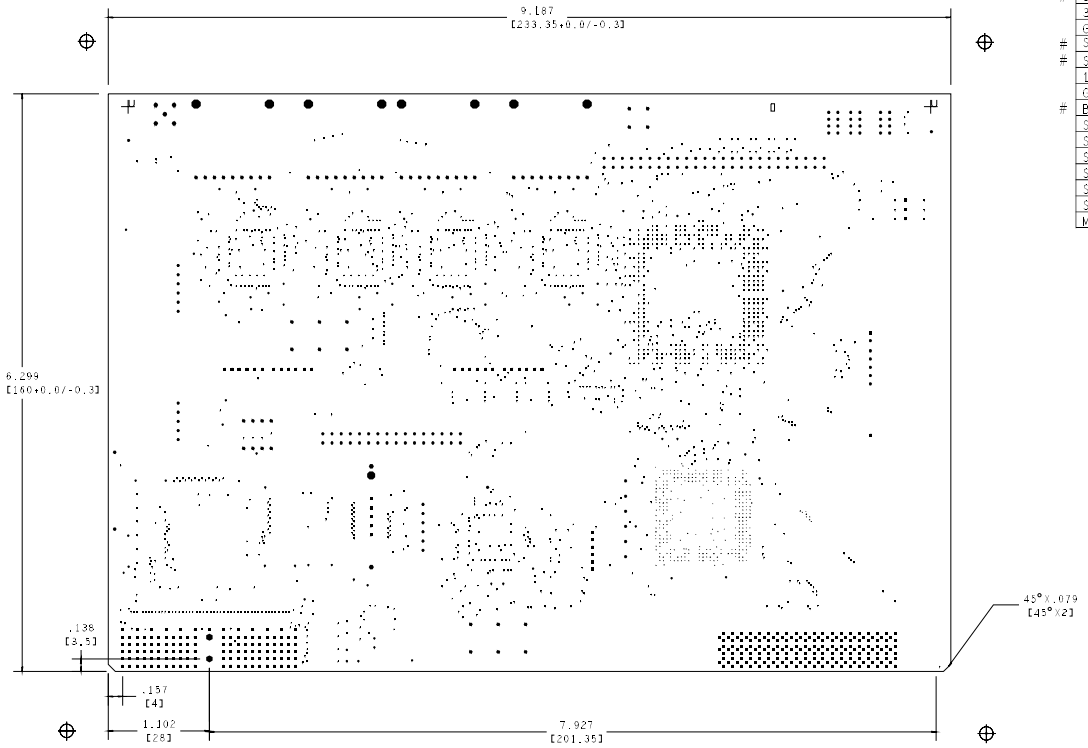
SOLDERMASK BOTTOM



REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED

	ARTWORK FILM
#	TOP LAYER
	GND_PLANE
	5V_PLANE
#	SIG1 LAYER
#	SIG2 LAYER
	3V3_PLANE
	GND2_PLANE
#	SIG3 LAYER
#	SIG4 LAYER
	1V8_PLANE
	GND3_PLANE
#	BOTTOM LAYER
	SILKSCREEN TOP
	SILKSCREEN BOTTOM
	SOLDER MASK TOP
	SOLDER MASK BOTTOM
	SOLDER PASTE TOP
	SOLDER PASTE BOTTOM
	MECH DRAWING

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	4 mil	4.5
COPPER	CONDUCTOR	5V_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	10 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	10 mil	4.5
COPPER	CONDUCTOR	3V3_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	4 mil	4.5
COPPER	CONDUCTOR	GND2_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	10 mil	4.5
COPPER	CONDUCTOR	SIG3	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	6 mil	4.5
COPPER	CONDUCTOR	SIG4	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	10 mil	4.5
COPPER	CONDUCTOR	1V8_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	4 mil	4.5
COPPER	CONDUCTOR	GND3_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------



PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	8.0	PLATED	289
·	13.0	PLATED	1607
·	25.0	PLATED	81
·	25.0	PLATED	180
·	26.0	PLATED	123
·	32.0	PLATED	40
·	36.0	PLATED	138
·	39.37	PLATED	2
·	42.0	PLATED	60
·	52.0	PLATED	5
·	55.0	PLATED	2
●	108.0	PLATED	8
⊕	149.606	PLATED	1
⊕	150.0	PLATED	1
·	78.74	NOT PLATED	2
●	94.0	NOT PLATED	1

NOTES:

1. COPPER THICKNESS IS 1/2 OZ ON OUTER LAYER AND 1 OZ ON INNER LAYERS, UNLESS OTHERWISE STATED.
2. TOTAL THICKNESS OF BOARD SHALL BE 90 MIL+/- 7 MIL.
3. MATERIAL: FR4 WITH IMMERSION GOLD SURFACE FINISH.
4. THE OUTLINE DIMENSION ARE SPECIFIED ON THIS DRAWING.
5. ALL HOLES SHALL HAVE 1 MIL MINIMUM COPPER WALL THICKNESS.
6. SOLDER MASK MATERIAL: LIGHT GREEN LIQUID PHOTOIMAGEABLE.
7. DIELECTRIC CONSTANT: SEE BOARD MATERIAL DETAILS ABOVE.
8. SILKSCREEN SHALL BE SCREENED IN MONOCONDUCTIVE WHITE BASE INK AND MUST BE CLIPPED AWAY FROM SOLDER PADS/VIAS.
9. MAXIMUM WARP AND TWIST OF FINISHED PCB SHALL NOT EXCEED 0.010 IN/IN PER IPC-D-300.
10. ALL MATERIAL COMPRISING THE PCB MUST BE RECOGNIZED BY UL TO THE 94V-0 RATING.
11. TEARDROPS MAY BE ADDED FOR INNER LAYER VIAS FOR MANUFACTUREABLITY IF NECESSARY.
12. UNFUNCTIONAL INNER LAYERS VIAS/PADS HAVE TO BE REMOVED FOR MANUFACTUREABILITY.

CAUTION

13. PLATED HOLES MARKED WITH SQUARE R & P SHOULD BE 0.026" WITH 0.004"/-0.0" TOLERANCE.
14. TRACE WIDTH 9 MIL ARE 50 OHM +/-10% CONTROLLED IMPEDANCE.
    TRACE WIDTH 5 MIL ARE 65 OHM +/-10% CONTROLLED IMPEDANCE.

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON;				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				
DOC# PMC-990474				
DOC ISSUE# 2				
REV # 2.0				
DATE:FEB 2000				

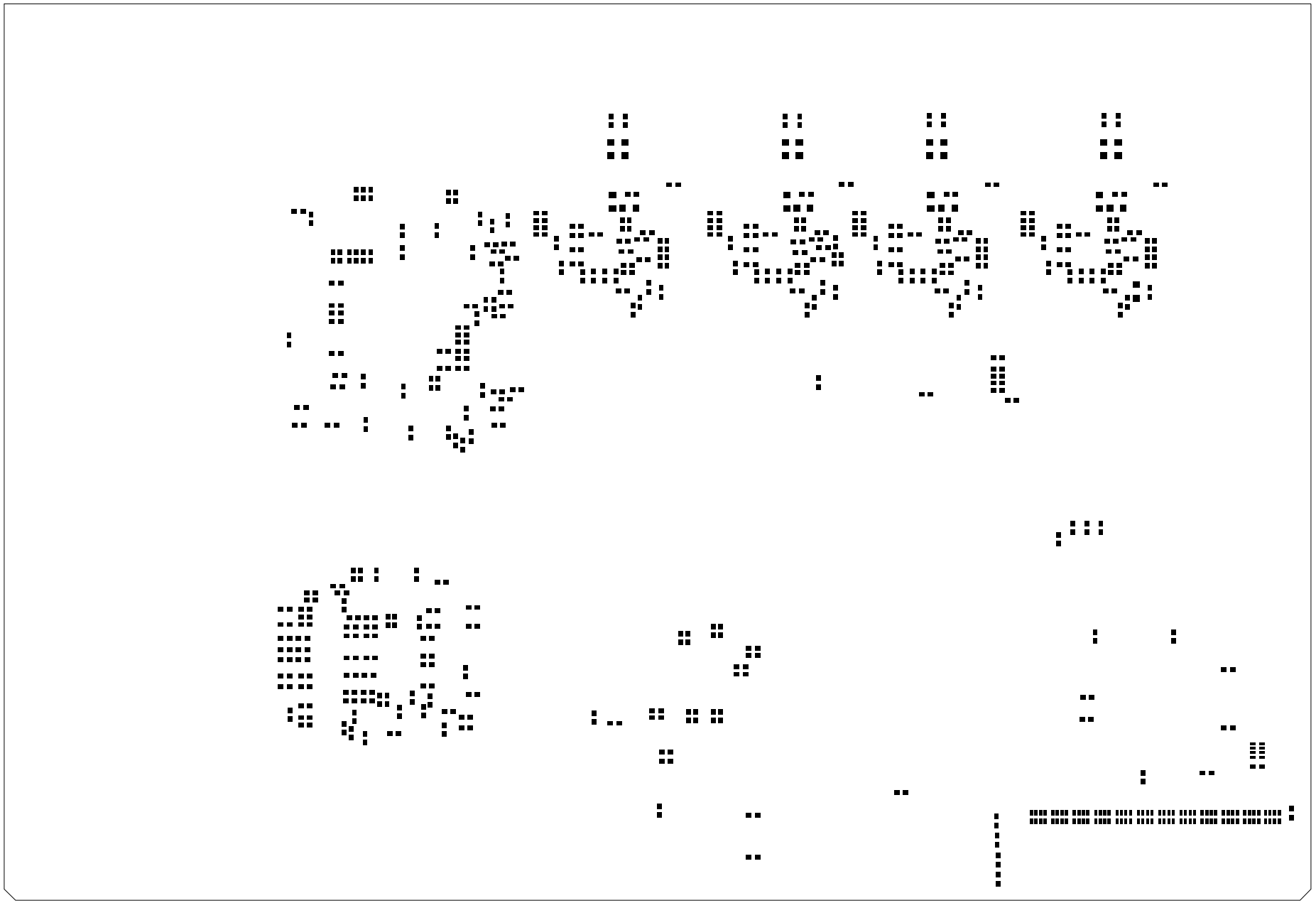
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

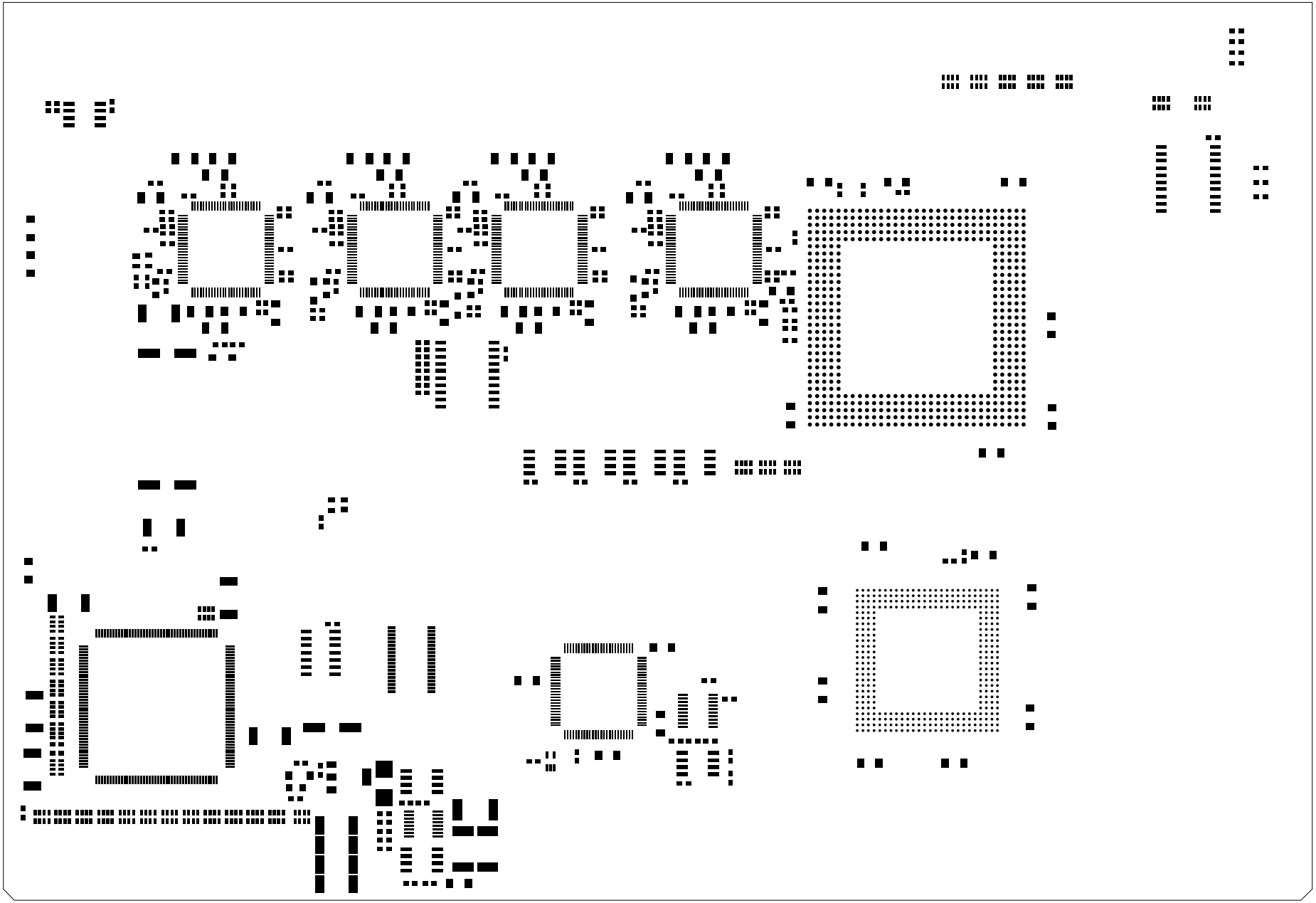
Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

PASTEMASK BOTTOM



PASTEMASK TOP



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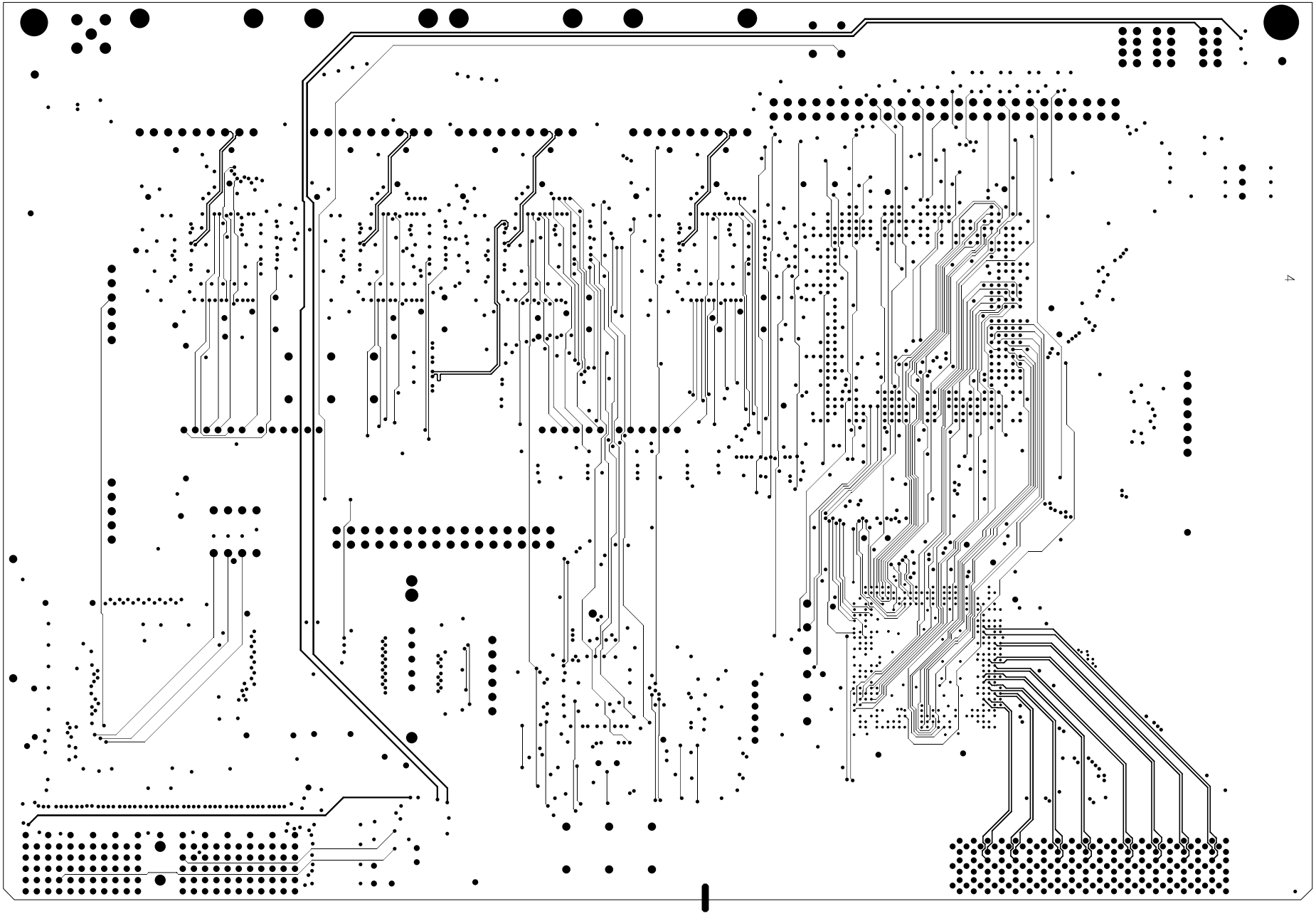
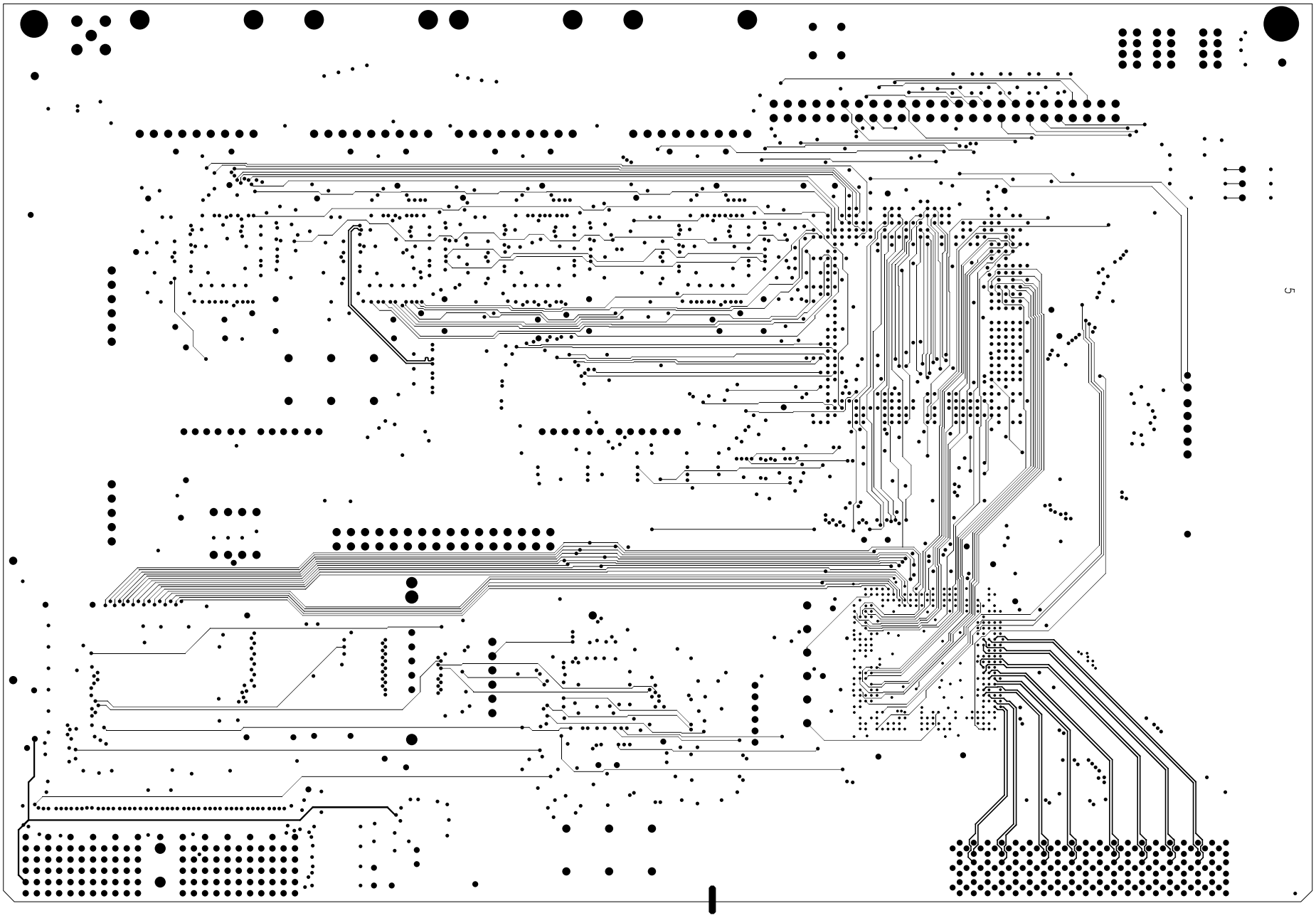
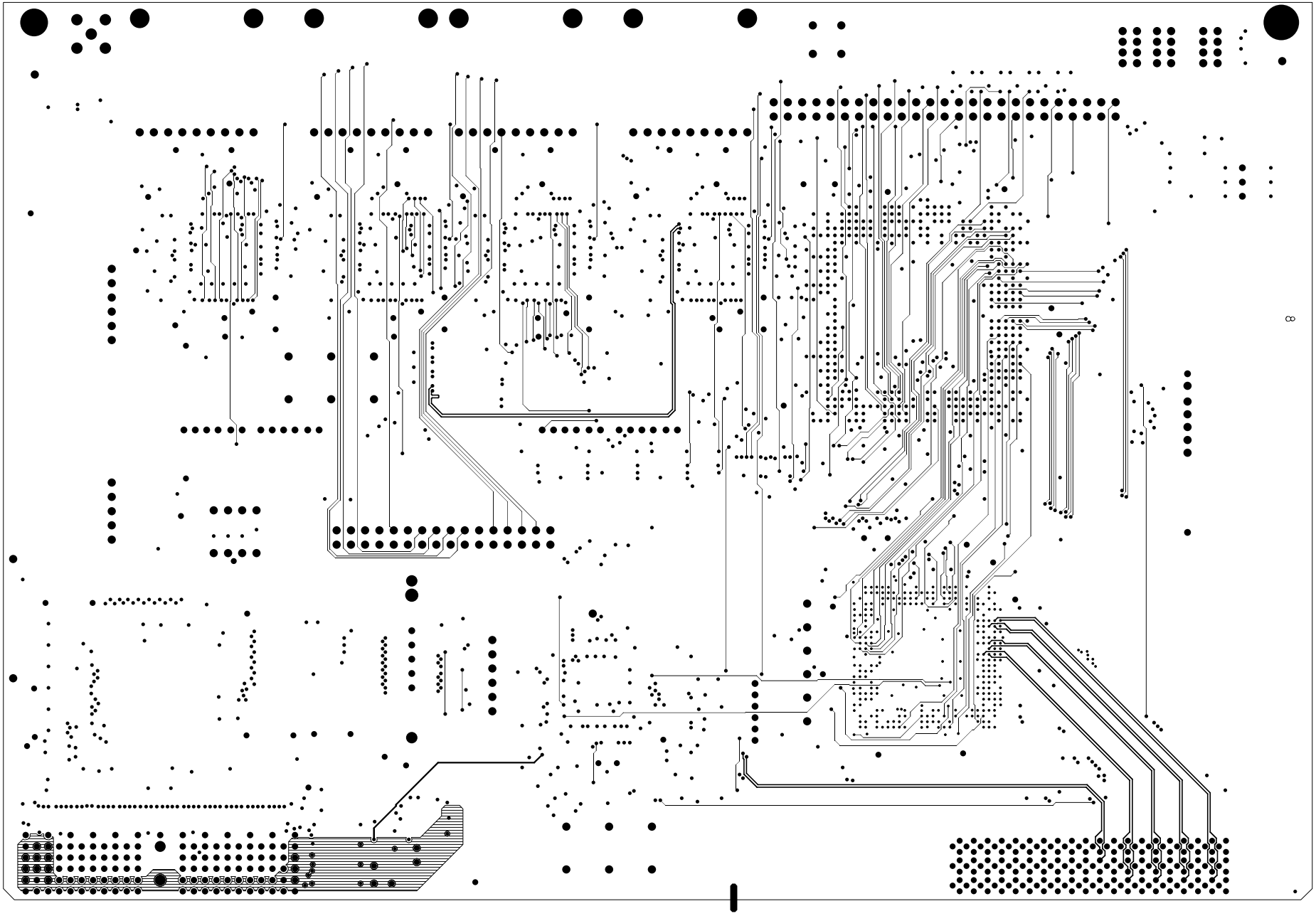
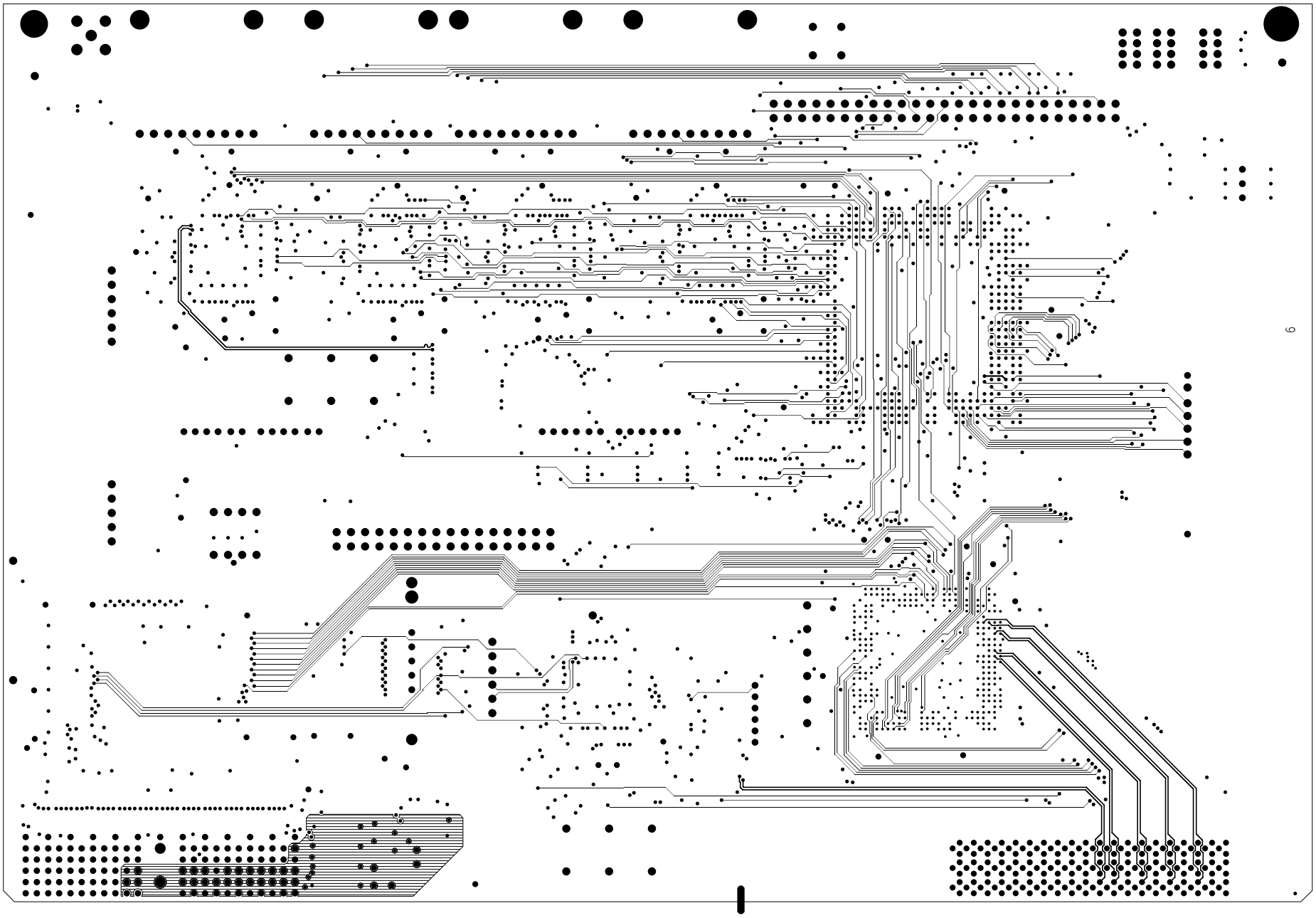
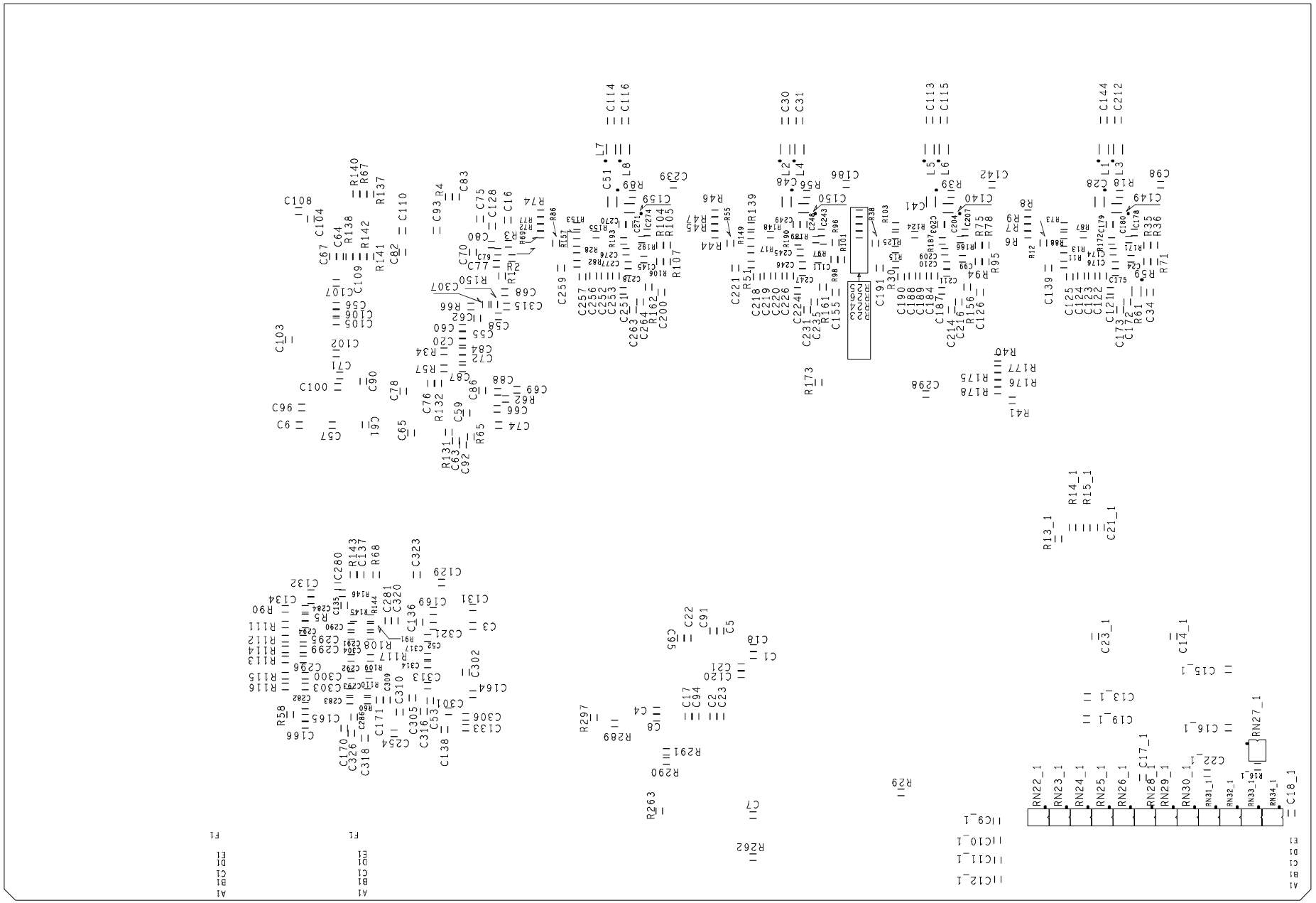


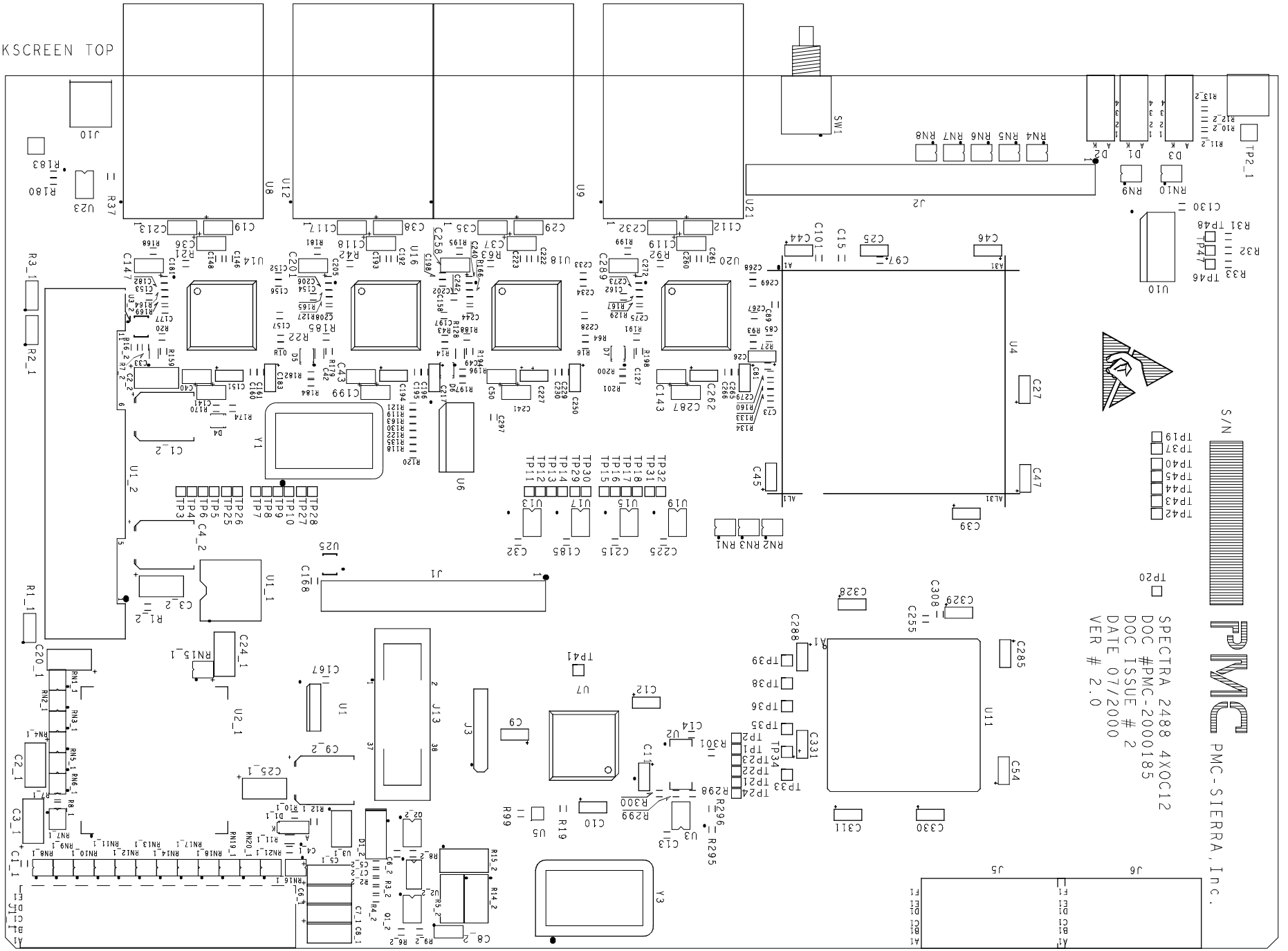






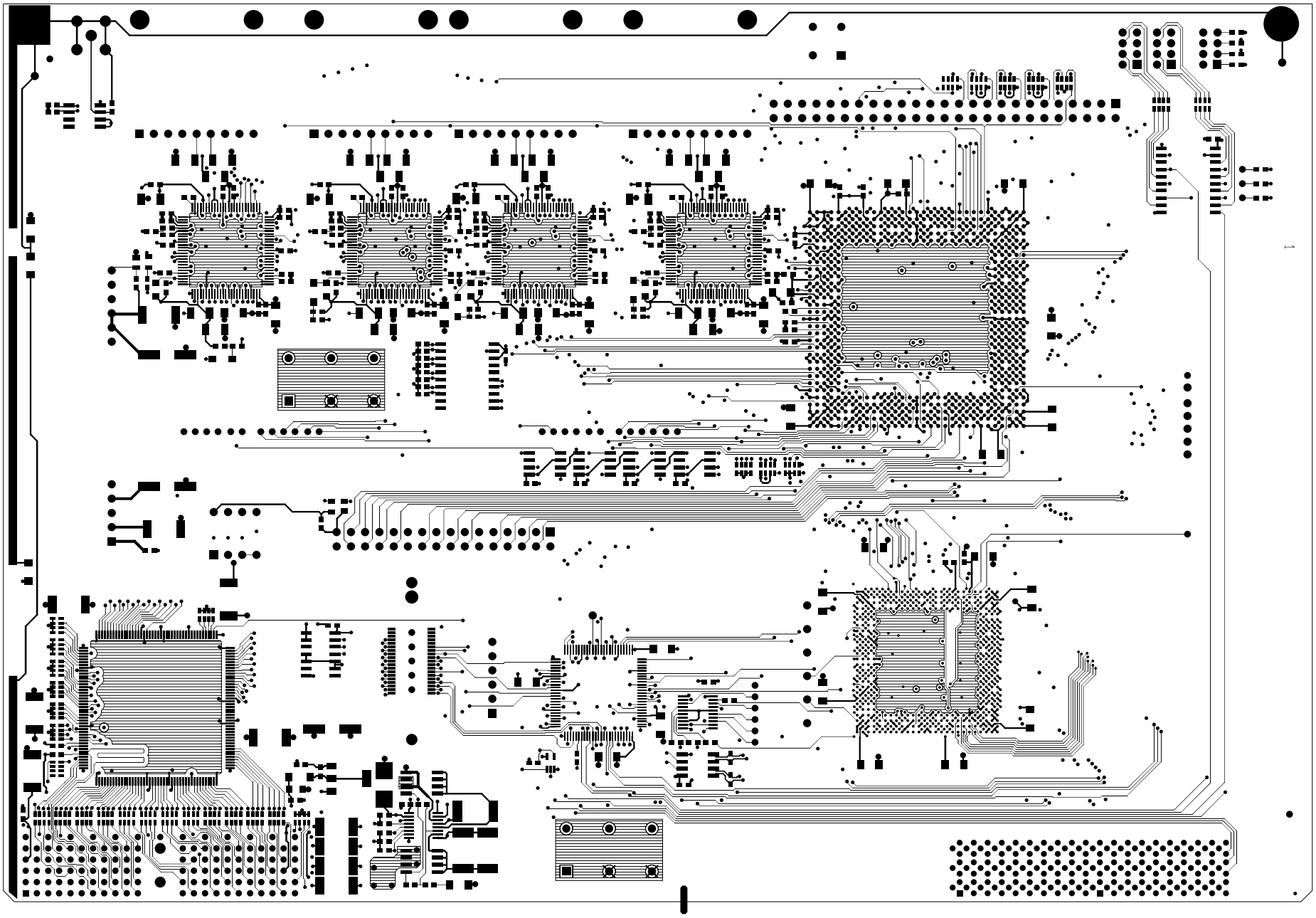


SILKSCREEN TOP



PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000

TOP LAYER



PMC-SIERRA SPECTRA 2488 4XOC12 REV. 2.0 2000

NOTES

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