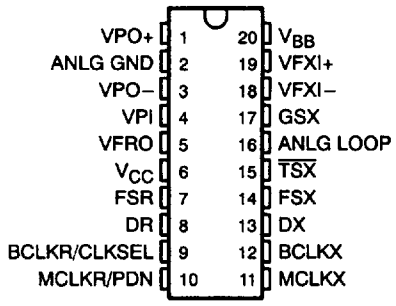
TP3064A, TP3067A, TP13064A, TP13067A
MONOLITHIC SERIAL INTERFACE COMBINED PCM CODEC AND FILTER

D4050, SEPTEMBER 1992

- **Complete PCM CODEC and Filtering System Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With Sin x/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **μ-Law – TP13064A and TP3064A**
- **A-Law – TP13067A and TP3067A**
- **Meets or Exceeds All D3/D4 Channel Bank Transmission and CCITT G.711 Specifications**
- **±5-V Operation**
- **Low Operating Power . . . 70 mV Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**
- **Improved Versions of National Semiconductor TP3064, TP3067, TP3064-X, and TP3067-X**

DW, J, OR N PACKAGE
(TOP VIEW)



description

The TP3064A, TP3067A, TP13604A, and TP13607A are comprised of a single-chip pulse-code modulated encoder and decoder (PCM CODEC) and PCM line filter. These devices provide all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are pin-for-pin compatible with the National Semiconductor TP3064 and TP3067, respectively. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital encryption systems
- Digital voice-band data storage
- Digital signal processing

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

TP3064A, TP3067A, TP13064A, TP13067A
MONOLITHIC SERIAL INTERFACE
COMBINED PCM CODEC AND FILTER

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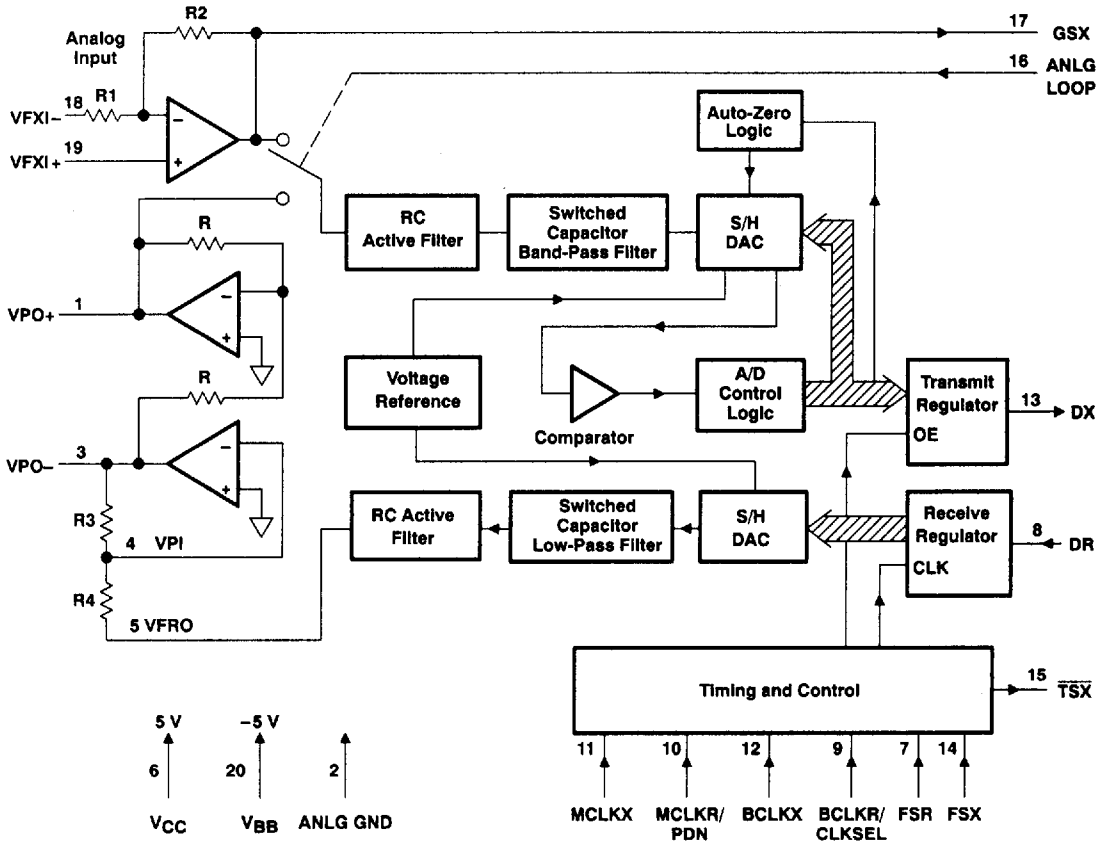
description (continued)

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated (PCM) system. They are intended to be used at the analog termination of a PCM line or trunk. The devices require two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses.

The TP3064A, TP3067A, TP13064A, and TP13067A provide the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones.

The TP13064A and TP13067A are characterized for operation from −40°C to 85°C. The TP3064A and TP3067A are characterized for operation from 0°C to 70°C.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
ANLG LOOP	16	Analog loopback control input. Must be set to logic low for normal operation. When pulled to logic high, the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO+ output of the receive power amplifier.
BCLKR/CLKSEL	9	The bit clock that shifts data into DR after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	12	The bit clock that shifts out the PCM data on DX. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	8	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	13	The 3-state PCM data output that is enabled by FSX.
FSR	7	Receive frame sync pulse input that enables BCLKR to shift PCM data in RD. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
FSX	14	Transmit frame sync pulse that enables BCLKX to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
GND	2	Analog ground. All signals are referenced to this pin.
GSX	17	Analog output of the transmit input amplifier. Used to externally set gain.
MCLKR/PDN	10	Receive master clock. Must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. May be synchronous with MCLKX, but should be synchronous for best performance. When MCLKX is connected continuously low, MCLKX is selected for all internal timing. When MCLKX is connected continuously high, the device is powered down.
MCLKX	11	Transmit master clock. Must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. May be asynchronous with MCLKR.
$\overline{TSX}$	15	Open-drain output that pulses low during the encoder time slot.
V_{BB}	20	Negative power supply. $V_{BB} = -5$ V ± 5%.
V_{CC}	6	Positive power supply. $V_{CC} = 5$ V ± 5%.
VFRO	5	Analog output of the receive filter
VFXI+	19	Noninverting input of the transmit input amplifier
VFXI−	18	Inverting input of the transmit input amplifier
VPI	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
VPO+	1	The noninverted output of the receive power amplifier
VPO−	3	The inverted output of the receive power amplifier

power up

Power-on reset circuitry initializes the TP13064A, TP3064A, TP13067A, and TP3067A when power is first applied and places it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to the MCLKR/PDN pin powers up the device and activates all circuits. DX, a 3-state PCM data output, will remain in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX, and MCLKX is used for both the transmit and receive direction. MCLKR/PDN is also used as a power-down control; a low level on MCLKR powers up the device and a high level powers it down. In either case, MCLKX will be selected as the master clock for both receive and transmit direction. BLCLX must also have a bit clock applied to it. The selection of the proper internal divider for a master clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on the BCLKR/CLKSEL pin will select BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKX/CLKSEL. In the synchronous mode, BCLKLX may be in the range from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.

synchronous operation (continued)

The encoding cycle begins with each FSX pulse and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight-bit clock periods, the three-state DX output is returned to a high-impedance state. With an FSR pulse, PCM data is latched via the DR input on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

asynchronous operation

For asynchronous operation, separate transmit and receive clocks may be applied. MCLKX and MCLKR must be 2.048 MHz for the TP3064A and TP13064A, 1.536 MHz or 1.544 MHz for the TP3067A and TP13067A and need not be synchronous. However, for best performance, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This will connect MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device will compensate for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX, and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR may operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long, with timing relationships specified in Figure 1. With FSX high during a falling edge of BCKLX, the next rising edge of BCLKX enables the three-state output buffer, DX, which outputs the sign bits. The remaining seven bits are clocked out on the following seven rising edges and the next falling edge disables the DX output. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the seven remaining bits. The short-frame sync pulse may be utilized in either the synchronous or asynchronous mode.

Table 1. Selection of Master Clock Frequencies

BCLKR/CLKSEL	MASTER CLOCK FREQUENCY SELECTED	
	TP3064A, TP13064A	TP3067A, TP13067A
Clock Input	1.536 MHz or 1544 MHz	2.048 MHz
Logic Input L (sync mode only)	2.048 MHz	1.536 MHz or 1.544 MHz
Logic Input H (Open) (sync mode only)	1.536 MHz or 1.544 MHz	2.048 MHz

long-frame sync operation

Both FSX and FSR must be 3 or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device will detect whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next 7 rising edges of BCLKX edges clock out the remaining 7 bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables the DX output. A rising edge on FSR, the receive-frame sync pulse, will cause the PCM date at DR to be latched in on the next 8 falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse may be used in either the synchronous or asynchronous mode.

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. Gains in excess of 20 dB across the audio pass band are possible via low noise and wide bandwidth. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eight-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law (TP3064A and TP13064A) or A-law (TP3067A and TP13067A) coding conventions, the ADC is a companding type. A precision voltage reference provides a input overload of nominally 2.5-V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay will be approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder is μ-law (TP3064A and TP13064A) or A-law (TP3067A and TP13067A) and the fifth-order low-pass filter corrects for the sin x/x attenuation caused by the 8-kHz sample/hold. The filter is followed by a second-order RC active post-filter with its output at VFRO. The receive section is unity-gain but gain can be added by using the power amplifiers. At FSR, the data at the DR input is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame) or a total of approximately180 μs.

receive power amplifiers

Two inverting mode power amplifiers are provided for directly driving a match-line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5-V peak output signal from the receive filter up to the ±3.3-V peak into an unbalanced 300-Ω load, or ±4.0 V into an unbalanced 15-kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600-Ω subscriber line termination is obtained by differentially driving a balanced transformer with $\sqrt{2}$:1 turns ratio, as shown in Figure 3. A total peak power of 15.6 dBm can be delivered to the load plus termination.

ENCODING FORMAT AT DX OUTPUT

	TP3064A, TP13064A μ-Law	TP3067A, TP13067A A-Law (INCLUDES EVEN-BIT INVERSION)
V_I = + Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_I = 0	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_I = – Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Supply voltage, V_{BB} (see Note 1) ..... −7 V
Voltage range at any analog input or output ..... V_{CC} + 0.3 V to V_{BB} − 0.3 V
Voltage range at any digital input or output ..... V_{CC} + 0.3 V to GND − 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TP3064A, TP3067A ..... 0°C to 70°C
TP13064A, TP13067A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltages are with respect to GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.6	V
Common-mode input voltage range, V_{ICR}†				±2.5	V
Load resistance at GSX, R_L		10			kΩ
Load capacitance at GSX, C_L				50	pF
Operating free-air temperature, T_A	TP3064A, TP3067A	0		70	°C
	TP13064A, TP13067A	−40		85	

† Measure with CMRR > 60 dB.

electrical characteristics over power supply variations and recommended free-air temperature range (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	TP306_A			TP1306_A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	

‡ All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

electrical characteristics at V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = −3.2 mA	2.4			V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA			0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open			0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}			±10	μA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}			±10	μA
I_{OZ}	Output current in high-impedance state	DX	V_O = GND to V_{CC}			±10	μA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop, Unit gain		1	3	Ω
	Output dynamic range	GSX	R_L ≥ 10 kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI−				±20	mV
CMRR	Common-mode rejection ratio			60			dB
k_{SVR}	Supply voltage rejection ratio			60			dB

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with power amplifiers

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current		V_{PI} = −1 V to 1 V				±100	nA
r_i	Input resistance		V_{PI} = −1 V to 1 V		10			MΩ
r_o	Output resistance	VPO+ or VPO−	Inverting unity gain			1		Ω
A_V	Voltage amplification	VPO− or VPO+	VPO− = 1.77 Vrms, R_L = 600 Ω			−1		
B_I	Unity-gain bandwidth	VPO−	Open loop			400		kHz
V_{IO}	Input offset voltage						±25	mV
k_{SVR}	Supply voltage rejection ratio of V_{CC} or V_{BB}		VPO− connected to VPI	0 kHz to 4 kHz	60			dB
				4 kHz to 50 kHz	36			
R_L	Load resistance		Connected from VPO+ to VPO−		600			Ω
C_L	Load capacitance						100	pF

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock	MCLX and MCLKR	Depends on the device used and the BCLKX/CLKSEL pin		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	MHz
t_{r1}	Rise time of master clock	MCLKX and MCLKR				50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR				50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX				50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX				50	ns
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads	0		180	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads			160	ns
t_{d3}	Delay time, BCLKX low to data output disabled			50		220	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKX↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 2)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 2)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3- to 8-bit clock periods long)	100			ns
t_{w5}	Pulse duration of the frame sync pulse (low level)		64K bit/s operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTE 2: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

operating characteristics, over operating free-air temperature range V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 0 dBm0, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

filter gains and tracking errors

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Maximum peak transmit overload level	TP3064A, TP13064A	3.17 dBm0		2.501		V
	TP3067A, TP13067A	3.14 dBm0		2.492		
Transmit filter gain, absolute (at 0 dBm0)		T_A = 25°C	−0.15		0.15	dB
Transmit filter gain, relative to absolute		f = 16 Hz			−40	dB
		f = 50 Hz			−30	
		f = 60 Hz			−26	
		f = 200 Hz	−1.8		−0.1	
		f = 300 Hz to 3000 Hz	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
		f ≥ 4600 Hz (Measure response from 0 Hz to 4000 Hz)			−32	
Absolute transmit gain variation with temperature and supply voltage		Relative to absolute transmit gain	−0.10		0.10	dB
Transmit gain tracking error with level		Sinusoidal test method; Reference level = −10 dBm0				dB
		VFXI+ = −40 to 3 dBm0			±0.2	
		VFXI+ = −50 to −41 dBm0			±0.4	
		VFXI+ = −55 to −51 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)		Input is digital code sequence for 0-dBm0 signal, T_A = 25°C	−0.15		0.15	dB
Receive filter gain, relative to absolute		f < 200 Hz		0.15		dB
		f ≥ 200 Hz			0.15	
		f = 300 Hz to 3000 Hz, T_A = 25°C	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
Absolute receive gain variation with temperature and supply voltage		T_A = Full range, See Note 3	−0.10		0.10	dB
Receive gain tracking error with level		Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10-dBm0 signal				dB
		PCM level = −40 to 3 dBm0			±0.2	
		PCM level = −50 to −41 dBm0			±0.4	
		PCM level = −55 to −51 dBm0			±0.8	
Receive output drive voltage		R_L = 10 kΩ			±2.5	V
Transmit and receive gain tracking error with level (A-law, CCITT C712)		Pseudo noise test method; reference input PCM code corresponds to an ideally encoded −10-dBm0 signal				dB
		PCM level = −40 to −10 dBm0			±0.25	
		PCM level = −50 to −41 dBm0			±0.30	
		PCM level = −55 to −51 dBm0			±0.45	

† Absolute rms signal levels are defined as follows: V_I = 0 dBm0 = 4 dBm = 1.2276 V at f = 1.02 kHz with R_L = 600 Ω.
‡ All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
NOTE 3: Full range for the TP3064A and TP3067A is 0°C to 70°C. Full range for the TP13064A and TP13067A is −40°C to 85°C.

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D4050, SEPTEMBER 1992

operating characteristics, over operating free-air temperature range V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 0 dBm0, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted) (see Note 3)

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit filter gain, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 601 Hz to 800 Hz		120	145	
	f = 801 Hz to 1000 Hz		50	75	
	f = 1001 Hz to 1600 Hz		20	40	
	f = 1601 Hz to 2600 Hz		55	75	
	f = 2601 Hz to 2800 Hz		80	105	
	f = 2801 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	−40	−25		µs
	f = 1001 Hz to 1600 Hz	−30	−20		
	f = 1601 Hz to 2600 Hz		70	90	
	f = 2601 Hz to 2800 Hz		100	125	
	f = 2801 Hz to 3000 Hz		140	175	

noise

PARAMETER		TEST CONDITIONS†	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	TP3064A, TP13064A	V_{FXI} = 0 V		9	14	dBrnC0
Transmit noise, P-message weighted (see Note 4)	TP3067A, TP13067A	V_{FXI} = 0 V		−78	−75	dBm0p
Receive noise, C-message weighted	TP3064A, TP13064A	PCM code equals alternating positive and negative zero		2	4	dBrnC0
Receive noise, P-message weighted	TP3067A, TP13067A	PCM code equals positive zero		−86	−83	dBm0p
Noise, single frequency		VFXI+ = 0 Vms, f = 0 kHz to 100 kHz, Loop-around measurement			−53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTES: 3. Full range for the TP3064A and TP3067A is 0°C to 70°C. Full range for the TP13064A and TP13067A is −40°C to 85°C.

4. Measured by extrapolation from the distortion test result

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operating characteristics, over operating free-air temperature range V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 0 dBm0, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted) (see Note 3)

power supply rejection

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT‡
Positive power supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, VFXI+ = −50 dBm0 (see Note 5)					
	f = 0 Hz to 4 kHz	A-law	38			dB
		μ-law	38			dBC
	f = 4 kHz to 50 kHz		40			dB
Negative power supply rejection, transmit	V_{BB} = −5 V + 100 mVrms, VFXI+ = −50 dBm0					
	f = 0 Hz to 4 kHz	A-law	35			dB
		μ-law	35			dBC
	f = 4 kHz to 50 kHz		40			dB
Positive power supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms					
	f = 0 Hz to 4 kHz	A-law	40			dB
		μ-law	40			dBC
	f = 4 kHz to 50 kHz		40			dB
Negative power supply rejection, receive	PCM code equals positive zero, V_{BB} = −5 V + 100 mVrms					
	f = 0 Hz to 4 kHz	A-law	38			dB
		μ-law	38			dBC
	f = 4 kHz to 50 kHz		40			dB
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300 Hz to 3400 Hz input applied to DR (measure individual image signals at VFRO)				−30	dB
	f = 4600 Hz to 7600 Hz				−33	dB
	f = 7600 Hz to 8400 Hz				−40	
	f = 8400 Hz to 100,000 Hz				−40	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

‡ The unit dBC applies to C-message weighting.

NOTES: 3. Full range for the TP3064A and TP3067A is 0°C to 70°C. Full range for the TP13064A and TP13067A is −40°C to 85°C.

5. The TP13064A and TP3064A are measured using C-message filter. The TP13067A and TP3067A are measured using P-message weighted filter.

operating characteristics, over operating free-air temperature range V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 0 dBm0, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

distortion

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT‡
Signal-to-total distortion ratio, transmit or receive half-channel	Sinusoidal test method (see Note 5)					
	Level = 3 dBm0		33			dBC
	Level = 0 dBm0 to −30 dBm0		36			
	Level = −40 dBm0	Transmit	29			
		Receive	30			
	Level = −55 dBm0	Transmit	14			
		Receive	15			
Single-frequency distortion products, transmit					−46	dB
Single-frequency distortion products, receive					−46	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz				−41	dB
Signal-to-total distortion ratio, transmit half-channel (A-Law) (CCITT G.714)	Pseudo noise test method					
	Level = −3 dBm0		33			dB
	Level = −6 dBm0 to −27 dBm0		36			
	Level = −34 dBm0		33.5			
	Level = −40 dBm0		28.5			
	Level = −55 dBm0		13.5			
Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)	Pseudo noise test method					
	Level = −3 dBm0		33			dB
	Level = −6 dBm0 to −27 dBm0		36			
	Level = −34 dBm0		34.2			
	Level = −40 dBm0		30			
	Level = −55 dBm0		15			

crosstalk

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Crosstalk, transmit-to-receive	f = 300 Hz to 3000 Hz, DR at steady PCM code		−90	−75	dB
Crosstalk, receive-to-transmit (see Note 6)	VFXI = 0 V, f = 300 Hz to 3000 Hz		−90	−72	dB

power amplifiers

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Maximum 0 dBm0 rms level for better than ±0.1 dB linearity over the range if −10 dBm0 to 3 dBm0	Balanced load, R_L, connected between VPO+ and VPO−				
	R_L = 600 Ω	3.3			V_{RMS}
	R_L = 1200 Ω	3.5			
	R_L = 30 kΩ	4			
Signal/distortion	R_L = 600 Ω	50			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ The unit dBC applies to C-message weighting.

NOTES: 5. The TP13064A and TP3064A are measured using C-message filter. The TP13067A and TP3067A are measured using P-message weighted filter.
6. Receive-to-transmit crosstalk is measured with a −50 dBm0 activation signal applied to VFXI+.

PARAMETER MEASUREMENT INFORMATION

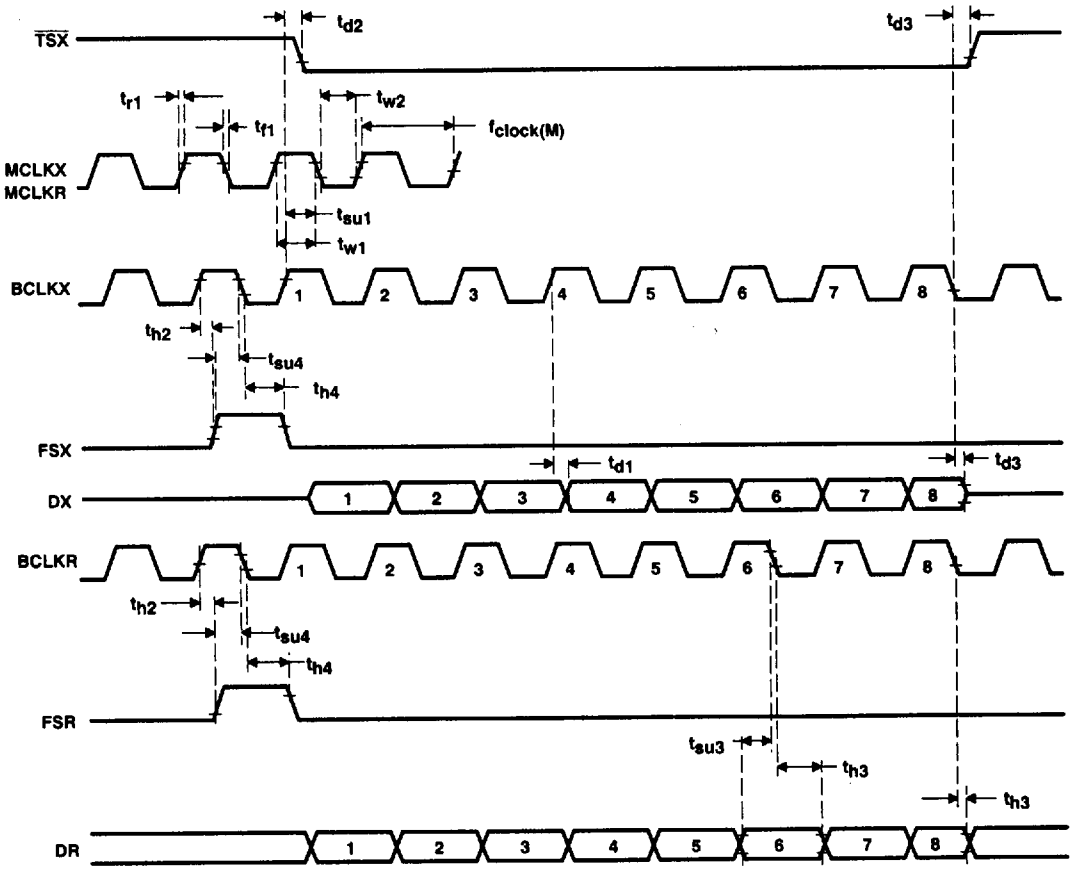

Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

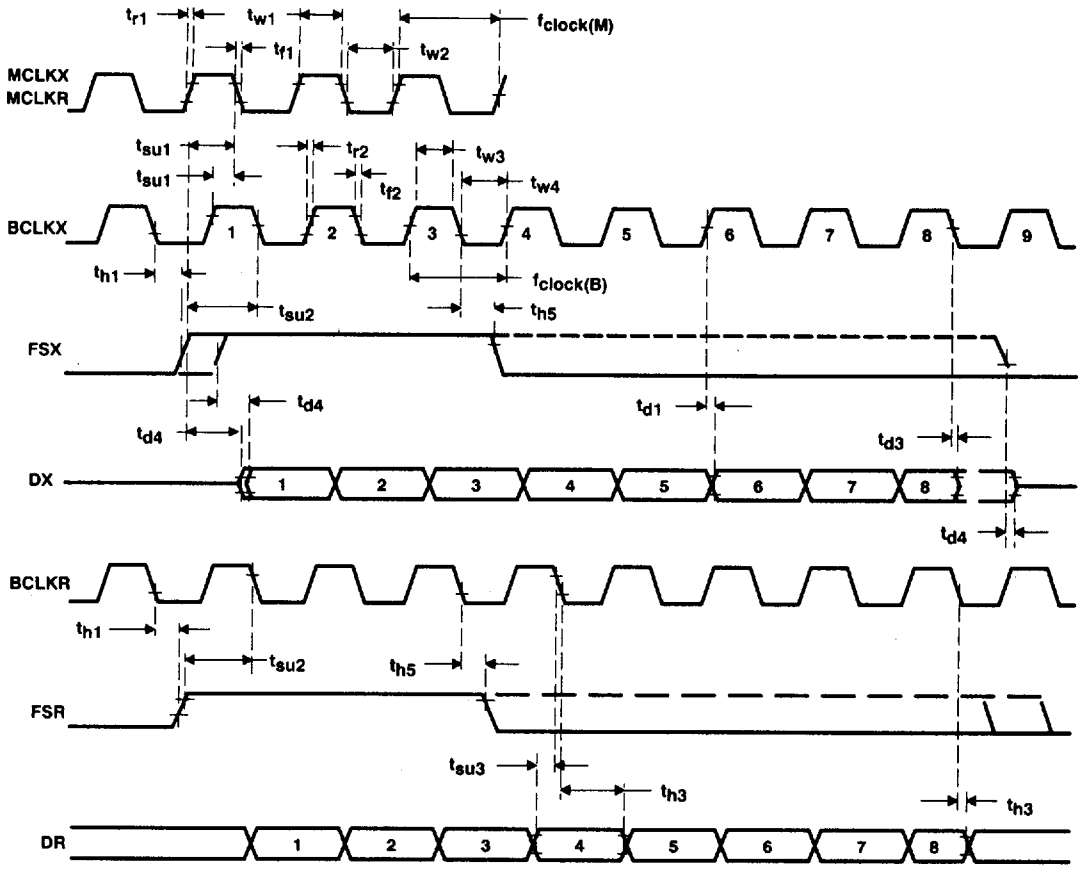

Figure 2. Long-Frame Sync Timing

APPLICATION INFORMATION

power supplies

While the pins of the TP1306_A and TP306_A families are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

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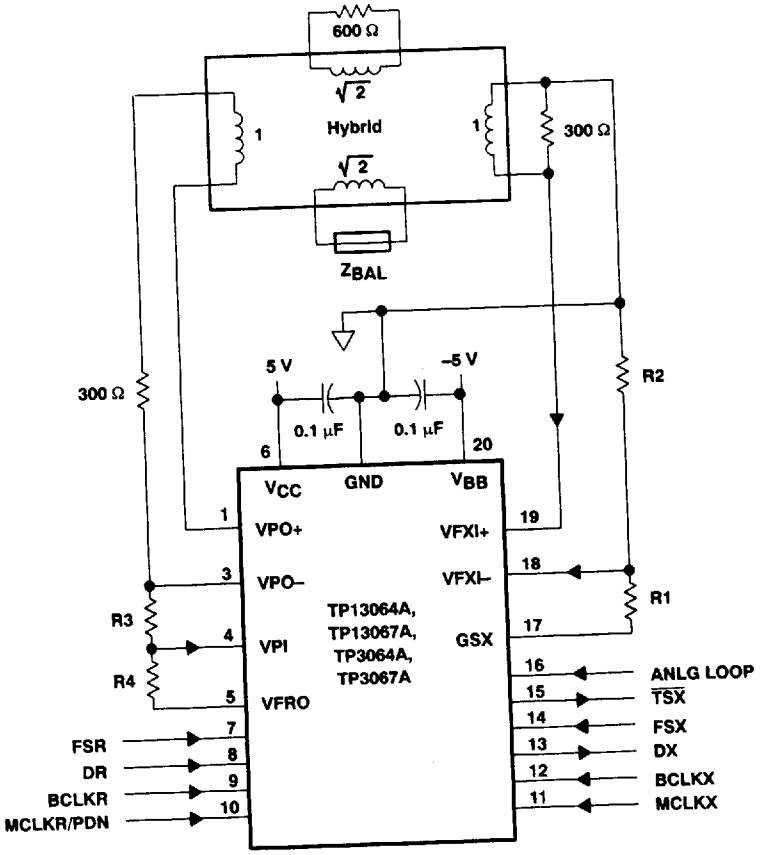
APPLICATION INFORMATION

power supplies (continued)

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-μF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to the V_{CC} and V_{BB} pins.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-μF capacitors.



NOTES: A. Transmit gain = $20 \log \left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) ≥ 10 kΩ

B. Receive gain = $20 \log \left(\frac{2 \times R3}{R4}\right)$ R4 ≥ 10 kΩ

Figure 3. Typical Asynchronous Application