CMOS 4-BIT MICROCONTROLLER

TMP47C858F

The 47C858 is a high performance 4-bit single chip microcomputer based on the TLCS-470 series. The 47C858 has plentiful operating modes (SLOW, SLEEP, HOLD) intended to save the power, with LCD driver and DTMF generator which are highly suitable for application in telephones.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C858F	8192 × 8-bit	512 × 4-bit	QFP100-P-1420-0.65A	TMP47C058G

FEATURES

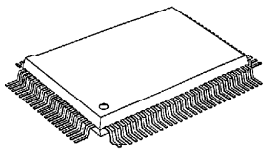
◆4-bit single chip microcomputer
◆Instruction execution time:
8.3 μs (at 960 kHz), 244 μs (at 32.8 kHz)
◆Low voltage operation: 2.7 V min.
◆92 basic instrutions
◆Table look-up instructions
◆Subroutine nesting: 15 levels max.
◆6 interrupt sources (External: 2, Internal: 4)
All sources have independent latchs each, and multiple interrupt control is available.
◆I/O port (36pins)
- Input 2ports 5pins
- I/O 8ports 31pins

◆Interval Timer (22 stages)
◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
◆Serial Interface with 8-bit buffer
External/internal clock, and leading/trailing edge shift, and 4/8-bit mode
◆LCD driver
LCD direct drive is available (440 dots display, 1/10 duty)
◆DTMF (Dual Tone Multi Frequency) output
- DTMF output with one instrution
- Single tone output function

◆Dual-clock operation
High-speed/Low-power-consumption operating mode
◆HOLD function
- Battery/Capacitor back-up

◆SLEEP function
- Battery/Capacitor back-up
- LCD is displaying

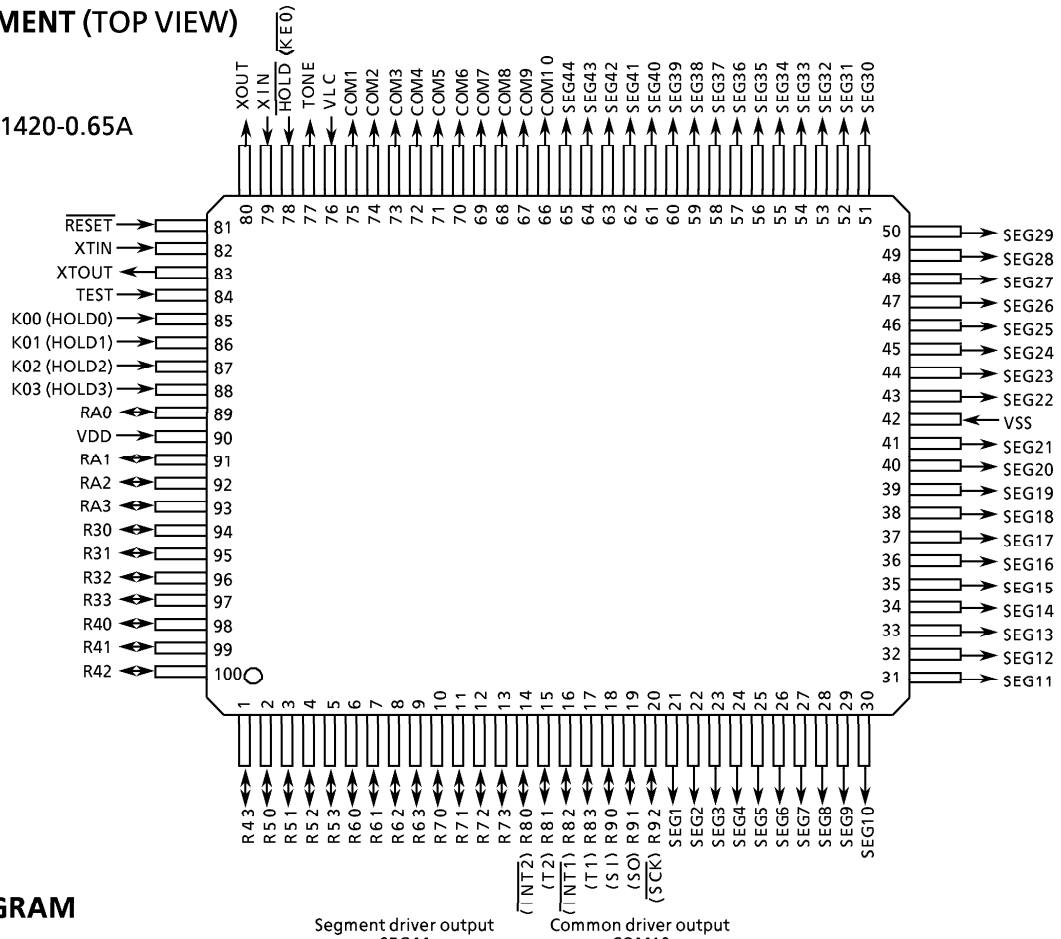
QFP100-P-1420-0.65A



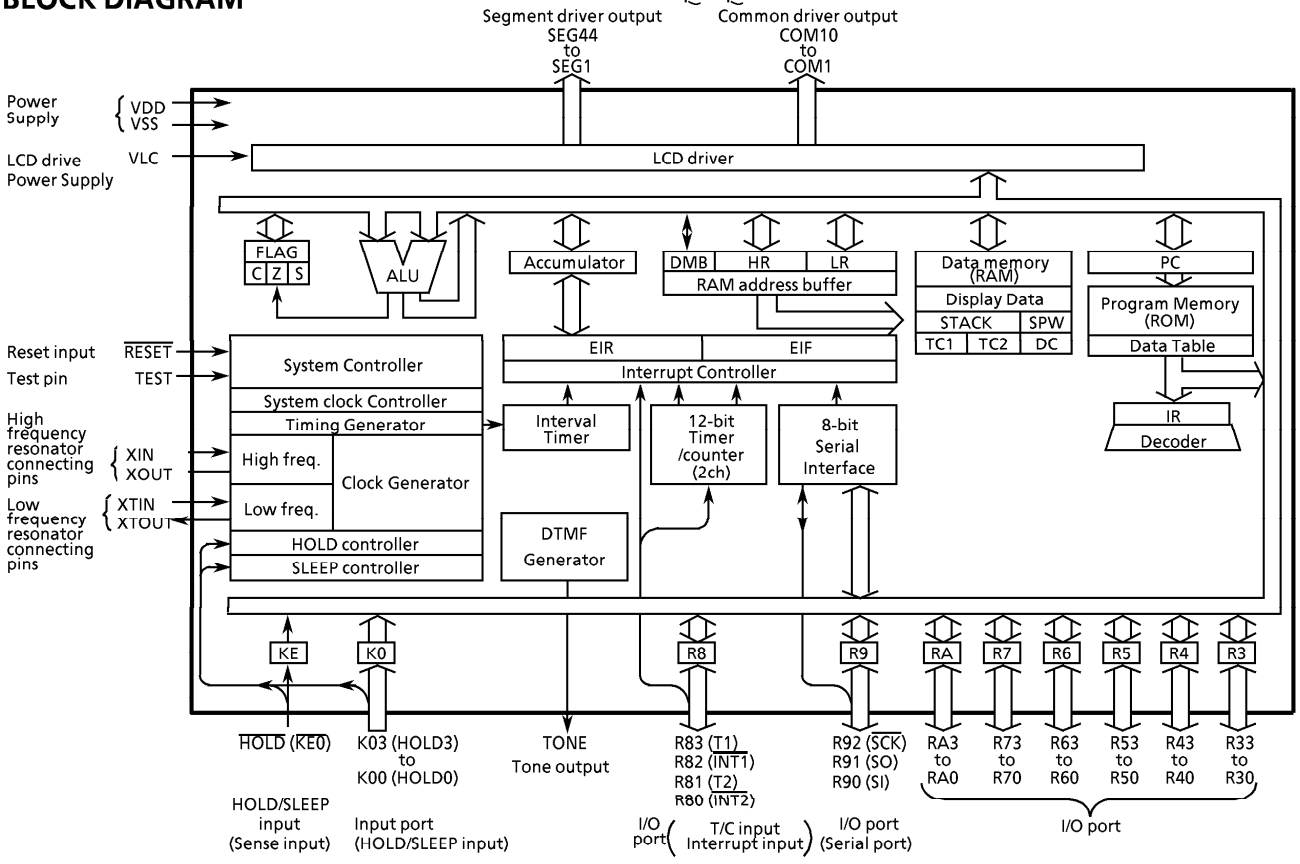
TMP47C858F

PIN ASSIGNMENT (TOP VIEW)

QFP100-P-1420-0.65A



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) to K00 (HOLD0)	Input (Input)	4-bit input port	HOLD and SLEEP request/release signal input (Active "H")
R33 to R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 to R40			
R53 to R50			
R63 to R60			
R73 to R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
RA3 to RA0	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
SEG44 to SEG1	Output	LCD segment driver output	
COM10 to COM1		LCD common driver output	
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins (High frequency). For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
XTIN	Input	Oscillator connecting pins (Low frequency). For inputting external clock, XTIN is used and XTOUT is opened.	
XTOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD and SLEEP request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 2.7 V to 6.0 V	
VSS		0 V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C858 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C655/855, the technical data sheets for the 47C655/855 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) CPU Core Function

Except for the system control circuit and RAM configuration, the functions are the same as those of the 47C655/855.

(2) Peripheral Hardware Functions

① I/O Port
② Interval Timer
③ Timer/Counter
④ One-second Signal Detection Circuit
⑤ LCD Driver
⑥ DTMF Generator
⑦ Serial Interface

The following are explanations of functions ① and ④ - ⑦ which have been added to the 47C858 or which are different from those of the 47C655/855, and the system clock control circuit.

2. CPU CORE FUNCTIONS

2.1 DATA MEMORY

The 47C858 has a total of 512 × 4bits of data memory. This memory is same as the data memory built into the 47C655/855, so refer to the technical data sheets for the 47C655/855 for an explanation of the operation.

2.2 SYSTEM CONTROL CIRCUIT

It is possible to shift from the SLOW operating mode to the SLEEP operating mode to further reduce power consumption and still maintain the internal status. In the SLEEP mode, all operations except for the timing generator (TG) binary counter and LCD driver are suspended.

2.2.1 System Clock Controller

The system clock controller starts or stops the high-frequency and low-frequency clock oscillator and switches between the basic clocks. The operating mode is generally divided into the single-clock mode and the dual-clock mode, which are controlled by command.

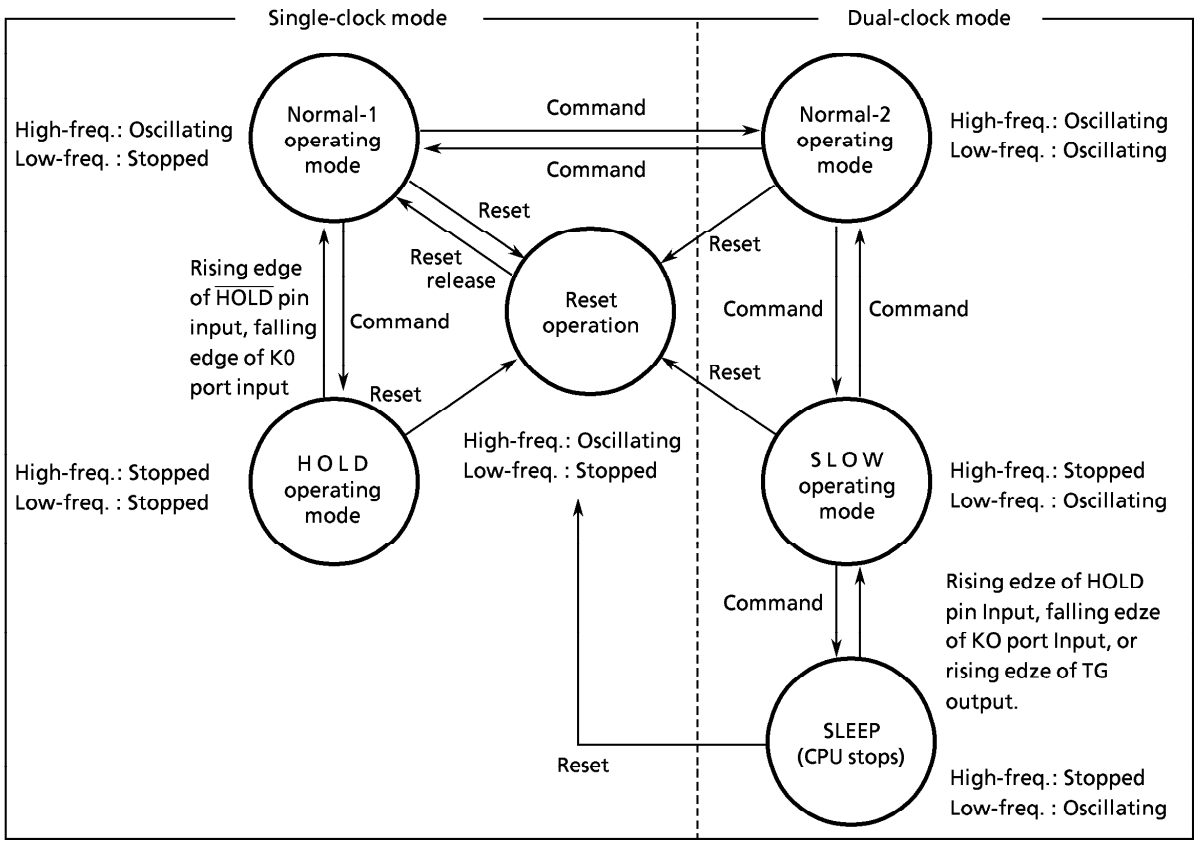


Figure 2-1. Operating Mode Transition Diagram

(1) Control of System Clock

The system clock is controlled by the command register (OP16). During a reset, the command register is reset to "0" and the single clock mode is selected. Oscillation of the low-frequency clock is started in the single clock mode by setting bit 3 of OP13.

System clock control
(Port address:OP16 Initial value:*000)

3	2	1	0
	DCLK		DWUT

DCLK	Operating mode selection
00: Single-clock mode (Normal-1)	
01: Dual-clock mode (Normal-2)	
10: Reserved	
11: Dual-clock mode (SLOW)	

DWUT	Warm-up time selection	Note2.
	Example:	fc = 960 kHz, fs = 32.8 kHz
0: 2^8/fs + 2^9/fc [s]	8.3 [ms]	
1: 2^{11}/fs + 2^9/fc [s]	63.0	

Low-frequency oscillation control
(Port address:OP13 Initial value:000*)

3	2	1	0
ESC	(SWU)		

ESC	Low-frequency oscillation control	Note3.
0: Oscillation stops		
1: Oscillation starts		

*Note1. *:don't care*
fc:High-frequency clock [Hz]
fs:Low-frequency clock [Hz]
Note2. It is valid only at switching from the SLOW to the Normal-2.
Note3. It is valid only in the Normal-1 operating mode
Note4. The access to command register (OP16) may cause the outputs over the eighth stage of timing generator to precede that to be expected by maximum 2^7/fc or 1/fs [s]

Figure 2-2. System Clock Control Command Register

2.2.2 Operating Mode

There are two operating modes : the Single-clock mode and the Dual-clock mode.

(1) Single-clock Mode

Canceling a reset starts the Normal-1 operating mode. Oscillation of the low-frequency clock can be started and stopped in this mode. To shift to the Dual-clock mode, start oscillation with the low-frequency oscillation control command register (OP13) and then switch to the Normal-2 operating mode with the system clock control command register (OP16).

There is also a HOLD operating mode used for low power consumption operation. To switch to HOLD operation, stop oscillation of the low-frequency clock (OP13) and then switch with the HOLD operation mode command register (OP10).

(2) Dual-clock Mode

In the Dual-clock mode, the instruction cycle is normally generated with the high-frequency clock (fc) and then the Normal-2 operating mode is used. When necessary, the SLOW operating mode can be used by generating the low-frequency clock (fs). In addition, the SLEEP operation mode, in which all operations except the low-frequency clock and LCD driver are suspended, can also be used. Switching between Normal-2 operation, SLOW operation and SLEEP operation in the Dual-clock mode is explained below. During a reset, the command register is initialized to the Single-clock mode. At this time, the low-frequency clock is not being oscillated; therefore, start oscillation of the low-frequency clock first and then switch to Normal-2 operation in the Dual-clock mode.

a) Switching from the Normal-2 operation to the SLOW operation

Setting DCLK (bit2 of OP16) to "1" switches to SLOW operation, but several seconds are required for low-frequency clock oscillation to stabilize. Consequently, when there is a possibility of switching to SLOW operation immediately after shifting to Normal-2 operation, it is necessary to wait until oscillation of the low-frequency clock stabilizes. Oscillation of the high-frequency clock will stop at this time.

b) Returning from the SLOW operation to the Normal-2 operation

When DCLK (bit 2 of OP16) is cleared to "0", the warm-up time for resetting to DWUT (bit 0 of OP16) is set at the same time. Normal-2 operation starts after the set warm-up time has elapsed.

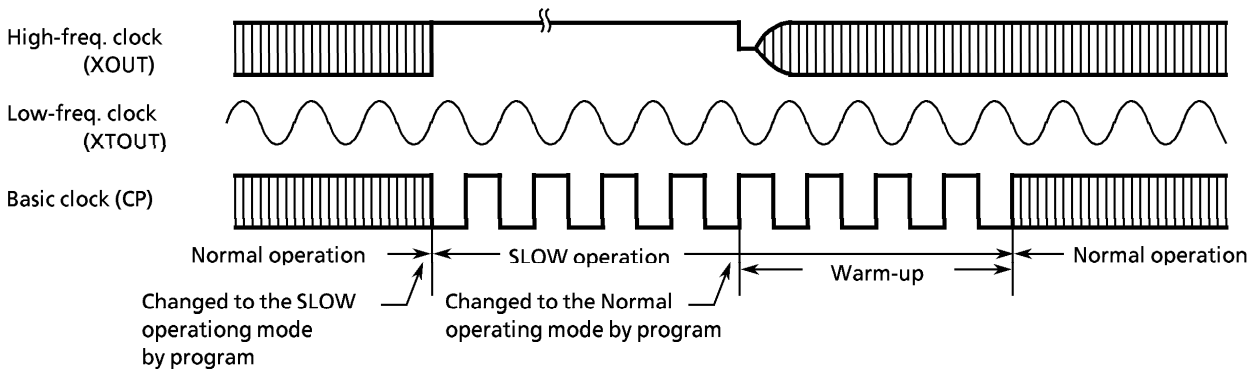


Figure 2-3. System Clock Switching Timing

c) Shifting from the SLOW operation to the SLEEP operation

After selecting the return conditions using the return conditions selection register (OP13), shift to SLEEP operation (refer to the SLEEP operation mode explanation) by setting the command in the command register (OP10). Occurrence of the selected condition returns to SLOW operation.

Note1. The command register (OP10) is used for both HOLD operation control and SLEEP operation control. This register is used for HOLD operation control when accessed during Normal-1 operation and for SLEEP operation control when accessed during SLOW operation.

Note2. During SLOW operation and SLEEP operation, oscillation of the high-frequency clock is automatically halted to enable low power supply voltage operation and low power consumption operation. However, while less power is consumed by the oscillator and internal hardware, the amount of power consumed by the pin interface (dependent on external circuitry and programs) is not directly related to the low power consumption operation mode; therefore, caution is required during system design and interface circuit design. Also, the execution of instructions is not interrupted by switching to SLOW operation but, in some cases, there is influence on some of the peripheral hardware functions; therefore, refer to the explanations of the various operations.

HOLD operating mode control

(Port address:OP10 Initial value:*0**)

3	2	1	0
HLDMS		HWUT	

HLDMS	Mode select/HOLD operation start
01: Starts HOLD operation in edze sensitive release mode	
11: Starts HOLD operation in level sensitive release mode	
*0: Reserved	

HWUT	Warm-up time selection	
	Example:	at fc = 960 kHz
00: 2^{18}/fc [s]	273	[ms]
01: 2^{14}/fc	17	
*1: Reserved		

*Note1. *: don't care*

Note2. Do not access command register OP10 unless the HOLD operation mode is being used

Figure 2-4. Command Register

2.2.3 HOLD Operation Mode

HOLD operation suspends system operation and holds the internal status immediately before the suspension with low power consumption. This mode is started by setting the command in the command register (OP10) in the Normal-1 operation mode, but it is necessary to stop the low-frequency clock (by clearing bit 3 of OP13) before accessing OP10. Hold control is possible not only from the HOLD pin but from the K0 port as well. Figure 2-5 shows the relationship between the KE port, KE0 input data and the HOLD control signal. The KE port is assigned to the lowest bit of port address IP0E and is read as the result of the logical operation of the KE0 pin and K0 pin input. When the KE0 pin is "L" and all four K0 pins are "H", for example, the KE0 input data is read as "1". "0" is read at all other times.

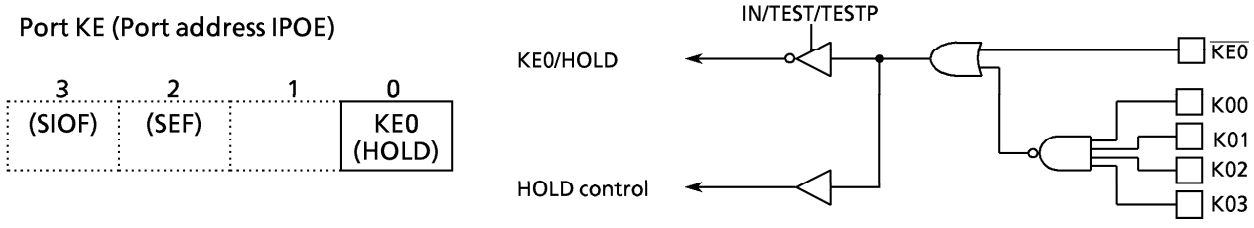


Figure 2-5. Port KE, KE0 input data and HOLD control signal

The HOLD operation mode is released when a hold control signal rise from "0" to "1" is sensed. Consequently, if the hook switch is connected to the HOLD pin and the key switch is connected to the K0 pin, it is possible to release HOLD operation by either turning off the hook switch or by pressing a key. Thus, an on-hook dialing function can easily be implemented. Other than that, the HOLD operation mode is the same as for the 47C800. For details, refer to the 47C800 technical data sheets.

2.2.4 SLEEP Operation Mode

The SLEEP operation mode suspends all SLOW operation operations except for the low-frequency clock, TG binary counter and LCD driver, and retains the internal status with low power consumption without stopping the clock function and LCD display.

SLEEP mode control

(Port address : OP10 Initial value : ****)

3	2	1	0
SLPMS			

SLPMS	Mode selection and SLEEP operation starts
0111: Starts SLEEP operation in edge sensitive release mode	
1111: Starts SLEEP operation in level sensitive release mode	
The other codes are reserved	

Return conditions selection register

(Port address : OP13 Initial value : 000*)

3	2	1	0
(ESC)	SWU		

SWU	Return conditions selection
00: HOLD and K0 pin input	
10: HOLD, K0 pin and 1 s signal	
*1: HOLD, K0 pin and 15.625 ms signal	

Figure 2-6. Command Register, Return Conditions Selection register.

Operation in the edge release mode and level release mode is the same as in the HOLD operation mode. To start SLEEP operation, select the return conditions during SLOW operation with the return conditions selection register (OP13) and then set start command in the command register (OP10). SLEEP operation is then return to SLOW operation when the conditions selected with the return conditions selection register occur.

Example : Starting SLEEP operation using the HOLD and K0 pin input, and the 1 s signal as return condition.

```
LD      A, #0CH      ; Selects HOLD, K0 pin input and 1 s signal
OUT     A, %OP13
LD      A, #7H       ; Starts SLEEP operation
OUT     A, %OP10
```

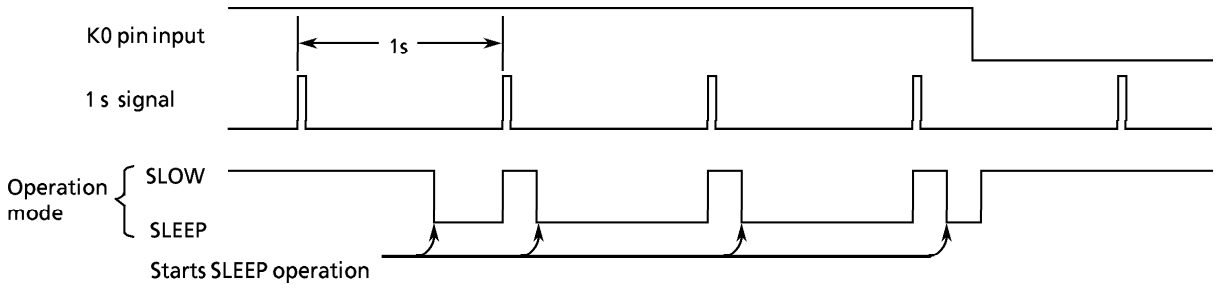


Figure 2-7. Return Conditions and operation Mode

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C858 has 10 ports (36 pins) each as follows;

① K0 ; 4-bit input (shared by hold request/release signal input)
② R4, R5, R6 ; 4-bit input/output
③ R3, R7, RA ; 4-bit input/output
④ R8 ; 4-bit input/output (shared by external interrupt input and timer/counter input)
⑤ R9 ; 3-bit input/output (shared by serial port)
⑥ KE ; 1-bit sense input (shared by hold request/release signal input)

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03 to K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

Port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

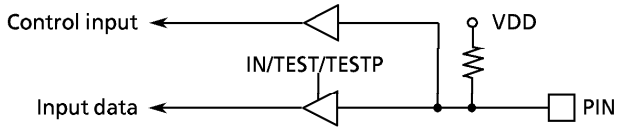


Figure 3-1. Port K0

(2) R3 (R33 to R30), R7 (R73 to R70), RA (RA3 to RA0)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R* (Port address OP0*/IP0*)

3	2	1	0
R*3	R*2	R*1	R*0

R* ; 3, 7, A

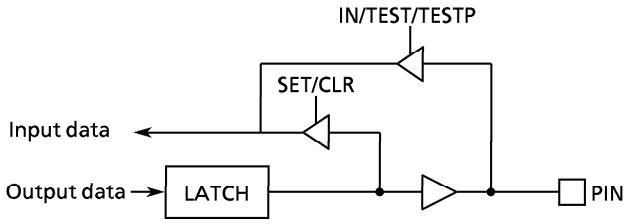


Figure 3-2. R3, R7, RA

3.2 One-second Signal Detection Circuit

A one-second signal detection circuit is built-in to enable clock functions. A flip-flop construction is used which is set by the rise (one second) of the TG final stage output and which is reset by accessing port address OP0D. The one-second detection circuit can be used in Nomal-2 operation, SLOW operation and SLEEP operation mode.

Example 1. Reads F/F
IN %IP0D, A
Example 2. Reads F/F
OUT A, %IP0D

One-seond Monitor
(Port address : IP0D)

3	2	1	0
*	*	*	SSD

SSD	Detection of one-second
0: Reset	
1: Set	

Figure 3-3. One-second Monitor

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB@HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note 2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○	○	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	1 sec signal status	Reset s F/F	○	○	○	–	–	–	–
0E	status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	undefined	Hold operating mode control	–	○	–	–	–	–	–
11	undefined	——	–	–	–	–	–	–	–
12	undefined	Single tone control	–	○	–	–	–	–	–
13	undefined	Slow clock/SLEEP operation control	–	○	–	–	–	–	–
14	undefined	——	–	–	–	–	–	–	–
15	undefined	——	–	–	–	–	–	–	–
16	undefined	System clock control	–	○	–	–	–	–	–
17	undefined	——	–	–	–	–	–	–	–
18	undefined	——	–	–	–	–	–	–	–
19	undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	undefined	——	–	–	–	–	–	–	–
1B	undefined	LCD driver control	–	○	–	–	–	–	–
1C	undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	undefined	Serial interface control 1	–	○	–	–	–	–	–
1F	undefined	Serial interface control 2	–	○	–	–	–	–	–

Note 1: "——" means the reserved state. Unavailable for the user program.

Note 2: The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ROW register and Column register.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.3 DTMF Generator

The 47C858 has a built-in DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF: Dual Tone Multi Frequency)

3.3.1 Configuration of DTMF Generator

Figure 3-4 shows configuration of the DTMF generator. The 47C858 generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

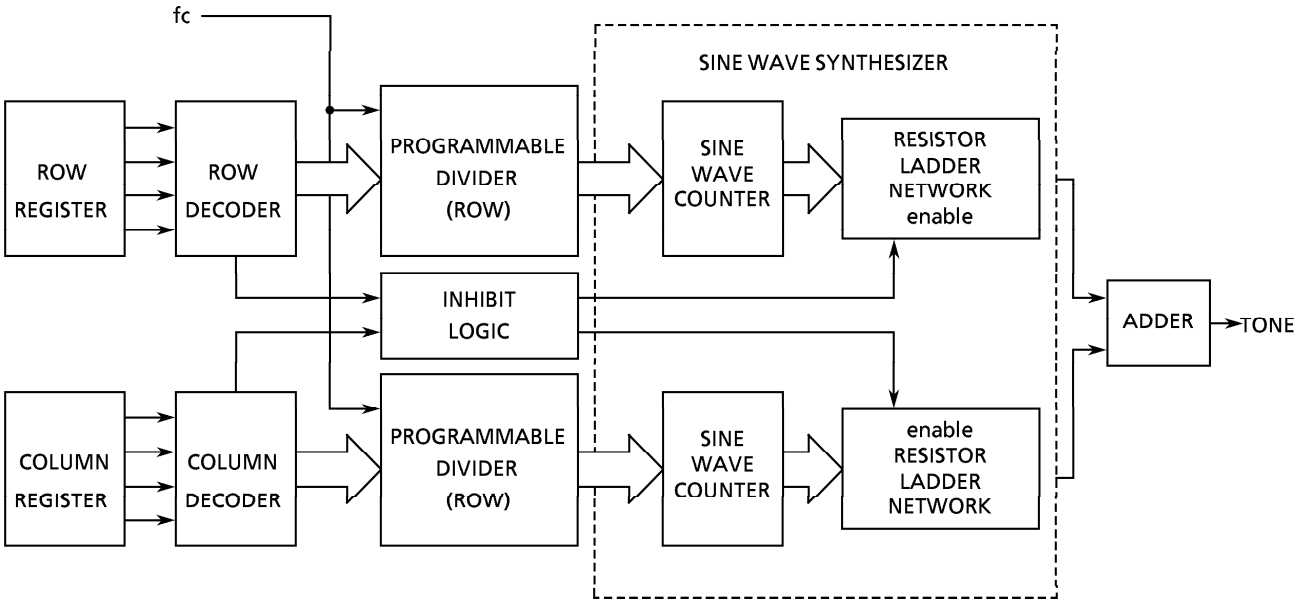


Figure 3-4. Configuration of DTMF Generator

3.3.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02). And single tone is controlled by TONE command register (OP12). ROW register, COLUMN register and TONE command register are initialized to "0" during the reset.

TONE command register (Port address OP12)

3	2	1	0	
			STE	(Initial value ***0)

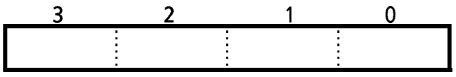
STE	Controls single tone output

0: Disable mode of single tone output
1: Enable mode of single tone output

*Note1. *: don't care*
Note2. When read SET bit, "1" is always read.

Figure 3-5. TONE command register

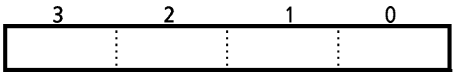
LOW register (Port address OP01/IP01)



(Initial value 0000)

Selects ROW tone frequency
0001: Outputs 697.7Hz single tone
0010: Outputs 769.2Hz single tone
0100: Outputs 857.1Hz single tone
1000: Outputs 937.5Hz single tone

COLUMN register (Port address OP02/IP02)



(Initial value 0000)

Selects COLUMN tone frequency
0001: Outputs 1212.1Hz single tone
0010: Outputs 1333.3Hz single tone
0100: Outputs 1481.5Hz single tone
1000: Outputs 1621.6Hz single tone

Figure 3-6. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-6 into the ROW and COLUMN registers. In the enable mode of single tone output and either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C858 has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1 : To output 1481.5Hz single tone

```
OUT     #8, %OP0D  ;  Sets the enable mode of single tone output.
OUT     #0, %OP01  ;  Sets an ineffective code into ROW register.
OUT     #4, %OP02  ;  Sets data "4" into COLUMN register.
```

Example 2 : 8 bits data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM1 address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN register, and dual tone is outputted.

```
LD      HL, #90H   ;  HL ← 90H (Sets the address of the data memory)
OUTB    @HL        ;  Sets the ROM data into the ROW and COLUMN register.
```

Table 3-2 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-3 shows the deviation between the 47C858 tone output frequency and standard frequency.

		COLUMN register (OP02/IP02)		
ROW register (OP01/IP01)	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-2. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency (Hz)	Standard frequency (Hz)	Deviation (%)
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	– 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	– 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency (Hz)	Standard frequency (Hz)	Deviation (%)
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	– 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	– 0.70

Table 3-3. Tone output frequencies and Deviation from standard

3.3.3 Test Mode for Tone Output

The 47C858 includes a test mode for checking tone output waveforms. Tones can be outputted by the circuit shown in Figure 3-7. ROW data are inputted from the R4 port and COLUMN data are inputted from the R5 port, and any desired single or dual tones can be outputted by setting the frequency selection codes shown in Figure 3-6. Figure 3-8 shows a single tone waveform and Figure 3-9 shows a dual tone waveform.

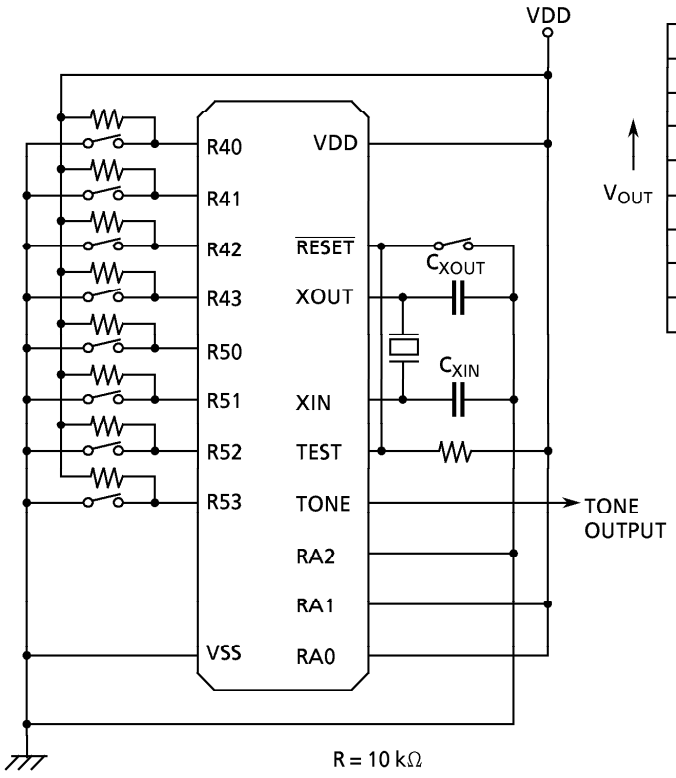


Figure 3-7. Tone test circuit

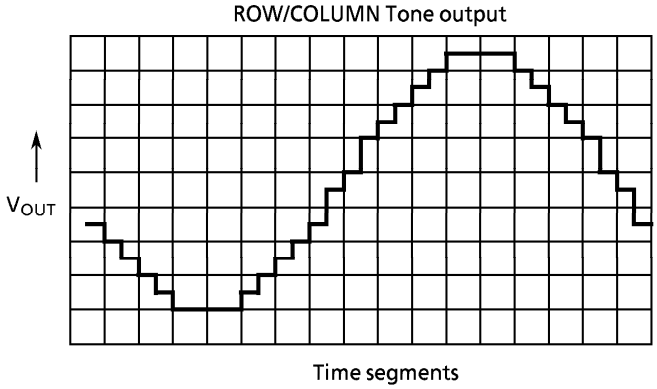


Figure 3-8. Single tone waveform

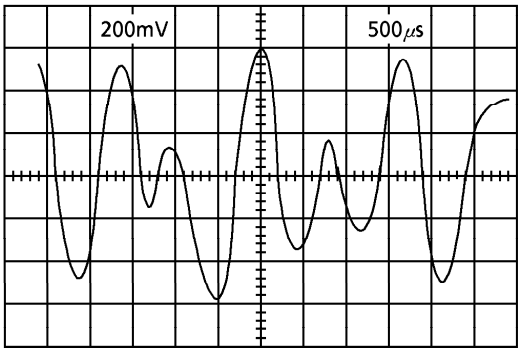


Figure 3-9. Dual tone waveform

3.4 LCD Driver

The 47C858 has a built-in driver and control circuit which directly drive the LCD display.
LCD with up to 440 pixels and duty of 1/10 (1/3 bias) can be driven.
The pins used for LCD connection are as follows.

① Segment output port 44pins (SEG44~SEG1)
② Common output port 10pins (COM10~COM1)

In addition, VLC pin is provided as the drive power pin.

3.4.1 Circuit configuration

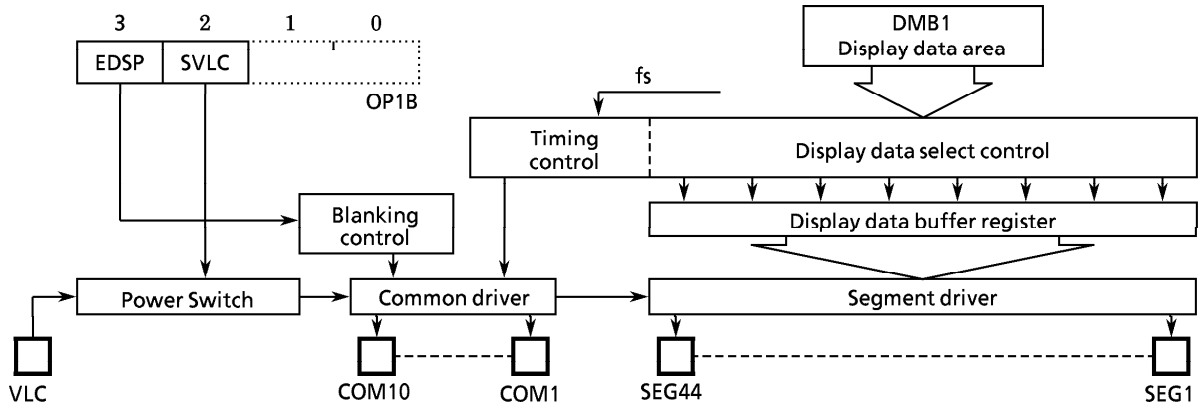


Figure 3-10. Configuration of LCD Driver

3.4.2 Control of LCD driver

The low-frequency clock is used as the base clock for the 47C858 LCD driver. Consequently, when using the LCD driver, it is necessary to start low-frequency oscillation beforehand with the low-frequency oscillation control command register (bit 3 of OP13), The LCD driver is controlled by the command register (OP1B) but commands cannot be set and any command executed will be canceled when the low-frequency clock is not being oscillated or when oscillation is unstable. After starting low-frequency oscillation with SVLC (bit 2 of OP1B) can be set after low-frequency clock oscillation stabilizes, This prevents displays while the oscillation status is unstable. The command register is reset to "0" not only during a reset but also when low-frequency oscillation is stopped (OP13).

LCD driver cintrol command register
(Port address : OP1B Initial value)

3	2	1	0
EDSP	SVLC		

EDSP	Blanking control

0 : Blanking
1 : Enables display

SVLC	Power switch control

0 : Power switch is turned off
1 : Power switch is turned on

Figure3-11. LCD Driver Control Command Register

3.4.3 LCD drive voltage

The LCD drive voltage is determined by the difference in electrical potential (VDD-VLC) between the vdd and vlc pins. Thus, when the CPU operating voltage and LCD drive voltage are the same, connect the VLC pin to the VSS pin. The LCD light when the difference in electrical potential between segment output and common output is $\pm V_{LCD}$ and are turned off at all other times. During a reset, the LCD driver power switch is turned off automatically to shut off the VLC level and the LCD display is turned off. The power switch is turned on by setting SVLC (bit 2 of OP1B) to"1" to supply VLC voltage to the LCD driver,

Example : Displaying LCD in Normal-2 mode.

```
LD    A, #8H     ; Low frequency clock starts
OUT   A, %OP13
LD    A, #2H     ; Shifts to Nomal-2 mode
OUT   A, %OP16
 ⋮                ; Setting of display data
 ⋮                ; Waiting for low frequency
                    oscillation become stable.
LD    A, #0CH    ;  Displaying LCD
OUT   A, %OP1B
```

3.4.4 LCD Display Operation

(1) Display data setting

Display data are stored to the display data area (110 words) of the data memory (bank1). The display data stored to the display data area are automatically read out and sent to the LCD driver by the hardware. The LCD driver generates the segment and common signals in accordance with the display data; therefore, display patterns can be changed by merely overwriting the contents of the display data area by program. This overwriting is mainly performed by the table lock-up instruction. Figure3-12 shows the correspondence between the display data area and the SEG and COM pins, A segment lights when the display data is "1" and turns off when "0". Data memory corresponding to addresses not connected to LCD can be used to store normal user processing data.

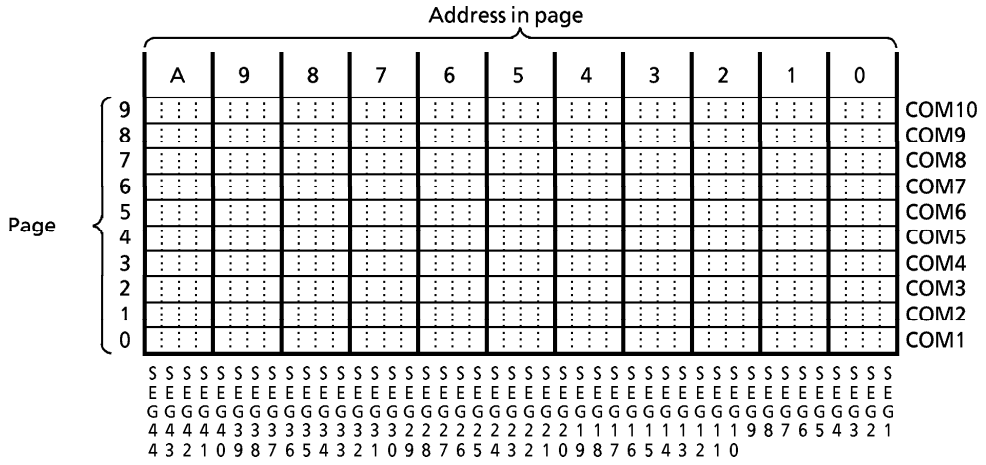


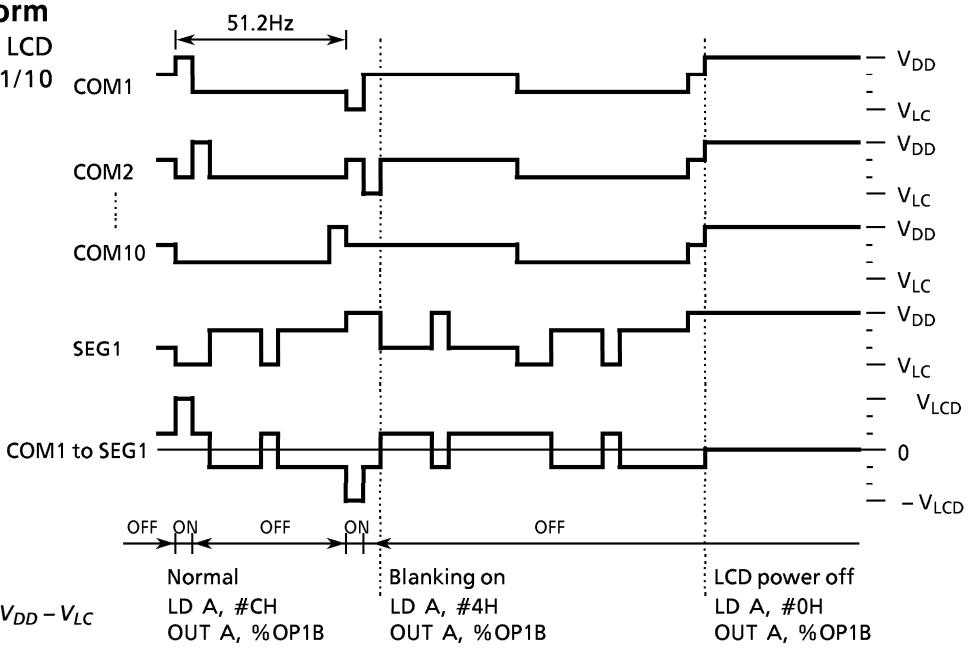
Figure 3-12. The Correspondence between the Display Data Area and SEG and COM Pins (DMB1)

(2) Blanking

Blanking can ge applied by clearing EDSP to "0". Blanking turns off LCDs by outputting the non-selection level to the COM pins, Signal levels are output continuously to the SEG pins in accordance with the display data.

3.4.5 LCD drive waveform

Figure3-13 is shown LCD drive waveform. (1/10 duty, 1/3 bias)



Note. $V_{LCD} = V_{DD} - V_{LC}$

Figure 3-13. LCD Drive Waveform

3.5 Serial Interface (SIO)

The 47C858 contains a serial interface with an 8-bit buffer. The serial interface is connected to the exterenal device via 3 pins (the serial port): R92 ($\overline{SCK}$), R91 (SO), and R90 (S I). The serial port is shared by port R9. For the serial port, the output latch of port R9 must be set to "1". In the transmit mode, R90 pin provides the I/O port; in the receive mode, R91 pin provides the I/O port.

3.5.1 Configuration of Serial Interface

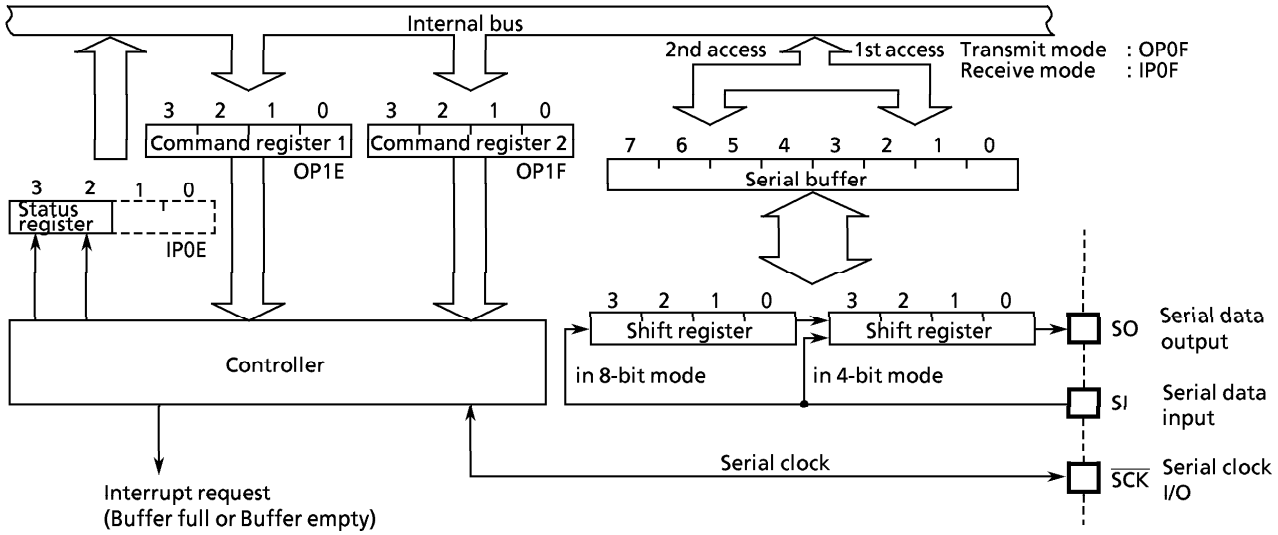


Figure 3-14. Configuration of Serial Interface

3.5.2 Control of Serial Interface

The serial interface is controlled by command registers (OP1E, OP1F). The operating states of the serial interface can be monitored by the status register (IP0E).

Serial interface status register (Port address IP0E)

3	2	1	0
SIOF	SEF		(HOLD)

SIOF	Monitors serial transfer operation state

0: Transfer is terminated
1: Transfer is in progress

SEF	Monitors shift operation states

0: Shift operation is tterminated
1: Shift in operation is in progress

Figure 3-15. Serial Interface Status Register

Serial interface control command register 1 (Port address OP1E)

3	2	1	0	
INH	SBIT	SCKR		(Initial value 0001)

INH	Forcible stop of serial transfer
0:	Transfer continues
1:	Forcible stop (Automatically clear, after stopped)

SBIT	Selects transfer bit number
0:	4-bit serial transfer
1:	8-bit serial transfer

SCKR: Selects serial clock frequency

	Single-clock mode	Dual-clock mode	
	Normal-1	Normal-2	SLOW
00:	fc /2^6 [Hz]	fc /2^6 [Hz]	Reserved
01:	fc /2^7	fc /2^7	Reserved
10:	fc /2^9	fs /2^2	Reserved
11:	fc /2^{12}	fs /2^5	fs /2^5 [Hz]

Note. fc ; High-frequency clock [Hz]
fs ; Low-frequency clock [Hz]

Serial interface control command register 2 (Port address OP1F)

3	2	1	0	
ESIO	RM	LM	ECKM	(Initial value 0000)

ESIO	Instructs serial transfer start/terminate
0:	Instructs serial transfer terminate
1:	Instructs serial transfer start

RM	Selects transfer mode
0:	Transmit mode
1:	Receive mode

LM	Selects shift edge
0:	Shift at the trailing edge of serial clock
1:	Shift at the leading edge of serial clock

ECKM	Selects shift clock
0:	Internal clock (output to $\overline{SCK}$ pin)
1:	External clock (input from $\overline{SCK}$ pin)

Note. When setting the transfer mode, ESIO must be "0". When Transmit mode, LM must be "1"

Figure 3-16. Serial Interface Control Command Register

(1) Serial clock

For the serial clock, one of the following can be selected according to the contents of the command register:

a. Clock source selection

① Internal clock

The serial clock frequency is selected by command register. The serial clock is output on the $\overline{SCK}$ pin. Note that the start of transfer, the $\overline{SCK}$ pin output goes high. This device provides the wait function in which the shift is not occurred until these processings are completed. The highest transfer rate based on the internal clock is 15000 bits/second (at fc = 960 kHz).

② External clock

The signal obtained by the clock supplied to the $\overline{SCK}$ pin from the outside is used for the serial clock. In this case, the output latch of R92 ($\overline{SCK}$) must be set to "1" beforehand. For the shift operation to be performed correctly, each of the serial clock's high and low levels needs 2 instruction cycles or more to be completed.

b. Shift edge selection

① Leading edge

Data is shifted at the leading edge (the falling edge of $\overline{SCK}$ pin input) of the serial clock.

② Trailing edge

Data is shifted at the trailing edge (the rising edge of $\overline{SCK}$ pin input) of the serial clock. However, in the transmit mode, the trailing-edge shift is not supported.

(2) Transfer bit number

SBIT (bit 2 of the command register 1) can select 4-bit/8-bit serial transfer.

a. 4-bit serial transfer

In this mode, transmission/reception is performed on 4-bit basis. ISIO interrupt is generated every 4-bit transfer. Transmit/receive data is written/read by accessing the buffer register (OP0F / IP0F) respectively.

b. 8-bit serial transfer

In this mode, transmission/reception is performed on 8-bit basis. ISIO interrupt is generated every 8-bit transfer.

Transmit/receive data is written/read by accessing the buffer register (OP0F / IP0F) twice. At the first access after setting transfer mode or generating the interrupt request, the write/read operation of lower 4-bit is performed to from the buffer register. At the second access, that of upper 4-bit is performed.

(3) Transfer modes

Selection between the transmit mode and the receive mode is performed by RM (bit 2 of the command register).

a. Transmit mode

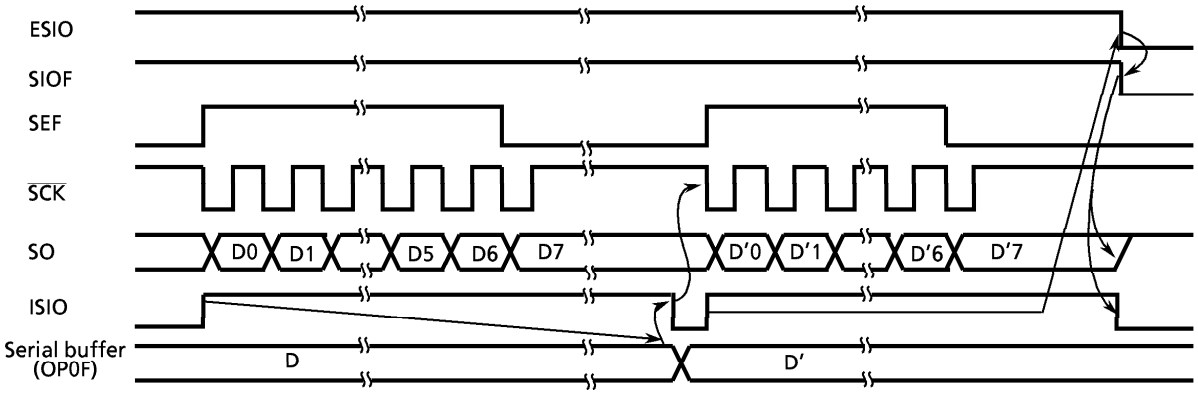
The transmit mode is set to the command register then writes the first transmit data (4bits or 8bits) to the buffer register (OP0F). If the transmit mode is not set, the data is not written to the buffer register.

In the 8-bit transfer mode, the 8-bit data is written by accessing the buffer register (OP0F) twice. Then, setting ESIO to "1" starts transmission. The transmit data is output to the SO pin in synchronization with the serial clock from the LSB side sequentially. When the LSB is output, the transmit data is moved from the buffer register to the shift register. When the buffer register becomes empty,the buffer empty interrupt (ISIO) to request for the next transmit data is generated. In the interrupt service program, when the next transmit data is written to the buffer register, the interrupt request is reset.

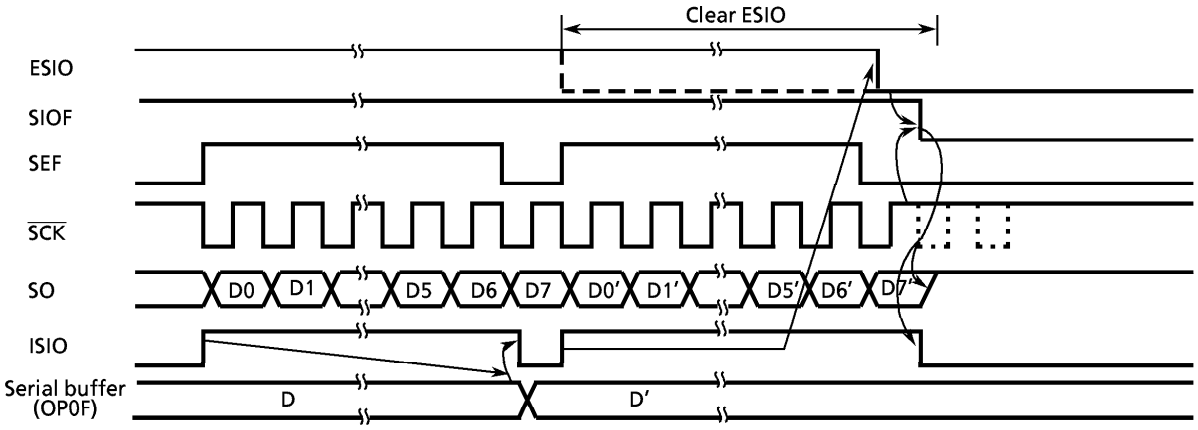
In the operation based on the internal clock, if no more data is set after the transmission of the 4-bit or 8-bit data, the serial clock is stopped and the wait state sets in. In the operation based on the external clock, the data must be set in the buffer register by the time the next data shift operation starts.
Therefore, the transfer rate is determined by the maximum delay time between the occurrence of the interrupt request and the writing of data to the buffer register by the interrupt serviced program.
To end transmission, ESIO is cleared to "0" instead of writing the next transmit data by the buffer empty interrupt service program. When ESIO is cleared,transmission stops upon termination of the currently shifted-out data.
The transmission end can be known by the SIOF state (SIOF goes "0" upon transmission end). In the operation based on the external clock, ESIO must be cleared to "0" before the next transmit data is shifted out. If ESIO is not cleared before, the transmission stops upon sending the next 4-bit or 8-bit data (dummy).

Example : To transmit (8-bit serial transfer) data stored in data memory (its address is specified by the HL register pair and the DMB) in synchronization with the internal clock ($fc/2^7$).

```
LD      A,  #0101B    ; OP1E←0101B (Sets the 8-bit serial transfer)
OUT     A,  %OP1E
LD      A,  #0010B    ; OP1F←0010B (Sets the transmit mode of the
                        operation based on internal clock)
OUT     A,  %OP1F
OUT     @HL, %OP0F    ; OP0F←RAM[HL] (Writes the transmit data of
                        lower 4-bits)
INC     L
OUT     @HL, %OP0F    ; OP0F←RAM[HL] (Writes the transmit data of
                        upper 4-bits)
LD      A,  #1010B    ; ESIO←1 (Instructs transmission start)
OUT     A,  %OP1F
```



(a) Internal-clock-based operation with wait



(b) External-clock-based operation

Figure 3-17. Transmit Mode

b. Receive mode

Data can be received when ESIO is set to "1" after setting the receive mode to the command register. The data is put from the SI pin to the shift register in synchronization with the serial clock. Then the 4/8-bit data is transferred from the shift register to the buffer register (IP0F), upon which the buffer full interrupt (ISIO) to request for reading received data is generated. The receive data is read from the buffer register by the interrup service program. In the 8-bit transfer mode, the received data is read after an interrupt request occurs: the lower 4 bits are read by the first access and the upper 4 bits by the next access. When the data has been read, the interrupt request is reset and the next data is put in the shift register to be transferred to the buffer register.

In the operation based on the internal clock, if the previous receive data has not been read from the buffer register at the end of capturing the next data, the serial clock is stopped and the wait operation is performed until the data has been read.

In the operation based on the external clock, the shift operation is performed in synchronization with the externally-supplied clock, so that the data must be read from the buffer register before the next receive data is transferred to it. The maximum transfer rate in the external-clock-based operation is determined by the maximum delay time between the generation of interrupt request and the reading of receive data. In the receive mode, the shift operation may be performed at either the leading edge or the trailing edge. In the leading edge shift operation,data is captured at the leading edge of the serial clock, so that the first shift data must be put in the SI pin before the first serial clock is applied at the start of transfer.

Example : To instruct the receive start operation with the 8-bit serial transfer, internal clock and leading edge shift (with the interrupt enable register already set).

```
LD      A,  #0100B      ;  OP1E←0100B (Sets the 8-bit serial transfer)
OUT     A,  %OP1E
LD      A,  #0110B      ;  OP1F←0110B (Sets the receive mode)
OUT     A,  %OP1F
EI                      ;  EIF←1 (Enables interrupt)
LD      A,  #1110B      ;  ESIO←1 (Instructs reception start)
OUT     A,  %OP1F
```

To end the receive operation, ESIO must be cleared to "0". When ESIO is cleared, the completion of the transfer of the current 4-bit or 8-bit data to the buffer register terminates the receive operation. To confirm the end of the receive operation by program, SIOF (bit 3 of the status register) must be sensed. SIOF goes "0" at the end of receive operation.

If the transfer modes are changed, the contents of the buffer register are lost. Therefore, the modes should not be changed until the last received data is read even after the end of reception is instructed (by clearing ESIO to "0").

The receive operation can be terminated in one of the following approaches determined by the transfer rate:

① When the transfer rate is sufficiently low (the external-clock-based operation)
If ESIO can be cleared to "0" before the next serial clock is applied upon occurrence of buffer full interrupt in the external-clock-based operation, ESIO is cleared to "0" by the interrupt service program, then the last received data is read.

Example : To instruct the receive end with sufficient low transfee rate (the leading edge shift).

```
LD      A,  #0111B      ;  ESIO←0 (Instructs reception end)
OUT     A,  %OP1F
IN      %IP0F,  A       ;  Acc←IP0F (Reads received data)
```

② When the transfer rate is sufficiently high (the external/internal clock-based operation)
If the transfer rate is high and,therefore, it is possible that the capture of the next data starts before ESIO is cleared to "0" upon acceptance of any interrupt, ESIO must be cleared to "0" by confirming that SEF (bit 2 of the status register) is set at reading the data proceeding the last data. Then, the data is read. In the interrupt serevicing following the reception of the last data, no operation is needed for termination; only the reading of the received data is performed.
This method is generally employed for the internal-clock-based operations. For an external-clock-based operation, ESIO must be cleared and the received data must be read before the last data is transferred to the buffer register.

Example : To instruct reception end when transfer rate is high (the internal clock, leading-edge shift).

```
SSEF0:  TEST    %IP0E,  2       ;  Waits until SEF = "1"
        B       SSEF0
        LD      A,  #0110B      ;  ESIO←0
        OUT     A,  %OP1F
        IN      %IP0F,  A       ;  Acc←IP0F (Reads received data)
```

③ One-word reception

When receiving only 1 word, ESIO is set to "1" then it is cleared to "0" after confirming that SEF has gone "1". In this case, buffer full interrupt is caused only once, so that the received data is read by the interrupt service program.

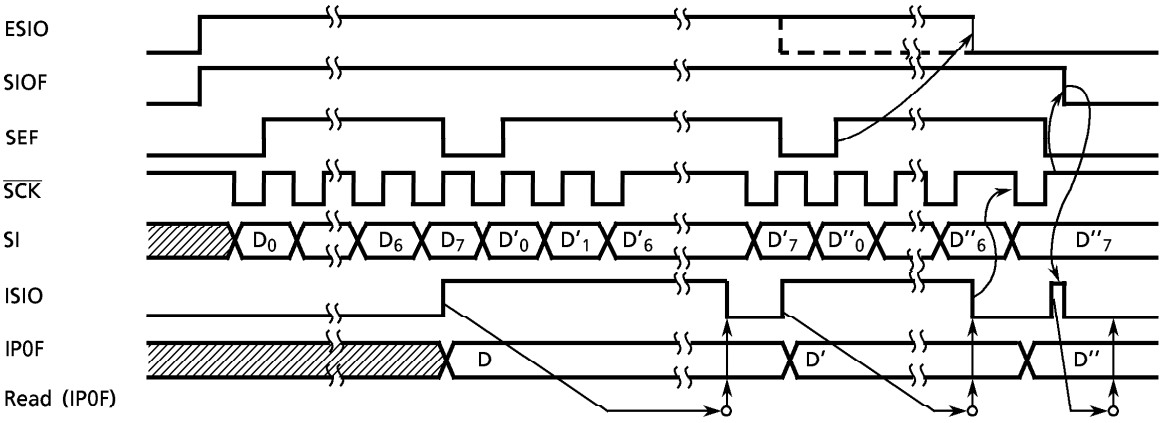
Example : To instruct the start/end of 1-word reception (the internal clock, the trailing edge shift).

```
        LD      A,  #0100B      ; OP1F←0100B (Sets in the receive mode)
        OUT     A,  %OP1F
        EI                      ; EIF←1 (Enables interrupt)
        LD      A,  #1110B      ; ESIO←1 (Instructs reception start)
        OUT     A,  %OP1F
SSEF0 : TEST    %IP0E,  2       ; Confirms that SEF = "1"
        B       SSEF0
        LD      A,  #0110B      ; ESIO←0 (Instructs reception end)
        OUT     A,  %OP1F
```

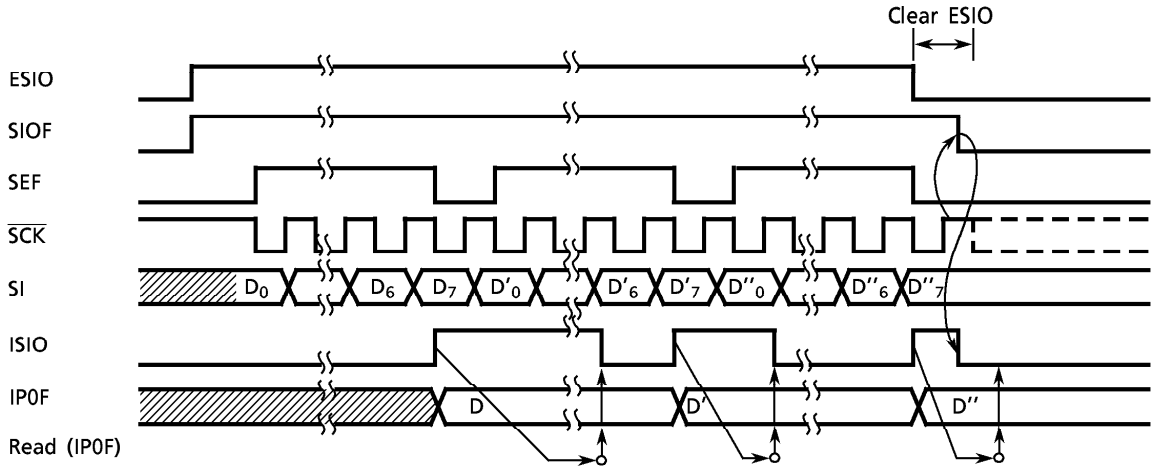
(4) Stopping serial transfer

A serial transfer operation can be stopped forcibly.

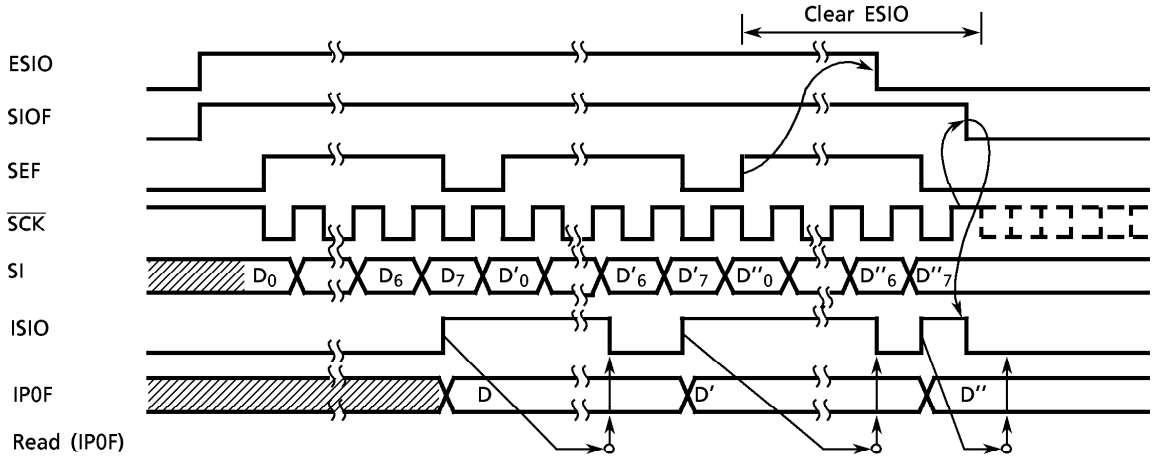
It is stopped by setting INH (bit 3 of command register 1) to "1", clearing the shift counter. When the serial transfer is over, $\overline{SCK}$ and SO terminal are set to "H"level, INH is automatically cleared to "0" with no other bits of command register affected. Further, in the transmit mode of this case, SO output is initialized to "H" level whereas the shift register is not cleared. Therefore, after the resumption of transmit, SO holds the data just before forcible stop via the shift register until the 1st shift data comes to SO.



(a) Internal-clock-based operation with wait, trailing-edge shift



(b) External-clock-based operation, leading-edge shift (when transfer rate is low)



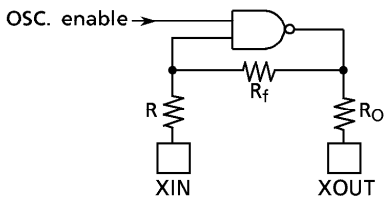
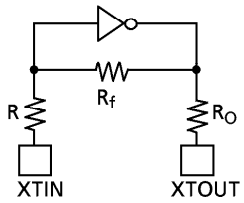
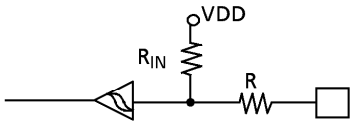
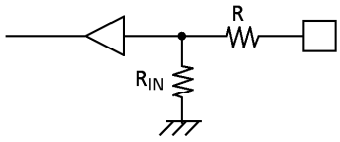
(c) Internal-clock-based operation, leading-edge shift (when transfer rate is high)

Figure 3-18. Receive Mode

INPUT/OUTPUT CIRCUITRY

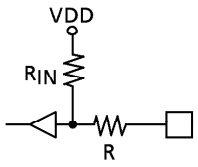
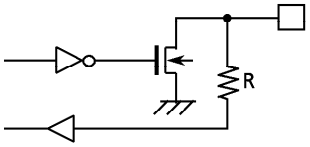
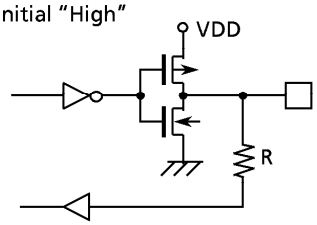
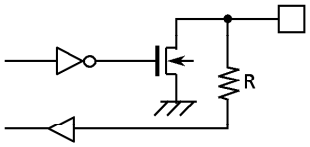
(1) Control pins

Input/Output circuitries of the 47C858 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins (High frequency) R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_O = 2 kΩ (typ.)
XTIN XTOUT	INPUT OUTPUT		Resonator connecting pins (Low frequency) R = 1 kΩ (typ.) R_f = 6 MΩ (typ.) R_O = 220 kΩ (typ.)
$\overline{\text{RESET}}$	INPUT		Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
TEST	INPUT		Pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)

(2) I/O Port

The input/output circuitries of the 47C858 I/O ports are shown below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

<table>
<tr><th>PORT</th><th>I/O</th><th colspan="2">INPUT/OUTPUT CIRCUTRY and CODE</th><th>REMARKS</th></tr>
<tr><td>K0</td><td>Input</td><td colspan="2"> 
</td><td>Pull-up resistor
R_{IN} = 70 kΩ (typ.)
R = 1 kΩ (typ.)</td></tr>
<tr><td rowspan="2">R3
R4
R5
R6</td><td rowspan="2">I/O</td><td>WB</td><td>WE, WH</td><td rowspan="2">Sink open drain
or
push-pull output
R = 1 kΩ (typ.)</td></tr>
<tr><td>Initial “Hi-Z”
 
</td><td>Initial “High”
 
</td></tr>
<tr><td rowspan="2">R7
RA</td><td rowspan="2">I/O</td><td>WB, WE</td><td>WH</td><td rowspan="2">Sink open drain
or
push-pull output
R = 1 kΩ (typ.)</td></tr>
<tr><td>Initial “Hi-Z”
 
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 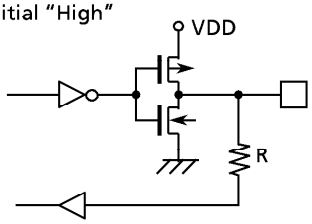
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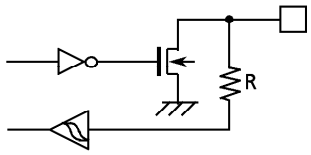
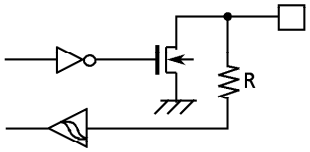
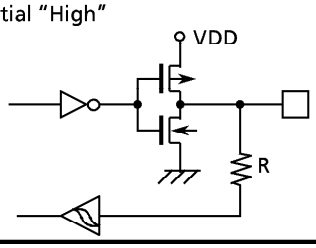
<tr><td>R8</td><td>I/O</td><td colspan="2"> 
</td><td>Sink open drain output
Initial “Hi-Z”
Hysteresis input
R = 1 kΩ (typ.)</td></tr>
<tr><td rowspan="2">R9</td><td rowspan="2">I/O</td><td>WB, WE</td><td>WH</td><td rowspan="2">Sink open drain
or
push-pull output
Hysteresis input
R = 1 kΩ (typ.)</td></tr>
<tr><td>Initial “Hi-Z”
 
</td><td>Initial “High”
 
</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation (T_{opr} = 70°C)	PD		600	mW
Soldering Temperature (time)	T_{sid}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 60 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.7	6.0	V
			In tne SLOW mode			
			In tne SLEEP mode			
			In tne HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		960		kHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

D.C. CHARACTERISTICS (V_{SS} = 0 V, T_{opr} = – 30 to 60 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V	–	–	± 2	μA
	I_{IN2}	Open drain R port	V_{IN} = 5.5 V / 0 V				
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Segment Output Registance	R_{OS}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	–	20	–	kΩ
Common Output Registance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG/COM pin		3.8	4.0	4.2	V
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 960 kHz	–	1.2	2.2	mA
	I_{DDT}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 960 kHz When tone is oscillating	–	3.0	5.0	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3 V, V_{LC} = V_{SS} fs = 32.768 kHz	–	30	60	μA
Supply Current (in the SLEEP mode)	I_{DDSP}			–	15	25	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$; Shows 2/3 level output voltage.
$V_{O1/3}$; Shows 1/3 level output voltage.

Note 5. Supply Current I_{DD} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.

Note 6. Supply Current I_{DDS} ; V_{IN} = 2.8 V / 0.2 V. Only low frequency clock is only oscillated (connecting XTIN, XTOUT).

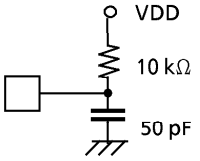
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 60 °C)

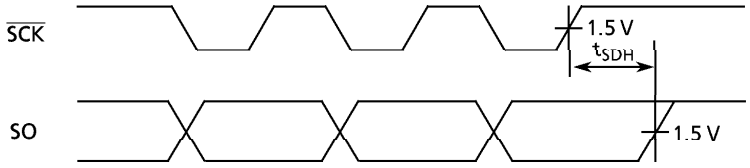
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Nomal mode	8.3			μs
		In the SLOW mode	235	–	267	μs
High level Clock pules Width	t_{WCH}	External clock	80	–	–	ns
Low level Clock pules Width	t_{WCL}					
Shifr Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	–	–	ns

Note. *Shift Data Hold Time:*

External Circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



TOME OUTPUT CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 60 °C)

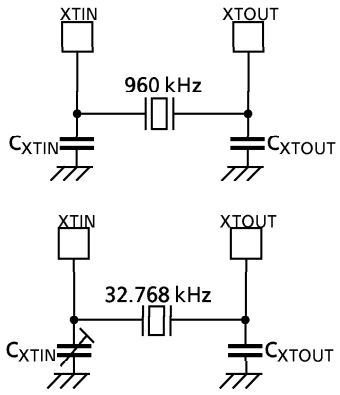
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10 kΩ, V_{DD} = 2.7 V	125	185	250	mVms
Pre-emphasis Hige Band (COL/ROW)	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Output Distortion	DIS		–	–	10	%
Frequency Stability	△f	Except error of osc. frequency	–	–	0.7	%

RECOMMENDED OSCILLATING CONDETIONS

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 60 °C)

(1) 960 kHz
Ceramic Resonator
KBR - 960H3 (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF
CSB960J21 (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF

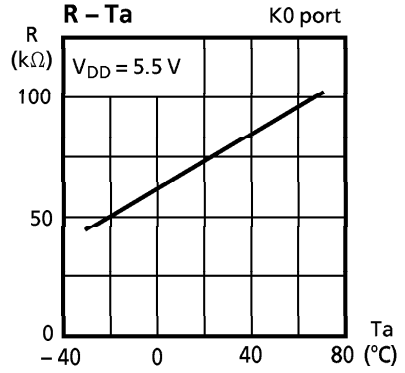
(2) 32.768 kHz
Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33 pF



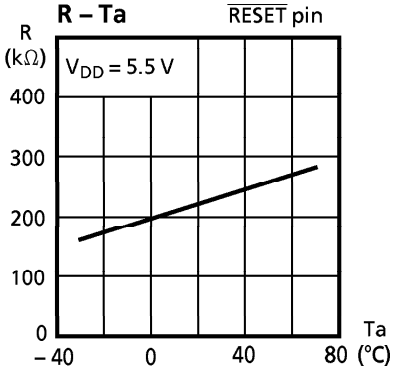
Note : *In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.*

TYPICAL CHARACTERISTICS

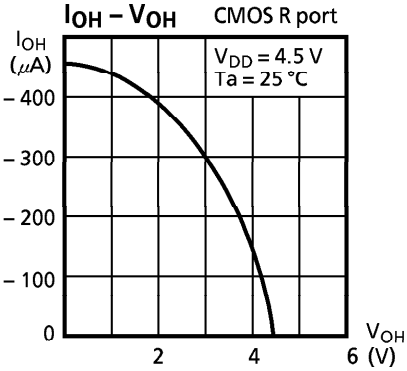
R – Ta K0 port



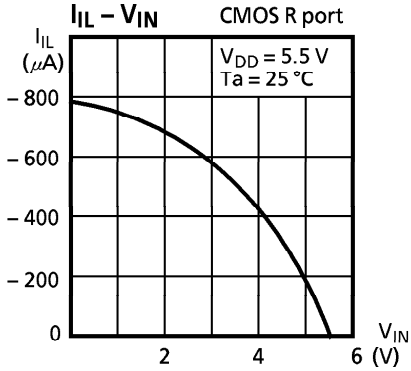
R – Ta $\overline{\text{RESET}}$ pin



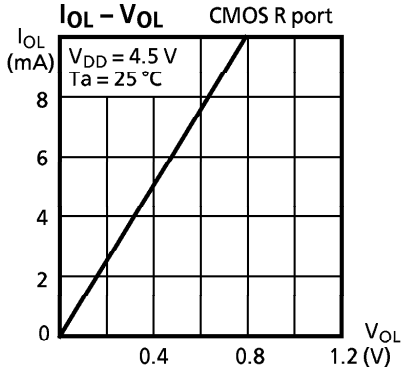
I_{OH} – V_{OH} CMOS R port



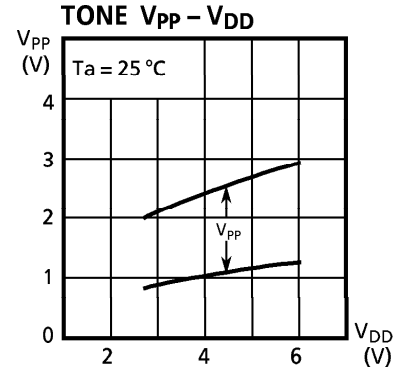
I_{IL} – V_{IN} CMOS R port



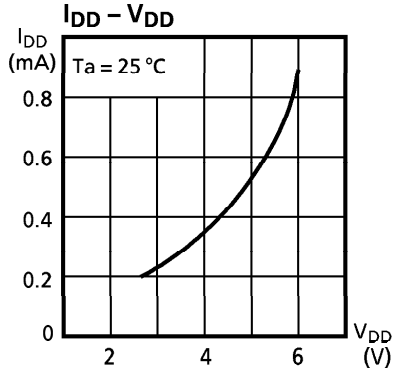
I_{OL} – V_{OL} CMOS R port



TONE V_{PP} – V_{DD}



I_{DD} – V_{DD}



I_{DDT} – V_{DD}