DATA SHEET

SAA7818HL
DVD and CD playback IC

Product specification

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- Host interface:
  - Supports ATAPI interface
  - Configurable as generic DMA interface; for use with external host interface devices
  - Automatic determination of block length for mode 2; Form 1 and Form 2 sectors; block length transferred is programmable
  - Supports synchronous UDE interface
  - Supports bufferless mode.
- Block decoder:
  - Supports CD-ROM, CDr, CD-DA, VCD, SVCD, CD-I, photo CD and DVD video formats
  - Supports real-time error detection and correction in hardware for CD-ROM mode
  - CD-ROM error corrector switchable between single or dual pass; both with Error Detection/Correction (EDC)
  - Internal registers are memory mapped
  - Embedded DVD video authentication module.
- Buffer memory controller:
  - Support for up to 64 Mbit external SDRAM memory
  - Block based sector addressing.
- Channel decoder:
  - Selectable differential and single-ended HF inputs; compatible with the TZA1033 and TZA1035; single-ended input has bypassable AGC
  - Internal 8-bit ADC
  - Digital PLL and slicer for HF clock regeneration
  - Supports EFM and EFM+ demodulation
  - Full CD error correction strategy; t = 2 and e = 4
  - On-chip CD error corrector memory with ±8 frame jitter margin
  - Built-in hardware for double pass DVD error corrector; can correct 5 errors in C1 frame; 16 errors in C2 frame
  - Error corrector monitor signal available
  - I^2S-bus output available via programmable vampire pins
  - Programmable frame sync loss indication
  - Increased tap settings for PLL equalizer compared with SAA7816
  - Enhanced playability of black dots and scratches with improved defect detector; it enables the HF PLL frequency, slicer, high-pass filter, AGC and offset loops to be held when a defect is detected
  - Improved tolerance to continuity errors in DVD play mode
  - Limit equalizer
  - Two extra motor gain settings compared to SAA7816
  - Support for copyright protection strategy for games applications
  - Hardware AGC loop, in combination with front-end IC (TZA1035)
  - Hardware automatic offset compensation loop, in combination with front-end IC (TZA1035)
  - Average jitter can be read back
  - Internal digital high-pass filter on HF input, with programmable cut-off frequencies
  - Run Length 3 (RL3) pushback feature
  - PLL monitor signal available
  - Interpolate and hold on audio output.
- Spindle motor control:
  - Advanced motor control loop allows CAV, CLV and pseudo-CLV playback
  - Support for 3-pin and 1-pin tacho control
  - Motor control via incoming bitstream or tacho.
- Speed operation:
  - Supports 18× CD-ROM playback
  - Supports 6× DVD-ROM playback.
- Multimedia functions:
  - Supports audio playback via DRAM buffer; allows audio discs to be played at higher speeds
  - IEC 60958 (SPDIF, AES/EBU and DOBM) output with Q-W subcode and programmable category code; output at n = 1 rate
  - Audio output via I^2S-bus vampire interface: 4 × oversampling filter, digital volume control, attenuator and mute.

- Microcontroller interface:
  - Embedded microcontroller can operate as 33 or 67 MHz equivalent 80C51
  - Embedded co-processor for fast multiply, divide, shift and normalize instructions; supported by C-compilers
  - Co-processor for MSF calculations
  - Memory mapped interfaces to sub functions
  - External microcontroller support
  - Embedded SRAM: 1.5 kbytes Xdata, 512 bytes Idata, 224 bytes data and registers
  - 4 banks; on Idata and registers, for better multi-tasking support
  - External flash EPROM programming support: serial boot possible with empty flash EPROM and internal program upload support
  - Code space support up to 1 Mbyte through built-in bank switching
  - Debug interface for embedded microcontroller.
- Servo processor:
  - Switched current Analog-to-Digital Converters (ADCs) for diode and error signal inputs
  - Selectable servo error or servo diode inputs
  - Focus and radial servo loops
  - Automatic closed-loop gain control available for focus and radial loops
  - Built-in access procedure with fast track count input
  - High-speed track crossing velocity measurement (>350 kHz) for CD and DVD
  - Special DVD track crossing support
  - Fast radial brake circuitry
  - Eight-to-Fourteen Modulation (EFM) actuator damping circuitry
  - Sledge motor servo loop with enhanced PCS support
  - Sledge stepper motor support
  - Adaptive Repetitive Control (ARC)
  - Debug interface for servo
  - DC offset compensation for servo
  - White and black dot defect detection and handling
  - Integrated envelope detection.
- Clock multiplier:
  - On-chip clock multipliers allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7818HL is a device for 6× DVD and 18× CD playback applications.

This device contains an embedded microcontroller which can operate as a 33 or 67 MHz equivalent 80C51 and interfaces to the channel decoder, block decoder and servo processor.

New features enable superior playability in both CD and DVD modes.

The block decoder has an embedded DVD video authentication module and supports up to 64 Mbit of external SDRAM memory. The data can be fed out in a number of different configurations including I^2S-bus, ATAPI and UDE. This device also includes the option to bypass the external memory altogether, creating a bufferless ATAPI or UDE data path solution.

The channel decoder has selectable differential and single-ended HF inputs, which are compatible with the TZA1033 and TZA1035 devices. There is an option to output the data as raw I^2S-bus via some programmable data I/O pins. With increased tap setting for the PLL equalizer compared with the SAA7816 device and enhanced playability of black dots and scratches, overall playability has been greatly improved. There are also benefits due to a new defect detector that allows holding the HF PLL frequency and slicer settings over a defect. These, together with an additional limit equalizer lead to improved tolerance to continuity errors in DVD playback mode. There are also two extra motor gain settings compared to the SAA7816 device and support for copyright protection strategies in games applications.

The servo processor has been upgraded to include an improved defect detection and handling process, an integrated envelope detection circuit and also DC offset compensation on the diode inputs.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DDD(C)}$	digital supply voltage for the core	1.65	1.8	1.95	V
$V_{DDD(P)}$	digital supply voltage for the pad cells (3 V)	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.0	3.3	3.6	V
I_{DDA}	analog supply current	–	65	–	mA
$I_{DDD(P)}$	digital supply current for the pad cells	–	135	–	mA
$I_{DDD(C)}$	digital supply current for the core	–	55	–	mA
f_{xtal}	crystal frequency	7	8.4672	9	MHz
T_{amb}	ambient temperature	–40	–	+85	°C
T_{stg}	storage temperature	–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7818HL	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1

5 BLOCK DIAGRAM

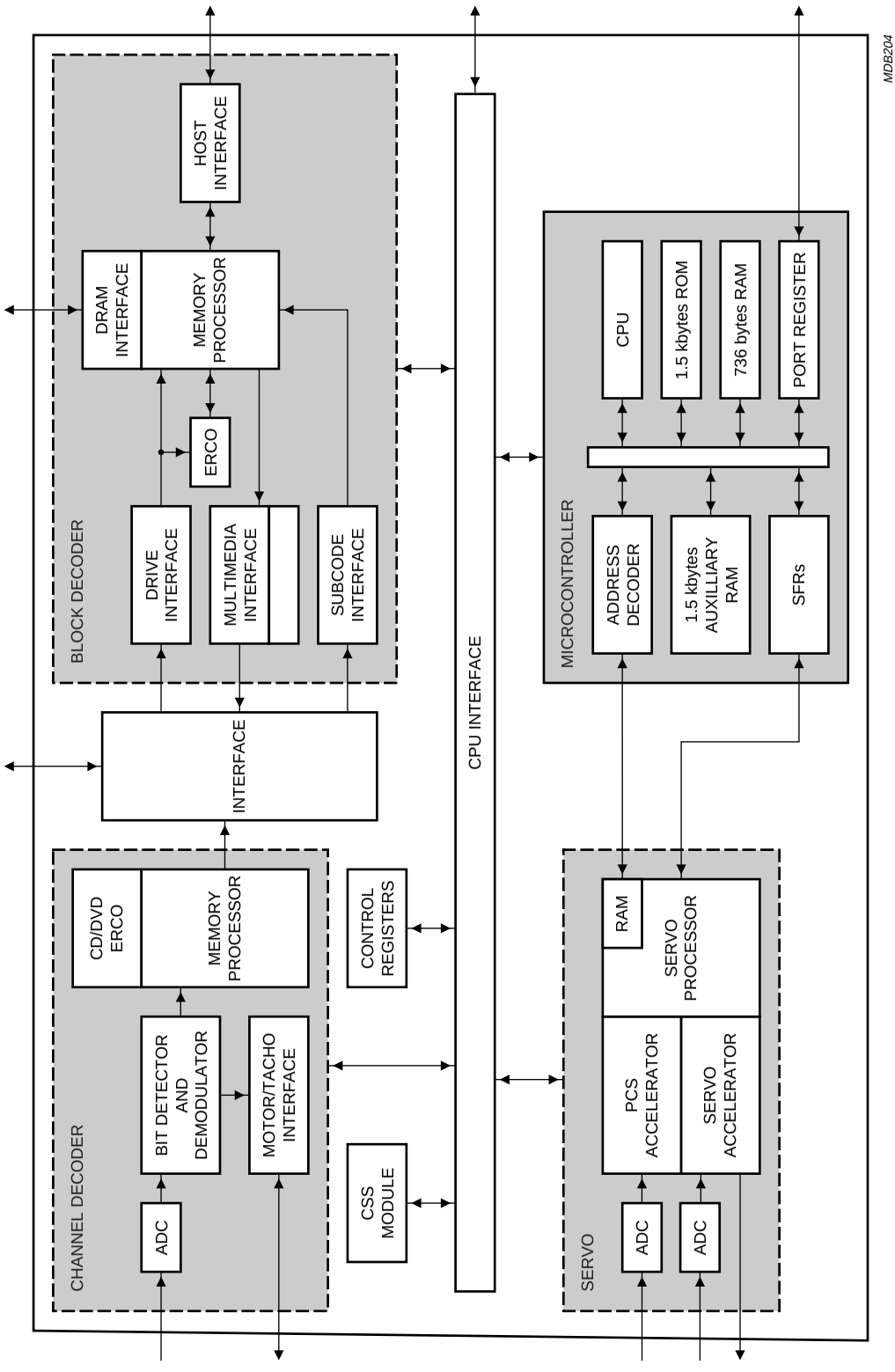


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
POR_NEG	1	I		Power-on reset input; active LOW
BCA	2	I		BCA input (mode 2 = SCCLK; mace_debug = opc_int)
MOTO1	3	O	M	motor control output
T1	4	I	T	tacho 1 input
T2	5	I	T	tacho 2 input
T3	6	I	T	tacho 3 input
$V_{DDD(P1)}$	7	P		digital supply voltage 1 for the pad cells (3.3 V)
$V_{SSD(P1)}$	8	P		digital ground 1 for the pad cells
TEST1	9	I		test input 1 (internal pull-down resistor)
TEST2	10	I		test input 2 (internal pull-down resistor)
V_{DDA1}	11	P		analog supply voltage 1 (3.3 V)
HFIN_DN	12	AI		negative differential HF input
HFIN_DP	13	AI		positive differential HF input
HFIN_SE	14	AI		single-ended HF input (AGC)
V_{SSA1}	15	P		analog ground 1
VCOM	16	AO		common mode reference output (TZA1035)
V_{DDA2}	17	P		analog supply voltage 2 (3.3 V)
ALPHA0	18	AO		DAC output
CRIN	19	AI		clock input
CROUT	20	AO		clock output
V_{SSA2}	21	P		analog ground 2
I_{REF}	22	AO		reference current output
UOPT	23	AI		upper reference input voltage for ADC ladder
SIN_PHI	24	AI		sine input from hall detectors
COS_PHI	25	AI		cosine input from hall detectors
XDET	26	AI		auxiliary ADC input
ACT_EMFP	27	AI		EMF of the actuator; positive input
ACT_EMFN	28	AI		EMF of the actuator; negative input
V_{DDA3}	29	P		analog supply voltage 3 (3.3 V)
UOPB	30	AI		decoupling point for ADC ladder
V_{SSA3}	31	P		analog ground 3
D1	32	AI		diode input 1
D2_TLN	33	AI		diode input 2/normal track-loss signal
D3_REN	34	AI		diode input 3/normal radial error signal
D4_FEN	35	AI		diode input 4/normal focus error signal
S1_MIRN	36	AI		satellite diode input 1/normal mirror signal
S2	37	AI		satellite diode input 2
V_{RIN}	38	AI/O		I/O reference voltage for servo ADC
FTCH	39	AI		track count input

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
$V_{SSD(P2)}$	40	P		digital ground 2 for the pad cells
$V_{DDD(P2)}$	41	P		digital supply voltage 2 for the pad cells (3.3 V)
P5_7_DEFO_N	42	B	M/T	defect output/general purpose I/O
P5_6_DEFI_N	43	B	M/T	defect input/general purpose I/O
P5_5_TL	44	B	M/T	track-loss measure output/general purpose I/O
P5_4_RP_FOK	45	B	M/T	radial polarity/focus OK/general purpose I/O
P5_3_CE1	46	B	M/T	CS external SRAM/general purpose I/O
P5_2_CLO	47	B	M/T	servo clock output/general purpose I/O
P5_1_SDA	48	B	M/T	I^2C-bus data/general purpose I/O
P5_0_SCL	49	B	M/T	I^2C-bus clock/general purpose I/O
SCCLK	50	O		internal/external microcontroller clock [mace_debug = int1 (PLUM)]
$V_{DDD(P3)}$	51	P		digital supply voltage 3 for the pad cells (3.3 V)
$V_{SSD(P3)}$	52	P		digital ground 3 for the pad cells
RA	53	O	M	radial output (3-state during reset)
FO	54	O	M	focus output (3-state during reset)
SL	55	O	M	sledge output (3-state during reset)
RAC_SW	56	O	M	disconnects radial actuator (1 = disconnect)
REF_SIN	57	O	M	PDM reference signal output; removes DC offset from sin_phi
REF_COS	58	O	M	PDM reference signal output; removes DC offset from cos_phi
$V_{DDD(P4)}$	59	P		digital supply voltage 4 for the pad cells (3.3 V)
$V_{SSD(P4)}$	60	P		digital ground 4 for the pad cells
P4_7_PXT2EN	61	B	M/T	timer 2 input enable/SILD for TZA1035
P4_6_PXT2	62	B	M/T	timer 2 clock input/SICL for TZA1035
P4_5_PXT0	63	B	M/T	timer 1 clock input/SIDA for TZA1035
P4_4_PXT	64	B	M/T	timer 0 clock input/CS2 for external device
P4_3_A19	65	B	M/T	general purpose I/O
P4_2_A18	66	B	M/T	general purpose I/O
$V_{DDD(C1)}$	67	P		digital supply voltage 1 for the core (1.8 V)
$V_{SSD(C1)}$	68	P		digital ground 1 for the core
UA0_P1_0	69	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 0
UA1_P1_1	70	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 1 (mode 3 = SCCLK)
UA2_P1_2	71	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 2 (mode 3 = OTD)
UA3_P1_3	72	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 3 (mode 3 = DEB_OUT)
UA4_P1_4	73	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 4 (mode 3 = MON_A)
UA5_P1_5	74	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 5 (mode 3 = MON_D)

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
UA6_P1_6	75	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 6 (mode 3 = vampire 6 to SYNC)
UA7_P1_7	76	B	M/T	Port 1; demultiplexed lower microcontroller address lines; bit 7 (mode 3 = vampire 7 to V4)
$V_{DDD(P5)}$	77	P		digital supply voltage 5 for the pad cells (3.3 V)
$V_{SSD(P5)}$	78	P		digital ground 5 for the pad cells
EAN_WAITN	79	B	M/T	address input/wait output (internal pull-up resistor)
DSDEN_SRST	80	O	M	microcontroller reset output [mace_debug = int0 (HDR66/PLUM)]
PSENN_CS	81	B	M/T	programmable strobe enable/output; enable for external device (internal pull-up resistor)
ALE_ASTB	82	B	M/T	address latch/chip select (internal pull-up resistor)
$V_{DDD(C2)}$	83	P		digital supply voltage 2 for the core (1.8 V)
$V_{SSD(C2)}$	84	P		digital ground 2 for the core
UA12	85	B	M/T	Port 2; upper microcontroller address line; bit 12
UA15	86	B	M/T	Port 2; upper microcontroller address line; bit 15
P4_0_A16	87	B	M/T	A16 to EPROM
P4_1_A17	88	B	M/T	A17 to EPROM
UA14	89	B	M/T	Port 2; upper microcontroller address line; bit 14
UA13	90	B	M/T	Port 2; upper microcontroller address line; bit 13
UA8	91	B	M/T	Port 2; upper microcontroller address line; bit 8
UA9	92	B	M/T	Port 2; upper microcontroller address line; bit 9
UA11	93	B	M/T	Port 2; upper microcontroller address line; bit 11
UA10	94	B	M/T	Port 2; upper microcontroller address line; bit 10
$V_{DDD(P6)}$	95	P		digital supply voltage 6 for the pad cells (3.3 V)
$V_{SSD(P6)}$	96	P		digital ground 6 for the pad cells
UDA7	97	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 7
UDA6	98	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 6
UDA5	99	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 5
UDA4	100	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 4
UDA3	101	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 3
UDA2	102	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 2
UDA1	103	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 1
UDA0	104	B	M/T	Port 0; multiplexed microcontroller data/lower address line; bit 0
$V_{DDD(P7)}$	105	P		digital supply voltage 7 for the pad cells (3.3 V)
$V_{SSD(P7)}$	106	P		digital ground 7 for the pad cells
P3_7_RDN	107	B	M/T	read signal input/general purpose I/O
P3_6_WRN	108	B	M/T	write signal output/general purpose I/O
P3_5_TXD2	109	B	M/T	UART 2 transmit line output/general purpose I/O
P3_4_RXD2	110	B	M/T	UART 2 receive line input/general purpose I/O
P3_3_INT1	111	B	M/T	interrupt 1 input/general purpose I/O

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
P3_2_INT0	112	B	M/T	interrupt 0 input/general purpose I/O
P3_1_TXD1	113	B	M/T	UART 1 transmit line output/general purpose I/O
P3_0_RXD1	114	B	M/T	UART 1 receive line input/general purpose I/O
$V_{DDD(C3)}$	115	P		digital supply voltage 3 for the core (1.8 V)
$V_{SSD(C3)}$	116	P		digital ground 3 for the core
HRESET	117	I		host reset input
DD7	118	B	AL/T	host interface/generic DMA; bit 7
DD8	119	B	AL/T	host interface/generic DMA; bit 8 (mode 1 = MEAS_CFLG)
DD6	120	B	AL/T	host interface/generic DMA; bit 6
DD9	121	B	AL/T	host interface/generic DMA; bit 9 (mode 1 = MEAS1)
DD5	122	B	AL/T	host interface/generic DMA; bit 5
DD10	123	B	AL/T	host interface/generic DMA; bit 10 (mode 1 = MON_A)
DD4	124	B	AL/T	host interface/generic DMA; bit 4
DD11	125	B	AL/T	host interface/generic DMA; bit 11 (mode 1 = MON_D)
$V_{DDD(P8)}$	126	P		digital supply voltage 8 for the pad cells (3.3 V)
$V_{SSD(P8)}$	127	P		digital ground 8 for the pad cells
DD3	128	B	AL/T	host interface/generic DMA; bit 3
DD12	129	B	AL/T	host interface/generic DMA; bit 12 (mode 1 = DEB_OUT)
DD2	130	B	AL/T	host interface/generic DMA; bit 2
DD13	131	B	AL/T	host interface/generic DMA; bit 13 (mode 1 = OTD)
DD1	132	B	AL/T	host interface/generic DMA; bit 1
DD14	133	B	AL/T	host interface/generic DMA; bit 14 (mode 1 = SCCLK)
DD0	134	B	AL/T	host interface/generic DMA; bit 0
DD15	135	B	AL/T	host interface/generic DMA; bit 15 (mace_debug = servo_int)
$V_{DDD(C4)}$	136	P		digital supply voltage 4 for the core (1.8 V)
$V_{SSD(C4)}$	137	P		digital ground 4 for the core
DMARQ_GACK	138	O	AL	host DMA request/generic DMA acknowledge
DIOW	139	I	T	host interface input write strobe
DIOR	140	I	T	host interface input read strobe
IORDY	141	O	AH	host interface ready output
DMACK_GRQ	142	I	T	host DMA acknowledge/generic DMA request input
INTRQ	143	O	AH	host interface interrupt request output
IOCS16	144	O	AH	host interface 8/16-bit Port output
DA1_GWR	145	B	AL/T	host address bit 1/generic write
$V_{DDD(P9)}$	146	P		digital supply voltage 9 for the pad cells (3.3 V)
$V_{SSD(P9)}$	147	P		digital ground 9 for the pad cells
PDIAG	148	B	AL/T	host interface passed test input/output (mode 1 = SYNC)
DA0	149	B	AL/T	host address bit 0 input/output
DA2_GRD	150	B	AL/T	host address bit 2/generic read
CS0	151	B	AL/T	host interface chip select 0 input/output

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
CS1	152	B	AL/T	host interface chip select 1 input/output
DASP	153	B	AL/T	host interface active slave present input/output (mode 1 = V4)
IECO_CL1	154	O	M	IEC 60958 output/CL1 output from HDR66
$V_{DDD(P10)}$	155	P		digital supply voltage 10 for the pad cells (3.3 V)
$V_{SSD(P10)}$	156	P		digital ground 10 for the pad cells
XDA3	157	O	L	DRAM address output; bit 3
XDA2	158	O	L	DRAM address output; bit 2
XDA1	159	O	L	DRAM address output; bit 1
XDA0	160	O	L	DRAM address output; bit 0
XDA10	161	O	L	DRAM address output; bit 10
$V_{DDD(P11)}$	162	P		digital supply voltage 11 for the pad cells (3.3 V)
$V_{SSD(P11)}$	163	P		digital ground 11 for the pad cells
XDD2	164	B	M/T	DRAM data bus input/output; bit 2
XDD1	165	B	M/T	DRAM data bus input/output; bit 1
XDD0	166	B	M/T	DRAM data bus input/output; bit 0
XDD3	167	B	M/T	DRAM data bus input/output; bit 3
XDD4	168	B	M/T	DRAM data bus input/output; bit 4
XDD5	169	B	M/T	DRAM data bus input/output; bit 5
XDD6	170	B	M/T	DRAM data bus input/output; bit 6
XDD7	171	B	M/T	DRAM data bus input/output; bit 7
$V_{DDD(C5)}$	172	P		digital supply voltage 5 for the core (1.8 V)
$V_{SSD(C5)}$	173	P		digital ground 5 for the core
LDQM	174	O	M	SDRAM data mask output LOW
XWR	175	O	M	DRAM write strobe output
XRAS	176	O	M	DRAM RAS strobe output
SDCS	177	O	M	SDRAM chip select output
XCAS	178	O	M	DRAM CAS strobe output
XDA12	179	O	M	DRAM address output; bit 12
XDA13	180	O	M	DRAM address output; bit 13
SDCK	181	O	L	SDRAM clock output
UDQM	182	O	M	SDRAM data mask output HIGH
$V_{DDD(P12)}$	183	P		digital supply voltage 12 for the pad cells (3.3 V)
$V_{SSD(P12)}$	184	P		digital ground 12 for the pad cells
XDD8	185	B	M/T	DRAM data bus input/output; bit 8
XDD9	186	B	M/T	DRAM data bus input/output; bit 9
XDD10	187	B	M/T	DRAM data bus input/output; bit 10
XDD11	188	B	M/T	DRAM data bus input/output; bit 11
XDD12	189	B	M/T	DRAM data bus input/output; bit 12
XDD15	190	B	M/T	DRAM data bus input/output; bit 15
XDD14	191	B	M/T	DRAM data bus input/output; bit 14

SYMBOL	PIN	TYPE[1]	DRIVE/ THRESHOLD	DESCRIPTION
XDD13	192	B	M/T	DRAM data bus input/output; bit 13
$V_{DDD(C6)}$	193	P		digital supply voltage 6 for the core (1.8 V)
$V_{SSD(C6)}$	194	P		digital ground 6 for the core
XDA11	195	O	M	DRAM address output; bit 11
XDA9	196	O	M	DRAM address output; bit 9
XDA8	197	O	M	DRAM address output; bit 8
XDA7	198	O	M	DRAM address output; bit 7
XDA6	199	O	M	DRAM address output; bit 6
XDA5	200	O	M	DRAM address output; bit 5
XDA4	201	O	M	DRAM address output; bit 4
$V_{DDD(P13)}$	202	P		digital supply voltage 13 for the pad cells (3.3 V)
$V_{SSD(P13)}$	203	P		digital ground 13 for the pad cells
FLAG	204	B	M/T	I^2S-bus flag input/output (mode 2 = DEB_OUT)
MCK	205	B	M/T	multimedia master clock input/output (mode 2 = MEAS_CFLG)
DATA_SDI	206	B	M/T	I^2S-bus data input/output (mode 2 = MON_A)
WCLK_WSI	207	B	M/T	I^2S-bus word clock input/output (mode 2 = MEAS1)
BCLK_SCKI	208	B	M/T	I^2S-bus bit clock input/output (mode 2 = MON_D)

Note

1. See Table 1 for the pin type definition.

Table 1 Pin type definition

TYPE	DEFINITION
I	input
O	output
OD	open-drain
B	bidirectional
T	3-state output
AI	analog input
AO	analog output
P	power connection; all supply pins must be connected to the same external power supply voltage

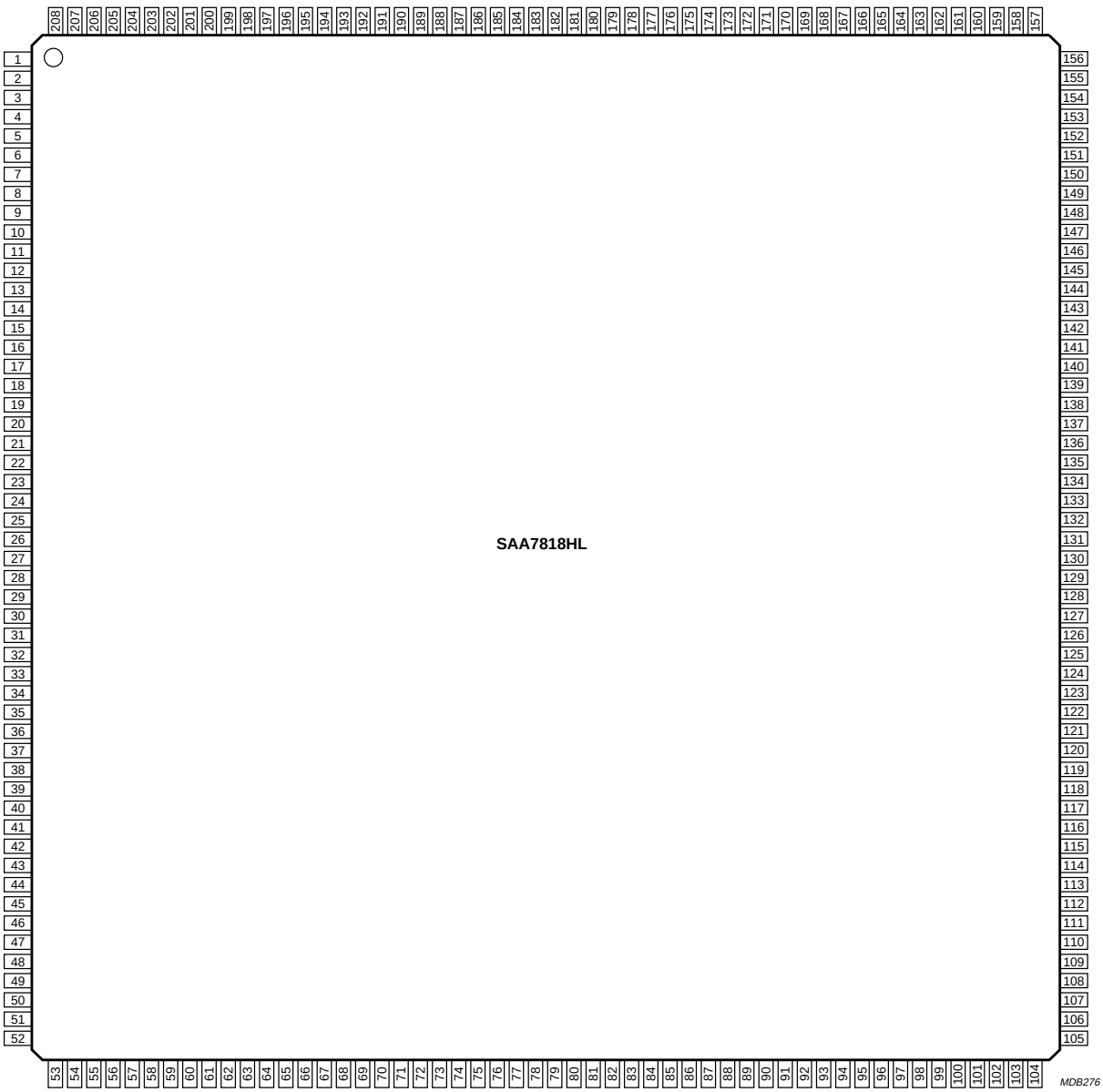


Fig.2 Pin configuration.

7 REGISTER/MEMORY MAP

The internal registers are SFRs within the address space of the internal microcontroller. They are accessed in the same way as standard 80C51 SFRs.

The external registers and memory spaces make up the external memory map of the internal microcontroller. Some of the memory spaces are on-chip and some are in the external DRAM. All registers are addressed as external memory space with respect to the internal microcontroller.

Table 2 Internal registers

ADDR (HEX)	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0080	P0	SP	DPL	DPH	–	–	–	PCON
0088	TCON	TMOD	TL0	TL1	TH0	TH1	–	–
0090	P1	–	–	–	–	–	–	–
0098	SCON	SBUF	–	–	–	–	CLK_GEN	DIV17
00A0	P2	P2SFR	–	–	–	–	–	–
00A8	–	–	INTLATCH	INTEN	–	–	–	–
00B0	P3	–	–	–	–	–	–	–
00B8	–	–	–	–	–	–	–	–
00C0	SCON2	SBUF2	–	–	–	–	–	–
00C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	–	–
00D0	TLS_CNTL	CSCNTRL	CSWAIT	–	–	–	–	–
00D8	SSR	SCR	–	–	–	–	–	–
00E0	ACC	–	–	–	–	–	–	–
00E8	PORT4	MD0	MD1	MD2	MD3	MD4	MD5	ARCON
00F0	–	–	DDR5	–	DACDEB	CONFIG4	CONFIG3	–
00F8	P5	DDR1	DDR4	DDR0	DDR2	DDR3	CONFIG	CONFIG2

Table 3 External registers/memory space

ADDR (HEX)	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0000	auxiliary RAM (internal)							
:								
05F8								
0600	external DRAM (PLUM subpage 1)							
:								
BFF8								
C000	TIME_KEEPER	FOC_STAT	RAD_STAT	MEM_ SLEDGE1_HI	DIST_LO	DIST_HI	MEM_ SLEDGE1_LO	RAD_INT_HI
C008	RAD_INT_LO	RAD_OFFSET _HI	RAD_ERROR_ GAIN_MEM_HI	TPI_GAIN_HI	FOCUS_ ERROR_MEM	RAD_ERROR_ MEM	SPEED_HI	SPEED_LO
C010	FOCUS_INT_ HI	FOCUS_INT_ LO	DROP_OUT_ CODE	FOC_PROP_ MEM	FOCUS_PROP _MULT	FOC_INT_ GAIN	RAMP_MEAN_ VALUE	SLEEP_MULT_ MEM
C018	RAMP_ HEIGHT	FE_LEVEL	TIMER	reserved	RAD_PROP_ MULT_MEM	RAD_ERROR_ ACC_MEM	RAD_INT_ GAIN_MEM	SPEED_MULT _MEM
C020	RAD_OFFSET _LO	RAD_ERROR_ GAIN_MEM_ LO	TPI_GAIN_LO	SP_MEM_LO	SP_MEM_HI	SPEED_ SETPOINT	TPI_SIGNAL_ MEM	RAD_CTRL_1_ MEM2
C028	RAD_CTRL_1_ MEM	reserved	RAD_GAIN_ MEM	STACK5	STACK4	STACK3	STACK2	STACK1
C030	STACK0	OLDCOM	STATE_MULT_ MEM	MEM_SLEDGE 2_LO	MEM_SLEDGE 2_HI	RAMP_INCR	SLEDGE_ MULT_MEM2	FAST_SPEED
C038	MEM_SLEDGE 2_LO_LO	reserved	reserved	SLEDGE_OUT _MEM	reserved	reserved	reserved	FOCUS_INT_ MEM1
C040	INTERRUPT REG	reserved	reserved	SLEDGE_PUL SE_MEM	reserved	SPEED_DREM PEL_MEM	HOLD_MULT_ MEM	XTRA_ PRESET
C048	reserved	reserved	reserved	reserved	SLEDGE_ LONG_BRAKE	reserved	SLEDGE_ POWER_MEM	RAD_MEM_ PART1
C050	SLEDGE_PUL SE_HEIGHT	FOCUS_ INJECT	RADIAL_ INJECT	DET_PHASE	AGCFREQ	INJECTLEVEL 1	INJECTLEVEL 2	OSC
C058	AGCGAINMEM	AGCGAINLO	FOCUS_ OFFSET_AGC	INJECT_LO	OFFTRACK_HI	OFFTRACK_MI	OFFTRACK_ LO	MIRN_MEM
C060	PCS_STAT	START_LO	START_HI	LOC_LO	LOC_MI	LOC_HI	ACT_FF	PCS_FF_ STROKE

ADDR (HEX)	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
C068	PCS_SPEED_GAIN	SPEED_SETPOINT_LO	SPEED_SETPOINT_HI	reserved	reserved	PCS_PD	PCS_PD_INT	PCS_PD_INT_LO
C070	PCS_ACC_STEP	PCS_ACC_JUMP	VEL_ROOT_HI	VEL_ROOT_LO	PCS_STP_POS	PCS_STP_NEG	FOCUS_OFFSET	PROT_STAT
C078	RE_FILTER_MEM	FE_FILTER_MEM	RE_DET_LEVEL	FE_DET_LEVEL	EMFREAD_MEM	EMF_DAMP_MEM	RACSWITCH_MEM	PCS_SEN
C080	reserved							
:								
C0A8								
C0B0	ARC_STAT	ARC_FOC_IN	ARC_RAD_IN	ARC_FOC_OUT	ARC_RAD_OUT	ARC_FOC_DIFF	ARC_RAD_DIFF	ARC_ANG
C0B8	DEFECTCNTRL1	DEFECTCNTRL2	DEFECTCNTRL3	HF_ENVELOPE	ALPHA0_DAC	CONTROL_REG	CALF_FORMAT	CNF_TEST_VALUE
C0C0	MIR_FIL_BLACK_HI	MIR_FIL_BLACK_LO	MIR_FIL_WHITE_HI	MIR_FIL_WHITE_LO	REG_FBK_BLACK_HI	REG_FBK_BLACK_LO	REG_FBK_WHITE_HI	REG_FBK_WHITE_LO
C0C8	CALF_PROBE_HI	CALF_PROBE_LO	reserved	reserved	reserved	reserved	reserved	reserved
C0D0	TLSLICECNTR	DECAY_RATE	ACTUAL_DIFF	FORCED_DIFF	AUX_ADC	PCS_HALL_PH	PEAK_PROBE	BOTTOM_PROBE
C0D8	PP_TPI_PROBE	reserved	PP_TPI_FIL_PROBE_HI	PP_TPI_FIL_PROBE_LO	reserved	reserved	DEFECT_COUNTER	DEFECT_SIGNALS
C0E0	OPC_STAT	OPC_CTRL1	OPC_CTRL2	OPC_REPEAT	OPC_DELAY	OPC_ADR_START	OPC_ADR_STOP	OPC_ALPHA0_START
C0E8	OPC_ALHPA0_STEP	OPC_PW_LPF	OPC_EMFH	OPC_EMFL	OPC_DEL_ACT	OPC_TIML	OPC_TIMH	reserved
C0F0	DEBUG0	DEBUG1	DEBUG2	DEBUG3	reserved	reserved	reserved	reserved
C0F8	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
C100	inaccessible							
:								
CFF8								
D000	external DRAM (PLUM subpage 2)							
:								
DFF8								

ADDR (HEX)	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
E000	external DRAM (PLUM subseg n)							
:								
FCF8								
FD00	BUFFERBASE		BUFFERTOP		TAGGED_CNT/TAGGED_CNT_UPD		UNTAGGED_CNT/UNTAGGED_CNT_UPD	
FD08	ACQ_AUTO_CTRL	STRMSTRTADDR			STRMSTOPADDR			ACQAUTO_INT
FD10	ACQAUTO_INTEN	NXTXFR_ADDR			ENDXFR_ADDR/REM_CNT			BYTESPERSECTOR(L)
FD18	BYTESPERSECTOR(H)	TAGSCAN_MASK	TAGSCAN_VALUE	MHEAD			ACQMISS_STAT	HOST_AUTO_CTRL
FD20	MATHPROC	TAGSCAN_CNTL	TAGSCAN_OFFS_H	TAGSCAN_OFFS_L	MATCHED_COUNT	reserved		
FD28	reserved							
:								
FD50								
FD58	reserved		DRAM_MODE/DRAM_FEAT/DRAM_COLW	reserved				
FD60	reserved							
FD68								
FD70	CAM_CMD/CAM_STAT	CAM_DAT	reserved					
FD78	reserved							
FD80	AGCBW	AGCTHR_HI	AGCTHR_LO	AGCTHR_HI2	AGC_TIMHI	HF_AMPLITUDE	AGC_SET	DEFIRA0
FD88	DEFIRA1	DEFIRA2	DEFIRA3	HIGHPASS	OFFSETCONT	OFFSETDATA	OFFSETBOUND	OFFSETSETTING
FD90	SIFCONTROL	SERIF1	SERIF2	SERIF3	HF_DETECT1	HF_DETECT2	HF_DETECT3	AGCDAC_DIV
FD98	OFFSET_LVL	HFMAX_PEAK	HFMIN_PEAK	HF_DETECT4	DECSTATUS3	HF_DETECT5	HF_DETECT6	OFFSETBW
FDA0	GLUE1	PORTADATA/PORTAREAD	PORTAMODE	reserved	DC_CONTROL	DC_VALUE	D1_OFFSET	D2_OFFSET

ADDR (HEX)	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
FDA8	D3_OFFSET	D4_OFFSET	S1_OFFSET	S2_OFFSET	DEMOD_ DCOD_ CONTROL	ENVELOPE_ CONTROL	CLIPLEVEL_ LE	GAIN_LE
FDB0	SWITCH_LE	LAST_GOOD_ HEADER	CONTROL_AD _STORAGE	LAST_GOOD_ ADDRESS	reserved			
FDB8	reserved							
FFC0	CHPLL_LOCK/ PLL_FREQ_R	CHPLL_SET/C HPLL_ASYM	CHPLL_FREQ/ CHPLL_JIT	CHPLL_EQU/C HPLL_LOCK_ IN	CHPLL_F_ME AS/CHPLL_ AVG_JIT	OUTPUT1	reserved	OUTPUT3
FFC8	CLOCKPRE2	SEMA2	MEAS_OUT_E N/AGC_GAIN	INT_EN/INT_ STAT	MOTOR1/ SLICE1	MOTOR2/ EYE_OPEN	MOTOR3/ TACHO4	MOTOR4
FFD0	MOTOR5	MOTOR6	CLOCKPRE1/ SUB_C_STAT	DECOMODE/ SUB_C_DATA	HFPLLMINMA X/SUB_C_END	ANASET/ FIFOFILL	VITSET/ BCASTAT	TACHO1/ BCADATA
FFD8	TACHO2	TACHO3	BCASET	SRESET	CHPLL_SET_2	MOTOR7	reserved	ANASET2
FFE0	reserved							
FFE8	reserved	HFDEFECTST ATUS	reserved		HFDEFECTDA TA	HFDEFECTDA TAEND	reserved	
FFF0	reserved							
FFF8	reserved	C1BLER	C2BLER	reserved				

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDD(P)}$	digital supply voltage for the pad cells (3 V)	notes 1 and 2	–0.5	+4.0	V
$V_{DDD(C)}$	digital supply voltage for the core (1.8 V)	note 2	1.65	1.95	V
V_{DDA}	analog supply voltage	note 2	–0.5	+4.0	V
$V_{I(max)}$	input voltage on any input		–0.5	V_{DD} + 0.5	V
V_O	output voltage on any output		–0.5	+6.5	V
I_O	output current	continuous	–	20	mA
I_{IK}	DC input diode current	continuous	–	20	mA
T_{stg}	storage temperature		–55	+125	°C
V_{esd}	electrostatic discharge voltage	human body model; note 3	–1000	+2000	V
		machine model; note 4	–200	+200	V

Notes

1. All pad supply connections [$V_{DDD(P)}$] must be made externally to the same power supply.
2. All V_{SS} pins must be connected to the same external voltage.
3. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
4. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

9 CHARACTERISTICS

$V_{DDD(P)}$ = 3.0 to 3.6 V; $V_{DDD(C)}$ = 1.65 to 1.95 V; V_{DDA} = 3.0 to 3.6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDD(C)}$	digital supply voltage for the core		1.65	1.8	1.95	V
$V_{DDD(P)}$	digital supply voltage for the pad cells		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
$I_{DDD(C)}$	digital supply current for the core	$V_{DDD(C)}$ = 1.8 V	–	55	–	mA
$I_{DDD(P)}$	digital supply current for the pad cells	$V_{DDD(P)}$ = 3.3 V	–	135	–	mA
I_{DDA}	analog supply current	V_{DDA} = 3.3 V	–	65	–	mA
Analog blocks ($V_{DDD(P)}$ = 3.3 V, $V_{DDD(C)}$ = 1.8 V, V_{DDA} = 3.3 V, V_{SS} = 0 and T_{amb} = 25 °C)						
PIN: I_{REF}						
V_{IREF}	reference voltage on pin I_{REF}		1.16	1.26	1.36	V
R_{IREF}	external resistor on pin I_{REF} (±1%)		–	24	–	kΩ
I_{IREF}	output current from pin I_{REF}		47	50	53	μA
PIN: VCOM						
V_{VCOM}	common mode reference voltage		1.08	1.2	1.32	V
Z_o	output impedance		–	–	10	Ω
C_{ext}	external capacitor on pin VCOM		47	–	–	nF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PINS: HFIN_DN AND HFIN_DP						
f_{clk}	clock sample rate		–	–	100	MHz
B	recovered bandwidth	1/3 Nyquist	–	46.6	–	MHz
ENOB	effective number of bits	at 100 MHz	–	7	–	
$V_{i(dif)(p-p)}$	differential input signal (peak-to-peak value)	0 dB; depends on V_{DDA}	–	2.0	$\frac{2.0V_{DDA}}{3.3}$	V
$V_{dif(offset)}$	differential offset voltage	V_{HFIN_DP} to V_{HFIN_DN}	–100	–	+100	mV
$V_{cm(offset)}$	common mode offset voltage		–200	–	+100	mV
$V_{ADC(offset)}$	ADC offset voltage		–60	–	+60	mV
$C_{i(stat)}$	static input capacitance	input to ground	–	7	–	pF
		input to input	–	3	–	pF
R_i	input resistance		–	infinite	–	kΩ
$t_{d(g)}$	group delay		–	–	100	ps
PIN: HFIN_SE						
f_{clk}	clock sample rate		–	–	100	MHz
B	recovered bandwidth		–	35	–	MHz
G	AGC gain range	32 steps	–2.1	–	+11.4	dB
THD	total harmonic distortion	f_{sig} = 25 MHz; at V_{dif} = 1.4 V (p-p)	–	–	–35	dB
S/N	signal-to-noise and distortion of AGC		–	50	–	dB
$V_{i(se)(p-p)}$	single-ended input signal (peak-to-peak value)	0 dB; depends on V_{DDA1}	–	1.4	$\frac{1.4V_{DDA}}{3.3}$	V
$C_{i(stat)}$	static input capacitance	input to ground	–	7	–	pF
R_i	input resistance		–	8.6	–	kΩ
$t_{d(g)}$	group delay flatness	0 to 35 MHz	–	–	600	ps
PINS: D1, D2_TLN, D3_REN, D4_FEN, S1_MIRN AND S2						
$I_{IO(max)}$	maximum input/output current	selectable via gain; note 1	1	–	16	μA
V_i	input voltage		–	V_{VRIN}	–	V
G_{tol}	gain tolerance		–20	0	+20	%
ΔG	variation of gain between channels					
	pins D1 to D2_TLN and D3_REN to D4_FEN		–4.5	–	+4.5	%
	pins S1_MIRN to S2		–6	–	+6	%
$C_{pcb(max)}$	maximum parasitic capacitance connected to input		–	–	25	pF
f_{clk}	sample rate		–	8.4672	–	MHz
B	recovered bandwidth		–	20	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	I_{sink} or I_{source} = 6 μA	–	–	–40	dB
DR	dynamic range	I_{sink} or I_{source} = 6 μA	50	–	–	dB
PIN: VRIN						
$V_{o(VRIN)}$	voltage on VRIN driving output		1.0	1.2	$0.5V_{DDA2}$ + 0.1	V
$V_{i(VRIN)}$	input voltage on VRIN		1.0	–	$0.5V_{DDA2}$ + 0.1	V
PIN: FTCH						
$V_{FTC(offset)}$	comparator FTC offset voltage		–20	–	+20	mV
$V_{FTC(hys)}$	comparator FTC hysteresis		–10	–	+10	mV
V_{cm}	common mode voltage		–	1.67	–	V
f_{clk}	clock sample rate		–	8.4672	–	MHz
$C_{i(stat)}$	static input capacitance	input to ground	–	7	–	pF
R_i	input resistance		100	–	–	kΩ
PINS: UOPB AND UOPT						
$V_{i(UOPB)}$	input voltage on pin UOPB		–	1	–	V
$V_{i(UOPT)}$	input voltage on pin UOPT		–	2.6	–	V
PINS: ACT_EMFP AND ACT_EMFN						
V_i	input voltage		0	–	V_{UOPT}	V
V_{cm}	common mode voltage		–	0	–	V
G	gain	note 2	–	5	–	V
B	bandwidth		–	265	–	kHz
R_i	input resistance		80	100	120	kΩ
$C_{i(stat)}$	input capacitance (static)		–	7	–	pF
PINS: SIN_PHI, COS_PHI, XDET AND ACT_EMFP; NOTE 3						
V_i	input voltage		0	–	V_{UOPT}	V
ΔG	gain matching between channels		–1	–	+1	%
R_i	input resistance		–	∞	–	kΩ
$C_{i(stat)}$	static input capacitance		–	7	–	pF
$C_{i(dyn)}$	dynamic input capacitance		–	5	–	pF
f_{clk}	sample rate		–	1.05	–	MHz
B	recovered bandwidth		5	–	–	kHz
ENOB	effective number of bits	at 1.05 MHz	–	7.2	–	
$CODE_{min(Vin)}$	output code for minimum V_{UOPB} input		0	5	10	
$CODE_{max(Vin)}$	output code for maximum V_{UOPT} input		251	253	255	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PIN: ALPHA0						
f_{clk}	sample rate		–	1.05	–	MHz
V_o	output voltage		0	–	V_{UOPT}	V
C_L	load capacitance		–	–	25	pF
R_L	load resistance		10	–	30	kΩ
CLOCK MULTIPLIERS						
f_{ref}	reference frequency		8	8.4672	17	MHz
MULT	multiplication ratios		5	–	24	
f_{out}	valid output frequencies		42.336	–	203.2128	MHz
$J_{clk(rms)}$	clock jitter (RMS value)		–	–	150	ps
t_{set}	settling time of clock		–	–	60	µs
Digital input						
INPUT: PORE_NEG, HRESET AND BCA (SCHMITT-TRIGGER INPUTS); TTL INPUT WITH HYSTERESIS						
$V_{th(r)}$	switching threshold rising		1.4	–	1.9	V
$V_{th(f)}$	switching threshold falling		0.9	–	1.45	V
V_{hys}	hysteresis voltage		0.4	–	0.7	V
C_i	input capacitance		–	–	10	pF
INPUT: DESIGNATED BY 'T'; TTL INPUT						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_{LI}	input leakage current	$V_i = 0 – V_{DDD(P)}$; note 4	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
Digital output						
OUTPUTS: DESIGNATED BY 'L' (CMOS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	$0.85V_{DDD(P)}$	–	–	V
C_L	load capacitance		–	–	20	pF
$t_{o(r)}$	output rise time	20% to 80% levels; C_L = 10 pF	–	1.0	–	ns
$t_{o(f)}$	output fall time	80% to 20% levels; C_L = 10 pF	–	1.0	–	ns
OUTPUTS: DESIGNATED BY 'M' (CMOS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.85V_{DDD(P)}$	–	–	V
C_L	load capacitance		–	–	20	pF
$t_{o(r)}$	output rise time	20% to 80% levels; C_L = 10 pF	–	0.9	–	ns
$t_{o(f)}$	output fall time	80% to 20% levels; C_L = 10 pF	–	0.9	–	ns
I_{LO}	3-state leakage current	$V_i = 0$ to $V_{DDD(P)}$	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUTS: DESIGNATED BY 'H' (CMOS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA	$0.85V_{DDD(P)}$	–	–	V
C_L	load capacitance		–	–	20	pF
$t_{o(r)}$	output rise time	20% to 80% levels; C_L = 10 pF	–	0.8	–	ns
$t_{o(f)}$	output fall time	80% to 20% levels; C_L = 10 pF	–	0.8	–	ns
I_{LO}	3-state leakage current	V_i = 0 to $V_{DDD(P)}$	–10	–	+10	µA
OUTPUTS: DESIGNATED BY 'AL' (ATA DATA BUS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.9V_{DDD(P)}$	–	–	V
C_L	load capacitance		–	–	100	pF
$t_{o(r)}$	output rise time	0.5 V to $0.9V_{DDD(P)}$; C_L = 100 pF	5	–	–	ns
$t_{o(f)}$	output fall time	$0.9V_{DDD(P)}$ to 0.5 V; C_L = 100 pF	5	–	–	ns
OUTPUTS: DESIGNATED BY 'AH' (ATA LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 12 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.9V_{DDD(P)}$	–	–	V
C_L	load capacitance		–	–	100	pF
$t_{o(r)}$	output rise time	0.5 V to $0.9V_{DDD(P)}$; C_L = 100 pF	5	–	–	ns
$t_{o(f)}$	output fall time	$0.9V_{DDD(P)}$ to 0.5 V; C_L = 100 pF	5	–	–	ns
INPUT: CRIN (EXTERNAL CLOCK)						
V_{IL}	LOW-level input voltage		–0.3	–	+0.5	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDA} + 0.3	V
t_{IH}	input high time	relative to period	45	–	55	%
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	7	pF

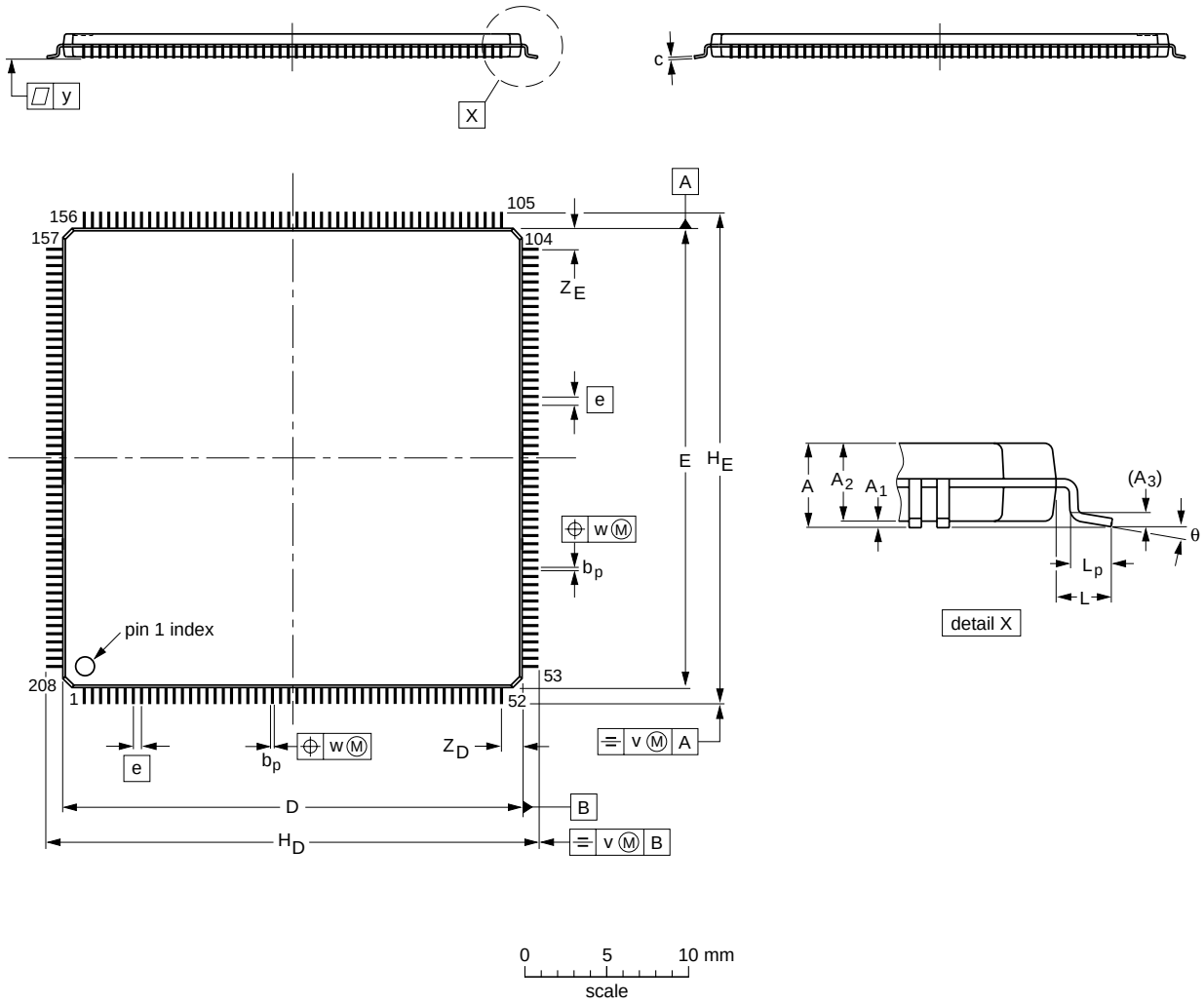
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT: CROUT						
f_{xtal}	crystal frequency	note 5	–	8.4672	–	MHz
g_m	mutual conductance at start-up		–	17	–	mA/V
C_{fb}	feedback capacitance		–	–	2	pF
C_o	output capacitance		–	–	7	pF
R_{bias}	internal bias resistor		–	200	–	kΩ

Notes

1. Clips at maximum gain setting; input can handle 2 × the maximum signal amplitude.
2. Gain depends on application components.
3. Operating in bypass mode.
4. Input leakage does not apply to EAN_WAITN, PSENN_CS and ALE_STB, as these pins have internal pull-up resistors.
5. It is recommended that the nominal running series resistance of the crystal or ceramic resonator is ≤60 Ω.

10 PACKAGE OUTLINE

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

11 SOLDERING

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 mm^3 so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 mm^3 so called small/thin packages.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

12 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

13 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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