

# Motorola Semiconductor Technical Data

## Addendum to MC68HC908BD48 Technical Data

This addendum provides corrections to:

*MC68HC908BD48 Technical Data* (Motorola document number  
MC68HC908BD48/D Rev. 1.0)


**Page 274:** Add VSYNC and HSYNC; and change LVI parameters in  
21.6 DC Electrical Characteristics.

**From:**

Characteristic	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Input High Voltage All ports, $\overline{\text{IRQ}}$ , $\overline{\text{RST}}$ , OSC1	$V_{\text{IH}}$	$0.7 \times V_{\text{DD}}$	—	$V_{\text{DD}}$	V
Input Low Voltage All ports, $\overline{\text{IRQ}}$ , $\overline{\text{RST}}$ , OSC1	$V_{\text{IL}}$	$V_{\text{SS}}$	—	$0.2 \times V_{\text{DD}}$	V
Low-Voltage Inhibit, trip falling voltage	$V_{\text{TRIPF}}$	3.5	3.8	4.5	V
Low-Voltage Inhibit, trip rising voltage	$V_{\text{TRIPR}}$	3.5	4.0	4.5	V

**To:**

Characteristic	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Input High Voltage All ports, $\overline{\text{IRQ}}$ , $\overline{\text{RST}}$ , OSC1 VSYNC, HSYNC	$V_{\text{IH}}$	$0.7 \times V_{\text{DD}}$ 2.0	—	$V_{\text{DD}}$ $V_{\text{DD}}$	V
Input Low Voltage All ports, $\overline{\text{IRQ}}$ , $\overline{\text{RST}}$ , OSC1 VSYNC, HSYNC	$V_{\text{IL}}$	$V_{\text{SS}}$ $V_{\text{SS}}$	—	$0.2 \times V_{\text{DD}}$ 0.8	V
Low-Voltage Inhibit, trip falling voltage	$V_{\text{TRIPF}}$	3.4	3.6	3.8	V
Low-Voltage Inhibit, trip rising voltage	$V_{\text{TRIPR}}$	3.6	3.8	4.0	V

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