Constant-Current/ Constant-Voltage 2A Battery Charger with Input Current Limiting

March 1999

FEATURES

- **Simple Design to Charge NiCd, NiMH and Lithium Rechargeable Batteries—Charging Current Programmed by Resistors or DAC**
- **Adapter Current Limit Allows Maximum Possible Charging Current During System Use***
- **Precision 0.5% Accuracy for Voltage Mode Charging**
- High Efficiency Current Mode PWM with 3A Internal Switch
- 5% Charging Current Accuracy
- Adjustable Undervoltage Lockout
- Automatic Shutdown When AC Adapter is Removed
- Low Reverse Battery Drain Current: 3μA
- Current Sensing Can Be at Either Terminal of the Battery
- Charging Current Soft Start
- Shutdown Control
- Available in 28-Lead Narrow SSOP Package

APPLICATIONS

- Chargers for NiCd, NiMH, Lead-Acid, Lithium Rechargeable Batteries
- Switching Regulators with Precision Current Limit

*US patent number 5,723,970

**See LT1510 for 1.5A Charger

DESCRIPTION

The LT®1769 current mode PWM battery charger is the simplest, most efficient solution to fast charge modern rechargeable batteries including lithium-ion (Li-Ion), nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd) that require constant-current and/or constant-voltage charging. The internal switch is capable of delivering 2A** DC current (3A peak current). Full-charging current can be programmed by resistors or a DAC to within 5%. With 0.5% reference voltage accuracy, the LT1769 meets the critical constant-voltage charging requirement for Li-Ion cells.

A third control loop is provided to regulate the current drawn from the AC adapter. This allows simultaneous operation of the equipment and battery charging without overloading the adapter. Charging current is reduced to keep the adapter current within specified levels.

The LT1769 can charge batteries ranging from 1V to 20V. Ground sensing of current is not required and the battery's negative terminal can be tied directly to ground. A saturating switch running at 200kHz gives high charging efficiency and small inductor size. A blocking diode is not required between the chip and the battery because the chip goes into sleep mode and drains only 3μA when the wall adapter is unplugged.

TYPICAL APPLICATION

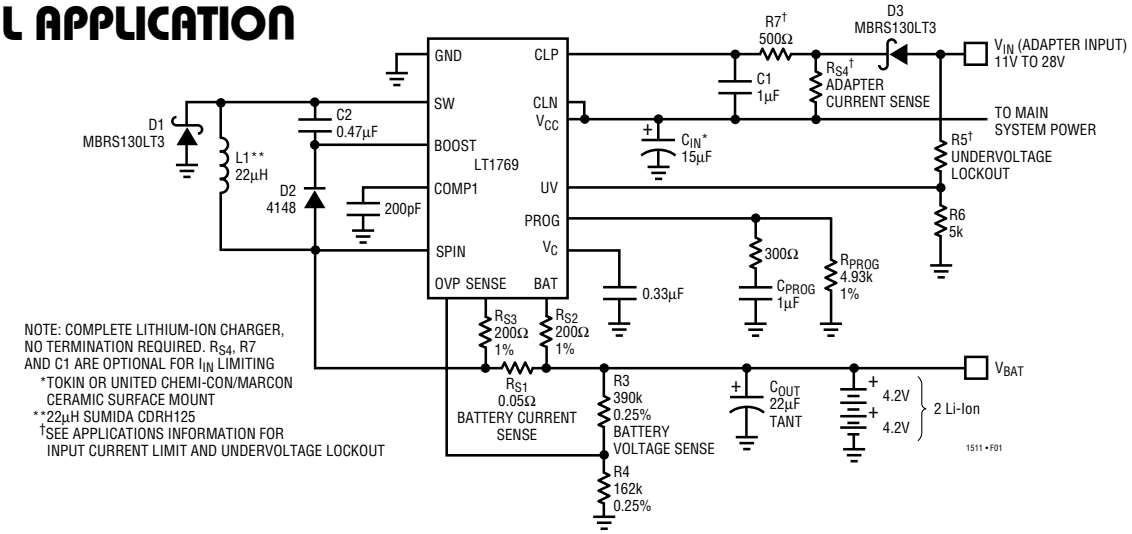


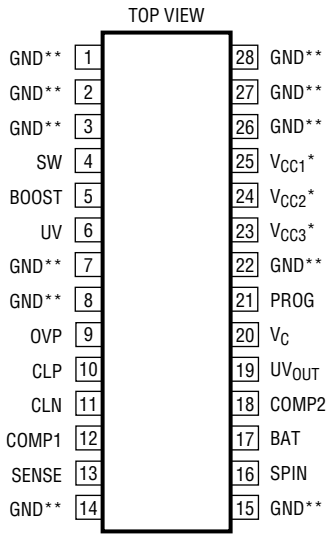
Figure 1. 2A Lithium-Ion Battery Charger

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
(V_{MAX}, CLP and CLN Pin Voltage) 30V
Switch Voltage with Respect to GND ..... –3V
Boost Pin Voltage with Respect to V_{CC} 25V
Boost Pin Voltage with Respect to GND 57V
Boost Pin Voltage with Respect to SW Pin 30V
V_C, PROG, OVP Pin Voltage 8V
I_{BAT} (Average) 2A
Switch Current (Peak) 3A
Operating Junction Temperature Range
Commercial ..... 0°C to 125°C
Industrial ..... –40°C to 125°C
Operating Ambient Temperature
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 35°C/W**

ORDER PART NUMBER

LT1769CGN
LT1769IGN

*ALL V_{CC} PINS SHOULD BE CONNECTED TOGETHER CLOSE TO THE PINS

** ALL GND PINS ARE FUSED TO INTERNAL DIE ATTACH PADDLE FOR HEAT SINKING. CONNECT THESE PINS TO EXPANDED PC LANDS FOR PROPER HEAT SINKING. 35°C/W THERMAL RESISTANCE ASSUMES AN INTERNAL GROUND PLANE DOUBLING AS A HEAT SPREADER

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 16V, V_{BAT} = 8V, V_{MAX} (maximum operating V_{CC}) = 28V, R_{S2} = R_{S3} = 200Ω (see Block Diagram), V_{CLN} = V_{CC}. No load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current	V_{PROG} = 2.7V, $V_{CC} \le$ 20V	●		4.5	6.8	mA
	V_{PROG} = 2.7V, 20V < $V_{CC} \le$ 25V	●		4.6	7.0	mA
Sense Amplifier CA1 Gain and Input Offset Voltage (With R_{S2} = 200Ω, R_{S3} = 200Ω) (Measured across R_{S1})(Note 2)	8V ≤ V_{CC} ≤ 25V , 0V ≤ V_{BAT} ≤ 20V					
	R_{PROG} = 4.93k	●	95	100	105	mV
	R_{PROG} = 49.3k	●	8	10	12	mV
	T_J < 0°C		7		12	mV
	V_{CC} = 28V, V_{BAT} = 20V					
	R_{PROG} = 4.93k	●	90		110	mV
	R_{PROG} = 49.3k	●	7		13	mV
	T_J < 0°C		6		14	mV
V_{CC} Undervoltage Lockout (Switch OFF) Threshold	Measured at UV Pin	●	6	7	8	V
UV Pin Input Current	0.2V ≤ V_{UV} ≤ 8V	●		0.1	5	µA
UV Output Voltage at UV_{OUT} Pin	In Undervoltage State, I_{UVOUT} = 70µA	●		0.1	0.5	V
UV Output Leakage Current at UV_{OUT} Pin	8V ≤ V_{UV}, V_{UVOUT} = 5V	●		0.1	3	µA
Reverse Current from Battery (When V_{CC} Is Not Connected, V_{SW} Is Floating)	$V_{BAT} \le$ 20V, $V_{UV} \le$ 0.4V			3	15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 16V, V_{BAT} = 8V, V_{MAX} (maximum operating V_{CC}) = 28V, R_{S2} = R_{S3} = 200Ω (see Block Diagram), V_{CLN} = V_{CC}. No load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Boost Pin Current	V_{CC} = 20V, V_{BOOST} = 0V			0.1	10	µA
	V_{CC} = 28V, V_{BOOST} = 0V			0.25	20	µA
	2V ≤ V_{BOOST} – V_{CC} < 8V (Switch ON)			6	9	mA
	8V ≤ V_{BOOST} – V_{CC} ≤ 25V (Switch ON)			8	12	mA
Switch						
Switch ON Resistance	8V ≤ V_{CC} ≤ V_{MAX}, I_{SW} = 2A, V_{BOOST} – V_{SW} ≥ 2V	●		0.15	0.25	Ω
$\Delta I_{BOOST}/\Delta I_{SW}$ During Switch ON	V_{BOOST} = 24V, I_{SW} ≤ 2A			25	35	mA/A
Switch OFF Leakage Current	V_{SW} = 0V, V_{CC} ≤ 20V	●		2	100	µA
	20V < V_{CC} ≤ 28V	●		4	200	µA
Minimum I_{PROG} for Switch ON		●	2	4	20	µA
Minimum I_{PROG} for Switch OFF at V_{PROG} ≤ 1V		●	1	2.4		mA
Maximum V_{BAT} for Switch ON		●			V_{CC} – 2	V
Current Sense Amplifier CA1 Inputs (Sense, BAT)						
Input Bias Current		●		–50	–125	µA
Input Common Mode Low		●	–0.25			V
Input Common Mode High		●			V_{CC} – 2	V
SPIN Input Current				–100	–200	µA
Reference						
Reference Voltage (Note 3)	R_{PROG} = 4.93k, Measured at OVP with VA Supplying I_{PROG} and Switch OFF		2.448	2.465	2.477	V
Reference Voltage	All Conditions of V_{CC}, T_J ≥ 0°C	●	2.441		2.489	V
	T_J < 0°C (Note 4)	●	2.43		2.489	V
Oscillator						
Switching Frequency			180	200	220	kHz
Switching Frequency	All Conditions of V_{CC}, T_J ≥ 0°C	●	170	200	230	kHz
	T_J < 0°C	●	160		230	kHz
Maximum Duty Cycle		●	85			%
	T_A = 25°C		90	93		%
Current Amplifier CA2						
Transconductance	V_C = 1V, I_{VC} = ±1µA		150	250	550	µmho
Maximum V_C for Switch OFF		●			0.6	V
I_{VC} Current (Out of Pin)	V_C ≥ 0.6V				100	µA
	V_C < 0.45V				3	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 16V, V_{BAT} = 8V, V_{MAX} (maximum operating V_{CC}) = 28V. No load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Amplifier VA						
Transconductance (Note 3)	Output Current from 50µA to 500µA		0.25	0.6	1.3	mho
Output Source Current	V_{OVP} = V_{REF} + 10mV, V_{PROG} = V_{REF} + 10mV		1.1			mA
OVP Input Bias Current	At 0.75mA VA Output Current At 0.75mA VA Output Current, T_J > 90°C		 –10	±3	±10 25	nA nA
Current Limit Amplifier CL1, 8V ≤ Input Common Mode						
Turn-On Threshold	0.75mA Output Current		93	100	107	mV
Transconductance	Output Current from 50µA to 500µA		0.5	1	2	mho
CLP Input Current	0.75mA Output Current, V_{UV} ≥ 0.4V			0.3	1	µA
CLN Input Current	0.75mA Output Current V_{UV} ≥ 0.4V			0.8	2	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

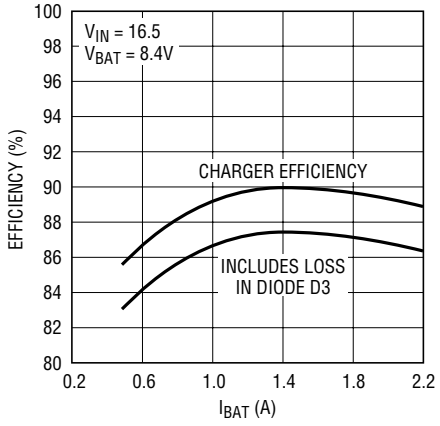
Note 2: Tested with Test Circuit 1.

Note 3: Tested with Test Circuit 2.

Note 4: A linear interpolation can be used for reference voltage specification between 0°C and –40°C.

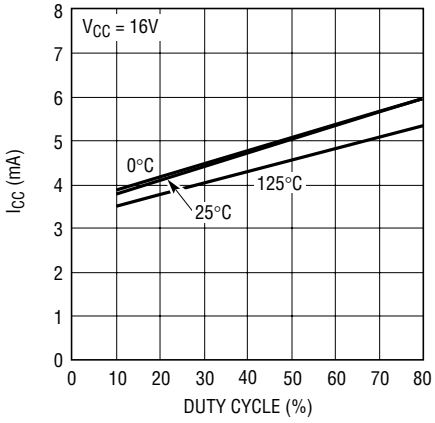
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency of Figure 1 Circuit



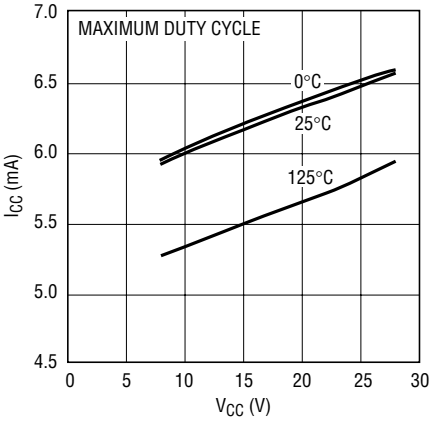
1769 G01

I_{CC} vs Duty Cycle



1769 G02

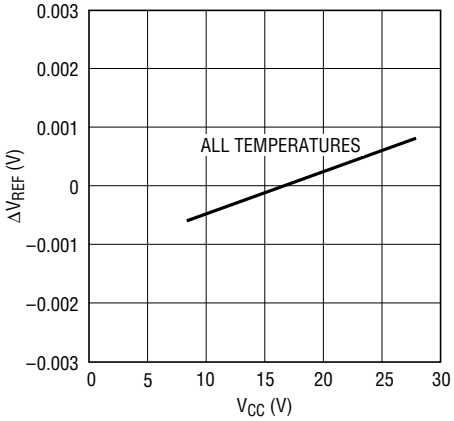
I_{CC} vs V_{CC}



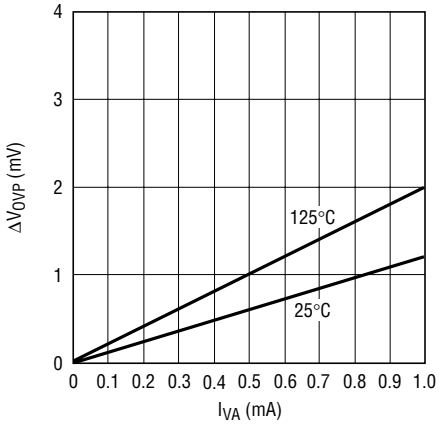
1769 G03

TYPICAL PERFORMANCE CHARACTERISTICS

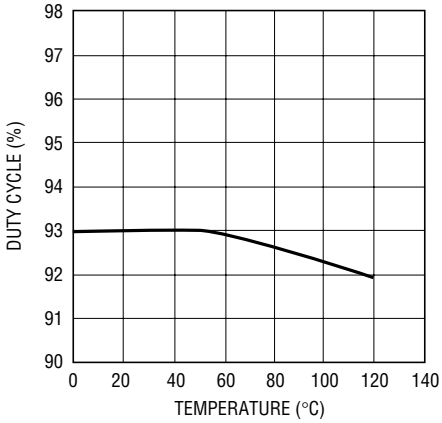
V_{REF} Line Regulation



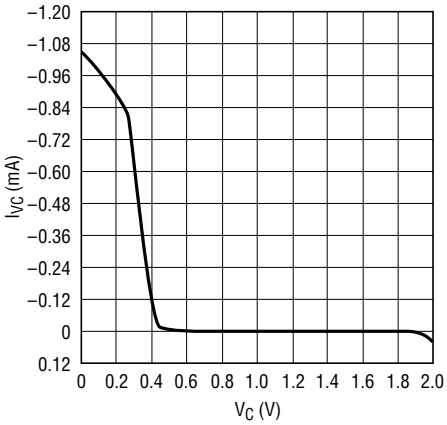
I_{VA} vs ΔV_{OVP} (Voltage Amplifier)



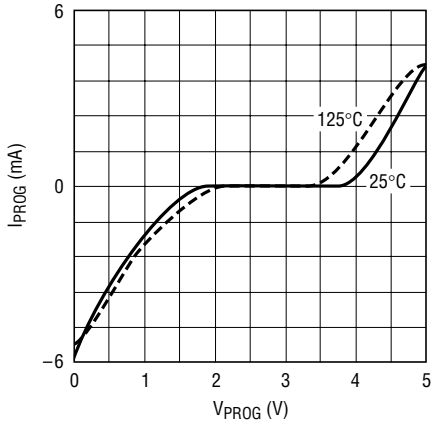
Maximum Duty Cycle



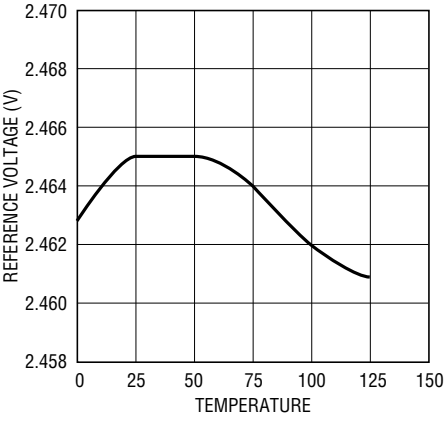
V_C Pin Characteristics



PROG Pin Characteristics



Reference Voltage vs Temperature



PIN FUNCTIONS

GND (Pins 1 to 3, 7, 8, 14, 15, 22, 26 to 28): Ground Pins. Must be connected to expanded PC lands for proper heat sinking. See Applications Information section for details.

SW (Pin 4): Switch Output. The Schottky catch diode must be placed with very short lead length in close proximity to SW pin and GND.

BOOST (Pin 5): This pin is used to bootstrap and drive the switch power NPN transistor to a low on-voltage for low power dissipation. In normal operation, $V_{BOOST} = V_{CC} + V_{BAT}$ when switch is on. Maximum allowable V_{BOOST} is 55V.

UV (Pin 6): Undervoltage Lockout Input. The rising threshold is at 6.7V with a hysteresis of 0.5V. Switching stops in undervoltage lockout. When the supply (normally the wall adapter output) to the chip is removed, the UV pin has to be pulled down to below 0.7V (a 5k resistor from adapter output to GND is required) otherwise the reverse battery current drained by the chip will be approximately 200μA instead of 3μA. Do not leave UV pin floating. If it is connected to V_{IN} with no resistor divider, the built-in 6.7V undervoltage lockout will be effective.

OVP (Pin 9): This is the input to the amplifier VA with a threshold of 2.465V. Typical input current is about 3nA out of pin. For charging lithium-ion batteries, VA monitors the battery voltage and reduces charging when battery voltage reaches the preset value. If it is not used, the OVP pin should be grounded.

CLP (Pin 10): This is the positive input to the supply current limit amplifier CL1. The threshold is set at 100mV. When used to limit supply current, a filter is needed to filter out the 200kHz switching noise.

CLN (Pin 11): This is the negative input to the amplifier CL1.

COMP1 (Pin 12): This is the compensation node for the amplifier CL1. A 200pF capacitor is required from this pin to GND if input current amplifier CL1 is used. At input adapter current limit, this node rises to 1V. By forcing COMP1 low with an external transistor, amplifier CL1 will be defeated (no adapter current limit). COMP1 can source 200μA.

SENSE (Pin 13): Current Amplifier CA1 Input. Sensing can be at either terminal of the battery.

SPIN (Pin 16): This pin is for the internal amplifier CA1 bias. It has to be connected to R_{S1} as shown in the 2A Lithium Battery Charger (Figure 1).

BAT (Pin 17): Current Amplifier CA1 Input.

COMP2 (Pin 18): This is also a compensation node for the amplifier CL1. It gets up to 2.8V at input adapter current limit and/or at constant-voltage charging.

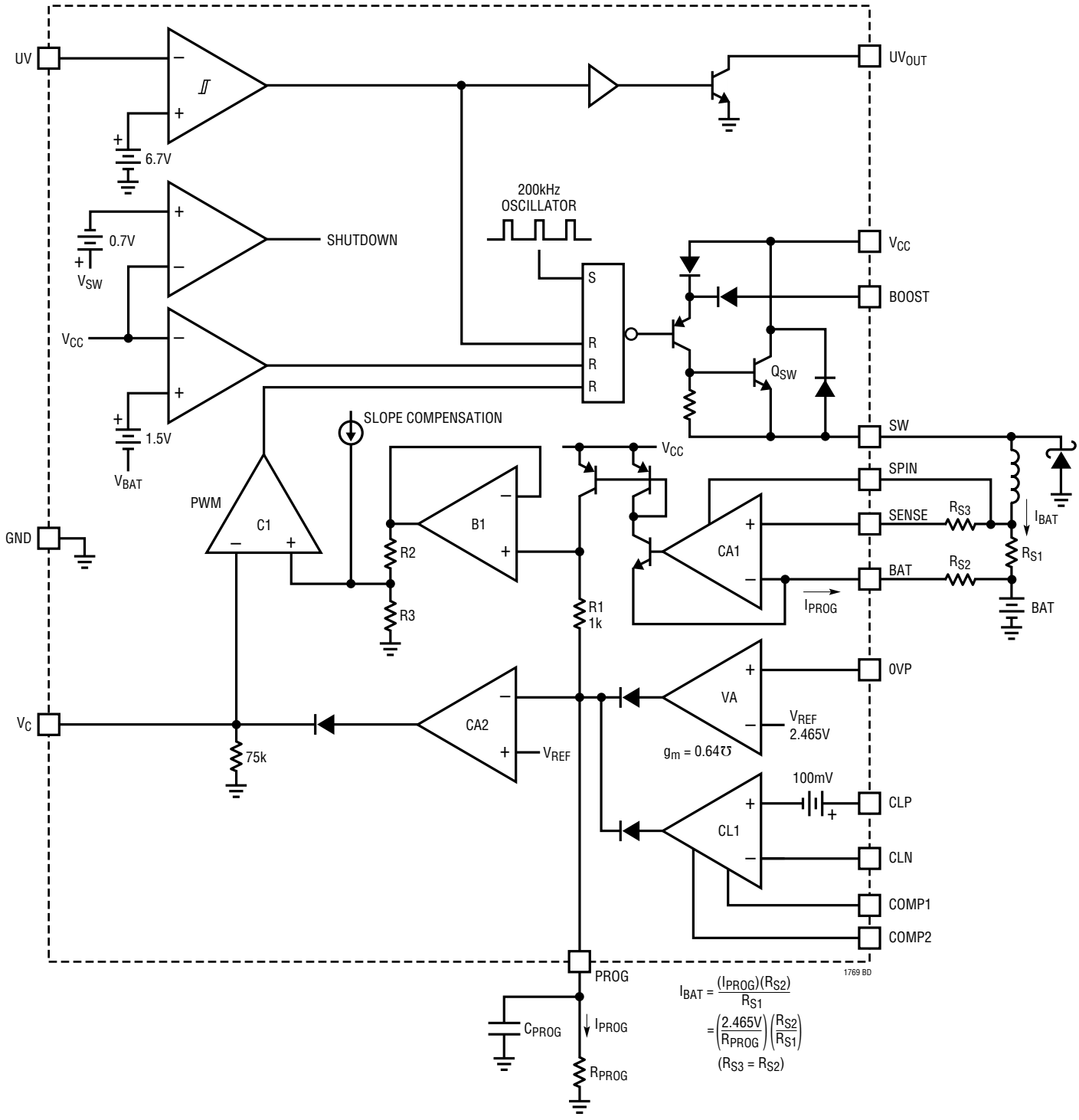
UV_{OUT} (Pin 19): This is an open-collector output for undervoltage lockout status. It stays low in undervoltage state. With an external pull-up resistor, it goes high at valid V_{CC}. Note that the base drive of the open-collector NPN comes from CLN pin. UV_{OUT} stays low only when CLN is higher than 2V. Pull-up current should be kept under 100μA.

V_C (Pin 20): This is the control signal of the inner loop of the current mode PWM. Switching starts at 0.7V. Higher V_C corresponds to higher charging current in normal operation. A capacitor of at least 0.33μF to GND filters out noise and controls the rate of soft start. To shut down switching, pull this pin low. Typical output current is 30μA.

PROG (Pin 21): This pin is for programming the charging current and for system loop compensation. During normal operation, V_{PROG} stays close to 2.465V. If it is shorted to GND the switching will stop. When a microprocessor controlled DAC is used to program charging current, it must be capable of sinking current at a compliance up to 2.465V.

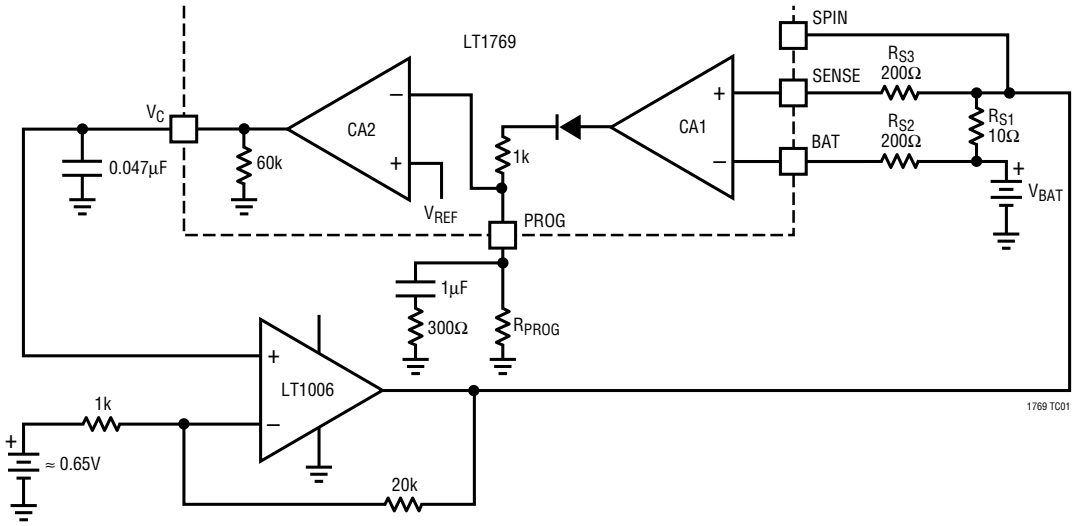
V_{CC1}, V_{CC2}, V_{CC3} (Pins 23 to 25): This is the supply of the chip. For good bypass, a low ESR capacitor of 15μF or higher is required, with the lead length kept to a minimum. V_{CC} should be between 8V and 28V and at least 3V higher than V_{BAT}. Undervoltage lockout starts and switching stops when V_{CC} goes below 7V. Note that there is a parasitic diode inside from SW pin to V_{CC} pin. Do not force V_{CC} below SW by more than 0.7V with battery present. All three V_{CC} pins should be shorted together close to the pins.

BLOCK DIAGRAM

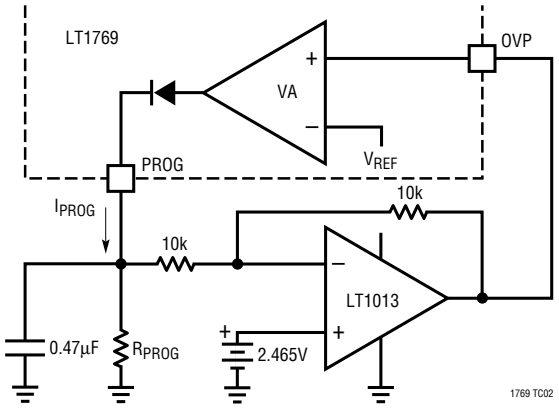


TEST CIRCUITS

Test Circuit 1



Test Circuit 2



OPERATION

The LT1769 is a current mode PWM step-down (buck) switcher. The battery DC charging current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin (see Block Diagram). Amplifier CA1 converts the charging current through R_{S1} to a much lower current I_{PROG} fed into the PROG pin. Amplifier CA2 compares the output of CA1 with the programmed current and drives the PWM loop to force them to be equal. High DC accuracy is achieved with averaging capacitor C_{PROG}. Note that I_{PROG} has both AC and DC components. I_{PROG} goes through R1 and generates a ramp signal that is fed to the PWM control comparator C1 through buffer B1 and level shift resistors R2 and R3, forming the current mode inner loop. The BOOST pin drives the switch NPN Q_{SW} into saturation and reduces power loss. For batteries like lithium-ion that require both constant-current and constant-voltage charging, the 0.5%, 2.465V reference and the amplifier VA reduce the charging current when battery voltage reaches the preset level. For NiMH and NiCd, VA can be used for overvoltage protection. When input voltage is not present, the charger goes into low current (3µA typically) sleep mode as input drops down to 0.7V below battery voltage. To shut down the charger, simply pull the V_C pin low with a transistor.

APPLICATIONS INFORMATION

Input and Output Capacitors

In the 2A Lithium Battery Charger (Figure 1), the input capacitor (C_{IN}) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not critical. Solid tantalum capacitors such as the AVX TPS and Sprague 593D series have high ripple current rating in a relatively small surface mount package, but *caution must be used when tantalum capacitors are used for input bypass*. High input surge currents can be created when the adapter is hot-plugged to the charger and solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (5µF to 20µF) from Tokin or United Chemi-Con/ Marcon, et al. Sanyo OS-CON can also be used.

The output capacitor (C_{OUT}) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29\ (V_{BAT})\left(1 - \frac{V_{BAT}}{V_{CC}}\right)}{(L1)(f)}$$

For example, V_{CC} = 16V, V_{BAT} = 8.4V, L1 = 20µH, and f = 200kHz, I_{RMS} = 0.3A.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 200kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C_{OUT} is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Soft Start

The LT1769 is soft started by the 0.33µF capacitor on the V_C pin. On start-up, V_C pin voltage will rise quickly to 0.5V, then ramp at a rate set by the internal 45µA pull-up current and the external capacitor. Battery charging current starts ramping up when V_C voltage reaches 0.7V and full current is achieved with V_C at 1.1V. With a 0.33µF capacitor, time to reach full charge current is about 10ms and it is assumed that input voltage to the charger will reach full value in less than 10ms. The capacitor can be increased up to 1µF if longer input start-up times are needed.

In any switching regulator, conventional timer-based soft starting can be defeated if the input voltage rises much slower than the time out period. This happens because the switching regulators in the battery charger and the computer power supply are typically supplying a fixed amount of power to the load. If input voltage comes up slowly compared to the soft-start time, the regulators will try to deliver full power to the load when the input voltage is still well below its final value. If the adapter is current limited, it cannot deliver full power at reduced output voltages and the possibility exists for a quasi "latch" state where the adapter output stays in a current limited state at reduced output voltage. For instance, if maximum charger plus computer load power is 25W, a 15V adapter might be current limited at 2A. If adapter voltage is less than (25W/2A = 12.5V) when full power is drawn, the adapter voltage will be sucked down by the constant 25W load until it reaches a lower stable state where the switching regulators can no longer supply full load. This situation can be prevented by utilizing *undervoltage lockout*, set higher than the minimum adapter voltage where full power can be achieved.

A fixed undervoltage lockout of 7V is built into the V_{CC} pin, but an additional adjustable lockout is also available on the UV pin. Internal lockout is performed by clamping the V_C pin low. The V_C pin is released from its clamped state when the UV pin rises above 6.7V and is pulled low when the UV pin drops below 6.2V (0.5V hysteresis). At the same time UV_{OUT} goes high with an external pull-up resistor. This signal can be used to alert the system that charging is about to start. The charger will start delivering current about 4ms after V_C is released, as set by the 0.33µF capacitor. A resistor divider is used to set the desired V_{CC} lockout voltage as shown in Figure 2. A typical value for R6 is 5k and R5 is found from:

$$R5 = \frac{R6(V_{IN} - V_{UV})}{V_{UV}}$$

APPLICATIONS INFORMATION

V_{UV} = Rising lockout threshold on the UV pin

V_{IN} = Charger input voltage that will sustain full load power

Example: With R6 = 5k, V_{UV} = 6.7V and setting V_{IN} at 12V;

R5 = 5k (12V – 6.7V)/6.7V = 4k

The resistor divider should be connected directly to the adapter output as shown, not to the V_{CC} pin to prevent battery drain with no adapter voltage. If the UV pin is not used, connect it to the adapter output (not V_{CC}) and connect a resistor no greater than 5k to ground. Floating the pin will cause reverse battery current to increase from 3µA to 200µA.

If connecting the unused UV pin to the adapter output is not possible for some reason, it can be grounded. Although it would seem that grounding the pin creates a permanent lockout state, the UV circuitry is arranged for phase reversal with low voltages on the UV pin to allow the grounding technique to work.

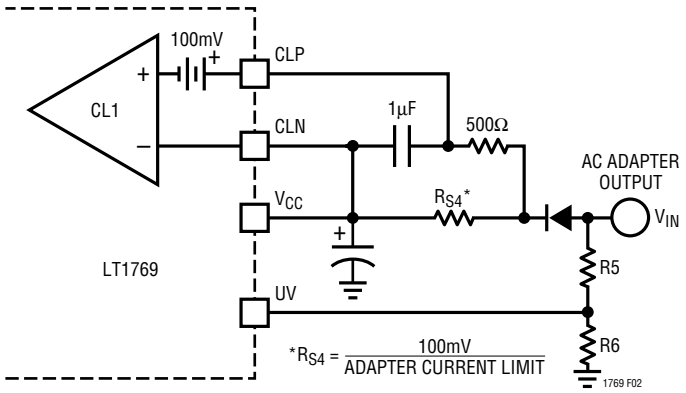


Figure 2. Adapter Current Limiting

Adapter Limiting

An important feature of the LT1769 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed-loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 2 senses the voltage across R_{S4}, connected between the CLP and CLN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to 100mV/R_{S4}. A lowpass filter formed by 500Ω and 1µF is required to eliminate switching noise. If the current limit is not used, both CLP and CLN pins should be connected to V_{CC}.

Charging Current Programming

The basic formula for charging current is (see Block Diagram):

$$I_{BAT} = I_{PROG}\left(\frac{R_{S2}}{R_{S1}}\right) = \left(\frac{2.465V}{R_{PROG}}\right)\left(\frac{R_{S2}}{R_{S1}}\right)$$

where R_{PROG} is the total resistance from PROG pin to ground.

For the sense amplifier CA1 biasing purpose, R_{S3} should have the same value as R_{S2} and SPIN should be connected directly to the sense resistor (R_{S1}) as shown in the Block Diagram.

For example, 2A charging current is needed. To have low power dissipation on R_{S1} and enough signal to drive the amplifier CA1, let R_{S1} = 100mV/2A = 0.05Ω. This limits R_{S1} power to 0.2W. Let R_{PROG} = 5k, then:

$$R_{S2} = R_{S3} = \frac{(I_{BAT})(R_{PROG})(R_{S1})}{2.465V}$$

$$= \frac{(2A)(5k)(0.05)}{2.465V} = 200\Omega$$

Charging current can also be programmed by pulse width modulating I_{PROG} with a switch Q1 to R_{PROG} at a frequency higher than a few kHz (Figure 3). Charging current will be proportional to the duty cycle of the switch with full current at 100% duty cycle.

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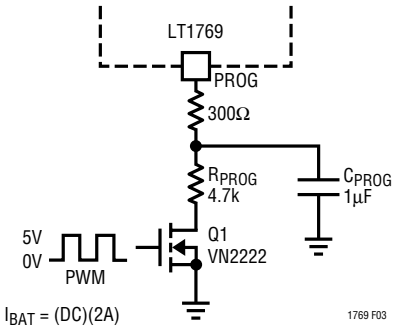

Figure 3. PWM Current Programming

Lithium-Ion Charging

The 2A Lithium Battery Charger (Figure 1) charges lithium-ion batteries at a constant 2A until battery voltage reaches a limit set by R3 and R4. The charger will then automatically go into a constant-voltage mode with current decreasing to zero over time as the battery reaches full charge. This is the normal regimen for lithium-ion charging, with the charger holding the battery at "float" voltage indefinitely. In this case no external sensing of full charge is needed.

Battery Voltage Sense Resistors Selection

To minimize battery drain when the charger is off, current through the R3/R4 divider is set at 15µA. The input current to the OVP pin is 3nA and the error can be neglected.

With divider current set at 15µA, R4 = 2.465/15µA = 162k and,

$$R3 = \frac{(R4)(V_{BAT} - 2.465)}{2.465} = \frac{162k(8.4 - 2.465)}{2.465}$$
$$= 390k$$

Li-Ion batteries typically require float voltage accuracy of 1% to 2%. Accuracy of the LT1769 OVP voltage is ±0.5% at 25°C and ±1% over full temperature. This leads to the possibility that very accurate (0.1%) resistors might be needed for R3 and R4. Actually, the temperature of the LT1769 will rarely exceed 50°C in float mode because charging currents have tapered off to a low level, so 0.25% resistors will normally provide the required level of overall accuracy.

When power is on, there is about 200µA of current flowing out of the BAT and SENSE pins. If the battery is removed during charging, and total load including R3 and R4 is less than the 200µA, V_{BAT} could float up to V_{CC} even though the loop has turned switching off. To keep V_{BAT} regulated to the battery voltage in this condition, R3 and R4 can be chosen to draw 0.5mA and Q3 can be added to disconnect them when power is off (Figure 4). R5 isolates the OVP pin from any high frequency noise on V_{IN}. An alternative way is to use a Zener diode with a breakdown voltage two or three volts higher than battery voltage to clamp the V_{BAT} voltage.

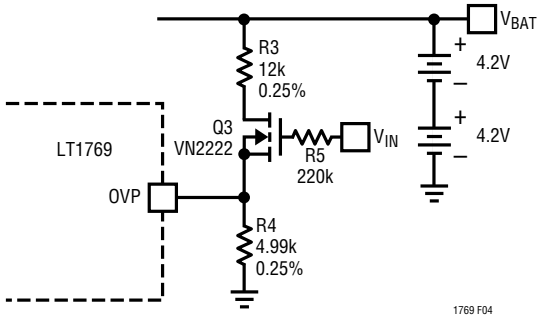

Figure 4. Disconnecting Voltage Divider

Some battery manufacturers recommend termination of constant-voltage float mode after charging current has dropped below a specified level (typically around 10% of the full current) *and* a further time out period of 30 minutes to 90 minutes has elapsed. This may extend the life of the battery, so check with manufacturers for details. The circuit in Figure 5 will detect when charging current has dropped below 270mA. This logic signal is used to initiate a timeout period, after which the LT1769 can be shut down by pulling the V_C pin low with an open collector or drain. Some external means must be used to detect the need for additional charging or the charger may be turned on periodically to complete a short float-voltage cycle.

Current trip level is determined by the battery voltage, R1 through R3 and the sense resistor (R_{S1}). D2 generates hysteresis in the trip level to avoid multiple comparator transitions.

APPLICATIONS INFORMATION

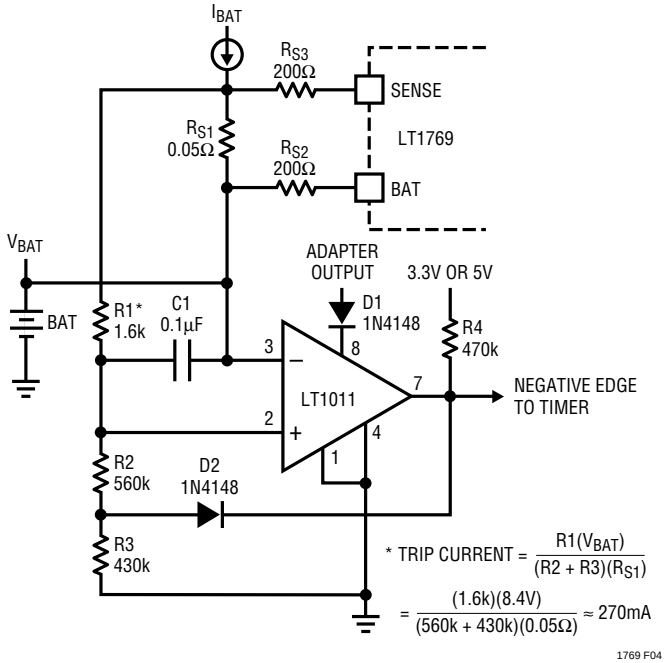

Figure 5. Current Comparator for Initiating Float Time Out

Nickel-Cadmium and Nickel-Metal-Hydride Charging

The circuit in the 2A Lithium Battery Charger (Figure 1) can be modified to charge NiCd or NiMH batteries. For example, 2-level charging is needed; 1A when Q1 is on and 100mA when Q1 is off.

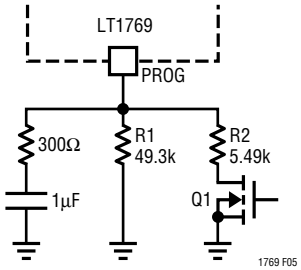

Figure 6. 2-Level Charging

For 1A full current, the current sense resistor (R_{S1}) should be increased to 0.1Ω so that enough signal (10mV) will be across R_{S1} at 0.1A trickle charge to keep charging current accurate.

For a 2-level charger, R1 and R2 are found from:

$$R1 = \frac{(2.465)(2000)}{I_{LOW}} \qquad R2 = \frac{(2.465)(2000)}{I_{HI} - I_{LOW}}$$

All battery chargers with fast charge rates require some means to detect full charge state in the battery to terminate the high charging current. NiCd batteries are typically charged at high current until temperature rise or battery voltage decrease is detected as an indication of near full charge. The charging current is then reduced to a much lower value and maintained as a constant trickle charge. An intermediate "top off" current may be used for a fixed time period to reduce 100% charge time.

NiMH batteries are similar in chemistry to NiCd but have two differences related to charging. First, the inflection characteristic in battery voltage as full charge is approached is not nearly as pronounced. This makes it more difficult to use dV/dt as an indicator of full charge, and change of temperature is more often used with a temperature sensor in the battery pack. Secondly, constant trickle charge may not be recommended. Instead, a moderate level of current is used on a pulse basis (≈ 1% to 5% duty cycle) with the time-averaged value substituting for a constant low trickle. Please contact the Linear Technology Applications department about charge termination circuits.

If overvoltage protection is needed, R3 and R4 should be calculated according to the procedure described in Lithium-Ion Charging section. The OVP pin should be grounded if not used.

When a microprocessor DAC output is used to control charging current, it must be capable of sinking current at a compliance up to 2.5V if connected directly to the PROG pin.

Thermal Calculations

If the LT1769 is used for charging currents above 1A, a thermal calculation should be done to ensure that junction temperature will not exceed 125°C. Power dissipation in the IC is caused by bias and driver current, switch resistance and switch transition losses. The GN package, with a thermal resistance of 35°C/W, can provide a full 2A charging current in many situations. A graph is shown in the Typical Performance Characteristics section.

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$$P_{BIAS} = (3.5mA)(V_{IN}) + 1.5mA(V_{BAT}) + \frac{(V_{BAT})^2}{V_{IN}}\left[7.5mA + (0.012)(I_{BAT})\right]$$

$$P_{DRIVER} = \frac{(I_{BAT})(V_{BAT})^2\left(1+\frac{V_{BAT}}{30}\right)}{55(V_{IN})}$$

$$P_{SW} = \frac{(I_{BAT})^2(R_{SW})(V_{BAT})}{V_{IN}} + (t_{OL})(V_{IN})(I_{BAT})(f)$$

R_{SW} = Switch ON resistance ≈ 0.16Ω
t_{OL} = Effective switch overlap time ≈ 10ns
f = 200kHz

Example: V_{IN} = 19V, V_{BAT} = 12.6V, I_{BAT} = 2A:

$$P_{BIAS} = \left(3.5mA\right)\left(19\right) + 1.5mA\left(12.6\right) + \frac{\left(12.6\right)^2}{19}\left[7.5mA + \left(0.012\right)\left(2000mA\right)\right] = 0.35W$$

$$P_{DRIVER} = \frac{\left(2\right)\left(12.6\right)^2\left(1+\frac{12.6}{30}\right)}{55\left(19\right)} = 0.43W$$

$$P_{SW} = \frac{\left(2\right)^2\left(0.16\right)\left(12.6\right)}{19} + 10^{-9}\left(19\right)\left(2\right)\left(200kHz\right) = 0.42 + 0.08 = 0.5W$$

Total Power in the IC is: 0.35 + 0.43 + 0.5 = 1.3W

Temperature rise will be (1.3W)(35°C/W) = 46°C. This assumes that the LT1769 is properly heat sunk by connecting the seven fused ground pins to expanded traces and that the PC board has a backside or internal plane for heat spreading.

The P_{DRIVER} term can be reduced by connecting the boost diode D2 (see Figure 1) to a lower system voltage (lower than V_{BAT}) instead of V_{BAT}.

$$\text{Then } P_{DRIVER} = \frac{(I_{BAT})(V_{BAT})(V_X)\left(1+\frac{V_X}{30}\right)}{55(V_{IN})}$$

For example, V_X = 3.3V then:

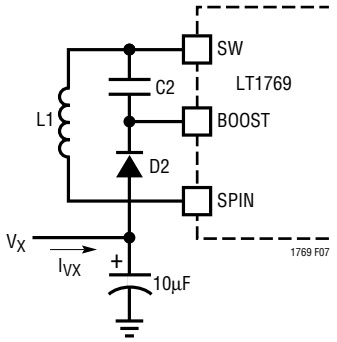

Figure 7. Lower V_{BOOST}

$$P_{DRIVER} = \frac{\left(2A\right)\left(12.6V\right)\left(3.3V\right)\left(1+\frac{3.3V}{30}\right)}{55\left(19V\right)} = 0.09\,W$$

The average I_{VX} required is:

$$\frac{P_{DRIVER}}{V_X} = \frac{0.09\,W}{3.3V} = 28mA$$

Fused-lead packages conduct most of their heat out the leads. This makes it very important to provide as much PC board copper around the leads as is practical. Total thermal resistance of the package-board combination is dominated by the characteristics of the board in the immediate area of the package. This means both lateral thermal resistance across the board and vertical thermal resistance through the board to other copper layers. Each layer acts as a thermal heat spreader that increases the heat sinking effectiveness of extended areas of the board.

Total board area becomes an important factor when the area of the board drops below about 20 square inches. The graph in Figure 8 shows thermal resistance vs board area for 2-layer and 4-layer boards with continuous copper planes. Note that 4-layer boards have significantly lower thermal resistance, but both types show a rapid increase for reduced board areas. Figure 9 shows actual measured lead temperatures for chargers operating at full current. Battery voltage and input voltage will affect device power dissipation, so the data sheet power calculations must be used to extrapolate these readings to other situations.

Vias should be used to connect board layers together. Planes under the charger area can be cut away from the

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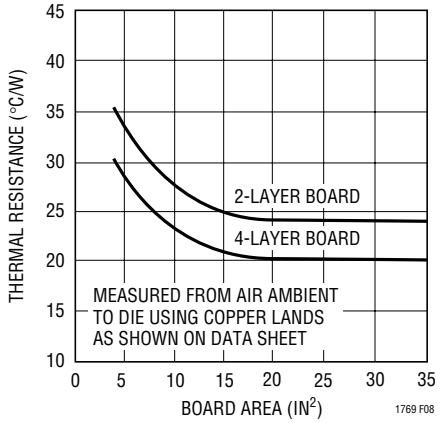

Figure 8. LT1769 Thermal Resistance

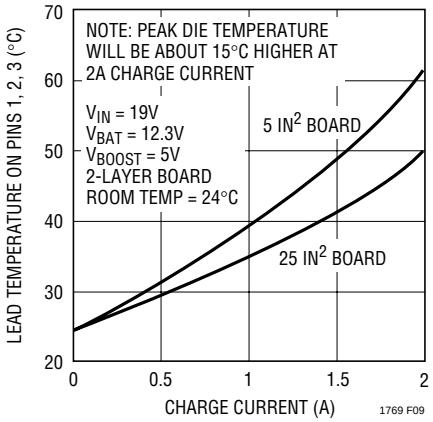

Figure 9. LT1769 Lead Temperature

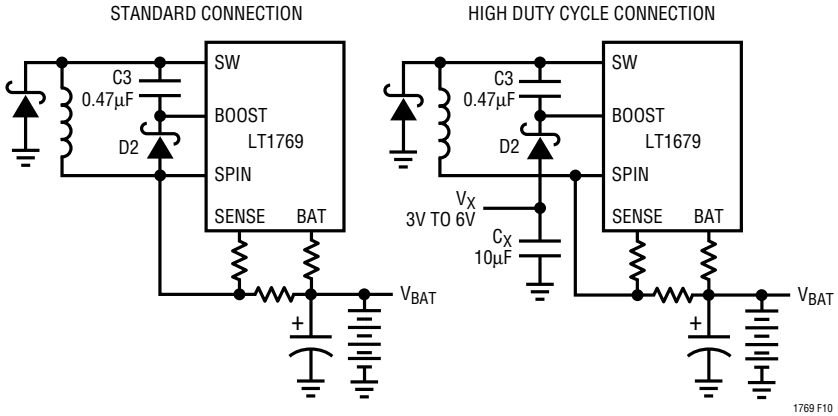

Figure 10. High Duty Cycle

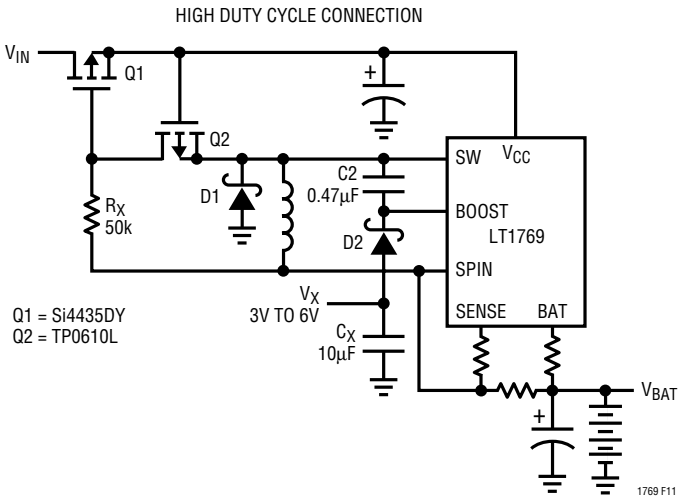

Figure 11. Replacing the Input Diode

rest of the board and connected with vias to form both a low thermal resistance system and to act as a ground plane for reduced EMI.

Glue-on, chip-mounted heat sinks are effective only in moderate power applications where the PC board copper cannot be used, or where the board size is small. They offer very little improvement in a properly laid out multilayer board of reasonable size.

Higher Duty Cycle for the LT1769 Battery Charger

Maximum duty cycle for the LT1769 is typically 90%, but this may be too low for some applications. For example, if an 18V ±3% adapter is used to charge ten NiMH cells, the charger must put out 15V maximum. A total of 1.6V is lost in the input diode, switch resistance, inductor resistance and parasitics, so the required duty cycle is 15/16.4 = 91.4%. As it turns out, duty cycle can be extended to 93% by restricting boost voltage to 5V instead of using V_{BAT} as is normally done. This lower boost voltage also reduces power dissipation in the LT1769, so it is a win-win decision. Connect an external source of 3V to 6V at V_X node in Figure 10 with a 10µF C_X bypass capacitor.

Even Lower Dropout

For even lower dropout and/or reducing heat on the board, the input diode D3 should be replaced with a FET (see Figure 11). It is pretty straightforward to connect a P-channel FET across the input diode and connect its gate to the battery so that the FET commutates off when the

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input goes low. The problem is that the gate must be pumped low so that the FET is fully turned on even when the input is only a volt or two above the battery voltage. Also there is a turn-off speed issue. The FET should turn off instantly when the input is dead shorted to avoid large current surges from the battery back through the charger into the FET. Gate capacitance slows turn-off, so a small P-channel (Q2) is to discharge the gate capacitance quickly in the event of an input short. The body diode of Q2 creates the necessary pumping action to keep the gate of Q1 low during normal operation. Note that Q1 and Q2 have a V_{GS} spec limit of 20V. This restricts V_{IN} to a maximum of 20V. For low dropout operation with V_{IN} > 20V consult factory.

Optional Connection of Input Diode and Current Sense Resistor

The typical application shown in Figure 1 on the first page of this data sheet shows a single diode to isolate the V_{CC} pin from the adapter input. This simple connection may be unacceptable in situations where the main system power must be disconnected from both the battery *and* the adapter under some conditons. In paticular, if the adapter is disconnected or turned off and it is desired to also disconnect the system load from the battery, the system will remain powered through the parasitic diode from the SW pin to the V_{CC} pin.

The circuit in Figure 12b allows system power to go to 0V without drawing battery current by adding an additional diode, D4. To ensure proper operation, the LT1769 current sense amplifier inputs (CLP and CLN) were designed to work above V_{CC} and not to draw current from V_{CC} when the inputs are pulled to ground by a powered-down adapter.

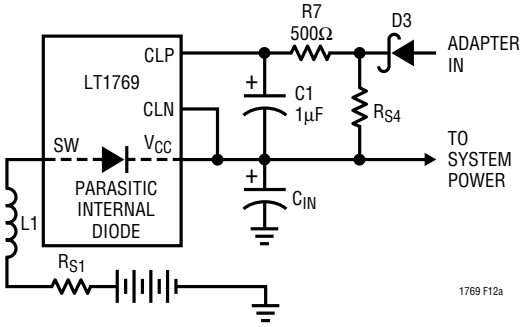

Figure 12a. Standard Connection

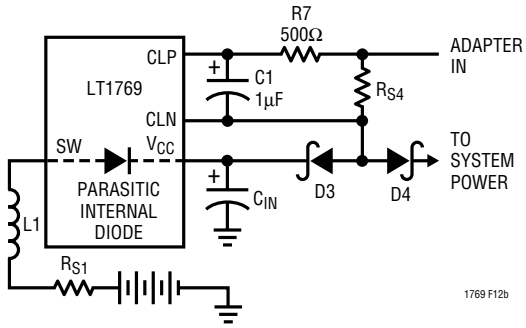

Figure 12b. Modified Input Diode Connection

Layout Considerations

Switch rise and fall times are under 10ns for maximum efficiency. To prevent radiation, the catch diode, SW pin and input bypass capacitor leads should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling and to act as a thermal spreading path. All ground pins should be connected to expanded traces for low thermal resistance. The fast-switching high current ground path, including the switch, catch diode and input capacitor, should be kept very short. Catch diode and input capacitor should be close to the chip and terminated to the same point. This path contains nanosecond rise and fall times with several amps of current. The other paths contain only DC and/or 200kHz tri-wave and are less critical. Figure 13 indicates the high speed, high current switching path. Figure 14 shows critical path layout. Contact Linear Technology for an actual LT1769 circuit PCB layout or Gerber file.

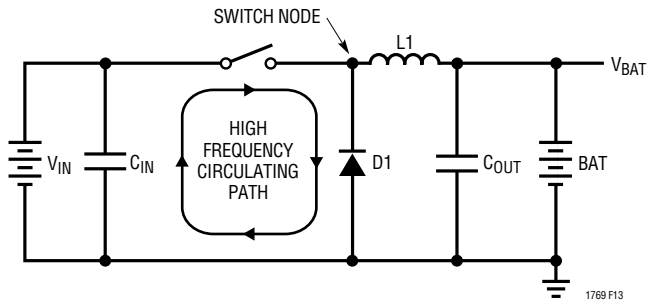

Figure 13. High Speed Switching Path

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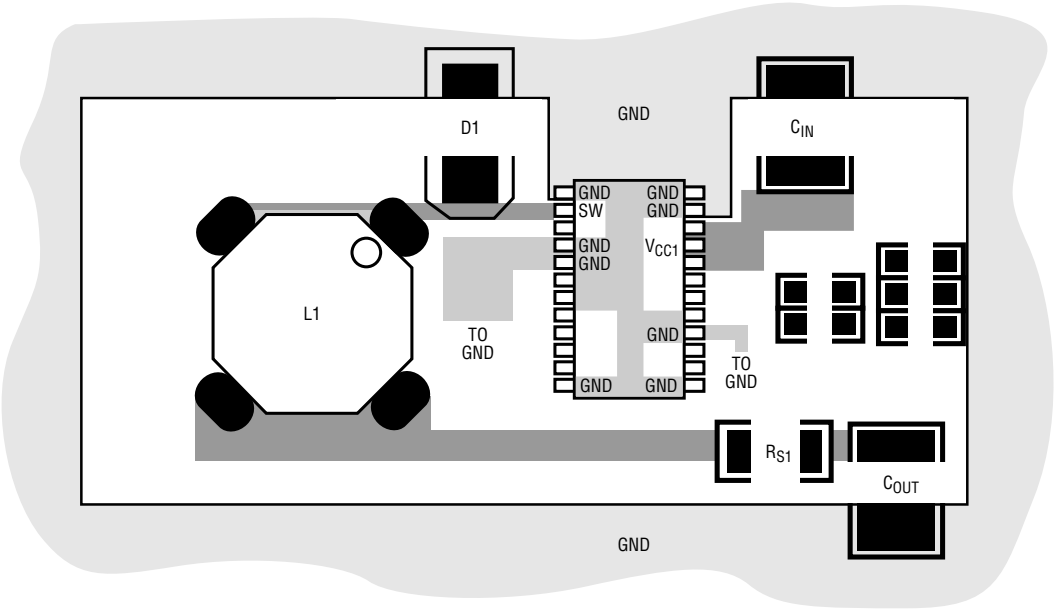
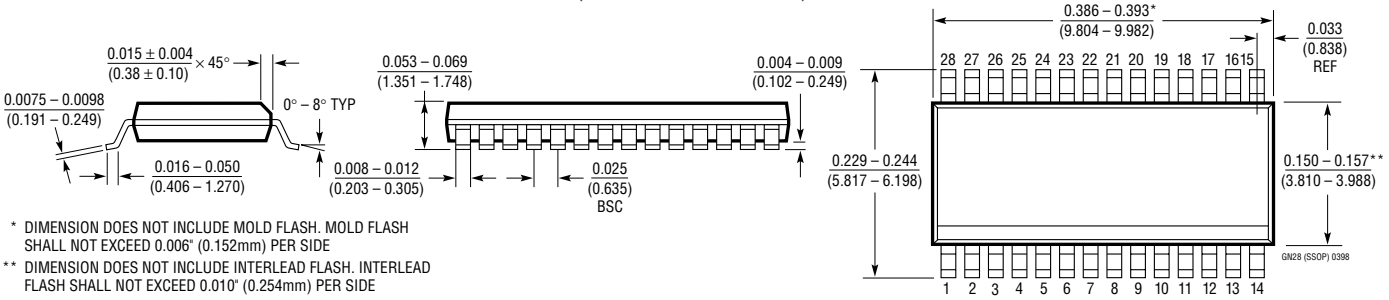


Figure 14. Critical Electrical and Thermal Path Layout

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
28-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1325	Microprocessor-Controlled Battery Management System	Can Charge, Discharge and Gas Gauge NiCd and Lead-Acid Batteries with Software Charging Profiles
LT1372/LT1377	500kHz/1MHz Step-Up Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LT1376	500kHz Step-Down Switching Regulator	High Frequency, Small Inductor, High Efficiency Switcher, 1.5A Switch
LT1505	High Current, High Efficiency Battery Charger	94% Efficiency, Synchronous Current Mode PWM
LT1510	Constant-Voltage/Constant-Current Battery Charger	Up to 1.5A Charge Current for Lithium-Ion, NiCd and NiMH Batteries
LT1511	Constant-Voltage/Constant-Current Battery Charger	Up to 3A Charge Current for Lithium-Ion, NiCd and NiMH Batteries
LT1512	SEPIC Battery Charger	V_{IN} Can Be Higher or Lower Than Battery Voltage

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