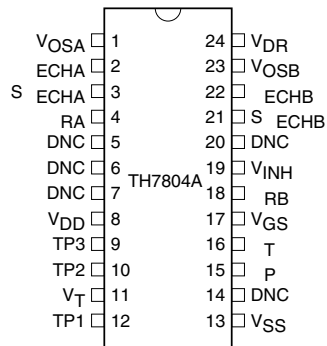


## Features

- Pixel Size: 13  $\mu\text{m}$  x 13  $\mu\text{m}$  (13  $\mu\text{m}$  pitch)
- High Data Output Rate: 20 MHz typ
- High Responsivity and Resolution over a Wide Spectral Range: from Blue (400 nm) up to Near Infrared (1100 nm)
- Improved Dark Signal and Photo Response Uniformity
- Low Temporal Noise and High Dynamic Range: Over 6000/1
- Ease and Flexibility of Operation:
  - Only two External Basic Drive Clocks
  - Internal or External Sample and Reset Clocks
- 24-lead DIL Package

## Pin Identification

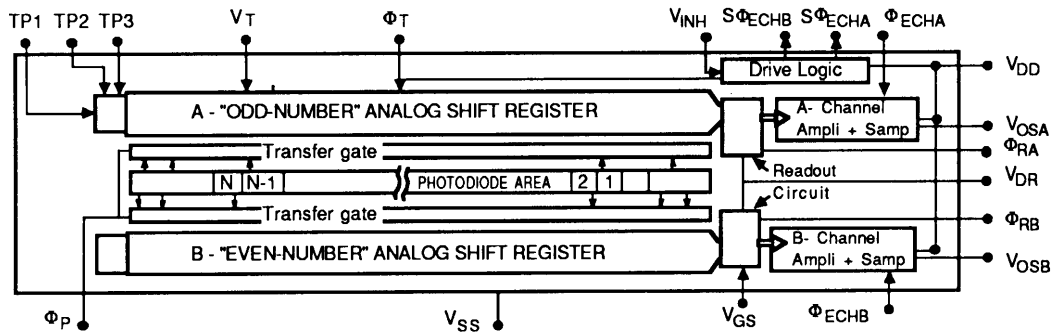
Pin Number	Symbol	Designation
1	$V_{\text{OSA}}$	Video Output Signal A (Odd Channel)
2	$\Phi_{\text{ECHA}}$	A Channel Sample-and-hold Gate Input
3	$S\Phi_{\text{ECHA}}$	A Channel Internal Sample Clock-output
4	$\Phi_{\text{RA}}$	A Channel External Reset Clock Input
8	$V_{\text{DD}}$	Output Amplifier Drain And Internal Logic Supply
9	TP3	Test Point 3
10	TP2	Test Point 2
11	VT	Register And Photosensitive Zone DC Bias
12	TP1	Test Point 1
13	$V_{\text{SS}}$	Substrate Bias (Ground)
15	$\Phi_{\text{P}}$	Transfer Clock
16	$\Phi_{\text{T}}$	Register Transport Clock
17	$V_{\text{GS}}$	Output Gate DC Bias
18	$\Phi_{\text{RB}}$	B Channel External Reset Clock Input
19	$V_{\text{INH}}$	Internal Sample Clock Inhibition
21	$S\Phi_{\text{ECHB}}$	B Channel Internal Sample Clock Input
22	$\Phi_{\text{ECHB}}$	B Channel Sample-and-hold Gate Input
23	$V_{\text{OSB}}$	Video Output Signal B (Even Channel)
24	$V_{\text{DR}}$	Reset DC Bias
5, 6, 7, 14, 20	DNC	Do Not Connected



# Linear Charged Couple Device (CCD) Image Sensor 1024 Pixels

## TH7804A





### Absolute Maximum Ratings\*

Storage Temperature .....	-55°C to +150°C
Operating Temperature .....	0°C to +70°C
Thermal Cycling .....	15°C/mn
Maximum Voltage:	
• Pins: 2, 4, 8, 12, 15, 16, 18, 19, 22, 24 .....	-0.3V to +18V
• Pins: 9, 10, 11, 17 .....	-0.3V to +18V
• Pin: 13 .....	0V

\*NOTICE: Stresses above those listed under absolute maximum ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### Operating Range

The operating range defines the temperature limits between which functionality is guaranteed: 0°C to 70°C.

### Operating Precautions

Shorting the video output to  $V_{SS}$  or  $V_{DD}$ , even temporarily, can permanently damage the output amplifier.

## Operating Conditions (T = 25°)

**Table 1. DC Bias Characteristics**

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max		
Output Amplifier Drain Supply	V <sub>DD</sub>	14	15	16	V	
Reset DC Bias	V <sub>DR</sub>	V <sub>DD</sub> - 2.4	V <sub>DD</sub> - 2	V <sub>DD</sub> - 1	V	
Output Gate DC Bias	V <sub>GS</sub>	5.5	6	6.5	V	
Photosensitive Zone And Register DC Bias	V <sub>T</sub>	0.95 V <sub>TN</sub>	V <sub>TN</sub>	1.05 V <sub>TN</sub>	V	(1)
Substrate Bias	V <sub>SS</sub>	0.0	0.0		V	
Test Point 1	TP1		V <sub>DD</sub>		V	(2)
Tests Points 2 And 3	TP2, TP3		V <sub>SS</sub>		V	(2)

- Notes: 1. Nominal value of V<sub>T</sub>:  
V<sub>TN</sub> = 6.7V if Φ<sub>T</sub> clock levels are at their typical value.  
2. No use for operation. For testing purpose only.

$$V_{TN} = \frac{(V\Phi T)HIGH + (V\Phi T)LOW}{2} \pm 5\%$$

## Basic Internal Configuration

SΦ<sub>ECHA</sub> and Φ<sub>RA</sub>  
SΦ<sub>ECHB</sub> and Φ<sub>RA</sub>

internal to TH7804A

**Table 2. Selection of Nominal Mode**

Option	Implementation	Remarks
Internal Sampling	V <sub>INH</sub> (19) Connected to V <sub>SS</sub> SΦ <sub>ECHA</sub> (3) and Φ <sub>ECHA</sub> (2) Strapped SΦ <sub>ECHB</sub> (21) and Φ <sub>ECHB</sub> (22) Strapped	(1) see note
Internal Reset	Φ <sub>RA</sub> (4) and Φ <sub>RB</sub> (18) Connected to V <sub>DD</sub>	

- Note: 1. Make the straps as short as possible to avoid any parasitic coupling to these connections. The load capacitance introduced by the strap should not exceed 5 pF.

Figure 1. Basic Test Configuration

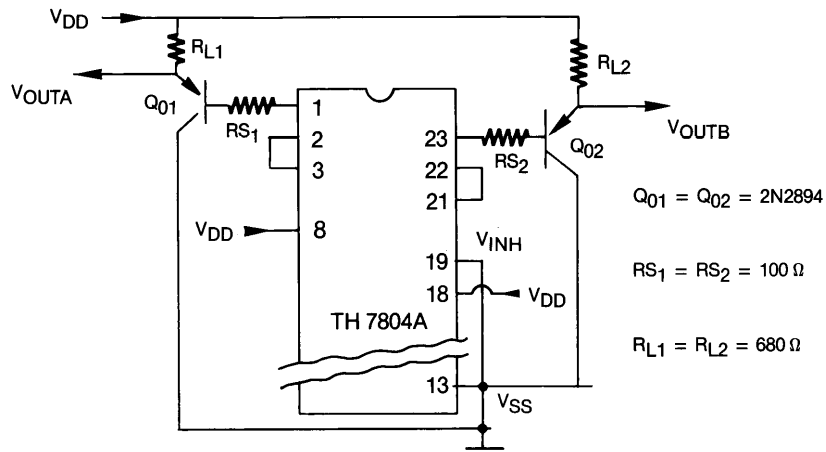
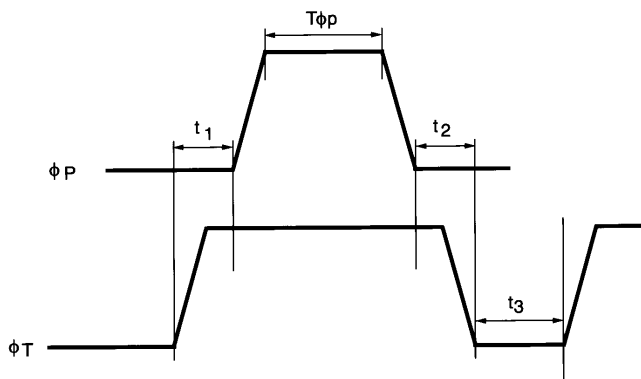
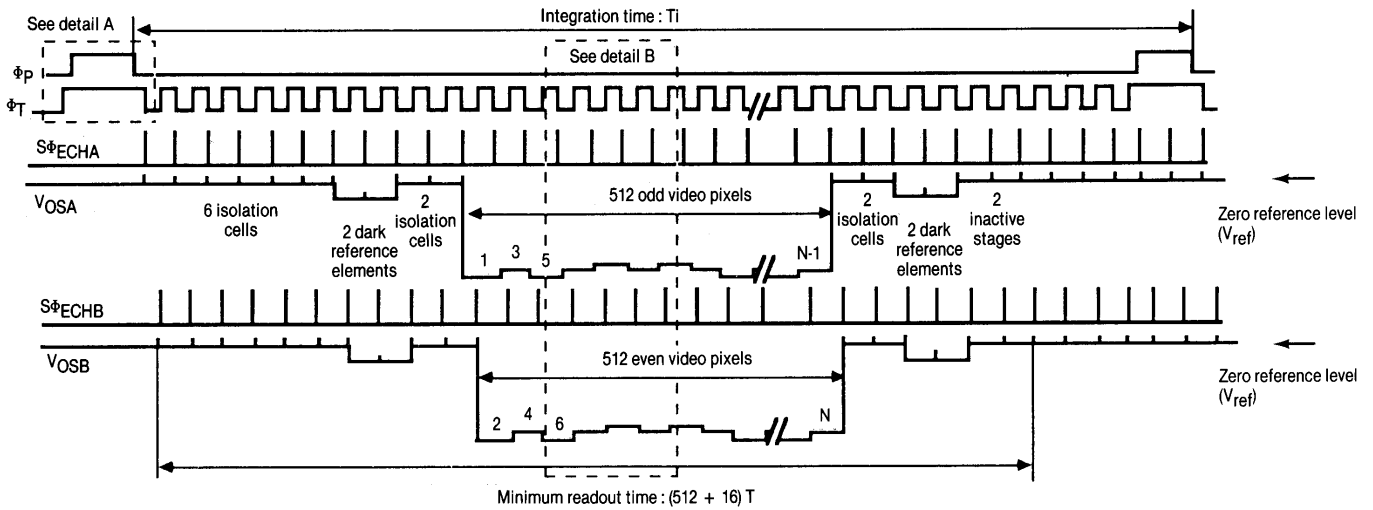
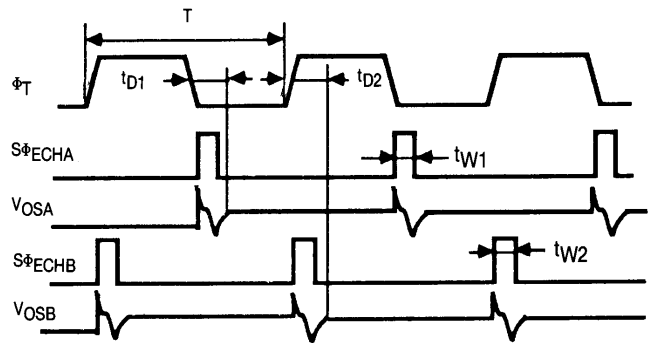


Figure 2. Timing Diagram in Basic Mode



Detail A

$T\phi_P$  : Minimum value : 100 ns  
 Recommended 0.5 to 1  $\mu$ s  
 $t_1$  and  $t_3 > 0$   $t_2 > 0$  or  $< 0$   
 $\phi_P$  = pulse may end before or after  
 $\phi_T$  returns to the low level.



Detail B

$\phi_T$  : duty cycle : 50  $\pm$  10 %  
 rise and fall time > 15 ns  
 $t_{W1} = t_{W2} = 30$  ns typ.  
 $t_{D1} = t_{D2} = 50$  ns typ.

**Table 3.** Drive Clock Characteristics (see Figure 2)

Parameter	Symbol	Logic	Value			Unit	Remark
			Min.	Typ.	Max.		
Transfer Clock	$\Phi_P \Phi_T$	High	11	13	14	V	(1)
Register Transport Clock		Low	0.0	0.4	0.6		
Register Transport Clock Capacitance	$C\Phi_T$			400	700	pF	
Transfer Clock Capacitance	$C\Phi_P$			130	200	pF	

Note: 1. Transients under 0.0V in the clock pulses will lead to charge injection, causing a localized increase in the dark signal. If such spurious negative transients are present, they can be suppressed by inserting a serial resistor of appropriate value (typically 20 to 100Ω) in the corresponding driver output.

**Table 4.** Static and Dynamic Electrical Characteristics

Parameter	Symbol	Value			Logic	Remark
		Min.	Typ.	Max.		
DC Output Level	$V_{REF}$	8	10	12	V	
Output Impedance	$Z_S$		500		Ω	
Register Single-stage Transfer Efficiency	CTE	99.992	99.998		%	$V_{OS} = 1V^{(1)}$
Max. Data Output Frequency	$F_{Smax}$	12	20		MHz	(2)
Input Current On Pins: 2, 9, 10, 11, 12, 15, 16, 17, 18, 22	$I_e$			2	μA	$V_{IN} = 15V$ All other pins: 0V
Peak Current Sink on $\Phi_T$ Clock	$(I\Phi_T)_P$		250		mA	$t_{RISE} = 15\text{ ns}$
Peak Current Sink on $\Phi_P$ Clock	$(I\Phi_P)_P$		80		mA	$t_{RISE} = 15\text{ ns}$
Output Amplifier + Internal Logic Supply Current	$I_{DD}$		17		mA	$V_{INH} = 0V$ $V_{DD} = 15V$
Static Power Dissipation	$P_D$		255	300	mW	$V_{INH} = 0V$ $V_{DD} = 15V$

Notes: 1.  $V_{OS}$  = average video output voltage.  
2.  $F_S = 2 F \Phi_T$ . The minimum clock frequency is limited by the increase in dark signal.

## Electro-optical Performance

General measurement conditions:  $T_C = 25^\circ C$ ;  $T_i = 1\text{ ms}$ ;  $F\Phi T = 2.5\text{ MHz}$  ( $F_{DATA} = 5\text{ MHz}$ )

Light source: tungsten filament lamp (2854 K) + B6 38 filter (2 mm thick), F/3.5 aperture.

The filter limits the spectrum to 700 nm; in these conditions  $1\mu J/cm^2$  corresponds to 3.5 lux.s.

Operating conditions (see Figure 1).

First and last pixels, as well as reference elements, are excluded from the specification.

Measurements taken on each output in succession.

**Table 5.** Electro-optical Performance

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Saturation Output Voltage	$V_{SAT}$	1.3	1.8	2.3	V	(1) (2)
Saturation Exposure	$E_{SAT}$		0.30		$\mu\text{J}/\text{cm}^2$	
Responsivity	R	4.5	6		$\text{V}/\mu\text{J}/\text{cm}^2$	
Responsivity Unbalance	$\Delta R/R$		2	8	%	(3)
Photo Response Non-uniformity Peak-to-peak	PRNU		$\pm 3$	$\pm 10$	% $V_{OS}$	$V_{OS} = 50 \text{ mV}$ to 1V
Contrast Transfer Function at FN (38 l p/mm)	CTF		70		%	$V_{OS} = 0.9\text{V}$
Temporal Noise In Darkness			180		$\mu\text{V}_{rms}$	(4)
Dynamic Range (Relative to rms Noise)	DR	4000	6000			
Average Dark Signal	$V_{DS}$		0.08	0.5	mV	
Dark Signal Non-uniformity Peak-to-peak	DSNU		0.15	0.5	mV	

Notes: 1. Value measured with respect to zero reference level (see Figure 2).

2. Conversion factor is typically  $1.5 \mu\text{V}/e^-$ .

3.  $\Delta R/R$  is defined as

$$\frac{200|RA - RB|}{RA + RB}$$

where RA is responsivity of video output A, RB is responsivity of video output B.

4. Measured in Correlated Double Sampling (C.D.S.) mode.

**Figure 3.** Typical Spectral Response

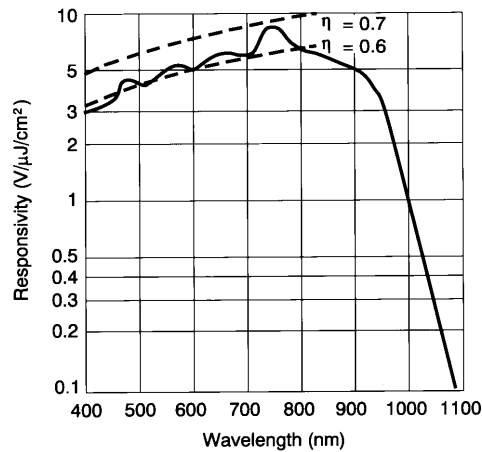
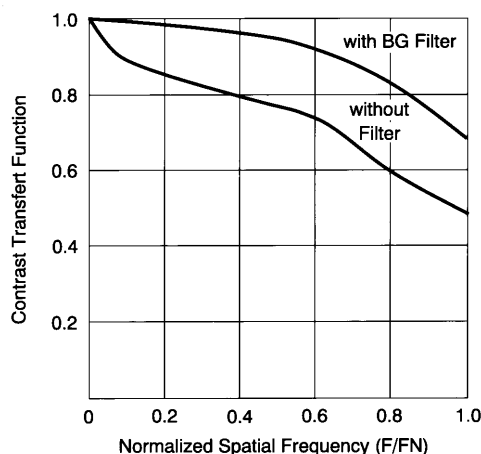


Figure 4. CTF Typical Curves (2854 K Source)



### Electro-optical Performance Without Infrared Cut-off Filtering

The TH7804A’s special semiconductor process enables it to exploit the silicon’s high near infrared sensitivity while maintaining good imaging performance in terms of response uniformity and resolution. Typical changes in performance with and without IR filtering are summarized below.

	With IR Cut-off Filter	No IR Cut-off Filter
Average Video Signal Due to a Given Scene Illumination	$V_{OS}$	$V_{OS} \times 4$
PRNU (Single Defects Excluded)	$\pm 5\%$	$\pm 5\%$
CTF at Nyquist Frequency	70%	50%

### Complementary Operating Modes

TH7804A may be used in several configurations in regards to video output sampling and charge sensing reset.

1. Sampling Options:

Inhibition of internal sampling pulses allows for two possibilities:

- a. no sampling: video output delivered in unsampled form,
- b. sampling by external clocks: external sampling pulses directly applied to  $\Phi_{ECHA}$ ,  $\Phi_{ECHB}$  inputs.

If internal sampling clocks  $S\Phi_{ECHA}$  and  $S\Phi_{ECHB}$  are not used, it is recommended of unpower the corresponding clock drivers, as this will greatly reduce on-chip power consumption.

2. External Reset Option:

The position and period of the charge reset clocks may be optimized by using external clocks on  $\Phi_{RA}$  and  $\Phi_{RB}$  inputs. This is specially interesting to optimize the video outputs for Correlated Double Sampling (in order to reduce noise and improve S/N ratio).

Control signals to be applied in the different configurations are shown in Table 6.

**Table 6.** Selection of Operating Modes

Option	Implementation	Remarks
No Sampling	$\Phi_{ECHA}$ (2) and $\Phi_{ECHB}$ (22) connected to $V_{DD}$ $S\Phi_{ECHA}$ (3) and $S\Phi_{ECHB}$ (21) unconnected $V_{INH}$ (19) connected to $V_{DD}$	(1)
Sampling by External Clocks	Sampling clocks connected to $\Phi_{ECHA}$ $\Phi_{ECHB}$ $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ unconnected $V_{INH}$ (19) connected to $V_{DD}$	see Figure 5 for sampling clock timing (1)
Reset Control by External Clocks	Ext. $\Phi_{RA}$ on $\Phi_{RA}$ (4) input Ext. $\Phi_{RB}$ on $\Phi_{RB}$ (18)	see Figure 4 for reset clock timing

Note: 1. Drain supply current  $I_{DD}$  decreases from 10 mA to 8 mA typically when internal sampling clock is disabled.

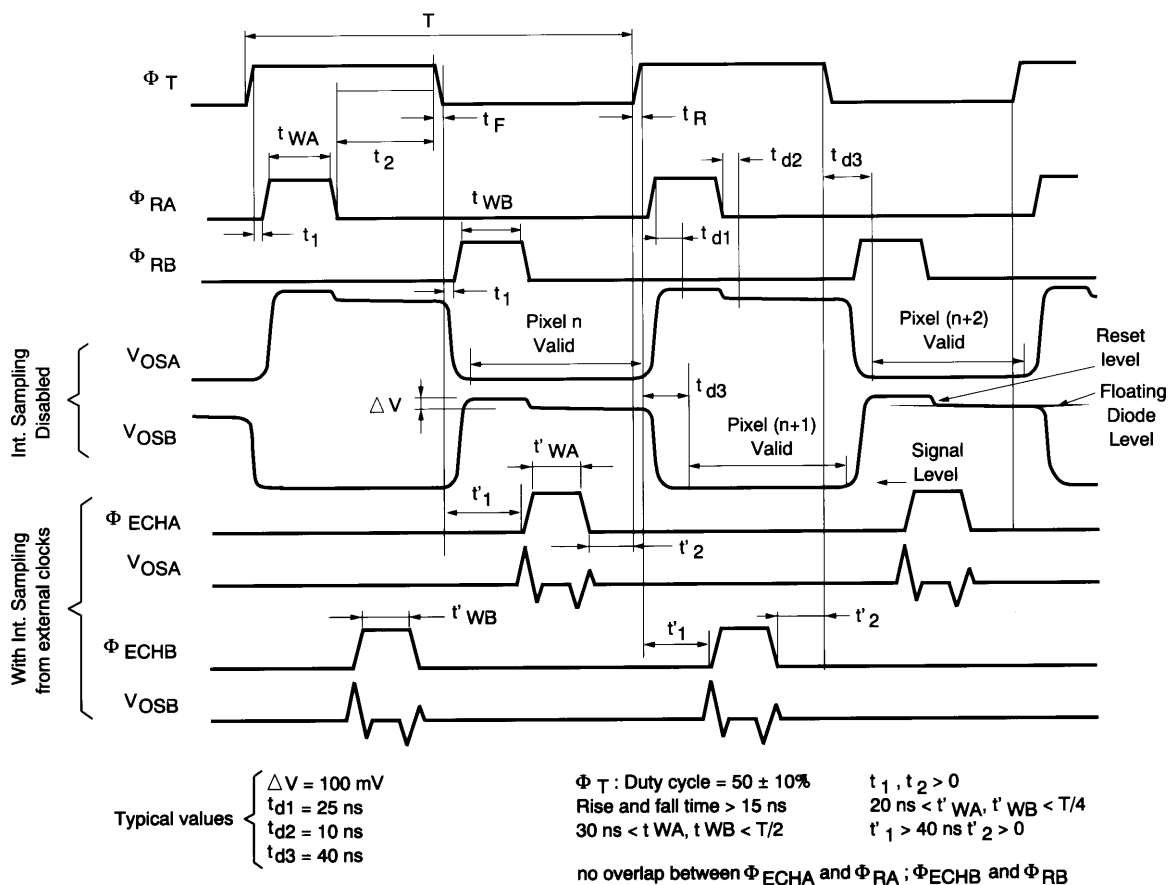
**Table 7.** External  $\Phi_{RA}$ ,  $\Phi_{RB}$ ,  $\Phi_{ECHA}$ ,  $\Phi_{ECHB}$  Clock Characteristics

Parameter	Symbol	Logic	Values			Unit
			Min.	Typ.	Max.	
External Reset Clock	$\Phi_{RA}$ , $\Phi_{RB}$	High	12	12.5	13	V
Sampling Clocks	$\Phi_{ECHA}$ , $\Phi_{ECHB}$	Low	0.0	0.4	0.6	V
Reset and Sampling Clock Capacitance	$C\Phi_{RA}$ , $C\Phi_{RB}$ $C\Phi_{ECHA}$ , $C\Phi_{ECHB}$			10	15	pF

Insertion of a serial resistor (typically 100 $\Omega$ ) at the driver output avoids spurious negative transients.



Figure 5. Timing Diagram — Clocks and Video Output Timing Diagram With and Without On-chip Sampling.



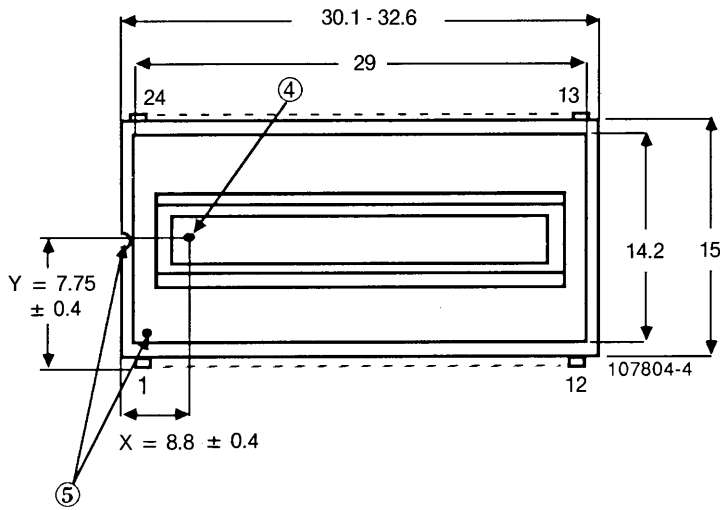
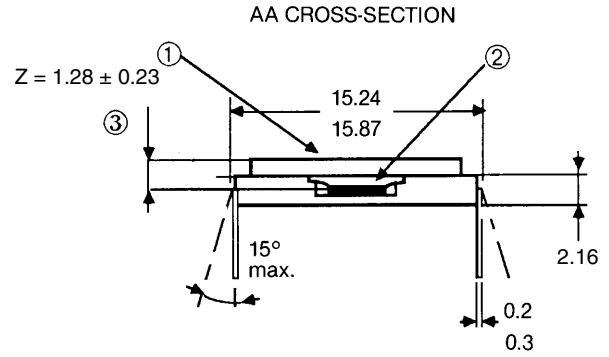
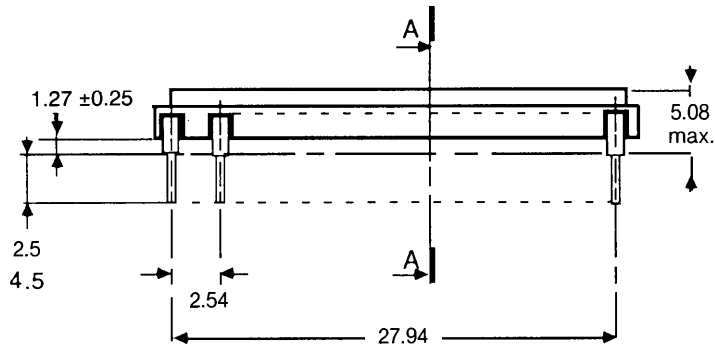
External reset clocks improve electro-optical performance, as listed below. Other operating conditions and other electro-optical parameters remain unchanged.

Table 8. Performance Improvements with External  $\Phi_{RA}$  and  $\Phi_{RB}$  Configuration

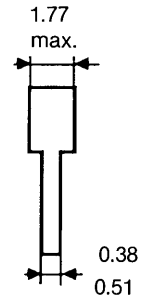
Parameter	Symbol	Value		Unit
		Typ.		
Saturation Output Voltage	$V_{SAT}$	2.0		V
Responsivity	R	8		$V/\mu\text{J}/\text{cm}^2$
Dynamic Range	DR	8000		

Electro-optical performances obtained with complementary modes are not guaranteed for the standard products.

# Outline Drawing



### PIN DETAIL



- ① Window.
- ② Photosensitive area.
- ③ Optical distance between external face of window and photosensitive area (notes 1 and 2).
- ④ Pixel n° 1 (first useful pixel in the video line defined by its X, Y, Z coordinates).
- ⑤ Index (notch or dot). Notch is under the package, dot is on the window.

Notes: 1. If an optical reference is needed, it is recommended to use the window face plane.  
 2. Variation of Z (azimuth) on the photosensitive area of a device is  $\leq \pm 0.1$  mm.  
 3. Value and tolerance of Y are applicable to each individual pixel of the photosensitive line.

Ordering Code TH7804ACC



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