

TOSHIBA POWER MOS FET MODULE SILICON N & P CHANNEL MOS TYPE (L<sup>2</sup>-π-MOSV 4 IN 1)

# MP4212

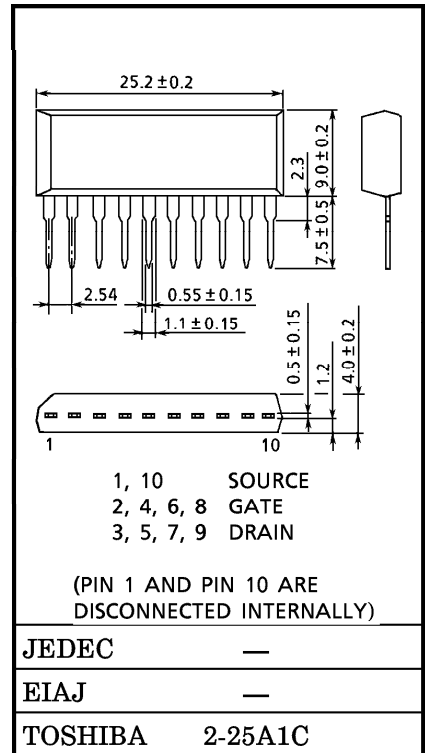
HIGH POWER HIGH SPEED SWITCHING APPLICATIONS  
H-SWITCH DRIVER

INDUSTRIAL APPLICATIONS  
Unit in mm

- 4 V Gate Drive
- Small Package by Full Molding (SIP 10 Pin)
- High Drain Power Dissipation (4 Devices Operation)  
:  $P_T = 4 \text{ W}$  ( $T_a = 25^\circ\text{C}$ )
- Low Drain-Source ON Resistance  
:  $R_{DS(ON)} = 120 \text{ m}\Omega$  (typ.) (N-ch)  
160 mΩ (typ.) (P-ch)
- High Forward Transfer Admittance  
:  $|Y_{fs}| = 5.0 \text{ S}$  (typ.) (Nch)  
4.0 S (typ.) (Pch)
- Low Leakage Current:  $I_{GSS} = \pm 10 \mu\text{A}$  (max.) ( $V_{GS} = \pm 16 \text{ V}$ )  
 $I_{DSS} = 100 \mu\text{A}$  (max.) ( $V_{DS} = 60 \text{ V}$ )
- Enhancement-Mode :  $V_{th} = 0.8 \sim 2.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1 \text{ mA}$ )

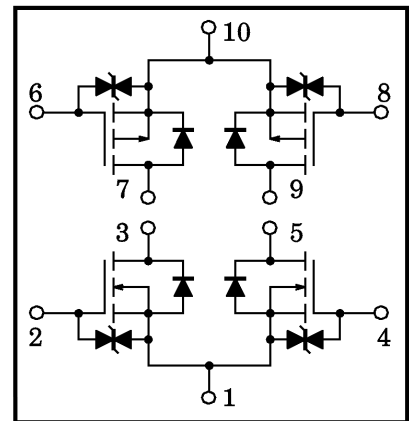
MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	RATING		UNIT	
		Nch	Pch		
Drain-Source Voltage	$V_{DSS}$	60	-60	V	
Drain-Gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	60	-60	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	$\pm 20$	V	
Drain Current	DC	$I_D$	5	-5	A
	Pulse	$I_{DP}$	20	-20	
Drain Power Dissipation (1 Device Operation, $T_a = 25^\circ\text{C}$ )	$P_D$	2.0		W	
Drain Power Dissipation (4 Devices Operation, $T_a = 25^\circ\text{C}$ )	$P_{DT}$	4.0		W	
Single Pulse Avalanche Energy*	$E_{AS}$	129	273	mJ	
Avalanche Current	$I_{AR}$	5	-5	A	
Repetitive Avalanche Energy**	1 Device Operation	$E_{AR}$ 0.2		mJ	
	4 Devices Operation	$E_{ART}$ 0.4			
Channel Temperature	$T_{ch}$	150		$^\circ\text{C}$	
Storage Temperature Range	$T_{stg}$	-55~150		$^\circ\text{C}$	



Weight : 2.1 g (typ.)

ARRAY CONFIGURATION



Note ;

\* Avalanche energy (single pulse) applied condition

Nch :  $V_{DD} = 25 \text{ V}$ , Starting  $T_{ch} = 25^\circ\text{C}$ ,  $L = 7 \text{ mH}$ ,  $R_G = 25 \Omega$ ,  $I_{AR} = 5 \text{ A}$

Pch :  $V_{DD} = -25 \text{ V}$ , Starting  $T_{ch} = 25^\circ\text{C}$ ,  $L = 14.84 \text{ mH}$ ,  $R_G = 25 \Omega$ ,  $I_{AR} = -5 \text{ A}$

\*\* Repetitive rating; Pulse Width Limited by maximum channel temperature.

**This transistor is an electrostatic sensitive device. Please handle with caution.**

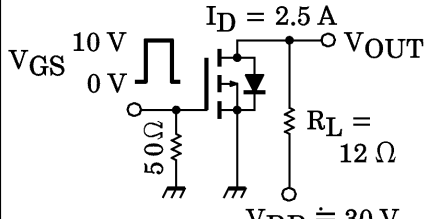
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## THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, $T_a = 25^\circ\text{C}$ )	$\Sigma R_{th}(\text{ch-a})$	31.2	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes (3.2 mm from Case for $t = 10\text{ s}$ )	$T_L$	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ ) (Nch MOS FET)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$	
Drain Cut-off Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	$\mu\text{A}$	
Drain-Source Breakdown Voltage	$V(\text{BR})_{DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	60	—	—	V	
Gate Threshold Voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	0.8	—	2.0	V	
Drain-Source ON Resistance	$R_{DS(\text{ON})}$	$V_{GS} = 4\text{ V}, I_D = 2.5\text{ A}$	—	0.21	0.32	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	—	0.12	0.16		
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 2.5\text{ A}$	3.0	5.0	—	S	
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	370	—	pF	
Reverse Transfer Capacitance	$C_{rss}$		—	60	—		
Output Capacitance	$C_{oss}$		—	180	—		
Switching Time	Rise Time	$t_r$		—	18	—	ns
	Turn-on Time	$t_{on}$		—	25	—	
	Fall Time	$t_f$		—	55	—	
	Turn-off Time	$t_{off}$		$V_{IN} : t_r, t_f < 5\text{ ns},$ $\text{Duty} \leq 1\%, t_w = 10\text{ }\mu\text{s}$	—	170	
Total Gate Charge (Gate-Source Plus Gate-Drain)	$Q_g$	$V_{DD} \approx 48\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 5\text{ A}$	—	12	—	nC	
Gate-Source Charge	$Q_{gs}$		—	8	—		
Gate-Drain ("Miller") Charge	$Q_{gd}$		—	4	—		

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	$I_{DR}$	—	—	—	5	A
Pulse Drain Reverse Current	$I_{DRP}$	—	—	—	20	A
Diode Forward Voltage	$V_{DSF}$	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse Recovery Time	$t_{rr}$	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V}$ $dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	70	—	ns
Reverse Recovery Charge	$Q_{rr}$		—	0.1	—	$\mu\text{C}$

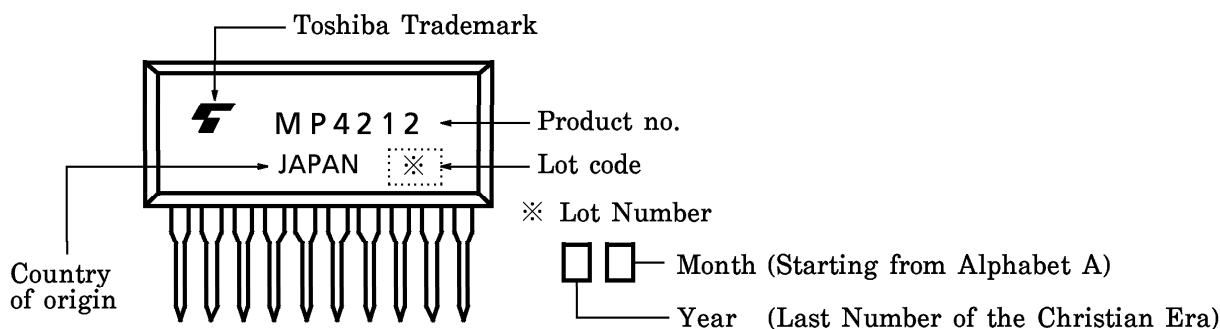
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Pch MOS FET)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain Cut-off Current		$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	—	—	-100	$\mu\text{A}$
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-60	—	—	V
Gate Threshold Voltage		$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-0.8	—	-2.0	V
Drain-Source ON Resistance		$R_{DS(ON)}$	$V_{GS} = -4\text{ V}, I_D = -2.5\text{ A}$	—	0.24	0.28	$\Omega$
			$V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	—	0.16	0.19	
Forward Transfer Admittance		$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}$	2.0	4.0	—	S
Input Capacitance		$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	630	—	pF
Reverse Transfer Capacitance		$C_{rss}$		—	95	—	
Output Capacitance		$C_{oss}$		—	290	—	
Switching Time	Rise Time	$t_r$		—	25	—	ns
	Turn-on Time	$t_{on}$		—	45	—	
	Fall Time	$t_f$		—	55	—	
	Turn-off Time	$t_{off}$		$V_{IN} : t_r, t_f < 5\text{ ns}$ $Duty \leq 1\%, t_w = 10\text{ }\mu\text{s}$	—	200	
Total Gate Charge (Gate-Source Plus Gate-Drain)		$Q_g$	$V_{DD} \cong -48\text{ V}, V_{GS} = -10\text{ V},$ $I_D = -5\text{ A}$	—	22	—	nC
Gate-Source Charge		$Q_{gs}$		—	16	—	
Gate-Drain ("Miller") Charge		$Q_{gd}$		—	6	—	

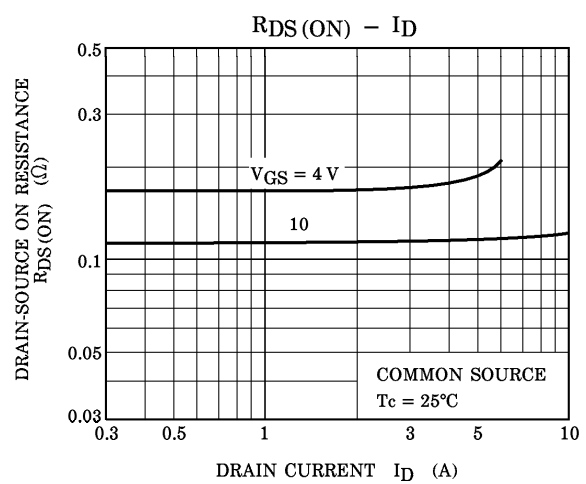
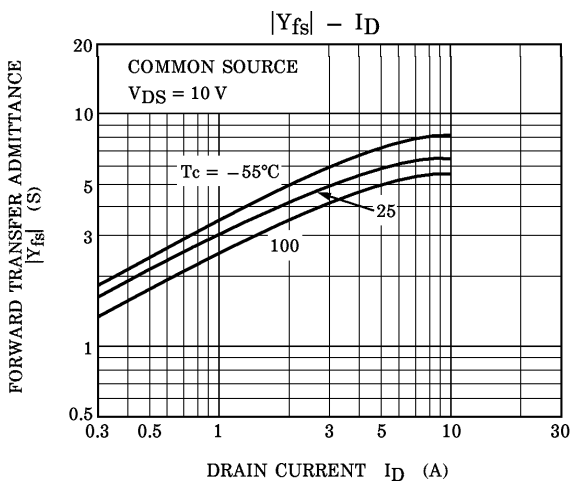
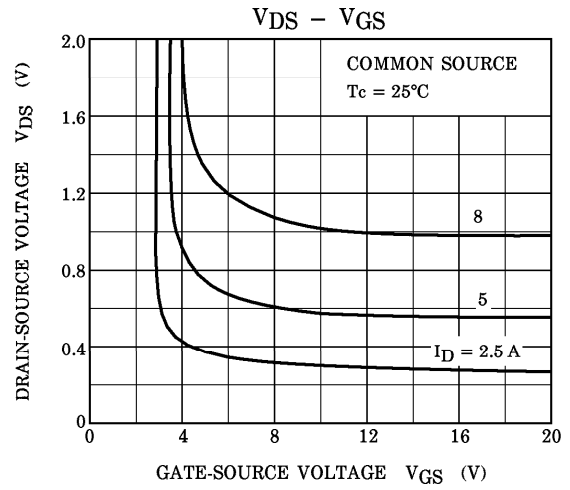
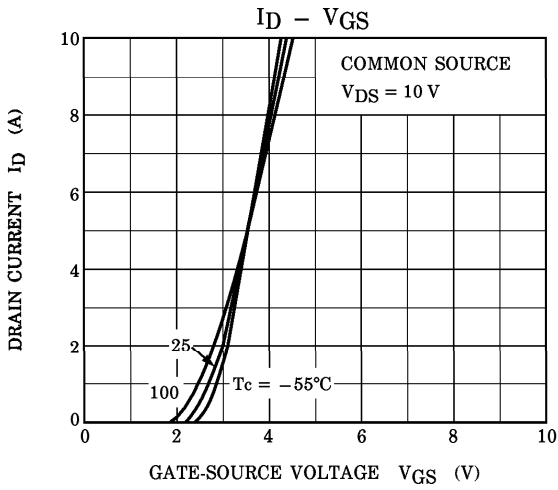
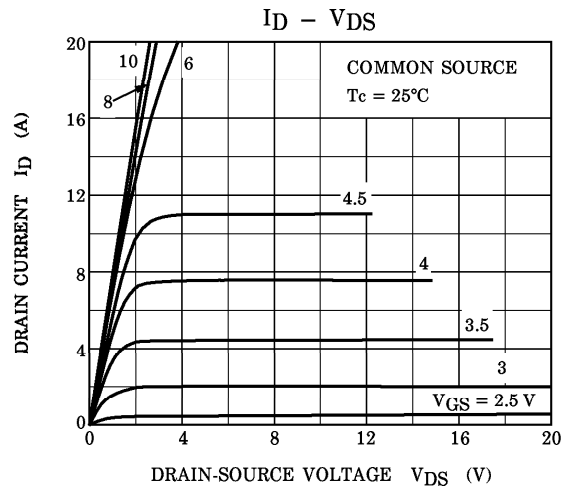
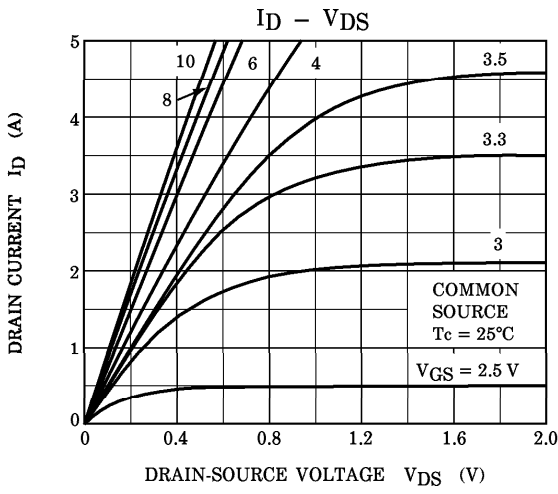
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS (Ta = 25°C)

	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	$I_{DR}$	—	—	—	-5	A
Pulse Drain Reverse Current	$I_{DRP}$	—	—	—	-20	A
Diode Forward Voltage	$V_{DSF}$	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.7	V
Reverse Recovery Time	$t_{rr}$	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	80	—	ns
Reverse Recovery Charge	$Q_{rr}$	$dI_{DR} / dt = 50\text{ A} / \mu\text{s}$	—	0.1	—	$\mu\text{C}$

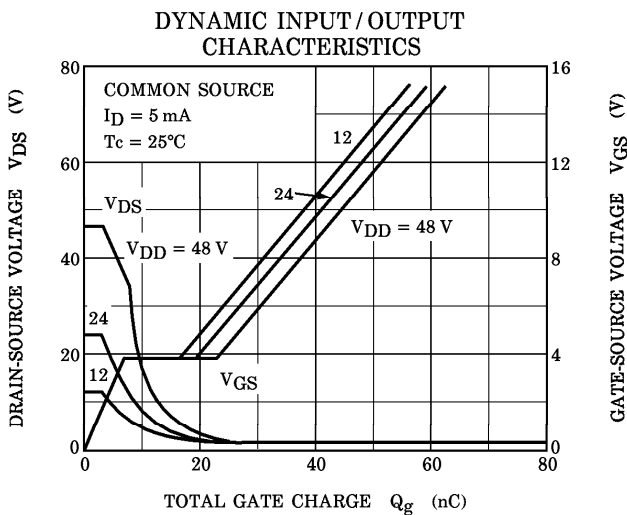
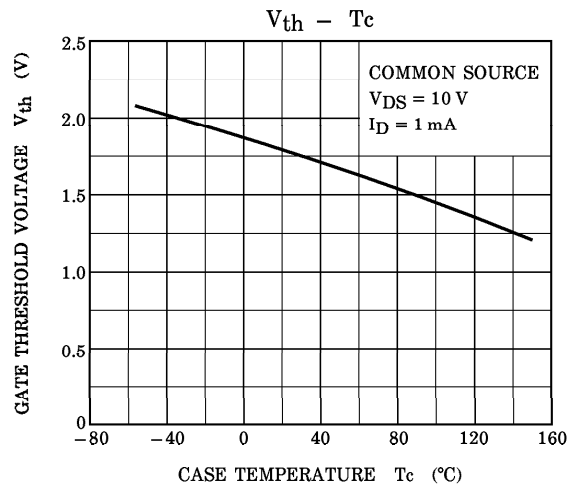
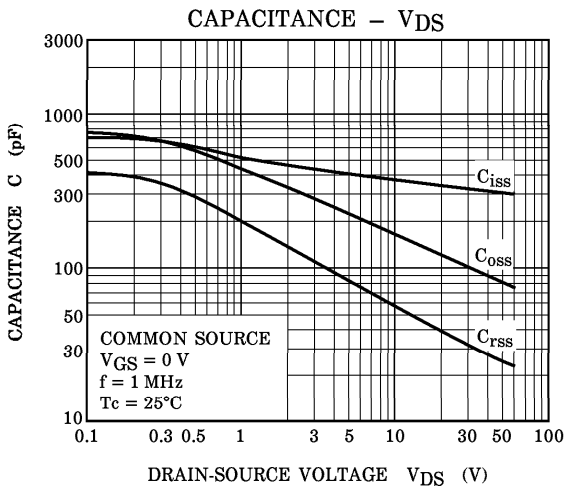
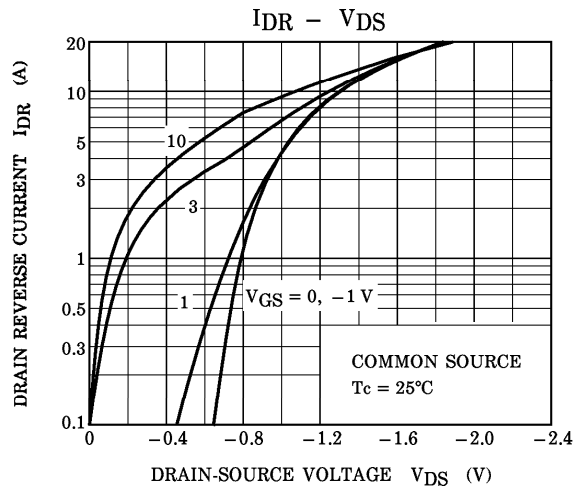
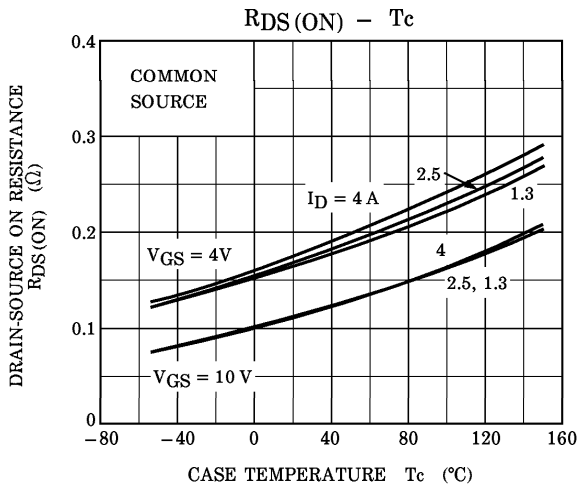
MARKING



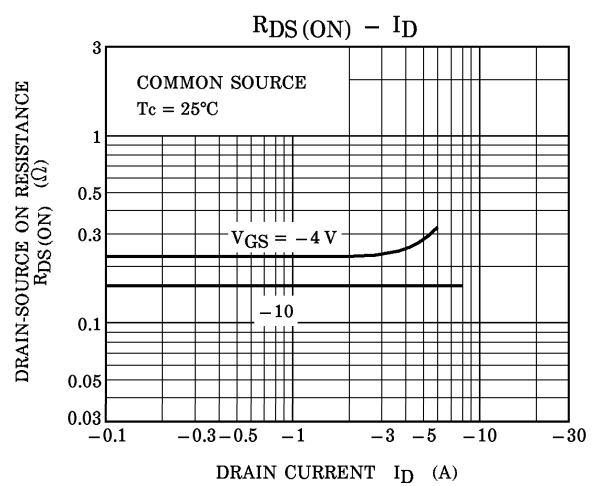
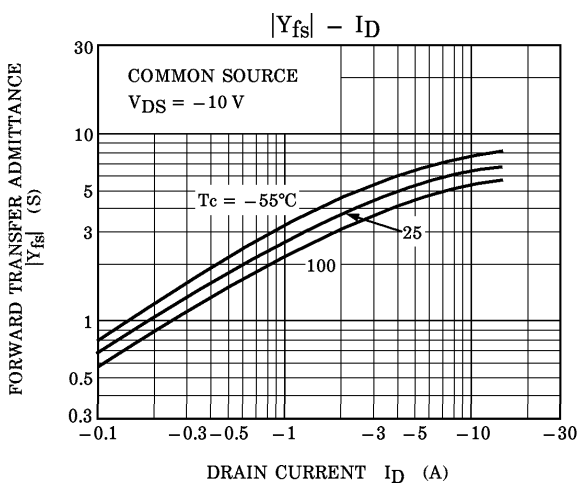
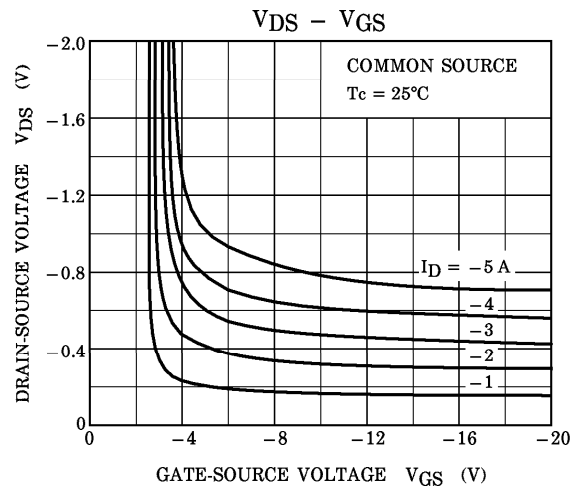
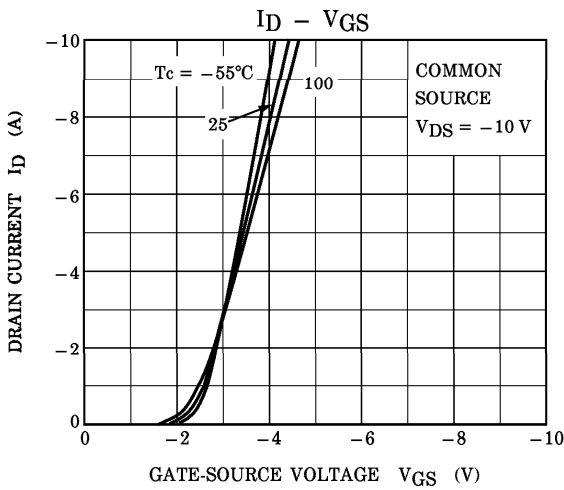
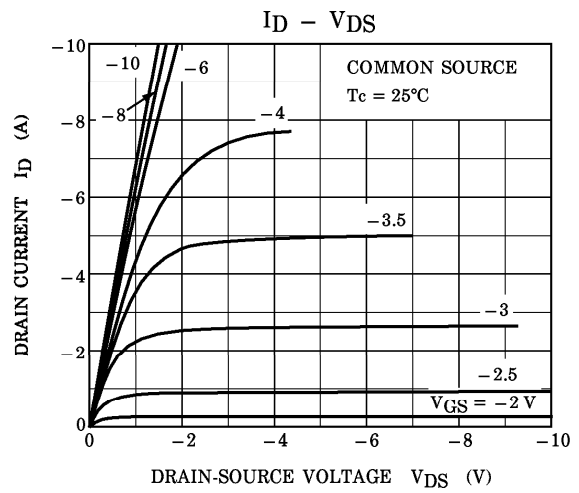
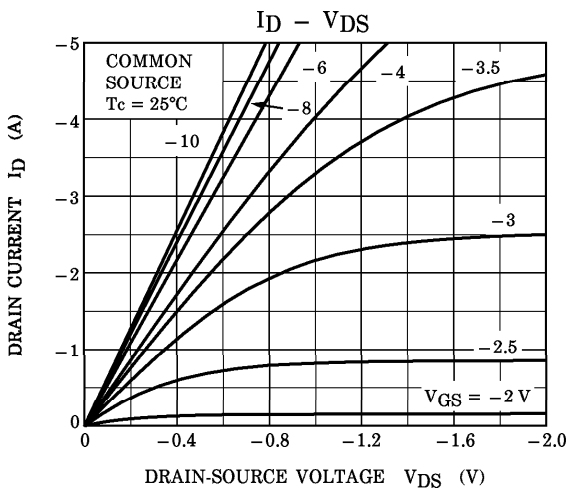
Nch MOS FET



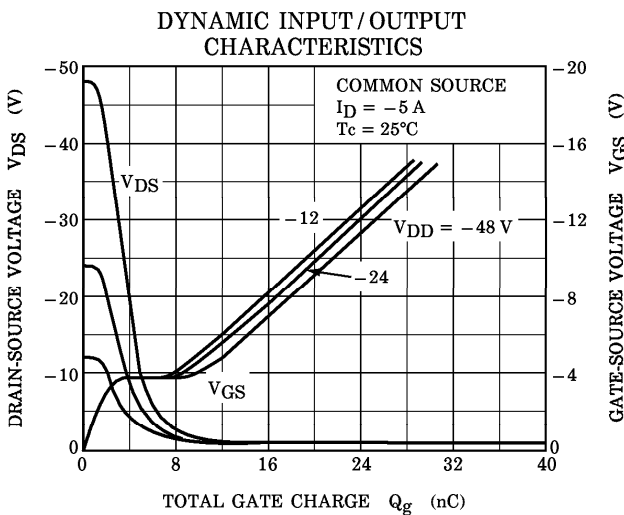
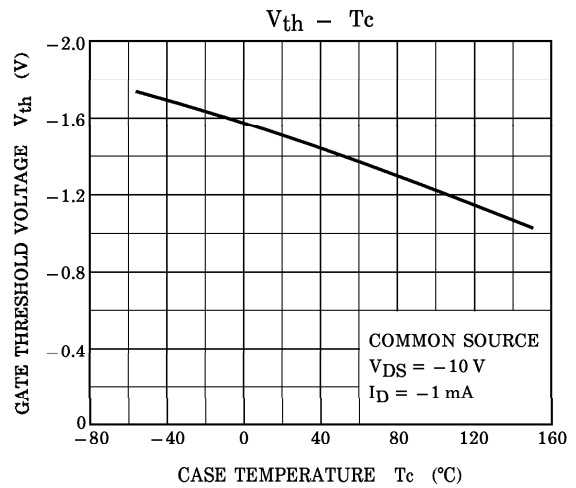
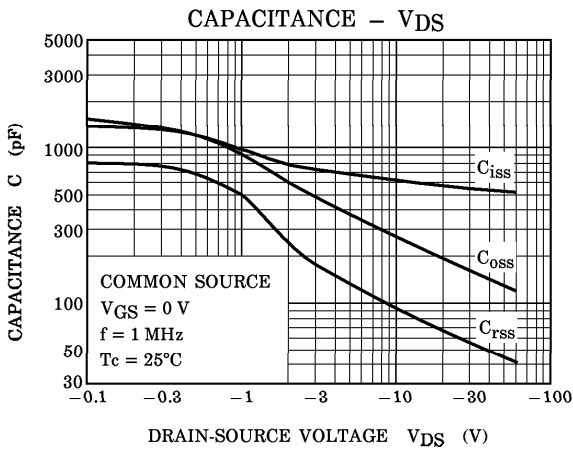
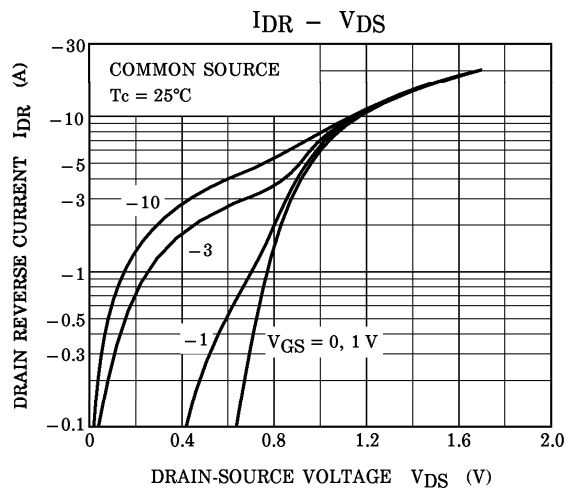
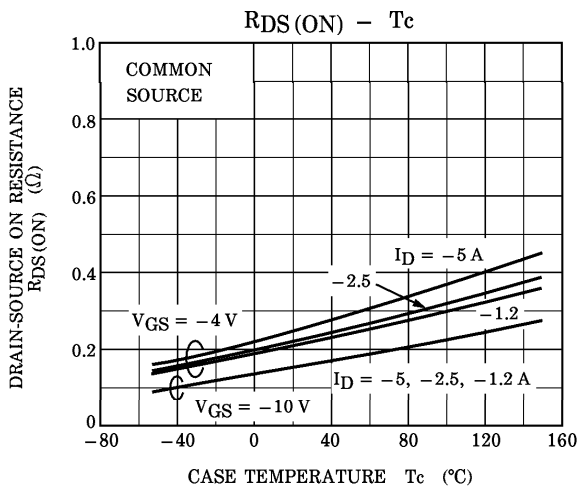
Nch MOS FET

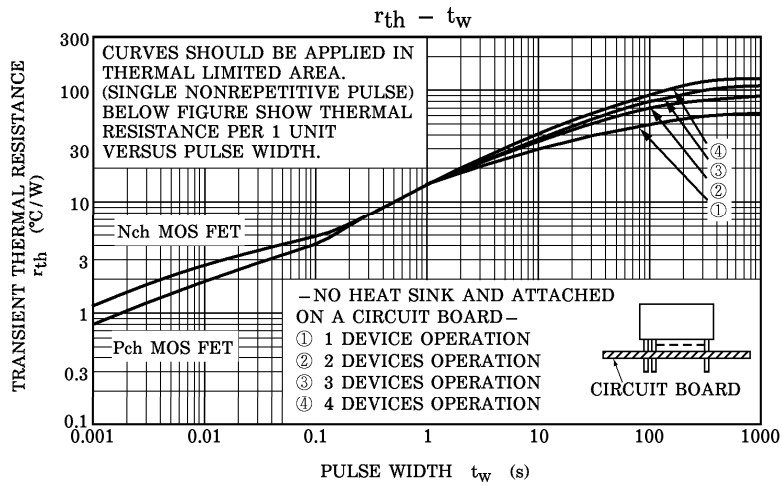
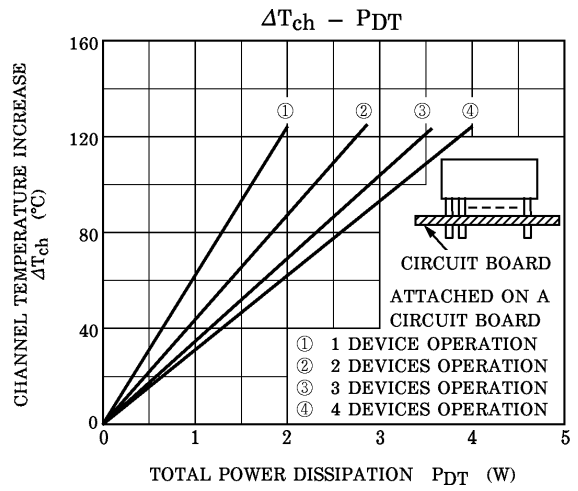
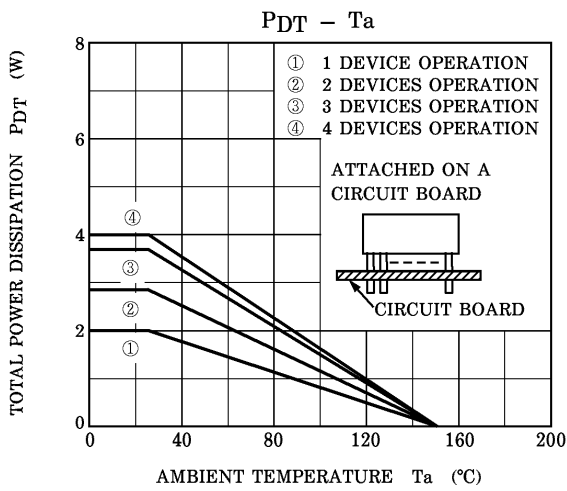


Pch MOS FET



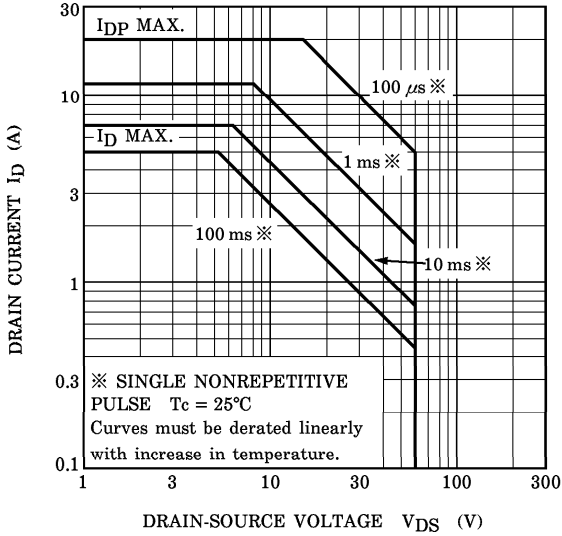
Pch MOS FET



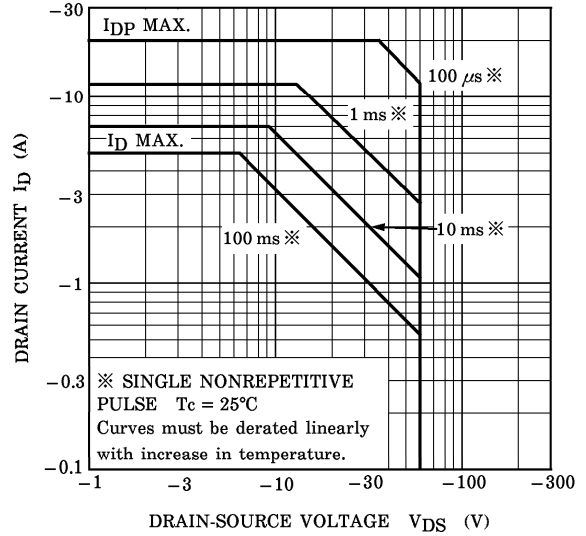




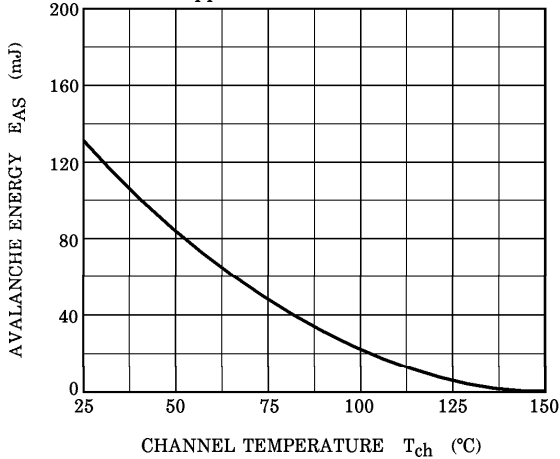
SAFE OPERATING AREA  
(Be applicable to Nch MOS FET)



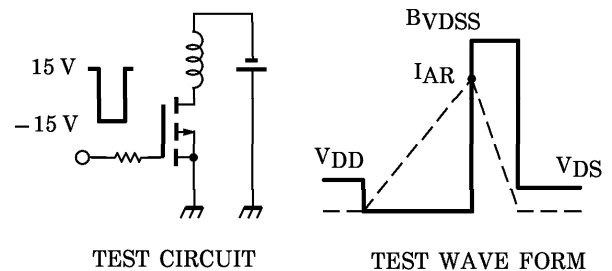
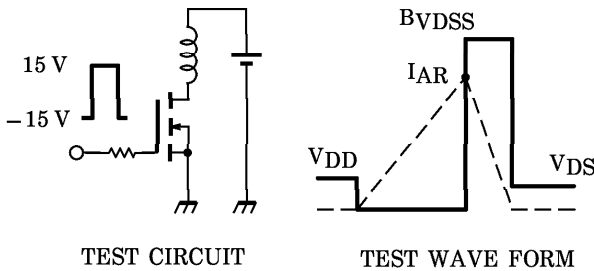
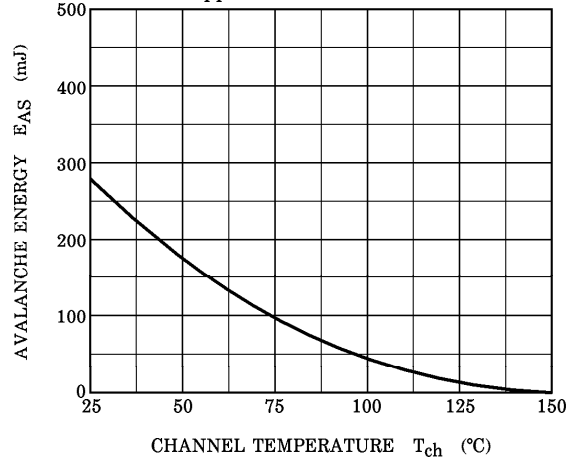
SAFE OPERATING AREA  
(Be applicable to Pch MOS FET)



EAS - T<sub>ch</sub>  
(Be applicable to Nch MOS FET)



EAS - T<sub>ch</sub>  
(Be applicable to Pch MOS FET)



Peak I<sub>AR</sub> = 5 A, R<sub>G</sub> = 25Ω  
V<sub>DD</sub> = 25 V, L = 7 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \right)$$

Peak I<sub>AR</sub> = -5 A, R<sub>G</sub> = 25Ω  
V<sub>DD</sub> = -25 V, L = 14.84 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \right)$$