M66221SP/FP

256 × 9-BIT MAIL-BOX

DESCRIPTION

The M66221 is a mail box that incorporates a complete CMOS shared memory cell of 256 × 9-bit configuration using high-performance silicon gate CMOS process technology, and is equipped with two access ports of A and B.

Access ports A and B are equipped with independent addresses $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ control pins and I/O pins to allow independent and asynchronous read/write operations from/to shared memory individually. This product also incorporates a port adjustment arbitration function in address contention from both ports.

FEATURES

- Memory configuration of 256 × 9 bits
- High-speed access, address access time 40ns (typ.)
- Complete asynchronous accessibility from ports A and B
- Completely static operation
- Built-in port arbitration function
- Low power dissipation CMOS design
- 5V single power supply
- $\overline{\text{Not Ready}}$ output pin is provided (open drain output)
- TTL direct-coupled I/O
- 3-state output for I/O pins.

APPLICATION

Inter-MPU data transfer memory, buffer memory for image processing system.

FUNCTION

The M66221 is a mail box most suitable for inter-MPU data transfer which is used in a multiport mode. Provision of two pairs of addresses and data buses in its shared memory cell of 256 × 9 bit configuration allows independent and asynchronous read/write operations from/to two access ports of A and B individually.

This allows access to shared memory as simple RAM when viewing from one MPU. The concurrent accessibility to shared memory from two MPUs provides remarkable improvement of a multiport mode processor system in throughput.

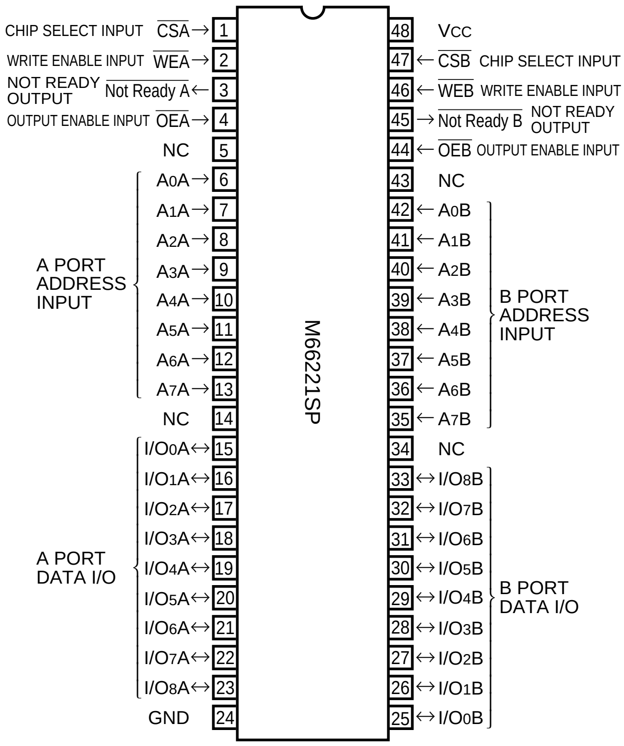
The arbitration function incorporated in the chip decides the first-in port to assign a higher priority to the access from one MPU, even if two MPUs contend for selection of the same address in shared memory from ports A and B. A $\overline{\text{Not Ready}}$ signal "L" is output to the last-in port and invalidates any access from the other MPU.

As a write operation to memory, one of addresses A_0 to A_7 is specified. The $\overline{CS}$ signal is set to "L" to place one of I/O pins in the input mode. Also, the $\overline{WE}$ signal is set to "L". Data at the I/O pin is thus written into memory.

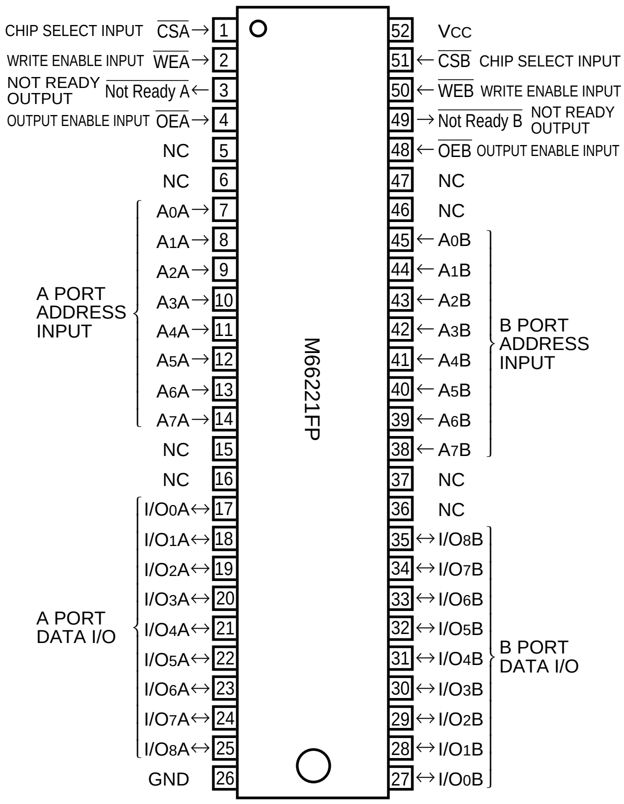
As a read operation, the $\overline{WE}$ signal is set to "H". Both $\overline{CS}$ signal and $\overline{OE}$ signal are set to "L" to place one of I/O pins in the output mode. One of addresses A_0 to A_7 is specified. Data at the specified address is output to the I/O pin.

When the $\overline{CS}$ signal is set to "H", the chip enters a non-select state which inhibits a read and write operation. At this time, the output is placed in the floating state (high impedance state), thus allowing OR tie with another chip. When the $\overline{OE}$ signal is set to "H", the output enters the floating state. In the I/O bus mode, setting the $\overline{OE}$ signal to "H" at a write time avoids contention of I/O bus data. When the $\overline{CS}$ signal is set to Vcc, the output enters the full stand-by state to minimize supply current (See Tables 1 and 2).

PIN CONFIGURATION (Top view)



Outline 48P4B



Outline 52P2G-A

NC: No Connection

BLOCK DIAGRAM

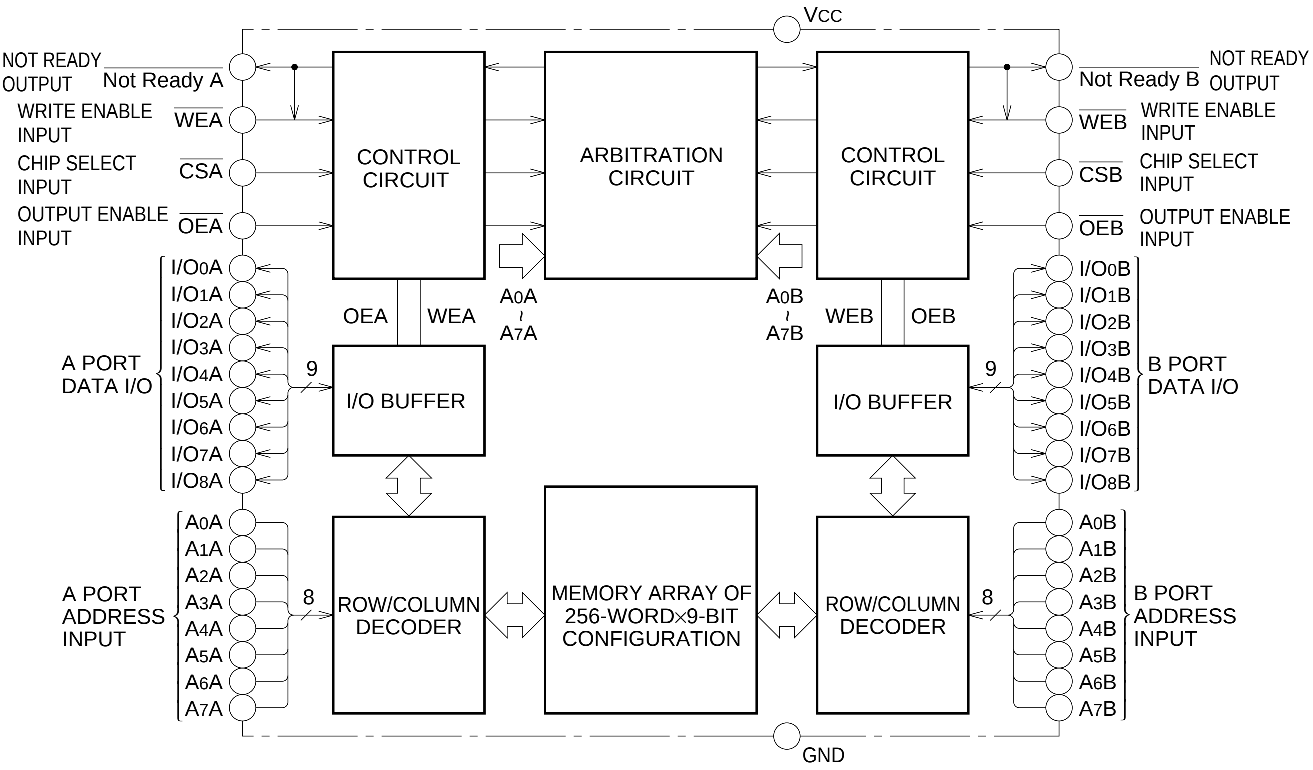


Table 1 Mode Settings of Ports ($A_0A \sim A_7A \neq A_0B \sim A_7B$)

A port input			B port input			Flag		Operation
$\overline{CSA}$	$\overline{WEA}$	$\overline{OEA}$	$\overline{CSB}$	$\overline{WEB}$	$\overline{OEB}$	$\overline{\text{Not}}$ Ready A	$\overline{\text{Not}}$ Ready B	
H	×	×	×	×	×	H	H	A port is set to the non-select mode.
×	×	×	H	×	×	H	H	B port is set to the non-select mode.
L	L	×	×	×	×	H	H	A port is set to the write mode for memory.
L	H	L	×	×	×	H	H	A port is set to the read mode for memory.
×	×	×	L	L	×	H	H	B port is set to the write mode for memory.
×	×	×	L	H	L	H	H	B port is set to the read mode for memory.

Table 2 Basic Functions of Ports

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O pin	ICC
H	×	×	Non-select	High impedance	Stand-by
L	L	×	Write	DIN	Operation
L	H	L	Read	DOUT	Operation
L	H	H		High impedance	Operation

Note 1: × indicates "L" or "H". (Irrelevant)
"H" = High level, "L" = Low level

FUNCTIONAL DESCRIPTION
Arbitration Function

The M66221 has asynchronous accessibility from two independent ports to shared memory, thus remarkably improving the throughput of the entire processor system used in the multiport mode. On the other hand, this accessibility causes a problem of contending for selecting the same address in shared memory during the addressing from both ports.

If the same address is contentionally selected, the following four basic operations are possible depending on an access mode set from both ports:

(1) A port .... Read B port .... Read
(2) A port .... Read B port .... Write
(3) A port .... Write B port .... Read
(4) A port .... Write B port .... Write

In this case, when both ports are operating in the read mode as given in (1), correct data is read to both ports and the contents of memory are not destroyed. There is no special problem. If the other port is in the read mode while one port is operating in the write mode as given in (2) or (3), however, data is written correctly but the data read from the other port in the read mode may change during the same cycle. This comes into question. When both ports are operating in the write mode as given in (4), reverse data is written into each port and the contents of memory may become uncertain. Consequently, no result will be guaranteed.

The M66221 incorporated an arbitration function circuit to solve such problems when contentionally selecting an address from both ports. The arbitration function decides which of A and B ports determines an address first, and unconditionally assigns access priority to the first-in port (At this time, the $\overline{\text{Not Ready}}$ signal holds “H”). As for the last-in port operation, the function inhibits any write to that port from MPU at the same time when “L” is output to the $\overline{\text{Not Ready}}$ output pin at the port regardless of a read or write operation during the period of address matching of both ports. If the address of the first-in port changes after that and both ports do not have the same address, the $\overline{\text{Not Ready}}$ output is reset to “H” and the access in the stopped state is accepted from the last-in port. If the same address is selected by an address input from both ports simultaneously, a decision by the arbitration function on the chip also affords access only from one port, and outputs “L” to the $\overline{\text{Not Ready}}$ output for the other port invalidate any access from MPU. Tables 3 and 4 give the relationship between the port arbitration function and port access.

Arbitration Function and Port Access

Contention No. 1 (Address control)

Table 3 gives the port access states and the $\overline{\text{Not Ready}}$ signal output states if the same address is selected in shared memory by an address input set from A and B ports with $\overline{\text{CSA}}$ = $\overline{\text{CSB}}$ = “L”.

Table 3 Contention Processing by Address Input

$\overline{\text{CSA}}$ = $\overline{\text{CSB}}$ = “L”

Address setting when selecting same address	A port			B port		
	Mode setting	Access	$\overline{\text{Not Ready A}}$	Mode setting	Access	$\overline{\text{Not Ready B}}$
First-in A port	Read	,	H	Read	,	L
First-in B port	Read	,	L	Read	,	H
First-in A port	Read	,	H	Write	×	L
First-in B port	Read	,	L	Write	,	H
First-in A port	Write	,	H	Read	,	L
First-in B port	Write	×	L	Read	,	H
First-in A port	Write	,	H	Write	×	L
First-in B port	Write	×	L	Write	,	H
Simultaneous A and B ports	Arbitration Resolved			Arbitration Resolved		

Contention No. 2 ($\overline{\text{CS}}$ control)

Table 4 gives the port access states and the $\overline{\text{Not Ready}}$ signal output states when setting the $\overline{\text{CS}}$ inputs from A and B ports valid, and selecting the same address in shared memory with A_0A to A_7A=A_0B to A_7B.

Table 4 Contention Processing by $\overline{\text{CS}}$ Input

A_0A ~ A_7A = A_0B ~ A_7B

$\overline{\text{CS}}$ input set when selecting same address	A port			B port		
	Mode setting	Access	$\overline{\text{Not Ready A}}$	Mode setting	Access	$\overline{\text{Not Ready B}}$
First-in A port	Read	,	H	Read	,	L
First-in B port	Read	,	L	Read	,	H
First-in A port	Read	,	H	Write	×	L
First-in B port	Read	,	L	Write	,	H
First-in A port	Write	,	H	Read	,	L
First-in B port	Write	×	L	Read	,	H
First-in A port	Write	,	H	Write	×	L
First-in B port	Write	×	L	Write	,	H
Simultaneous A and B ports	Arbitration Resolved			Arbitration Resolved		

Note 2: “H” = High level, “L” = Low level

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	When defining GND pin as a reference.	–0.3 ~ +7.0	V
V_I	Input voltage		–0.3 ~ V_{CC} + 0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Maximum power dissipation	T_a = 25°C	800	mW
T_{stg}	Storage temperature range		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
V_I	Input voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{IH}	"H" input voltage		2.2		V_{CC}+0.3	V
V_{IL}	"L" input voltage		–0.3		0.8	V
V_{OH}	"H" output voltage (I/O)	I_{OH} = –2mA	2.4			V
V_{OL}	"L" output voltage (I/O)	I_{OL} = 4mA			0.5	V
V_{OL}	Open drain "L" output voltage ($\overline{\text{Not Ready}}$)	I_{OL} = 8mA			0.5	V
I_{IH}	"H" input current	V_I = V_{CC}			10.0	µA
I_{IL}	"L" input current	V_I = GND			–10.0	µA
I_{OZH}	Off state "H" output current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} V_O = V_{CC}			10.0	µA
I_{OZL}	Off state "L" output current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} V_O = GND			–10.0	µA
I_{CC}	Static current dissipation (active)	$\overline{CS}$ < 0.2V, Another input V_{IN} > V_{CC} – 0.2V or V_{IN} < 0.2V, Output pin open			60	mA
I_{SB1}	Stand-by current: Two-port stand-by	$\overline{CSA}$, $\overline{CSB}$ = V_{IH}			5	mA
I_{SB2}	Stand-by current: One-port stand-by	$\overline{CSA}$ or $\overline{CSB}$ = V_{IH} I_{OUT} = 0mA (Active port output pin open)			60	mA
I_{SB3}	Stand-by current: Two-port full stand-by	$\overline{CSA}$, $\overline{CSB}$ > V_{CC} – 0.2V Another input V_{IN} > V_{CC} – 0.2V or V_{IN} < 0.2V			0.1	mA
I_{SB4}	Stand-by current: One-port full stand-by	$\overline{CSA}$ or $\overline{CSB}$ > V_{CC} – 0.2V Another input V_{IN} > V_{CC} – 0.2V or V_{IN} < 0.2V, I_{OUT} = 0mA (Active port output pin open)			30	mA
C_I	Input capacitance				10	pF
C_O	Output capacitance in off state				15	pF

Notes 3: The direction in which current flows into the IC is defined as positive (no sign).
4: The above typical values are standard values for V_{CC} = 5V and T_a = 25°C.

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5V±10%, unless otherwise noted)
Read cycle

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CR}	Read cycle time	70			ns
$t_{a(A)}$	Address access time			70	ns
$t_{a(CS)}$	Chip select access time			70	ns
$t_{a(OE)}$	Output enable access time			35	ns
$t_{dis(CS)}$	Output disable time after $\overline{CS}$ (Note 5)			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ (Note 5)			35	ns
$t_{en(CS)}$	Output enable time after $\overline{CS}$ (Note 5)	5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ (Note 5)	5			ns
$t_{v(A)}$	Data effective time after Address	10			ns

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, Vcc = 5V±10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CW}	Write cycle time	70			ns
$t_{w(WE)}$	Write pulse width	45			ns
$t_{su(A)}$	Address setup time	0			ns
$t_{su(A-WEH)}$	Address setup time for rise of $\overline{WE}$	65			ns
$t_{su(CS)}$	Chip select setup time (for $\overline{WE}$)	65			ns
$t_{su(D)}$	Data setup time	40			ns
$t_{h(D)}$	Data hold time	0			ns
$t_{rec(WE)}$	Write recovery time	0			ns
$t_{dis(WE)}$	Output disable time after $\overline{WE}$ (Note 5)			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ (Note 5)			35	ns
$t_{en(WE)}$	Output enable time after $\overline{WE}$ (Note 5)	0			ns

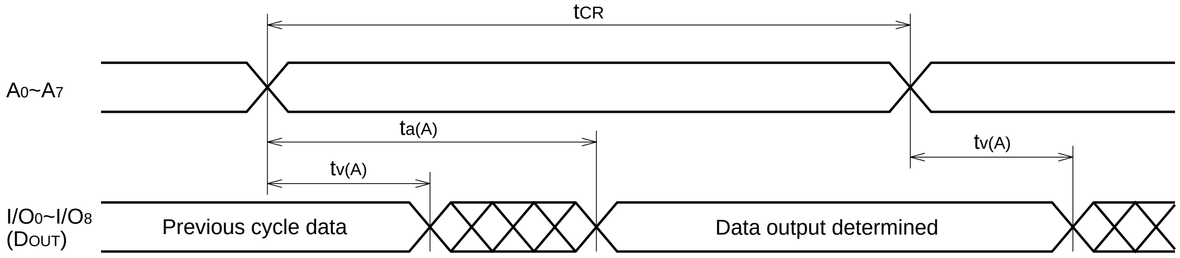
Note 5: The time required for the output to change from a steady state to ±500mV under the load conditions shown in Fig. 2.
This parameter is guaranteed but is not tested at shipment.

NOT READY TIMING (Ta = 0 ~ 70°C, Vcc = 5V±10%, unless otherwise noted)

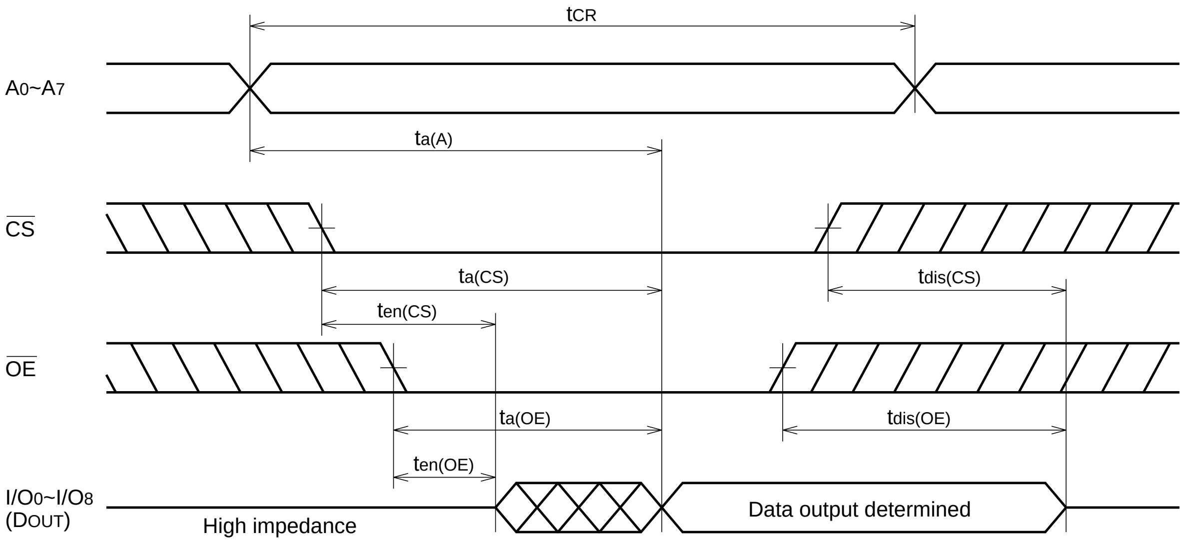
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{NAA}	$\overline{\text{Not Ready}}$ access time from Address			50	ns
t_{NDA}	$\overline{\text{Not Ready}}$ disable time from Address			50	ns
t_{NAC}	$\overline{\text{Not Ready}}$ access time from $\overline{CS}$			50	ns
t_{NDC}	$\overline{\text{Not Ready}}$ disable time from $\overline{CS}$			50	ns
t_{APS}	Arbitration priority setup time	15			ns
t_{NO}	Data output access time from $\overline{\text{Not Ready}}$			0	ns
t_{NW}	Write hold time from $\overline{\text{Not Ready}}$	65			ns

TIMING DIAGRAM
Read Cycle ($\overline{WE}$ = VIH)

Read cycle No. 1 (Address control) ($\overline{CS}$ = $\overline{OE}$ = VIL)

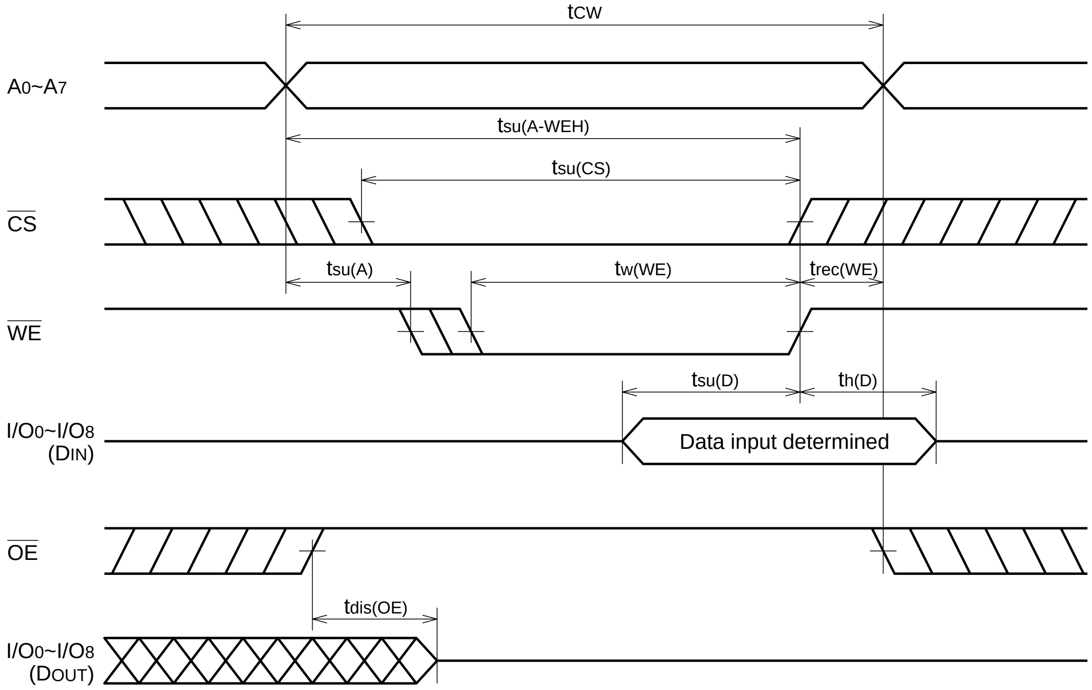


Read cycle No. 2 ($\overline{CS}$ control)

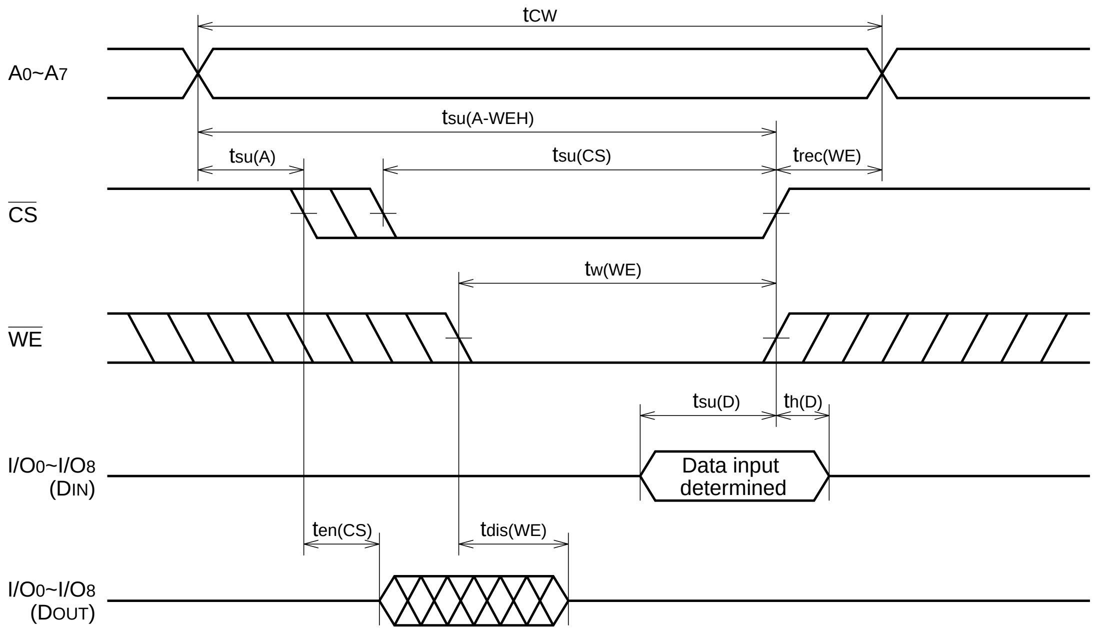


Write Cycle

Write cycle No. 1 ($\overline{WE}$ control)   See Notes 6, 7 and 8.



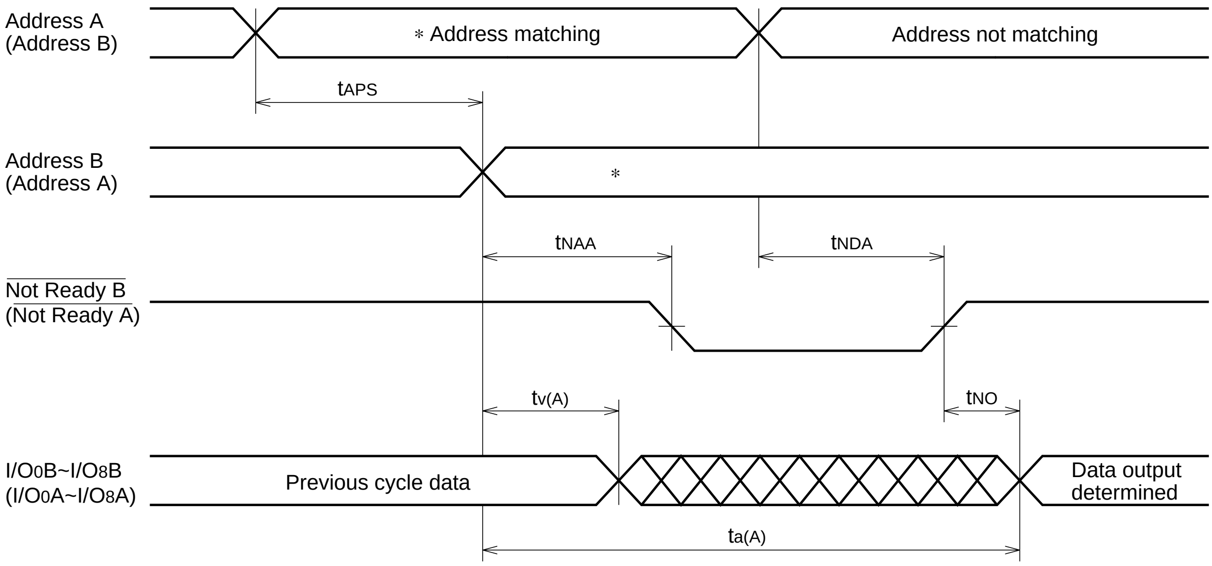
Write cycle No. 2 ($\overline{CS}$ control)   See Notes 6, 7 and 8.



Notes 6: The $\overline{WE}$ of the port must be set to “H” when an address input changes.
7: A write operation is performed during the overlap period when both $\overline{CS}$ and $\overline{WE}$ are “L”.
8: Do not apply any negative-phase signal from outside when an I/O pin is in output state.
9: The shaded part means a state in which a signal can be “H” or “L”.

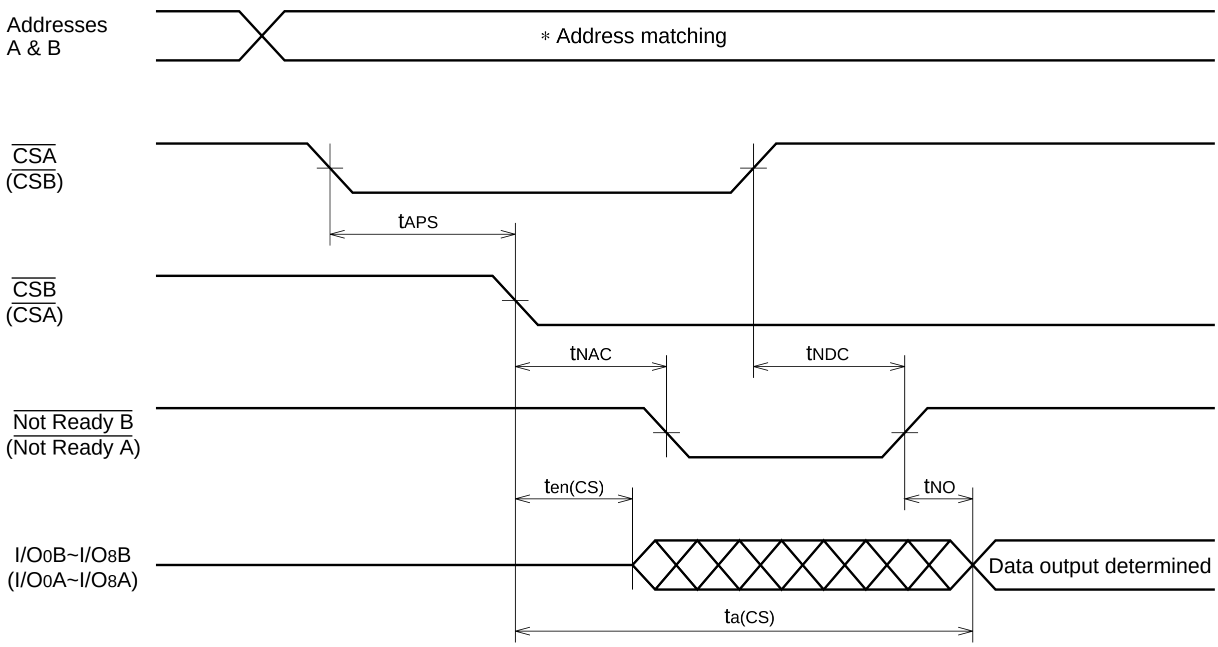
Contention Read Cycle ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})

Contention read cycle No .1 (Address control)   See Notes 10 and 11.



∗ Address A = Address B

Contention read cycle No. 2 ($\overline{CS}$ control)   See Notes 10 and 12.

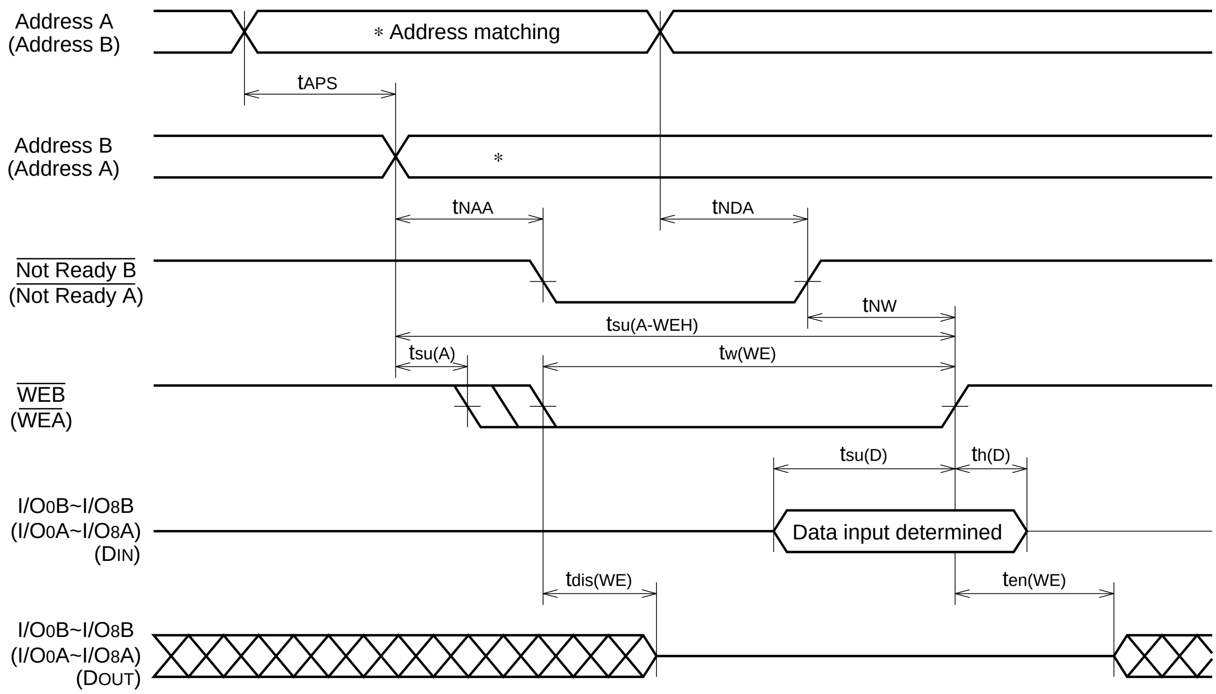


∗ Address A = Address B

Notes 10: The $\overline{\text{Not Ready}}$ output of the first-in port holds "H".
11: When $\overline{CS}$ is set to "L" before the address input is determined.
12: When the address input is determined before $\overline{CS}$ transition to "L".

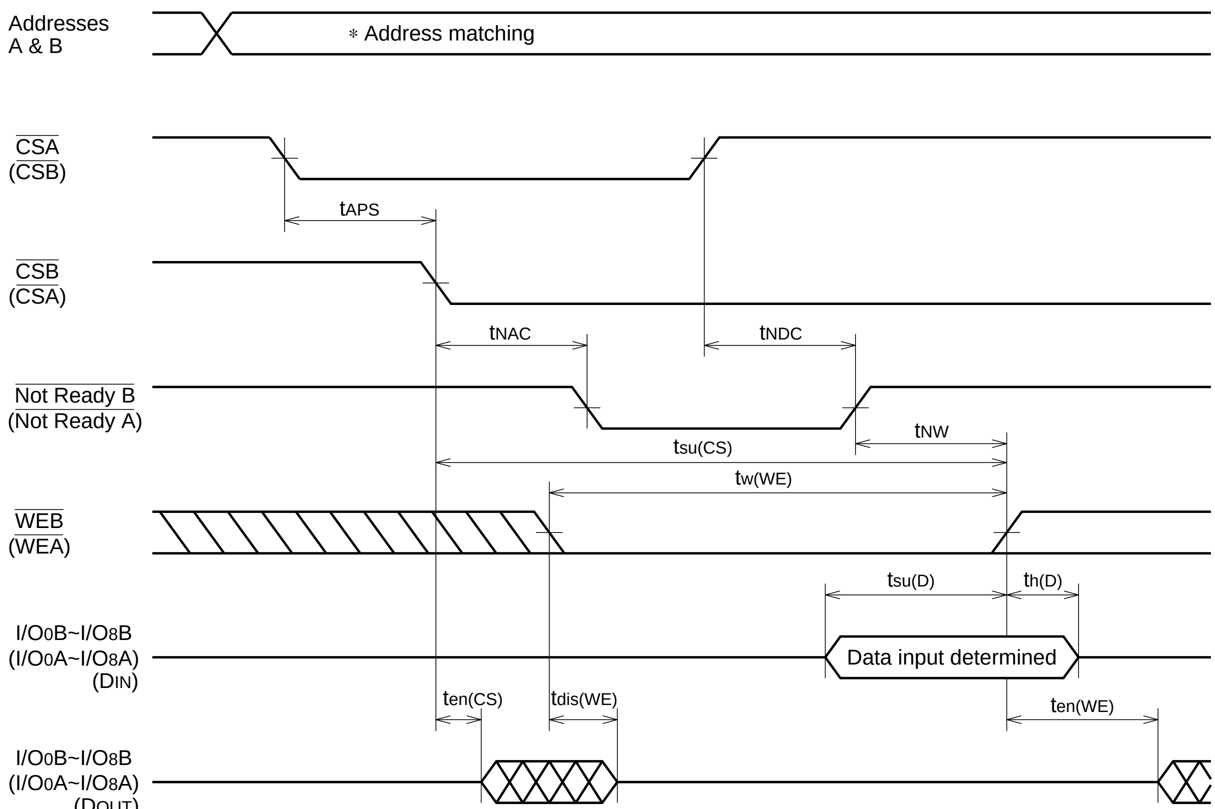
Contention Write Cycle

Contention write cycle No. 1 (WE control)   See Notes 6, 8, 10 and 11.



∗ Address A = Address B

Contention write cycle No. 2 (CS control)   See Notes 6, 8, 10 and 12.



∗ Address A = Address B

MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT

Input pulse level	: V_{IH} = 3.0V, V_{IL} = 0V
Input pulse rise/fall time	: t_r/t_f = 5ns
Input timing reference voltage	: 1.5V
Output timing decision voltage	: 1.5V
Output load	: Figure 1 ~ 3 (The capacitance includes stray wiring capacitance and the probe input capacitance.)

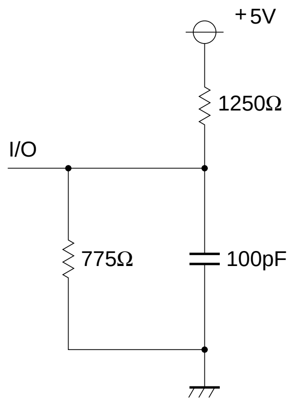


Fig 1. I/O Output Load

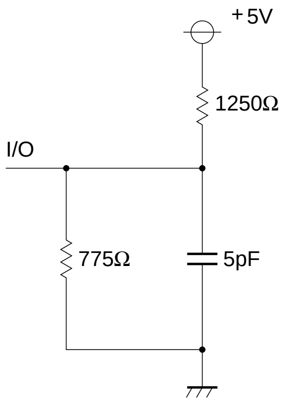


Fig 2. I/O Output Load (to t_{en}, t_{dis})

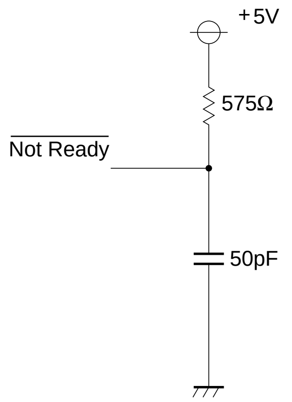


Fig 3. $\overline{\text{Not Ready}}$ Output Load