3.3 VOLT MULTIMEDIA FIFO 256 x 16, 512 x 16, 1,024 x 16, 2,048 x 16, and 4,096 x 16

PRELIMINARY
IDT72V11165, IDT72V12165
IDT72V13165, IDT72V14165
IDT72V15165

FEATURES:

- **256 x 16-bit organization array (IDT72V11165)**
- **512 x 16-bit organization array (IDT72V12165)**
- **1,024 x 16-bit organization array (IDT72V13165)**
- **2,048 x 16-bit organization array (IDT72V14165)**
- **4,096 x 16-bit organization array (IDT72V15165)**
- **15 ns read/write cycle time**
- **5V input tolerant**
- **Independent Read and Write Clocks**
- **Empty/Full and Half-Full flag capability**
- **Output enable puts output data bus in high-impedance state**
- **Available in a 64-lead thin quad flatpack (10x10mm and 14x14mm TQFP)**
- **Industrial temperature range (–40°C to +85°C)**

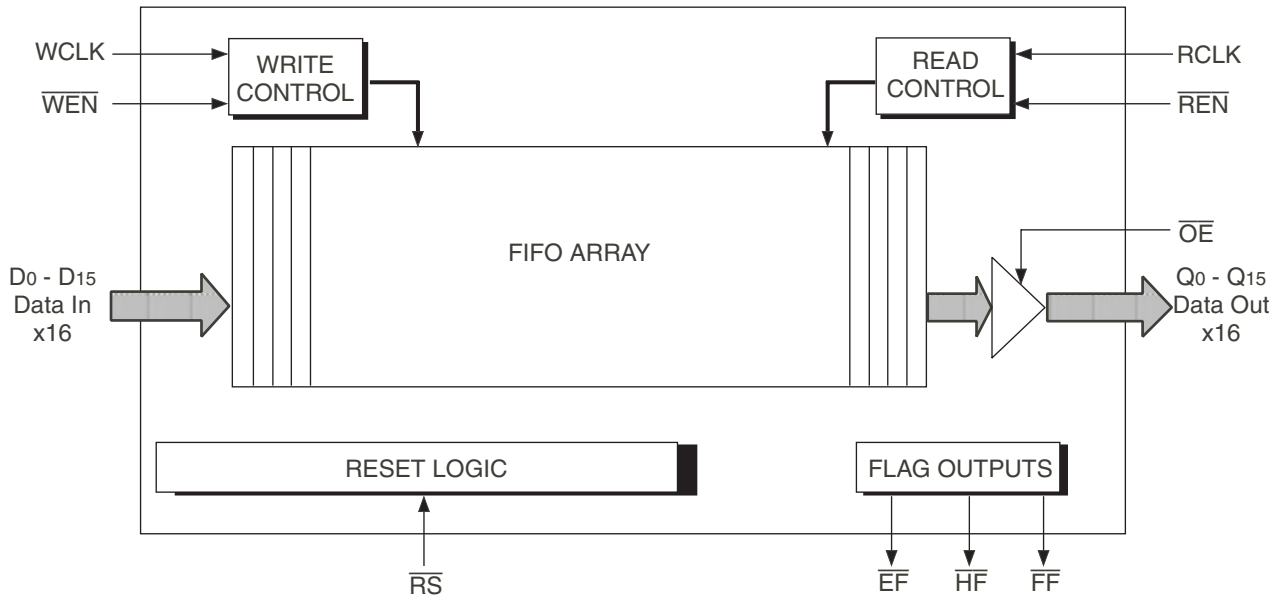
DESCRIPTION:

The IDT72V11165/72V12165/72V13165/72V14165/72V15165 devices are First-In, First-Out (FIFO) memories with clocked read and write controls.

These FIFOs have 16-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and an input enable pin ($\overline{WEN}$). Data is written into the Multimedia FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The Read Clock (RCLK) can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

These Multimedia FIFOs support three fixed flags: Empty Flag ($\overline{EF}$), Full Flag ($\overline{FF}$), and Half Full Flag ($\overline{HF}$).

FUNCTIONAL BLOCK DIAGRAM



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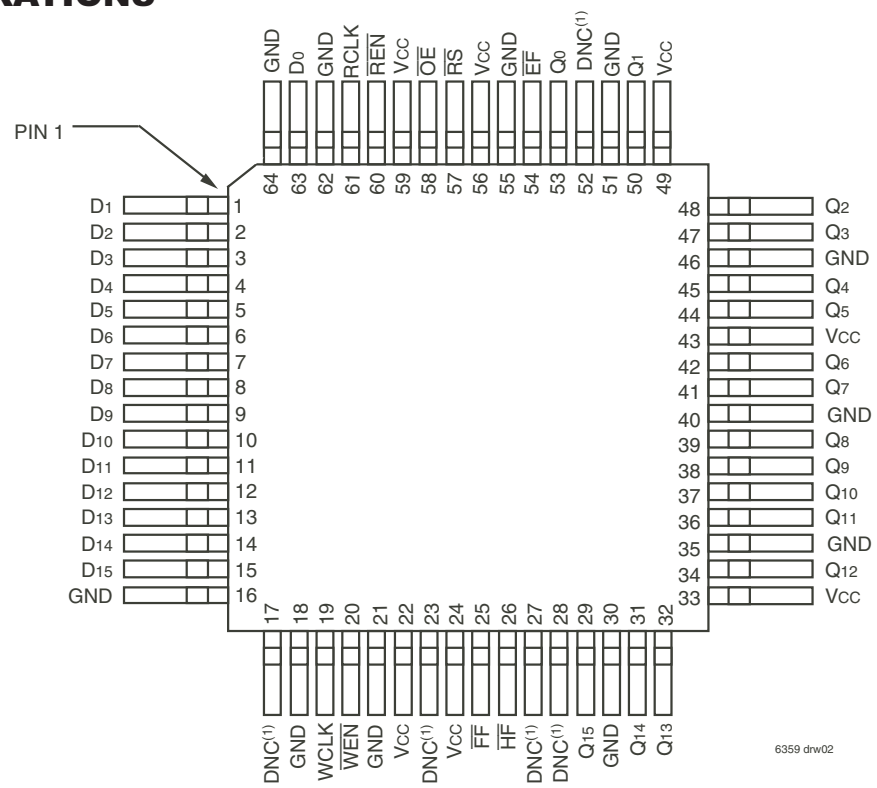
PIN CONFIGURATIONS



NOTE:
1. DNC = Do Not Connect.

STQFP (PP64-1, order code: TF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–D15	Data Inputs	I	Data inputs for an 16-bit bus.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ indicates whether or not the FIFO memory is empty.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ indicates whether or not the FIFO memory is full.
$\overline{HF}$	Half-Full Flag	O	The device is more than half full when $\overline{HF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
Q0–Q15	Data Outputs	O	Data outputs for an 16-bit bus.
RCLK	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ goes HIGH, and $\overline{EF}$ goes LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
VCC	Power	I	+3.3V power supply pins.
GND	Ground	I	Ground pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Industrial	Unit
V_{TERM}[2]	Terminal Voltage with respect to GND	–0.5 to +5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Industrial	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Industrial	2.0	—	5.5	V
V_{IL}[1]	Input Low Voltage Industrial	-0.5	—	0.8	V
T_A	Operating Temperature Industrial	-40	—	85	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	IDT72V11165 IDT72V12165 IDT72V13165 IDT72V14165 IDT72V15165 Industrial t_{CLK} = 15 ns			Unit
		Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (any input)	–1	—	1	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC1}[3,4,5]	Active Power Supply Current	—	—	30	mA
I_{CC2}[3,6]	Standby Current	—	—	5	mA

NOTES:
1. Measurements with $0.4 \le V_{IN} \le V_{CC}$.
2. $\overline{OE} \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$.
3. Tested with outputs disabled (I_{OUT} = 0).
4. RCLK and WCLK toggle at 20 MHZ and data inputs switch at 10 MHz.
5. Typical I_{CC1} = 2.04 + 0.88*fs + 0.02*C_L*fs (in mA).
   These equations are valid under the following conditions:
   V_{CC} = 3.3V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected, ($\overline{OE} \ge V_{IH}$).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Industrial: VCC = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	Industrial IDT72V11165 IDT72V12165 IDT72V13165 IDT72V14165 IDT72V15165 Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	66.7	MHz
t_A	Data Access Time	2	10	ns
t_{CLK}	Clock Cycle Time	15	—	ns
t_{CLKH}	Clock HIGH Time	6	—	ns
t_{CLKL}	Clock LOW Time	6	—	ns
t_{DS}	Data Set-up Time	4	—	ns
t_{DH}	Data Hold Time	1	—	ns
t_{ENS}	Enable Set-up Time	4	—	ns
t_{ENH}	Enable Hold Time	1	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	ns
t_{RSS}	Reset Set-up Time	10	—	ns
t_{RSR}	Reset Recovery Time	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[3]	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	ns
t_{OHZ}	Output Enable to Output in High-Z[3]	3	8	ns
t_{WFF}	Write Clock to Full Flag	—	10	ns
t_{REF}	Read Clock to Empty Flag	—	10	ns
t_{HF}	Clock to Half-Full Flag	—	20	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for $\overline{FF}$ and $\overline{EF}$	6	—	ns

NOTES:
1. Industrial temperature range product for the 15ns speed grade available.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

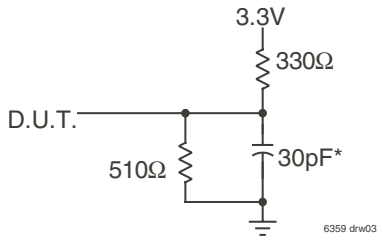


Figure 1. Output Load

* Includes jig and scope capacitances.

FUNCTIONAL DESCRIPTION

WRITE/READ AND FLAG FUNCTION

To write data into to the FIFO, Write Enable ($\overline{WEN}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH. Subsequent writes will continue to fill up the FIFO.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the Half-Full Flag ($\overline{HF}$) would toggle to LOW once the 129th (72V11165), 257th (72V12165), 513th (72V13165), 1,025th (72V14165), and 2,049th (72V15165) word respectively was written into the FIFO.

When the FIFO is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO. D = 256 writes for the IDT72V11165, 512 for the IDT72V12165, 1,024 for the IDT72V13165, 2,048 for the IDT72V14165 and 4,096 for the IDT72V15165, respectively.

If the FIFO is full, the first read operation will cause $\overline{FF}$ to go HIGH. Subsequent read operations will cause the Half-Full Flag ($\overline{HF}$) to go HIGH. Continuing read operations will cause the FIFO to be empty. When the last word has been read from the FIFO, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{15})

Data inputs for 16-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Half-Full Flag ($\overline{HF}$) to HIGH after t_{RSF}. The Full Flag ($\overline{FF}$) will reset to HIGH. The Empty Flag ($\overline{EF}$) will reset to LOW. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the Write Clock (WCLK). Data setup and hold times must be met with respect to the LOW-to-HIGH transition of WCLK.

The Write and Read Clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. The $\overline{FF}$ flag is updated on the rising edge of WCLK.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the Read Clock (RCLK), when Output Enable ($\overline{OE}$) is set LOW.

The Write and Read Clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0-Q_n maintain the previous data value.

Every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH allowing a read to occur. The $\overline{EF}$ flag is updated on the rising edge of RCLK.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (HIGH), the Q output data bus is in a high-impedance state.

OUTPUTS

FULL FLAG/INPUT READY ($\overline{FF}$)

When the FIFO is full, $\overline{FF}$ will go LOW, inhibiting further write operations. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO. D = 256 writes for the IDT72V11165, 512 for the IDT72V12165, 1,024 for the IDT72V13165, 2,048 for the IDT72V14165 and 4,096 for the IDT72V15165.

$\overline{FF}$ is synchronous and updated on the rising edge of WCLK.

EMPTY FLAG/OUTPUT READY ($\overline{EF}$)

When the FIFO is empty, $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

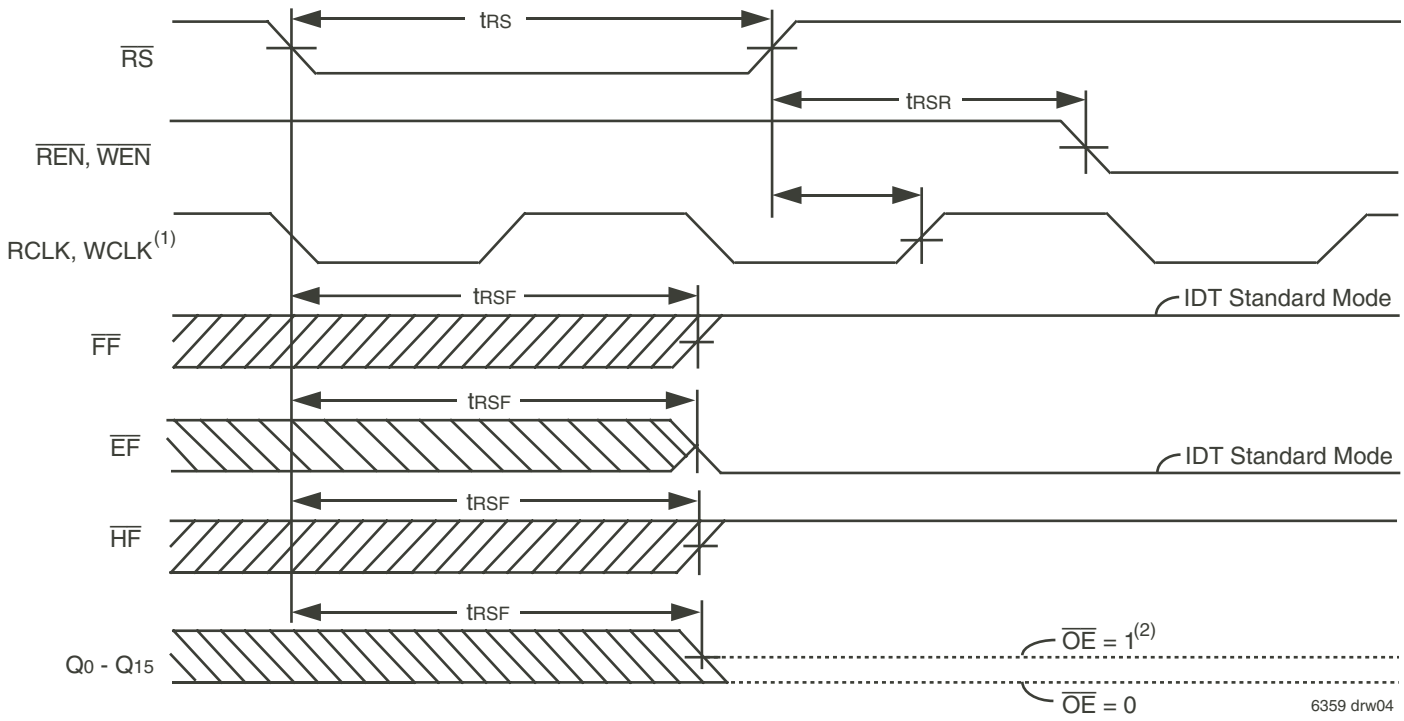
$\overline{EF}$ is synchronous and updated on the rising edge of RCLK.

HALF-FULL FLAG ($\overline{HF}$)

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to HIGH by the LOW-to-HIGH transition of the Read Clock (RCLK). The $\overline{HF}$ is asynchronous.

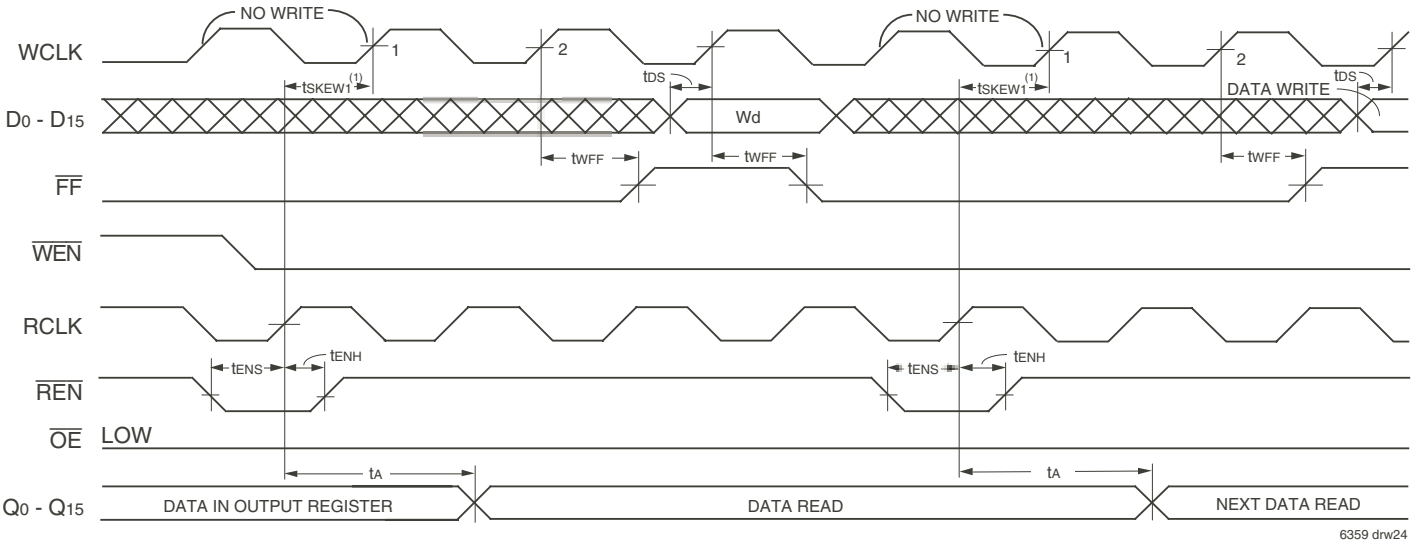
DATA OUTPUTS (Q0-Q15)

Data outputs for 16-bit wide data.



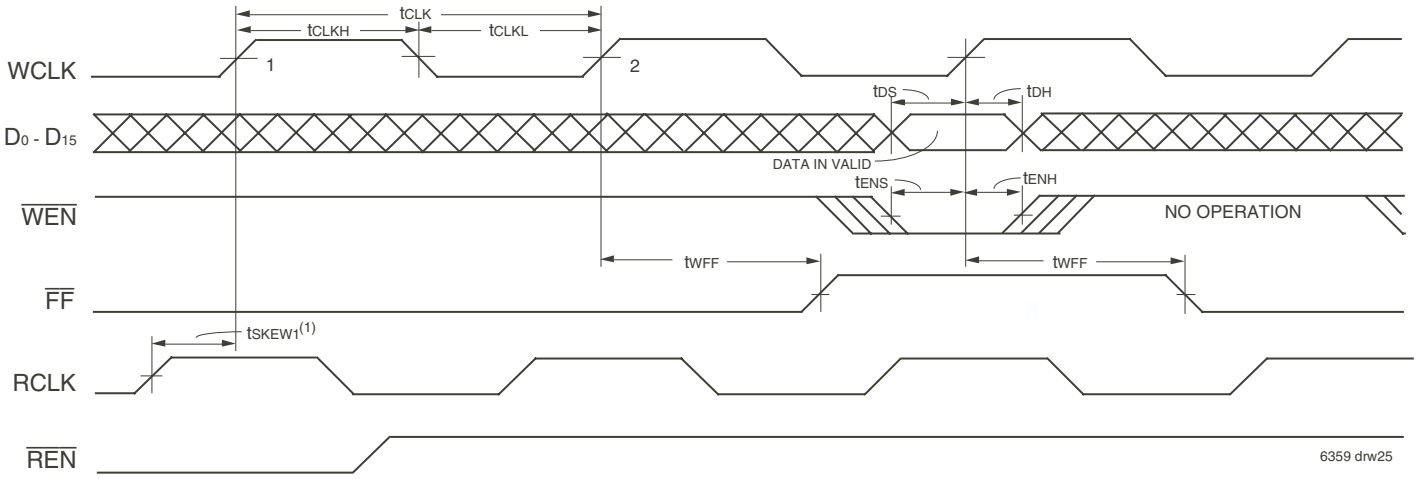
NOTES:
1. The clocks (RCLK, WCLK) can be free-running asynchronously or coincidentally.
2. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and high-impedanced if $\overline{OE}$ = 1.

Figure 2. Reset Timing(1)



NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH after one WCLK cycle plus tWFF. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then the $\overline{FF}$ deassertion time may be delayed an extra WCLK cycle.

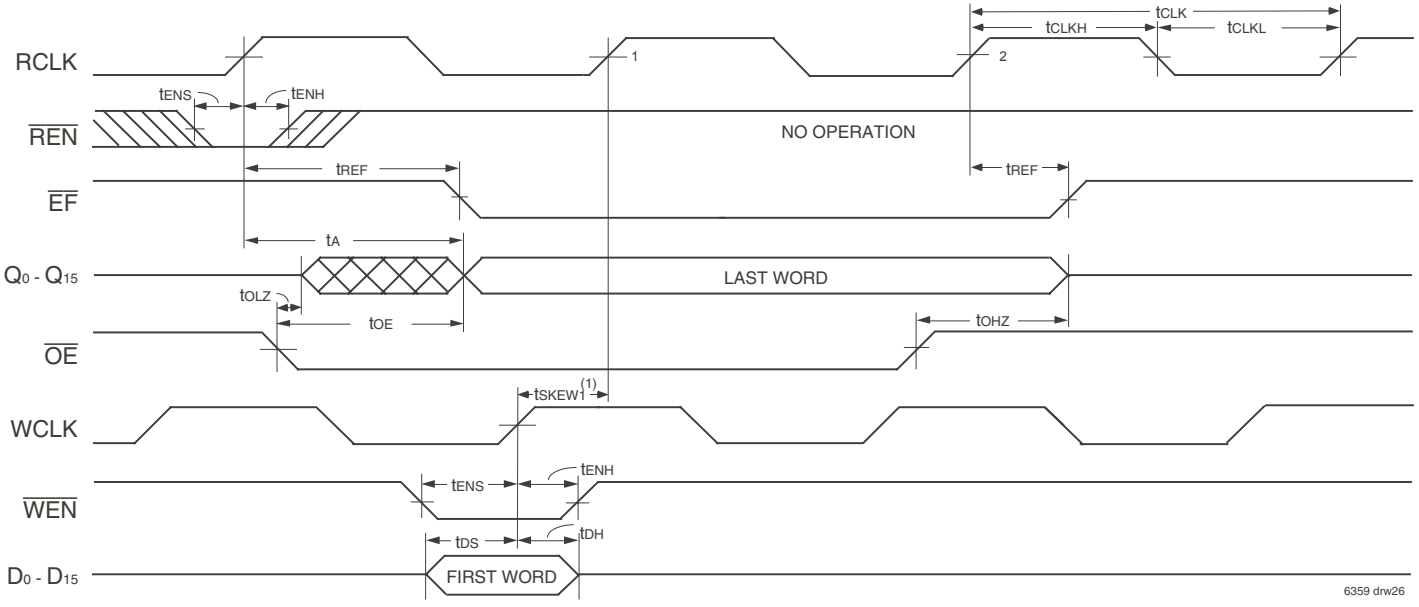
Figure 3. Full Flag Timing



NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH after one WCLK cycle plus t_{RFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}. then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.

Figure 4. Write Cycle Timing

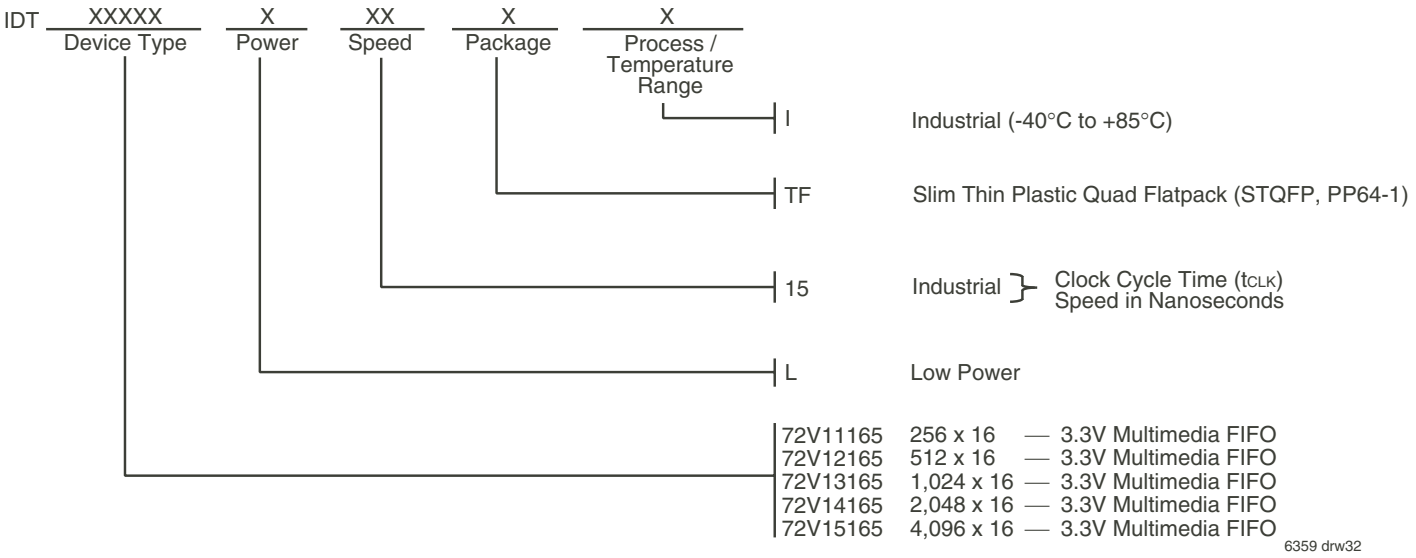


NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH after one RCLK cycle plus t_{REF}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}. then the $\overline{EF}$ deassertion may be delayed an extra RCLK cycle.

Figure 5. Read Cycle Timing

ORDERING INFORMATION



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