PM7341, PM7342, PM7340

S/UNI-IMA PRODUCT FAMILY
S/UNI-IMA-84, S/UNI-IMA-32, S/UNI-IMA-8

84 / 32 / 8 LINK INVERSE MULTIPLEXING OVER ATM (IMA) / UNI PHY

TECHNICAL OVERVIEW

PRELIMINARY

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CONTENTS

1 INTRODUCTION

This document is a technical overview of the S/UNI-IMA product family. It focuses on the features and benefits the product family offers, provides an overview of the devices, describes example applications and summarizes the collateral package available.

This document assists designers of communications equipment in understanding and evaluating the S/UNI-IMA devices by answering the following questions:

1. What functions do the S/UNI-IMA products fulfill in the overall system architecture?
2. What are the applications and equipment that the S/UNI-IMA devices are designed for?
3. How the S/UNI-IMA devices interface seamlessly with other PMC devices and standard products to provide complete high-density and low-density IMA and other ATM-based solutions.

This is a companion document to the following:

- PMC-1991415, PM7341 S/UNI-IMA-84 Datasheet
- PMC-2001724, PM7342 S/UNI-IMA-32 Datasheet
- PMC- 2001723, PM7340 S/UNI-IMA-8 Datasheet

2 S/UNI-IMA PRODUCT FAMILY – FEATURES AND BENEFITS

The S/UNI-IMA product family comprises three monolithic single chip devices: the PM7341 S/UNI-IMA-84, the PM7342 S/UNI-IMA-32 and the PM7340 S/UNI-IMA-8 that implement the ATM Forum Inverse Multiplexing over ATM (IMA) protocol and the Transmission Convergence (TC) layer functions.

The PM7341 S/UNI-IMA-84 supports an industry leading 84 T1 or 63 E1 links in a single device and is optimized for T1/E1 over fiber applications in Multi-Service ATM switches, Metro-Optical Access switches and Third Generation (3G) Wireless Base Station Controllers. The PM7342 S/UNI-IMA-32 supports up to 32 links and is optimized for high density T1, E1 or G.SHDSL applications in DSL Access Multiplexers (DSLAMs), Multi-Service Access Multiplexers, and 3G Wireless Base Station Controllers. For applications requiring low link density such as Integrated Access Devices (IAD) and 3G Base Stations, the PM7340 supports up to 8 T1, E1 or unchannelized links. Unchannelized links may be used to support applications such as for ADSL. See Figure 1.

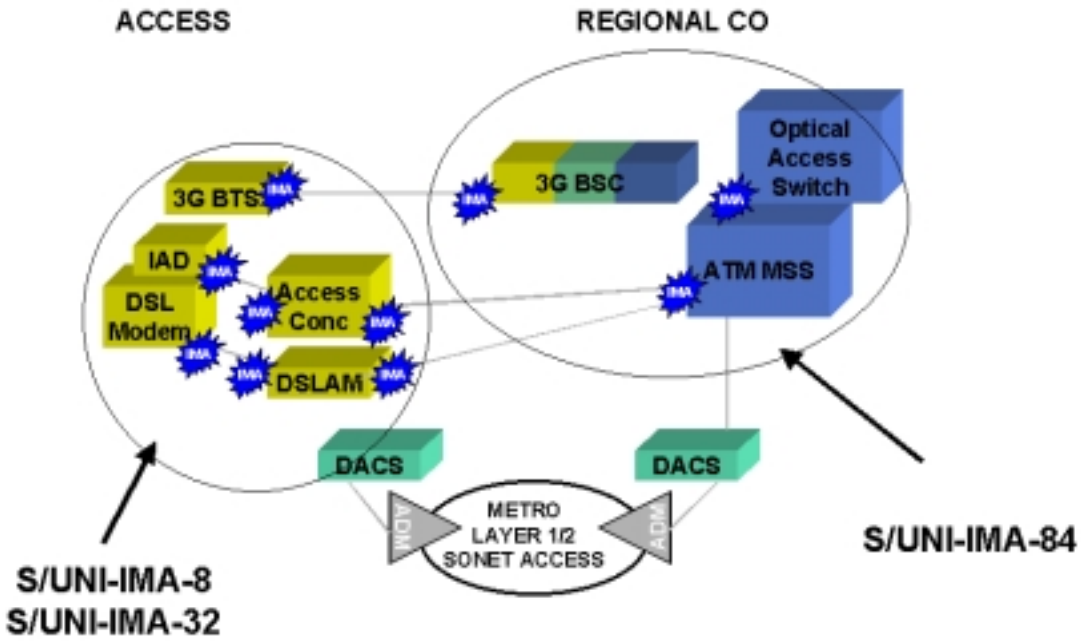

Figure 1. Typical S/UNI-IMA System Applications.

2.1 S/UNI-IMA Overcomes Scalability Issues

Before the introduction of the S/UNI-IMA products, typical IMA devices didn't efficiently scale to high densities for several reasons - throughput limitations in the interfaces and requirements for an external processor for handling data plane processing (IMA link and group state machines). The S/UNI-IMA devices overcome these limitations by both providing higher speed interfaces and implementing link and group state machines on chip thereby radically reducing the requirements for real-time application software.

2.2 Radically Reducing Real Time Application Software Requirements

Other available IMA solutions are software intensive requiring time-critical interrupt processing during normal, ongoing operation as well as during startup, teardown and failure conditions. For every link and for every group, typical IMA solutions require interrupt-driven state machines to be maintained in software. And worst of all, state transitions and the communication of these state transitions to the other end place an *absolutely time-critical* requirement on the embedded software. Not only does this require significant effort in developing, debugging and optimizing real-time IMA software but also limits the ability to scale to higher link densities.

To alleviate the software development effort and the real-time constraints during normal on going operation, the S/UNI-IMA products implement link and group state machines on-chip thereby providing *deterministic wire-rate performance* and *radically reducing real-time embedded software requirements*. With an on-chip implementation of link and group state machines, the S/UNI-IMA devices provide the ability to easily scale to support from nxT1/E1/xDSL unchannelized links to unprecedented channelized OC-48 rates.

An external processor is used for configuration, to collect statistics and to manage fault conditions.

2.3 High Speed System Interfaces

The S/UNI-IMA products break the throughput bottlenecks found in the system interfaces of typical IMA devices. In addition to supporting the UTOPIA L2 standard, the S/UNI-IMA devices support the Any-PHY bus which overcomes the 31 PHY limit of UTOPIA L2. With the Any-PHY bus, which provides seamless interconnect to PMC-Sierra's PM7326 S/UNI-APEX ATM/Packet Traffic Manager and Switch device, all 84 PHYs in the S/UNI-IMA-84 are fully addressable.

On the lineside interface, eighty-four sets of clock/data signals would be unwieldy. To overcome this rat's nest of connections, the S/UNI-IMA-84 provides a high density Scaleable Bandwidth Interconnect (SBI™) bus. The SBI bus is an 8-bit time-division multiplexed bus which efficiently and seamlessly interconnects several multi-port layer 2 devices such as the S/UNI-IMA-84 to multiple high density layer 1 framers such as the PM8316 TEMUX-84. The SBI bus operates at a 19.44 MHz clock rate and is capable of transferring both synchronous and asynchronous data up to OC-3 rates per bus segment. For higher rate applications, multiple SBI buses can be used in parallel. For example four SBI buses can be used for channelized OC-12 applications as shown in Figure 3.

For those applications requiring a clock and data interface the S/UNI-IMA-84 also supports 32 two-pin clock and data interfaces for interconnecting, for example, to standard framers.

2.4 High Density Linecards

As shown in Figure 2, a typical 3 x DS3 IMA design requires over forty devices including DS3 Framers, M13 Multiplexers, T1/E1 Framers, Cell Delineation / IMA devices, SRAM and an external microprocessor for implementing either the link, the group or both the link and group state machines. In comparison, the two chip S/UNI-IMA-84 / TEMUX-84 design, with a single low-cost SDRAM, shown on the right replaces over forty devices providing lower power per link, lower cost per link and a significant savings in board space. With the reduction in board space and power, the optimized S/UNI-IMA-84 / TEMUX-84 solution enables a new generation of high density OC-12 and OC-48 IMA / UNI and Any Service Any Port linecards.

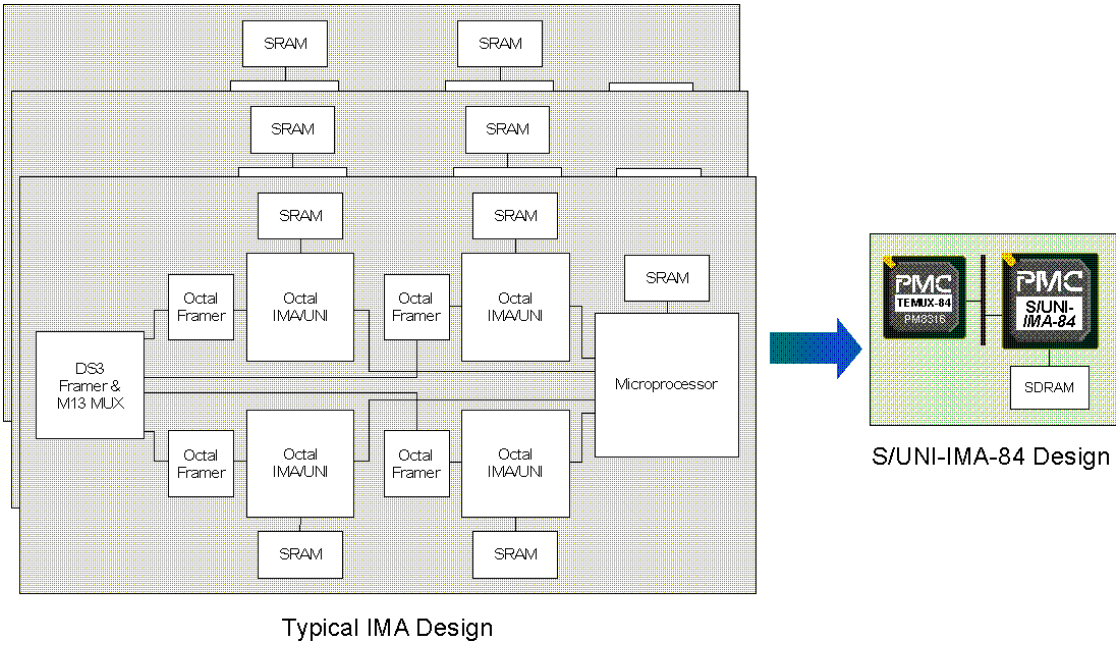

Figure 2. The S/UNI-IMA-84 and TEMUX-84 provide over Ten Times the Density of Other Available Solutions.

2.5 Complete Architectural Solutions

With the S/UNI-IMA-84 and its support for the SBI™ bus, high density Any Service Any Port linecards can be easily designed with PMC-Sierra's SPECTRA™, TEMUX™, AAL1gator™, MECA™, FREEDM™, S/UNI -APEX™ and S/UNI -ATLAS™ products for supporting a broad spectrum of existing and emerging services including Frame Relay (FR), Internet Protocol (IP), Dedicated Private Line, Integrated Voice and Data, Voice-over- IP and Voice-over-ATM as shown in Figure 3.

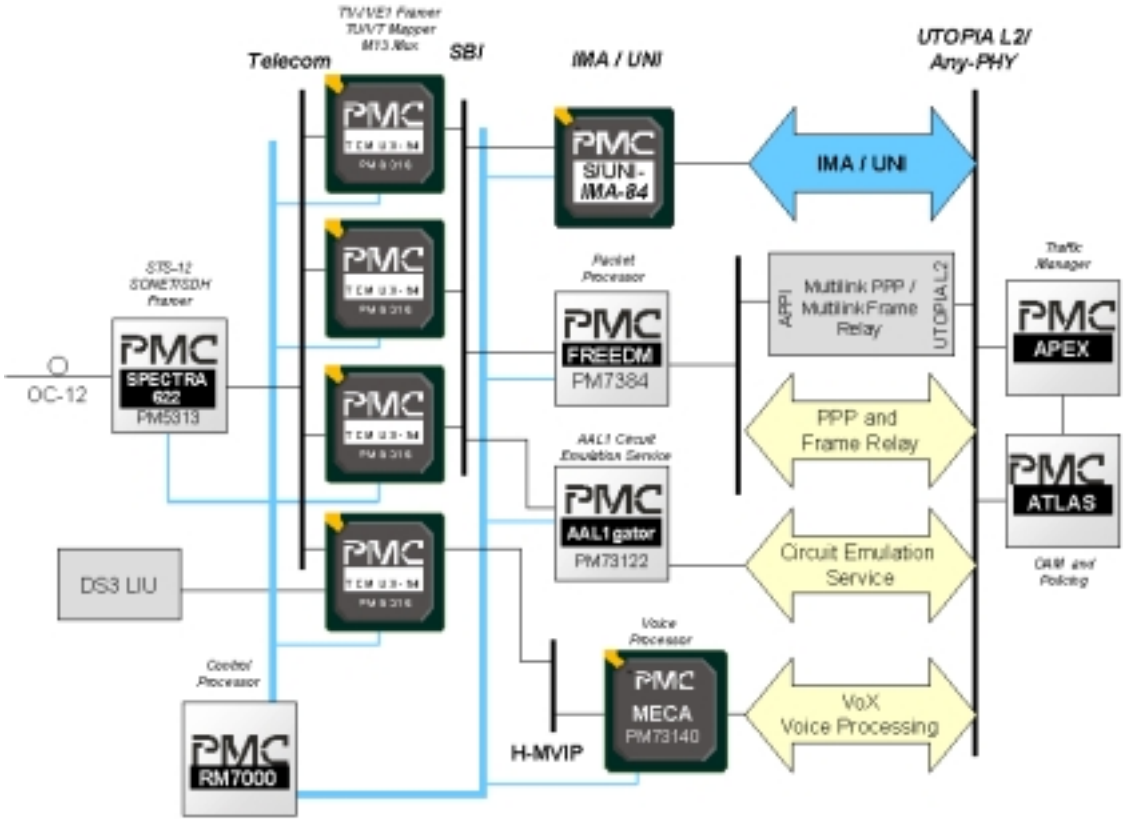

Figure 3. High-Density Any-Service Any Port Linecard Supporting FR, IP, CES, ATM IMA/UNI and VoATM.

2.6 Wide Range of Rates

The S/UNI-IMA devices support a wide range of rates from nxDS0, nxT1/E1/xDSL up to DS3 as shown in Figure 4 supporting either IMA or Transmission Convergence layer functions.

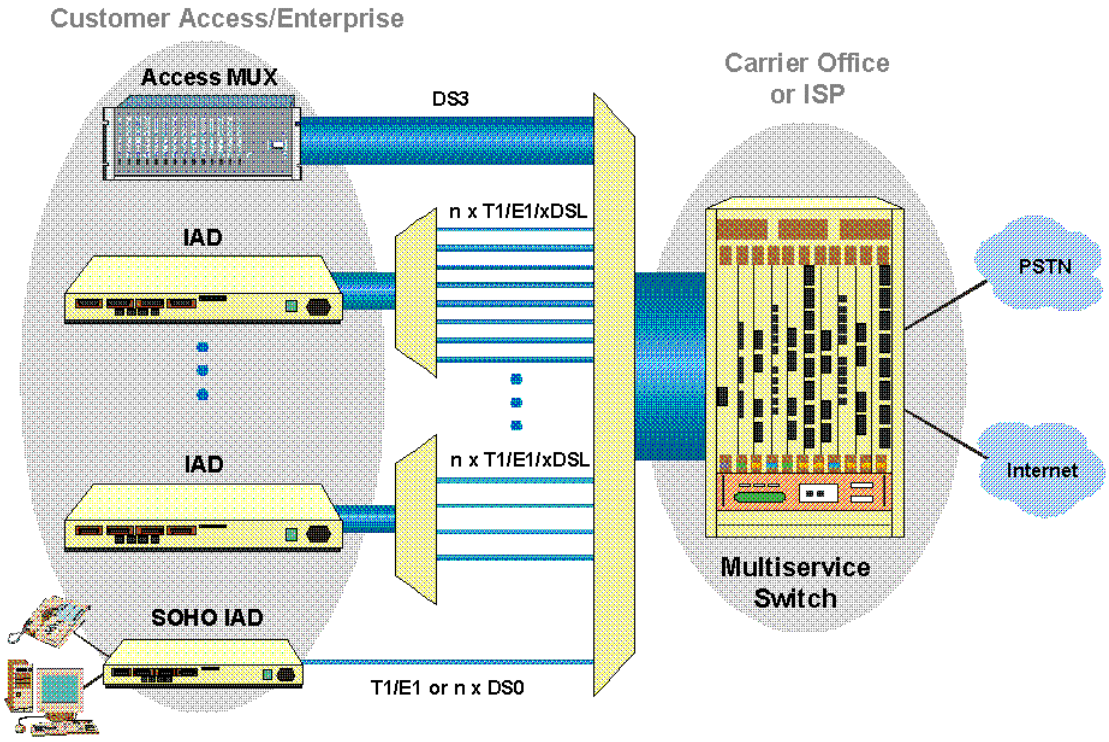

Figure 4. S/UNI-IMA Devices Support a Wide Range of Rates.

2.7 Time To Market

In addition to the benefits described above of:

- on-chip link and group state machines reducing real-time embedded software requirements,
- simplified hardware design with seamless interconnect using the 52 MHz UTOPIA L2 / Any-PHY bus and the SBI bus or clock and data interface and
- integrated cell delineation, IMA, data plane processing and cell FIFOs with a glueless interface to a single low cost external SDRAM,

The S/UNI-IMA product family offers a comprehensive support package including datasheets, royalty-free software drivers with freely available source code, user manual, hardware reference designs, programmer's manual and device models available on PMC-Sierra's web site at http://www.pmc-sierra.com. See Section 7 for reference material availability.

2.8 Standards Compliant

Because of the stringent IMA deployment requirements demanded by major carriers, S/UNI-IMA development was executed in close collaboration with major network equipment vendors. The S/UNI-IMA devices support the following standards:

- ATM Forum Inverse Multiplexing for ATM Specification Version 1.1, March 1999
- ATM Forum Inverse Multiplexing for ATM Specification Version 1.0 – supports the method of reporting Rx cell information as in Appendix C.8 of the ATM Forum Inverse Multiplexing for ATM Specification Version 1.1 for symmetrical configurations with M=128.
- I.432-1 B-ISDN User Network Interface – Physical Layer Specification: General Characteristics
- I.432-3 B-ISDN User Network Interface – Physical Layer Specification: 1544 kbps and 2048 kbps operation
- DS3 Physical Layer Interface Specification, af-phy-0054.000 January, 1996
- ATM on Fractional E1/T1, af-phy-0130.00 October, 1999

3 S/UNI-IMA DEVICE OVERVIEW

The S/UNI-IMA devices integrate IMA and extend the T1/E1 UNI functionality found in the PM7344 S/UNI-MPH and the DS3 UNI functionality found in the PM7346 S/UNI-QJET and PM7347 S/UNI-JET devices as illustrated in Figure 5.

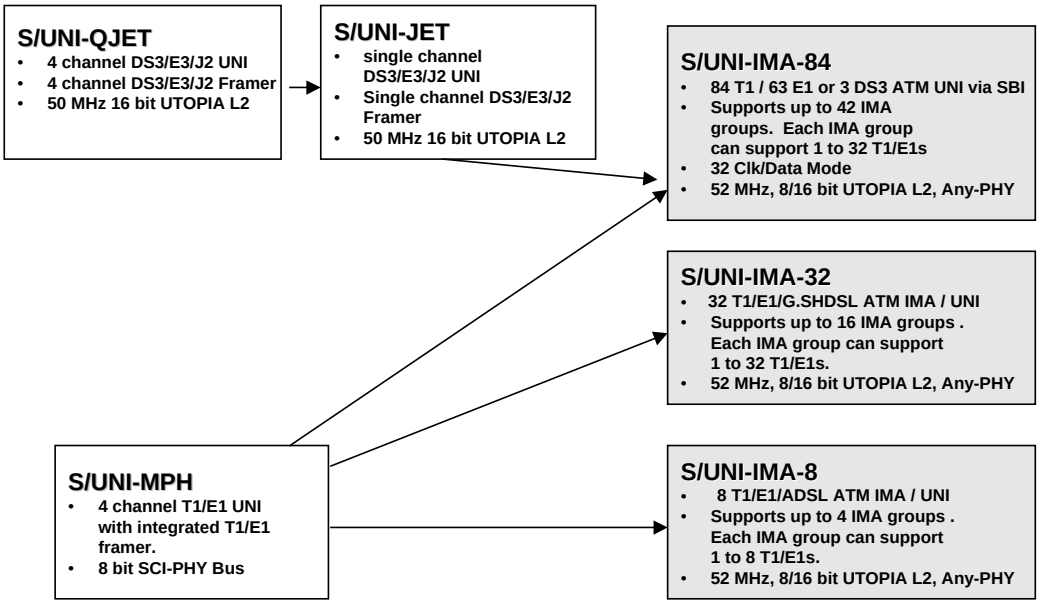

Figure 5. S/UNI-IMA Extends and Integrates Functionality.

3.1 S/UNI-IMA-84

The S/UNI-IMA-84 implements the IMA 1.1 protocol with backward compatibility to IMA 1.0 and the Transmission Convergence (TC) layer function. The S/UNI-IMA-84 has two lineside interface modes that determine the total number of links supported: the SBI bus interface mode and the Clock and Data interface mode. In SBI mode, the S/UNI-IMA-84 supports up to 84 T1, 63 E1 or 3 DS3 (Transmission Convergence (TC) only for DS3) links where each T1 or E1 link is dynamically configurable to support either IMA 1.1, backward compatible IMA 1.0 or ATM over T1/E1. In SBI mode, the S/UNI-IMA-84 mates seamlessly to the PM8316 TEMUX-84 and PM8315 TEMUX devices.

In the Clock and Data interface mode, the S/UNI-IMA-84 supports 32 independent T1, E1, G.SHDSL or unchannelized links. All links are dynamically configurable to support either IMA 1.1, backward compatible IMA 1.0, ATM over

T1/E1, ATM over fractional T1/E1 or ATM HEC cell delineation for G.SHDSL or unchannelized links. Up to 84 fractional T1/E1 streams can be supported across the 32 T1/E1 links of the device. In Clock/Data mode the S/UNI-IMA-84 mates seamlessly to eight PM4354 COMET-QUAD 4-port T1/E1 framer and LIUs or other standard framers.

3.2 S/UNI-IMA-32

The S/UNI-IMA-32 is pin-compatible and software-compatible to the S/UNI-IMA-84 and provides a Clock and Data interface only – SBI is not supported. The S/UNI-IMA-32 supports 32 independent T1, E1, G.SHDSL or unchannelized links. All links are dynamically configurable to support either IMA 1.1, backward compatible IMA 1.0, ATM over T1/E1, ATM over fractional T1/E1 or ATM HEC cell delineation for G.SHDSL or unchannelized links. On individual T1/E1 links, multiple ATM over fractional T1/E1 streams can be supported. The S/UNI-IMA-32 mates seamlessly to eight PM4354 COMET-QUAD 4-port T1/E1 framer and LIUs or other standard framers.

3.3 S/UNI-IMA-8

The S/UNI-IMA-8 is software-compatible to the S/UNI-IMA-84 and S/UNI-IMA-32 devices and provides a Clock and Data interface only – SBI is not supported. The S/UNI-IMA-8 supports 8 independent T1, E1, G.SHDSL or unchannelized links. All links are dynamically configurable to support either IMA 1.1, backward compatible IMA 1.0, ATM over T1/E1, ATM over fractional T1/E1 or ATM HEC cell delineation for G.SHDSL, ADSL or unchannelized links. On individual T1/E1 links, multiple ATM over fractional T1/E1 streams can be supported. The S/UNI-IMA-8 mates seamlessly to two PM4354 COMET-QUAD 4-port T1/E1 framer and LIUs or other standard framers.

3.4 S/UNI-IMA Product Family Comparison

Table 1 summarizes the differences between the S/UNI-IMA devices.

	S/UNI-IMA-84	S/UNI-IMA-32	S/UNI-IMA-8
Physical Links, SBI Mode	84 T1, 63 E1 or 3 DS3	Not Supported	Not Supported
Physical Links, Clock / Data Mode	32 T1/E1/Fractional T1/E1, G.SHDSL, unchannelized	32 T1/E1/Fractional T1/E1, G.SHDSL, unchannelized	8 T1/E1/Fractional T1/E1, ADSL, unchannelized
IMA Groups	42	16	4
IMA 1.1 and 1.0 Support	Yes	Yes	Yes
System Interface	52 MHz 8/16 bit UTOPIA L2 with Parity, Any-PHY	52 MHz 8/16 bit UTOPIA L2 with Parity, Any-PHY	52 MHz 8/16 bit UTOPIA L2 with Parity, Any-PHY
UNI / IMA Support	84 T1 (UNI/IMA), 63 E1 (UNI/IMA) or 3 DS3 UNI over SBI	32 T1/E1/G.SHDSL/ Unchannelized (UNI/IMA) Fractional T1/E1 (UNI)	8 T1/E1/ADSL/ Unchannelized (UNI/IMA) Fractional T1/E1 (UNI)
External Memory	16 bit wide SDRAM, 1Mbit x 16 or 4Mbit x 16	16 bit wide SDRAM, 1Mbit x 16	16 bit wide SDRAM, 1Mbit x 16
Package	416 PBGA (27mm x 27mm)	416 PBGA (27mm x 27mm)	324 PBGA (23 mm x 23 mm)
Max Power	~1.37 W	~1.2 W	~1.09 W
Maximum Differential Delay	279 ms (T1), 226 ms (E1)	279 ms (T1), 226 ms (E1)	279 ms (T1), 226 ms (E1)
Power	1.8V Core, 3.3V I/O	1.8V Core, 3.3V I/O	1.8V Core, 3.3V I/O
Fractional T1/E1	Yes, via Clk/Data	Yes	Yes
Link and Group State Machines	Internal	Internal	Internal

Table 1. S/UNI-IMA Product Family Comparison.

4 SYSTEM APPLICATIONS

4.1 Any Service Any Port Linecards

With the S/UNI-IMA-84 and its support for the SBI™ bus, high density Any Service Any Port linecards can be easily designed with PMC-Sierra's SPECTRA™, TEMUX™, AAL1gator™, MECA™, FREEDM™, S/UNI -APEX™ and S/UNI -ATLAS™ products. The design shown in Figure 3 supports a broad spectrum of existing and emerging services including Frame Relay (FR), Internet Protocol (IP), Dedicated Private Line, Integrated Voice and Data, Voice-over- IP and Voice-over-ATM.

The S/UNI-IMA-84 implements the IMA 1.1 protocol (with backward compatibility to IMA 1.0) including link and group state machines, HEC cell delineation (UNI), cell scheduling and provides internal cell FIFOs. The S/UNI-IMA-84 interfaces seamlessly over a standard UTOPIA Level 2 or Any-PHY bus to an ATM Traffic Management device such as the PM7326 S/UNI-APEX. Depending on the S/UNI-IMA-84's register configuration, ATM traffic is sent over the network as part of an IMA 1.1 or IMA 1.0 group or over a standard ATM over T1/E1 or DS3 UNI. Through register programming, for example, the number of links, groups, minimum and maximum number of links/group, frame sizes (M=32, 64, 128, 256), differential delay tolerance, transmit clock mode (independent and common) and symmetrical/asymmetrical configuration and operation are dynamically configurable. An external low-cost standard 4Mx16 SDRAM is required to buffer data for tolerating up to a maximum of 279 msec (T1) / 226 msec (E1) of differential delay across the links.

With the dramatic reduction in board space and power, the optimized S/UNI-IMA-84 / TEMUX-84 solution enables a new generation of OC-3, OC-12 and OC-48 IMA / UNI and Any Service Any Port linecards.

4.2 ATM Multi-Service Switch IMA and UNI Linecards

Figure 6 and Figure 7 illustrate examples of channelized OC-3 and channelized OC-12 ATM IMA / UNI linecard applications.

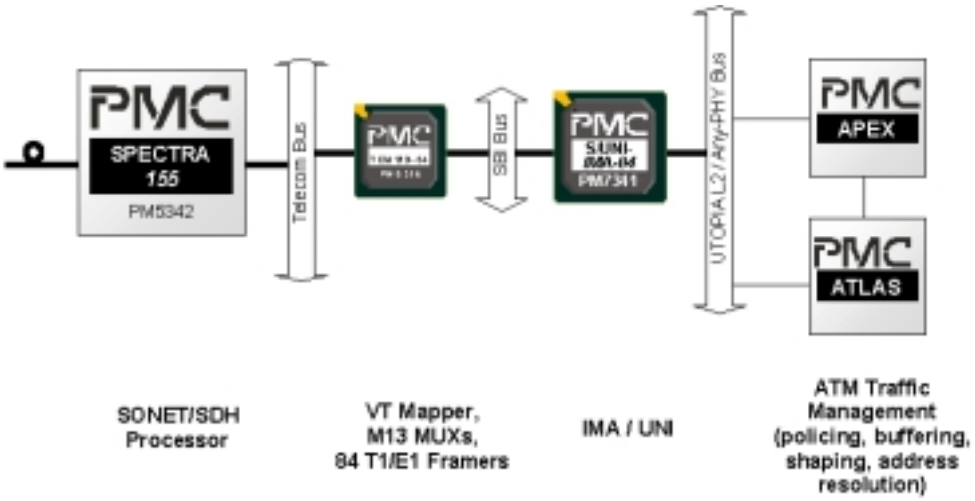

Figure 6. ATM Multi-Service Switch OC-3 IMA and UNI Linecard.

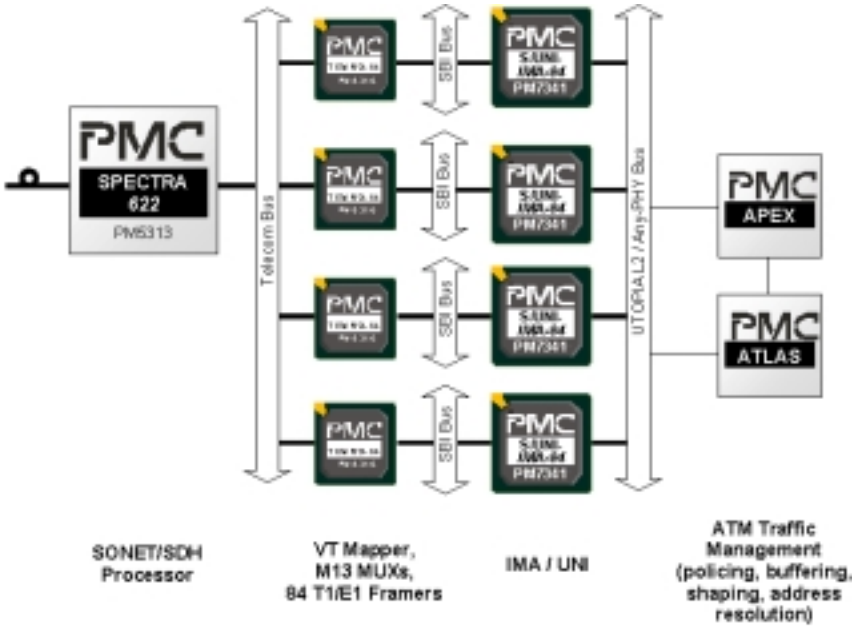

Figure 7. ATM Multi-Service Switch OC-12 IMA and UNI Linecard.

The PM5342 SPECTRA-155 and PM5313 SPECTRA-622 provide SONET/SDH overhead processing and interface seamlessly via the Telecom Bus to the PM8316 TEMUX-84. Each TEMUX-84 provides 84 T1 or 63 E1 framers, a VT/TU Mapper and three M13 Multiplexers. The TEMUX-84s interfaces seamlessly to S/UNI-IMA-84s over the SBI bus.

4.3 3G Wireless and IMA over DSL

The S/UNI-IMA-32 supports 32 T1/E1/G.SHDSL links providing IMA, ATM over T1/E1, ATM over fractional T1/E1 and ATM over xDSL functionality ideal for 3G Wireless and IMA over xDSL applications as shown in Figure 8.

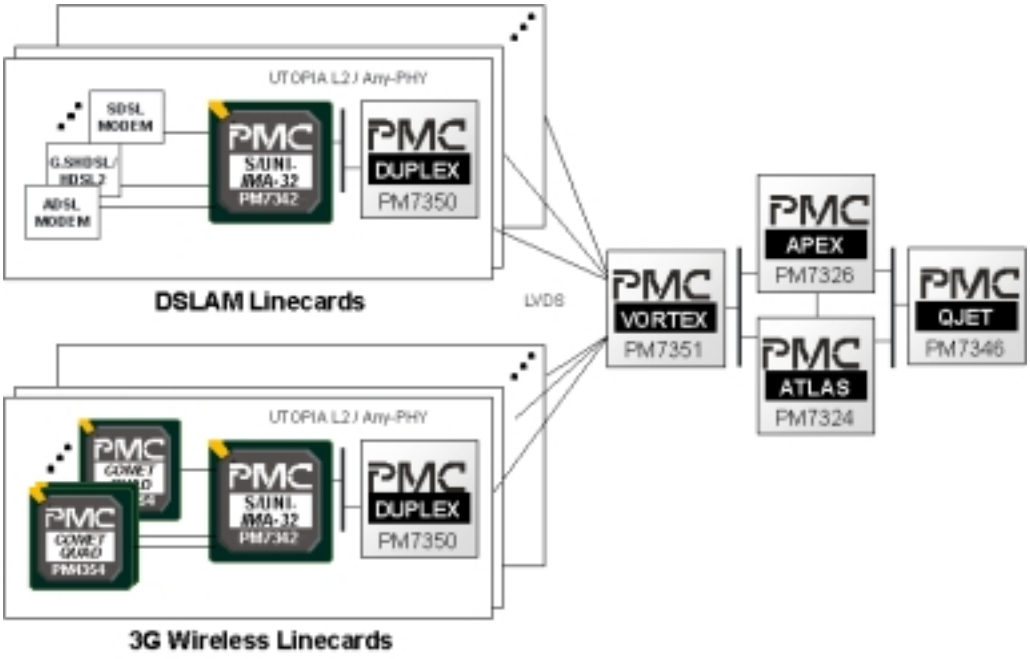

Figure 8. S/UNI-IMA-32 in 3G Wireless and IMA over xDSL Applications.

The design shown in Figure 8 is built upon the Vortex Chipset which comprises the PM7351 S/UNI-VORTEX, PM7350 S/UNI-DUPLEX (not shown), PM7326 S/UNI-APEX and PM7324 S/UNI-ATLAS devices. Each S/UNI-VORTEX aggregates traffic from up to eight S/UNI-DUPLEXs which, in turn, aggregate traffic from multiple DSL MODEMs and/or COMET-QUAD Framer plus LIUs. The S/UNI-APEX is an ATM/Packet Traffic Manager and Switch device which aggregates, shapes and switches traffic from multiple S/UNI-VORTEXs. The S/UNI-ATLAS performs OAM, policing and address translation functions (see document PMC-1990712, “VORTEX Chip Set Introduction for details).

The S/UNI-IMA-8 mates seamlessly to the Vortex Chipset over a standard UTOPIA Level 2 / Any-PHY bus and the COMET-QUAD over a clock and data interface.

4.4 Multi-Service Access – IADs, Access Concentrators

Multi-Service access equipment such as Integrated Access Devices (IADs) and Access Concentrators consolidate voice, data, Internet, and video wide-area network services over ATM unifying the functions of many different types of equipment including CSUs, DSUs, multiplexers and FRADs. Figure 9 illustrates an example of a multi-service access box using IMA over multiple T1/E1 lines for WAN access.

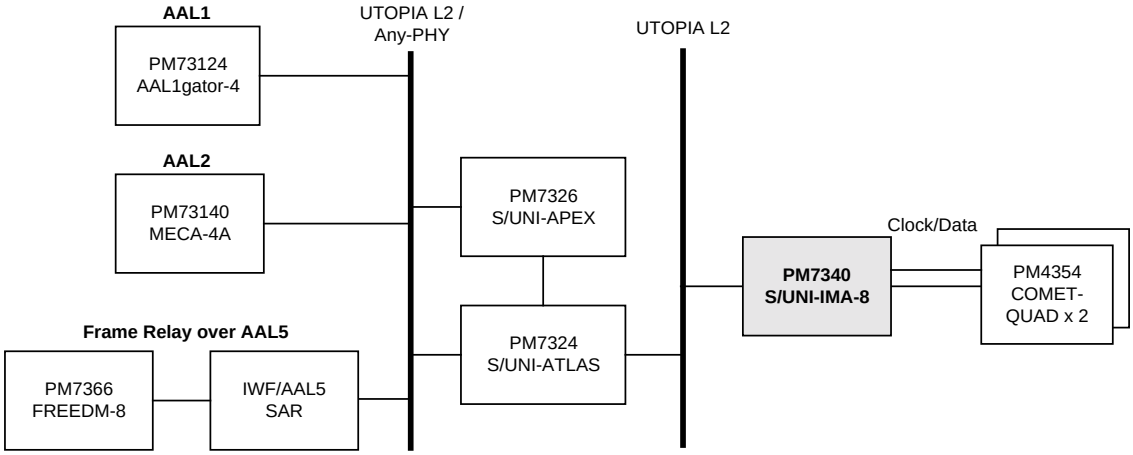

Figure 9. Multi-Service Access – IADs and Access Concentrators.

On the lineside, the S/UNI-IMA-8 interfaces seamlessly to standard devices such as the PM4354 COMET-QUAD T1/E1 Framer plus LIU.

4.5 Remote DSLAM WAN Uplink

IMA is ideally suited for remote DSLAM applications for several reasons. Firstly, remote DSLAMs are physically located at remote sites of which many are served by T1 or E1 lines. Secondly, the benefits of ATM have resulted in its almost exclusive use in DSLAMs. Coupled with ATM, DSLAMs enable service providers to utilize the bandwidth of the T1/E1 infrastructure for delivering integrated services such as high-speed Internet access and real-time voice and video. ATM over T1/E1 is a suitable DSLAM WAN uplink technology and IMA, due to its benefits of higher bandwidth, statistical gain and fault tolerance, is even more suitable.

Figure 10 illustrates an example of the S/UNI-IMA-8 in a remote DSLAM WAN uplink application.

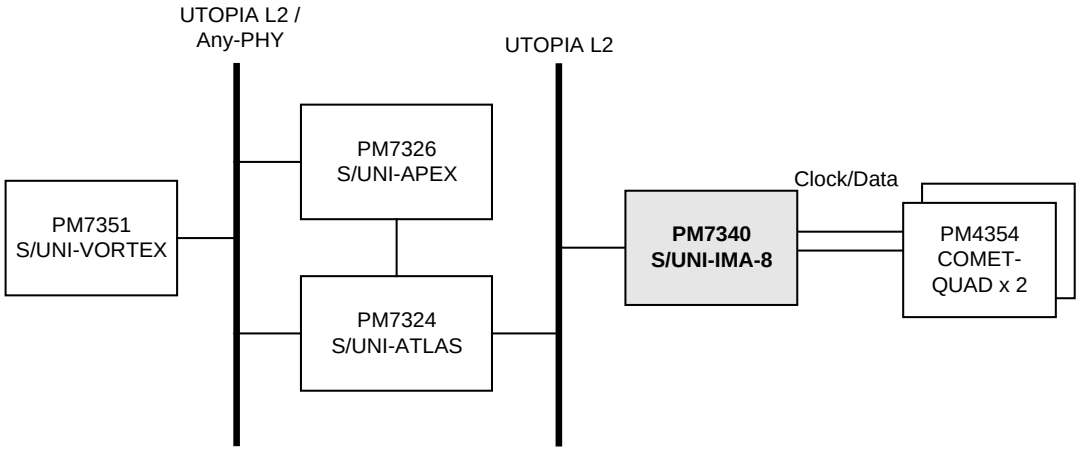

Figure 10. S/UNI-IMA-8 in a Remote DSLAM WAN Uplink Application.

5 SOFTWARE DRIVER

The S/UNI-IMA software device driver, compatible across the entire S/UNI-IMA family of devices: the S/UNI-IMA-84, S/UNI-IMA-32 and S/UNI-IMA-8, is written in ANSI C and runs on an external processor that communicates to the S/UNI-IMA device through its standard microprocessor interface.

5.1 Features

The device driver provides fault management, configuration management and statistics collection functions through a well-defined Application Programming Interface (API). To facilitate porting to any Real Time Operating System (RTOS) and any processor, software wrappers are used for all RTOS-related functions.

The driver API, common to all S/UNI-IMA devices, comprises high-level functions that can be invoked by application software to configure, control and monitor S/UNI-IMA devices. The API includes functions that:

- Initialize the device(s)
- Perform diagnostic tests
- Validate configuration information
- Retrieve status and statistics information

Low level utility functions are also provided for diagnostics and debugging purposes.

5.2 Free Source Code

The software device driver source code is available free of charge and will be distributed via the PMC website, www.pmc-sierra.com. See Section 7 for availability information.

5.3 Royalty Free

The software device driver is completely free of any royalties. Although the software is extensively tested, it is provided on an “as-is” basis and is intended to serve as a reference.

6 REFERENCE DESIGNS

6.1 S/UNI-IMA-84

A hardware reference design of an OC-3 IMA CompactPCI card complete with schematics and bill of material is available for the S/UNI-IMA-84. The design details the interconnection between the SPECTRA-155, TEMUX-84, S/UNI-IMA-84 and S/UNI-DUPLEX. A block diagram of the development kit is shown in Figure 11.

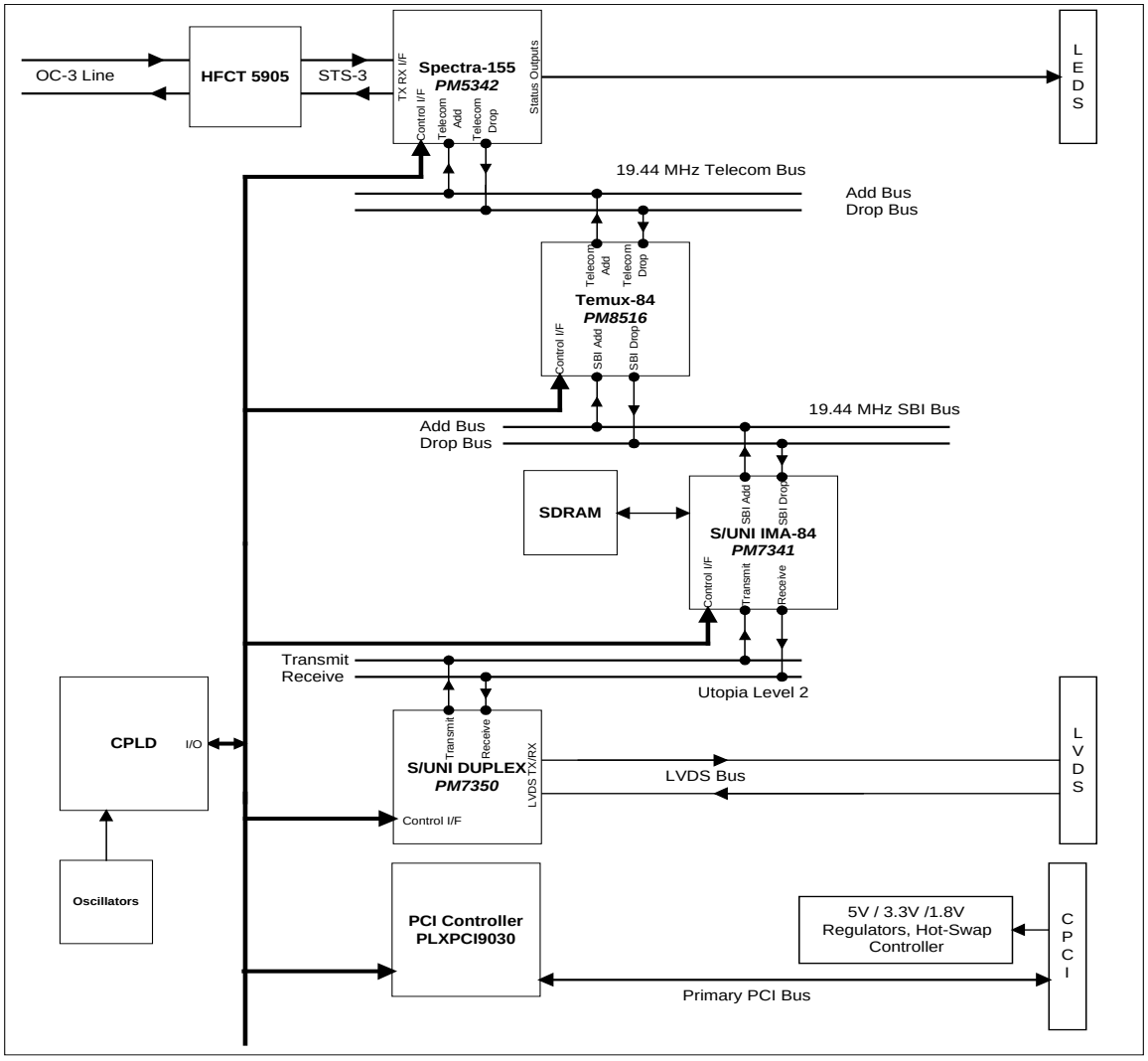

Figure 11. S/UNI-IMA-84 Reference Design Block Diagram.

6.2 S/UNI-IMA-8

A hardware reference design of an eight link IMA CompactPCI card is also available for the S/UNI-IMA-8. The design details the interconnection between the S/UNI-IMA-8, COMET-QUAD and S/UNI-DUPLEX. A block diagram of the development kit is shown in Figure 12.

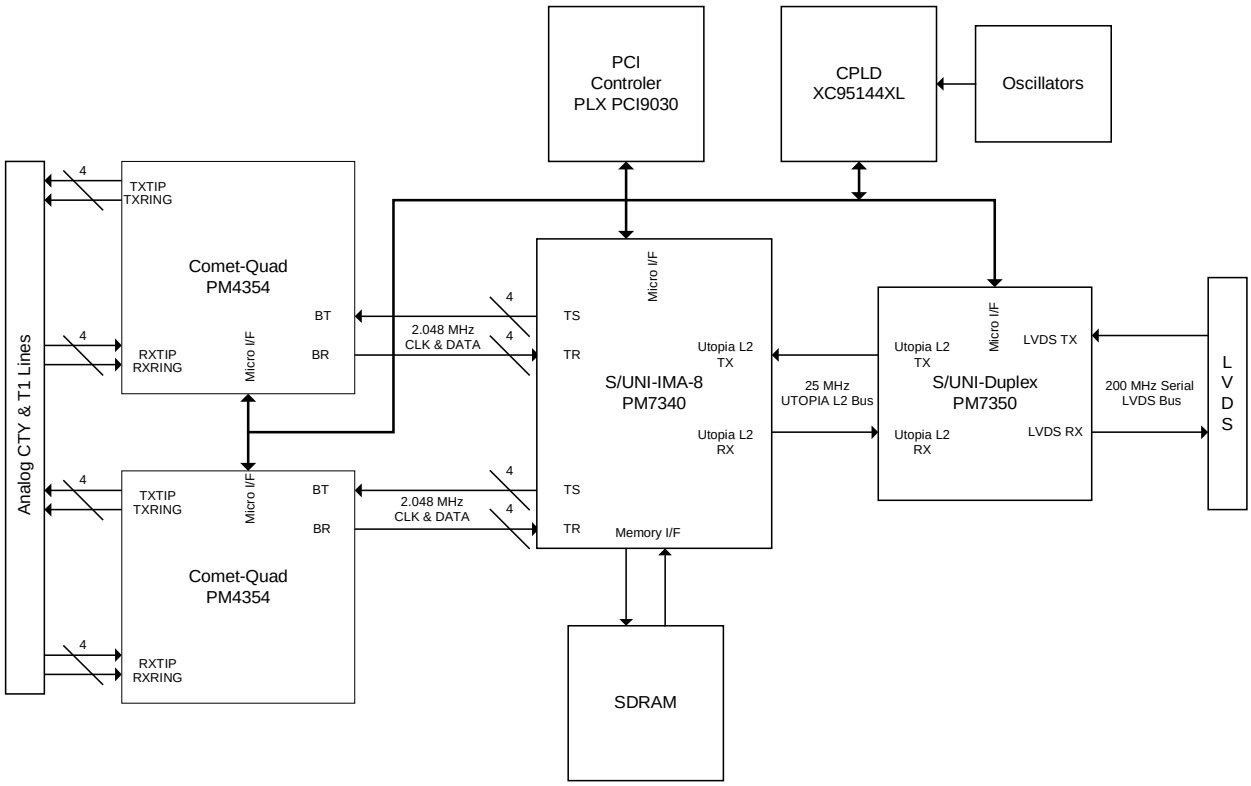

Figure 12. S/UNI-IMA-8 Reference Design Block Diagram.

7 REFERENCE MATERIAL

Table 2 summarizes the S/UNI-IMA reference material. For availability please visit the PMC website, www.pmc-sierra.com.

Reference Material	Document #
S/UNI-IMA Product Family Technical Overview	PMC-2000167
S/UNI-IMA-84	
Longform Datasheet	PMC-2000223
Shortform Datasheet	PMC-2001522
VHDL Model	
BSDL Model	
IBIS Model	
Reference Design Document	PMC-2002050
S/UNI-IMA-32	
Longform Datasheet	PMC-2001724
Shortform Datasheet	PMC-2001523
VHDL Model	
BSDL Model	
IBIS Model	
S/UNI-IMA-8	
Longform Datasheet	PMC-2001723
Shortform Datasheet	PMC-2001521
VHDL Model	
BSDL Model	
IBIS Model	
Reference Design Document	PMC-2002117
Software	
S/UNI-IMA Programmers Guide	PMC-2010279
S/UNI-IMA Software Drivers, Beta	
S/UNI-IMA Software Driver Manual, Alpha Rel.	PMC-2010086

Table 2. S/UNI-IMA Reference Material.

8 GLOSSARY

DS0	Digital Service, level 0: There are 24 DS0 channels in a DS1. Each DS0 channel has a bandwidth of 64 Kbps full duplex.
DS1	Digital Service, level 1.
DSL	Digital Subscriber Line
DSLAM	DSL Access Multiplexer
E1	E1 carries information at the transmission rate of 2 Mbps. This is the rate used by European CEPT carriers to transmit 30, 64 Kbps digital channels for voice or data calls, plus a 64 Kbps channel for signaling and a 64 Kbps channel for framing.
HEC	Header Error Check
IAD	Integrated Access Device
IMA	Inverse Multiplexing over ATM
OC-12	Optical Carrier 12. SONET channel of 622.08 Mbps.
OC-3	Optical Carrier 3. A SONET channel that has a bandwidth of 155.52 Mbps
PHY	Physical layer device.
RTOS	Real Time Operating System
SBI	Scaleable Bandwidth Interconnect: A synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links.
SDH	Synchronous Digital Hierarchy: A set of standard fiber-optic transmission standards used outside North America.
SONET	Synchronous Optical NETwork: A family of fiber optic transmission standards used in North America.
S/UNI	SATURN User-Network-Interface
T1	Trunk Level 1: A digital transmission link with a total signaling speed of 1.544 Mbps.
TC	Transmission Convergence
UTOPIA	Universal Test and Operations Interface: Refers to an electrical interface between the TC and PMD sublayers of the physical layer. UTOPIA is the interface for devices connecting to an ATM network.
VT	Virtual Tributary: A structure designed for transport and switching of sub-DS3 payloads. A unit of sub-SONET bandwidth that can be combined or concatenated, for transmission through the network. VT1.5 is equivalent to 1.544 Mbps and VT2 equals 2.048 Mbps

WAN	Wide Area Network: A data network that is used to interconnect remote LANs or users over leased lines, packet or cell switch services

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