

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

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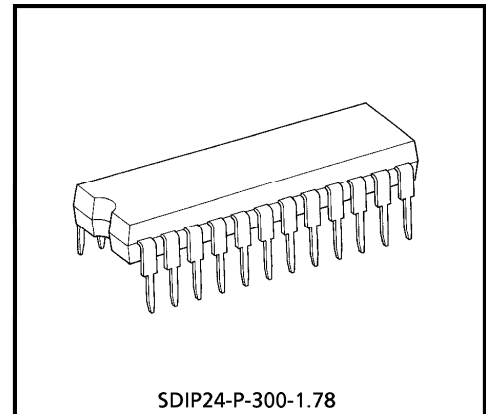
16BIT SHIFT REGISTER, LATCH & CONSTANT CURRENT DRIVERS

The TB62701AN is specifically designed for LED and LED-DISPLAY constant current drivers.

This constant current output circuit is able to set up external resistor ($I_{OUT} = 5$ to 50mA).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 16bit Shift Register, Latch, AND-GATE and Constant Current Driver.



Weight : 1.2g (Typ.)

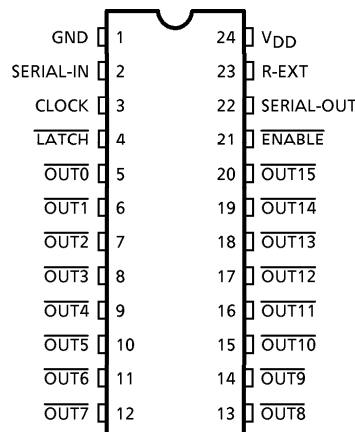
FEATURES

- OUTPUT CURRENT : Set-up at 50mA maximum with an external resistor.
- A LITTLE CHANGE OF OUTPUT CURRENT ($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$)

OUT-GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	I_{OUT} [mA]
$\geq 0.4\text{V}$	$\pm 7\%$	5~50mA
$\geq 0.7\text{V}$		

- 5V CMOS Compatible Input
- PACKAGE : SDIP-24 (SDIP24-P-300)
- MAXIMUM CLOCK FREQUENCY : $f_{MAX} = 2.5\text{MHz}$ (cascade operation, $T_a = 25^\circ\text{C}$)

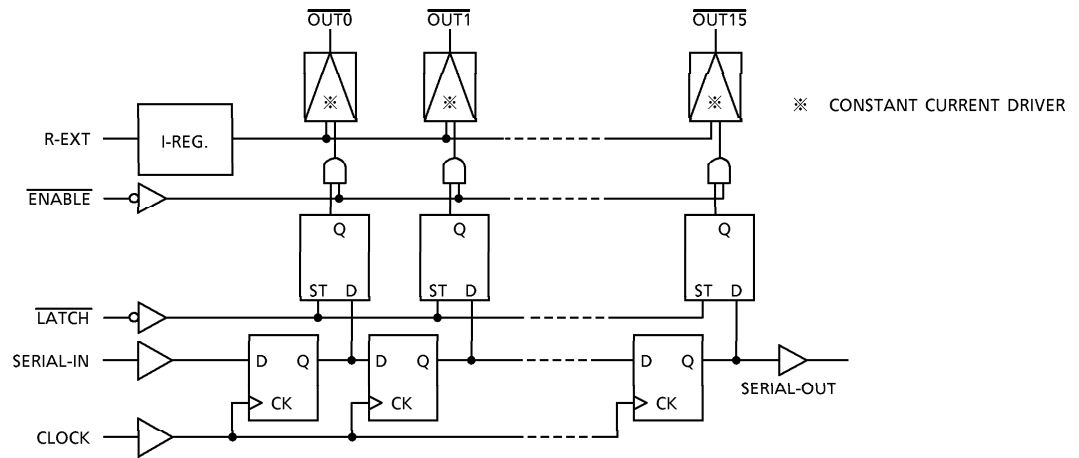
PIN CONNECTION (TOP VIEW)



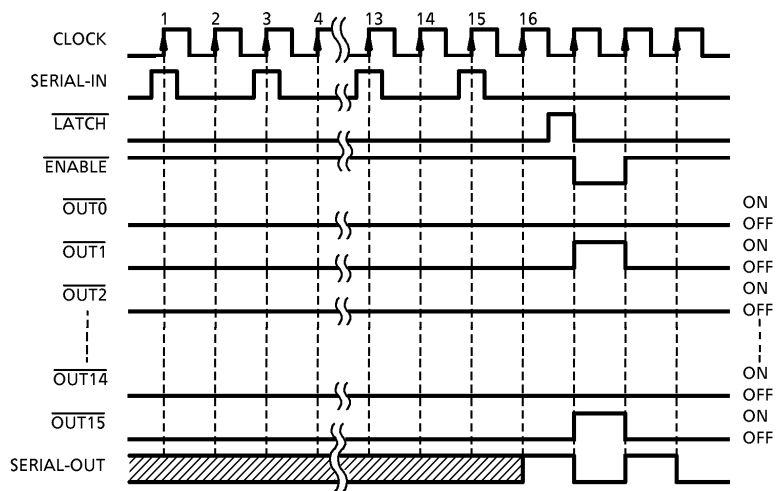
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BLOCK DIAGRAM



TIMING DIAGRAM



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TERMINAL DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL-IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up-edge
4	LATCH	"H" Level : data through, "L" Level : data hold
24	V _{DD}	Supply voltage terminal
5~12 13~20	OUT _n	Output terminals
21	ENABLE	"H" Level output off, "L" Level : latch data = "H" Level then output on, latch data = "L" Level then output off
22	SERIAL-OUT	Serial data output terminal for shift register
23	R-EXT	The register which connects between R-EXT and GND sets the constant output current.

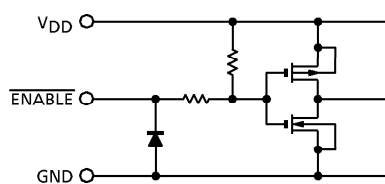
TRUTH TABLE

INPUT				OUTPUT $\overline{OUT}_n (t = n)$			
CLOCK	LATCH	ENABLE	SERIAL-IN	OUT ₀ ... OUT ₇ ... OUT ₁₅	SERIAL-OUT		
	H	L	D _n	D _n	D _{n-7}	D _{n-15}	D _{n-15}
	L	L	D _n	No change			D _{n-15}
	※	H	D _n	OFF	OFF	OFF	D _{n-15}
	※	※	D _n	No change			No change

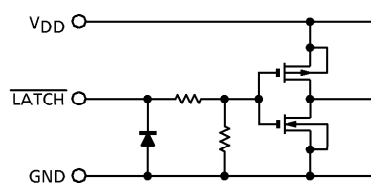
(Note) D_n~D_{n-15} = "H" then OUT_n is ON, "L" then OUT_n is OFF.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

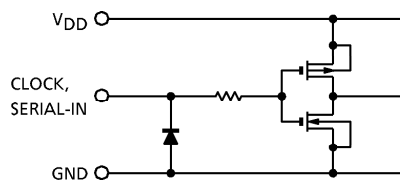
1. ENABLE terminal



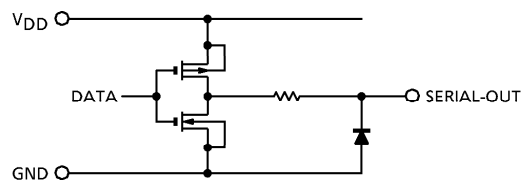
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	0~7.0	V
Output Voltage	V _{CE}	-0.5~30	V
Output Current	I _{OUT}	50	mA
Input Voltage	V _{IN}	-0.4~V _{DD} +0.4	V
GND Terminal Current	I _{GND}	800	mA
Clock Frequency	f _{CK}	2.5	MHz
Power Dissipation	P _D	1.78	W
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 14.2mW/°C.

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V	
Output Voltage	V _{OUT}	—	—	—	30.0	—	
Output Current	$\overline{\text{OUTn}}$	I _{OUT}	DC 1 circuit	—	—	45	mA
	S-OUT	I _{OH}	—	—	—	-1.0	
		I _{OL}	—	—	—	1.0	
Input Voltage	V _{IN}	—	0	—	V _{DD}	V	
Data Set Up Time	t _{setup} (D)	—	100	—	—	ns	
Data Hold Time	t _{hold} (D)	—	20	—	—	ns	
Latch Set Up Time	t _{setup} (L)	—	300	—	—	ns	
Latch Hold Time	t _{hold} (L)	—	100	—	—	ns	
Clock Pulse Width	t _w CLK	—	100	—	—	ns	
	t _w $\overline{\text{CLK}}$	—	100	—	—		
Latch Pulse Width	t _w LAT	—	300	—	—	ns	
	t _w $\overline{\text{LAT}}$	—	300	—	—		
Clock Frequency	f _{CK}	Cascade operation	—	—	2.0	MHz	
Power Dissipation	P _D	Ta = 85°C	—	—	0.72	W	

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0V$, $T_a = 25^\circ C$ unless otherwise noted)

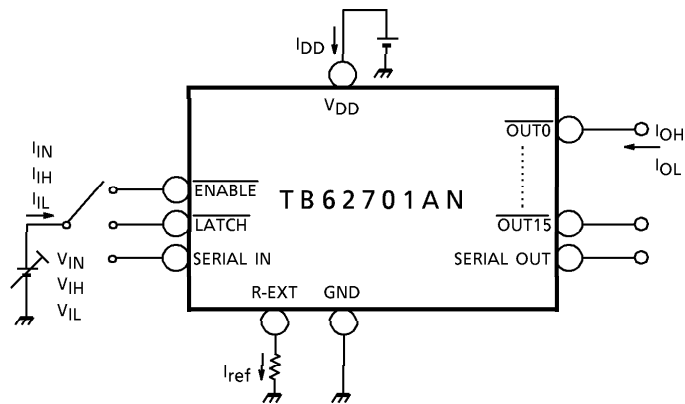
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V_{IH}	—	—	$70\%V_{DD}$	—	V_{DD}	V
	"L" level	V_{IL}	—	—	GND	—	$30\%V_{DD}$	
Output Leakage Current		I_{OH}	—	$V_{OH} = 30V$	—	—	10	μA
Output Voltage	S-OUT	V_{OL}	—	$I_{OL} = +1.0mA$	—	—	0.4	V
		V_{OH}	—	$I_{OH} = -1.0mA$	4.6	—	—	
Output Current 1		I_{OL1}	—	$V_{CE} = 0.7V$ $R_{EXT} = 560\Omega$	35.2	41.5	47.7	mA
		I_{OL2}	—	$V_{CE} = 0.4V$ (include ΔI_{OL1})	33.1	39.0	44.9	
Delta I_{OUT}		ΔI_{OL1}	—	$R_{EXT} = 560\Omega$ $I_{OUT} = 40mA, V_{CE} = 0.4V$	—	± 3.0	± 7.0	%
Supply Voltage Regulation		$\% / V_{DD}$	—	$R_{EXT} = 560\Omega$	—	18	—	$\% / V$
Reference Voltage		V_{ref}	—	$R_{EXT} = 560\Omega, T_a = -40\sim 85^\circ C$	—	1.26	—	V
Pull Up / Down Resister		R_{IN}	—	—	100	200	400	$k\Omega$
Supply Current	"OFF"	$I_{DD} (off) 1$	—	$R_{EXT} = OPEN, OUTn = Off$	—	0.4	0.6	mA
		$I_{DD} (off) 2$	—	$R_{EXT} = 560\Omega, OUTn = Off$	—	6.5	10.0	
	"ON"	$I_{DD} (on)$	—	$R_{EXT} = 560\Omega, OUTn = Off$	—	13.5	20.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

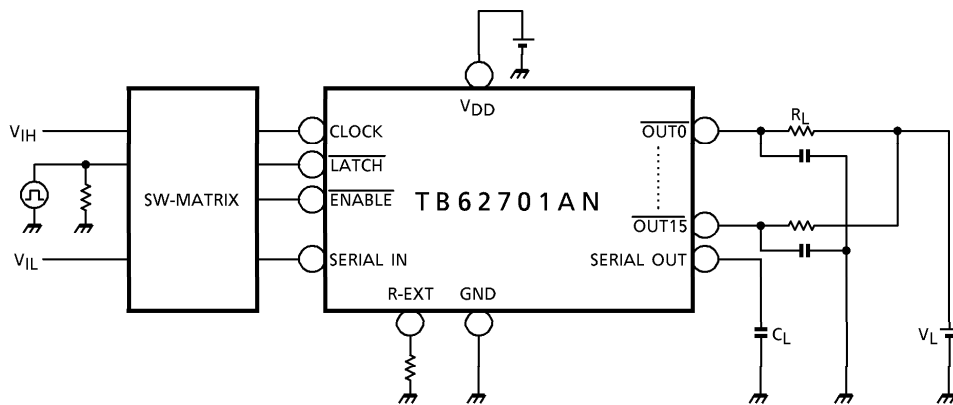
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT				
Propagation Delay Time ("L" to "H")	CK-S-OUT	t_{pLH}	$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	—	95	500	ns				
	CK-OUTn			—	130	500					
	LATCH-OUTn			—	130	500					
	EN-OUTn			—	130	500					
Propagation Delay Time ("H" to "L")	CK-S-OUT	t_{pHL}		$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	—	95	720	ns			
	CK-OUTn				—	130	500				
	LATCH-OUTn				—	130	500				
	EN-OUTn				—	130	500				
Maximum Clock Frequency		$f_{MAX} (*1)$			$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	2.0	—	2.5	MHz		
Minimum Pulse Width	CK	$t_w CK$				—	45	80	ns		
	LATCH	$t_w LAT$				—	10	50			
Data Set Up Time		$t_{setup}(D)$				$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	—	17	50	ns	
Data Hold Time		$t_{hold}(D)$	—				-7	10			
Latch Set Up Time	LH	$t_{LATsetup}$	$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$				—	70	200	ns	
	HL						—	70	200		
Latch Hold Time	LH	$t_{LAThold}$					$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	—	-70	50	ns
	HL			—				-70	50		
Maximum Clock Rise Time		t_r		$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$				—	—	10	μs
Maximum Clock Fall Time		t_f						—	—	10	
Maximum Output Rise Time		t_{or}						$V_{DD} = 5.0V$ $V_{CE} = 1.0V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $f_{CK} = 2MHz$ $R_{EXT} = 560\Omega$ $I_{OUT} = 30mA$	—	35	80
Maximum Output Fall Time		t_{of}			—				40	80	

*1 : Cascade operation

DC CHARACTERISTIC TEST CIRCUIT

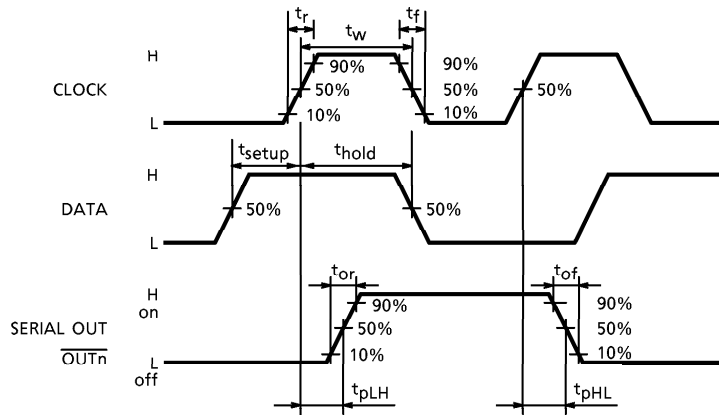


AC CHARACTERISTIC TEST CIRCUIT

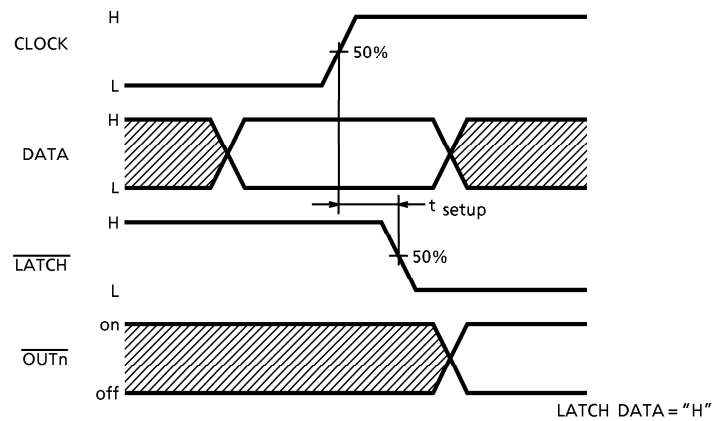


TIMING WAVE FORM

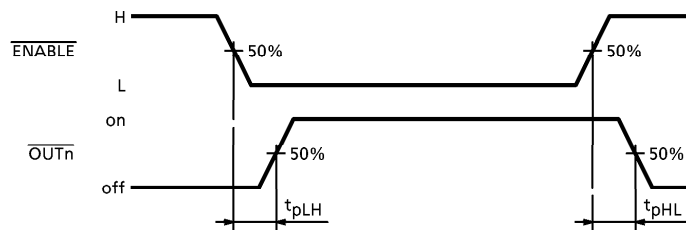
1. CLOCK-SERIAL OUT, $\overline{\text{OUTn}}$

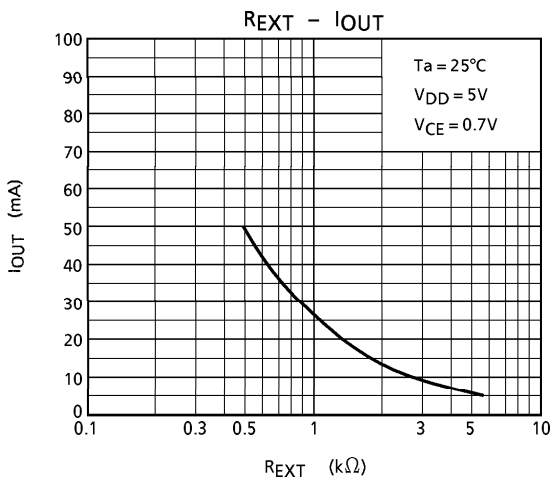
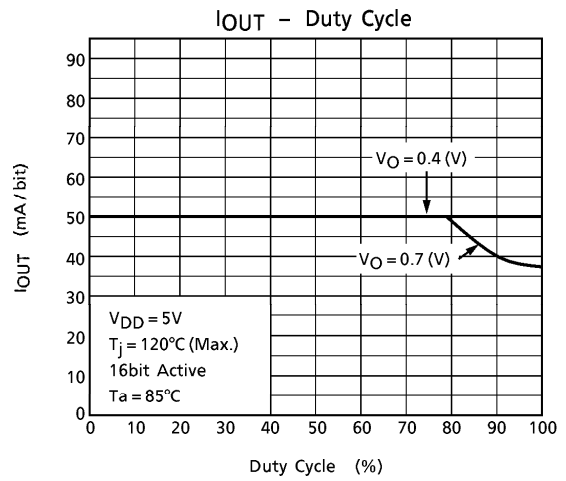
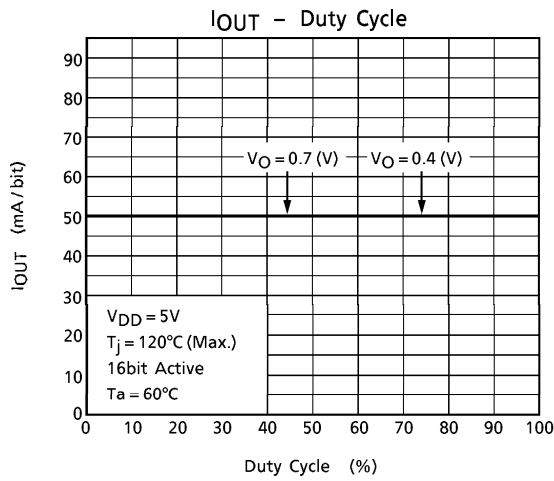
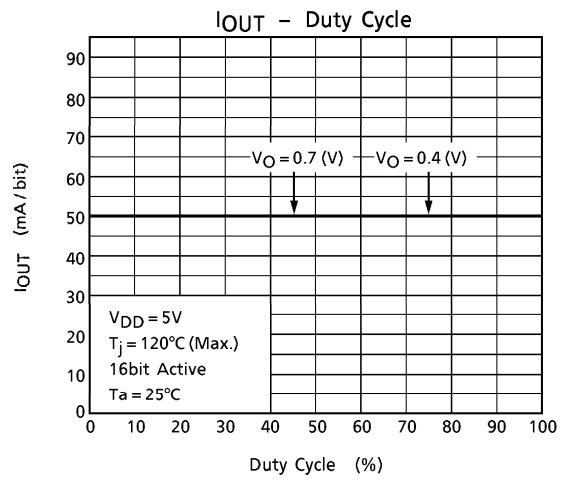
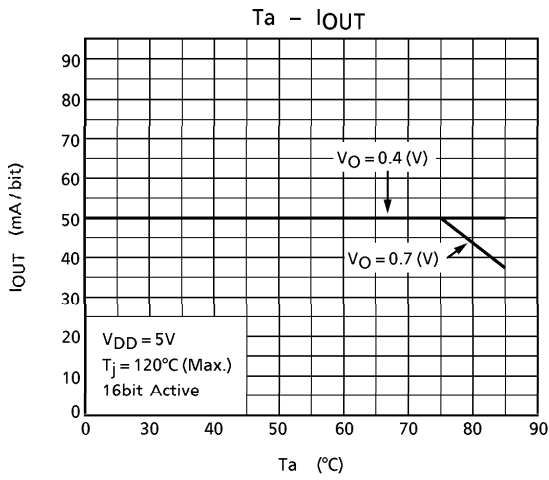


2. CLOCK-LATCH

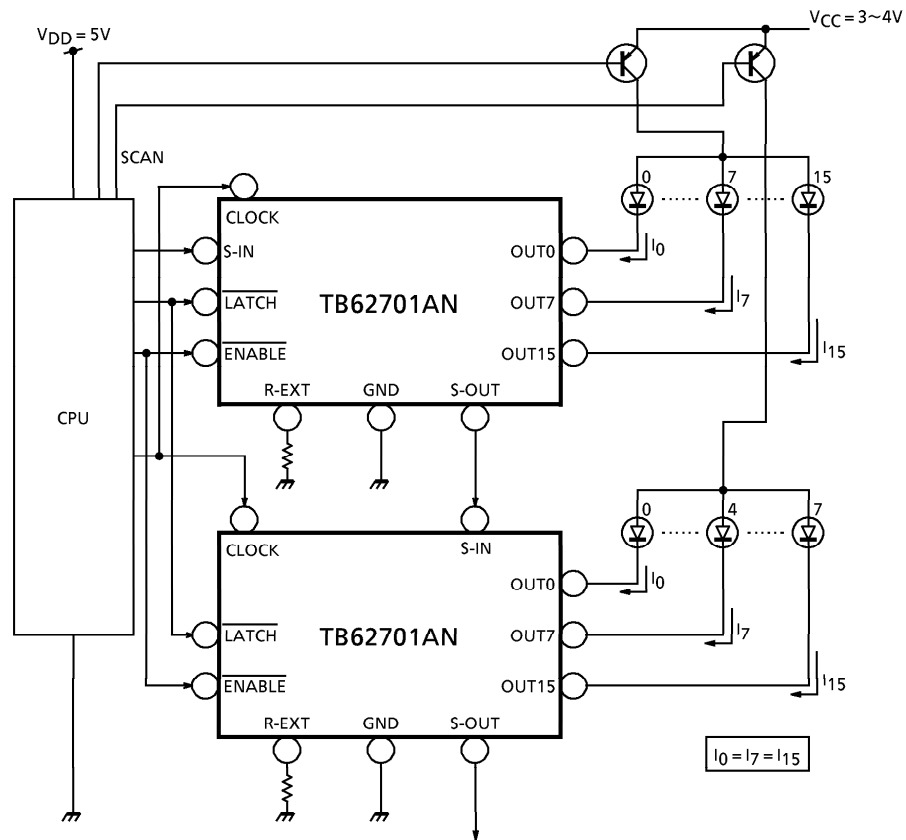


3. ENABLE





APPLICATION CIRCUIT

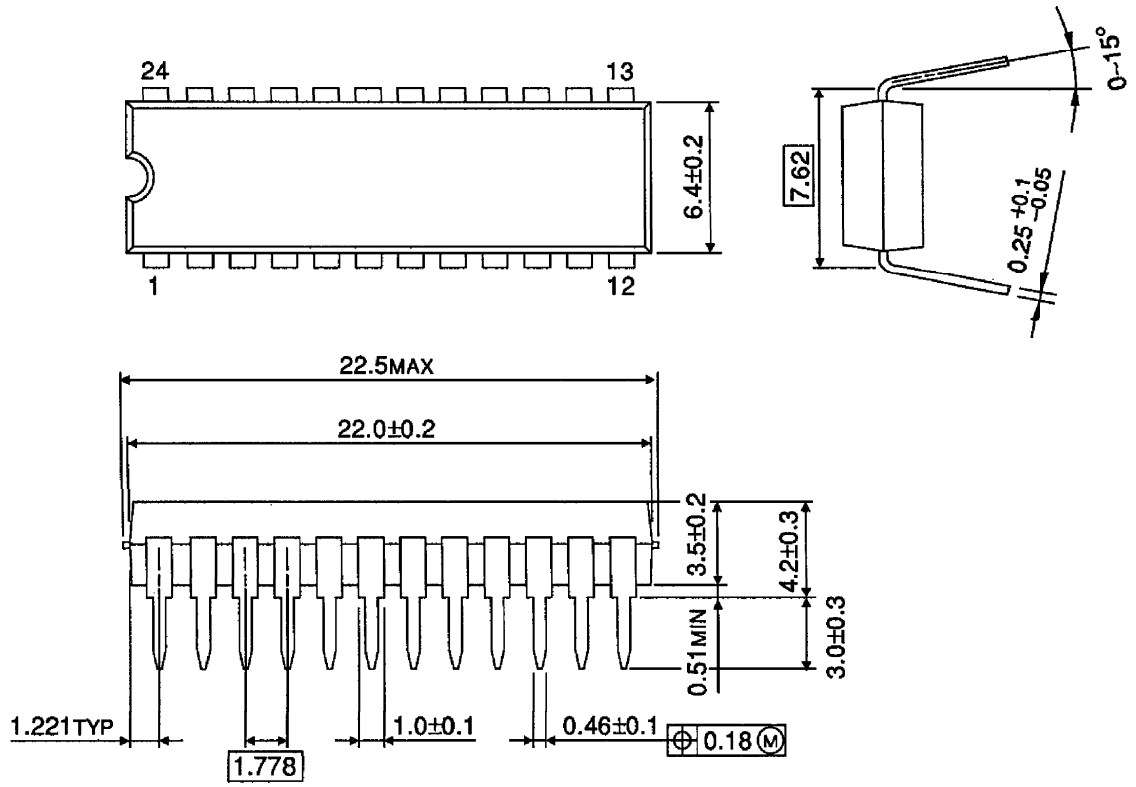


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
SDIP24-P-300-1.78

Unit : mm



Weight : 1.2g (Typ.)