MC33561

Product Preview

Power Management and Interface IC for Smartcard Readers and Couplers

The MC33561 is an integrated circuit dedicated to the Smartcard interface applications. The device handles any type of smart or memory based card through a simple and flexible microcontroller interface. On top of that, thanks to the built–in chip select pin, several couplers can be connected in parallel. The MC33561 is particularly suited for low cost, low power applications, with high extended battery life coming from extremely low quiescent current.

Features

- 100% Compatible with ISO 7816–3 Standard
- Wide Battery Supply Voltage Range: 1.8 V < V_{bat} < 6.6 V
- Programmable V_{CC} Supply to Cope with either 3 V or 5 V Card Operation
- Very Low Quiescent Current in Standby Mode: 5 μA Max
- Built–in DC/DC Converter Generates the V_{CC} Supply with Minimum External Components
- Full Control of the Power Up/Down Sequence Yields High Signal Integrity on both the Card I/O and the Signal Lines
- Programmable Card Clock Generator
- Built–in Chip Select Logic Allows Parallel Coupling Operation
- ESD Protection on Card Pins (4 kV, Human Body Model)
- Fault Monitoring Includes V_{batlow}, V_{cclow} and I_{cclim}

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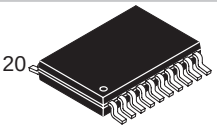
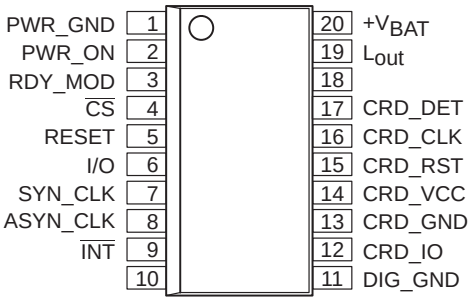


TSSOP–20
DTB SUFFIX
CASE 948E

PIN CONNECTIONS



Preliminary Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

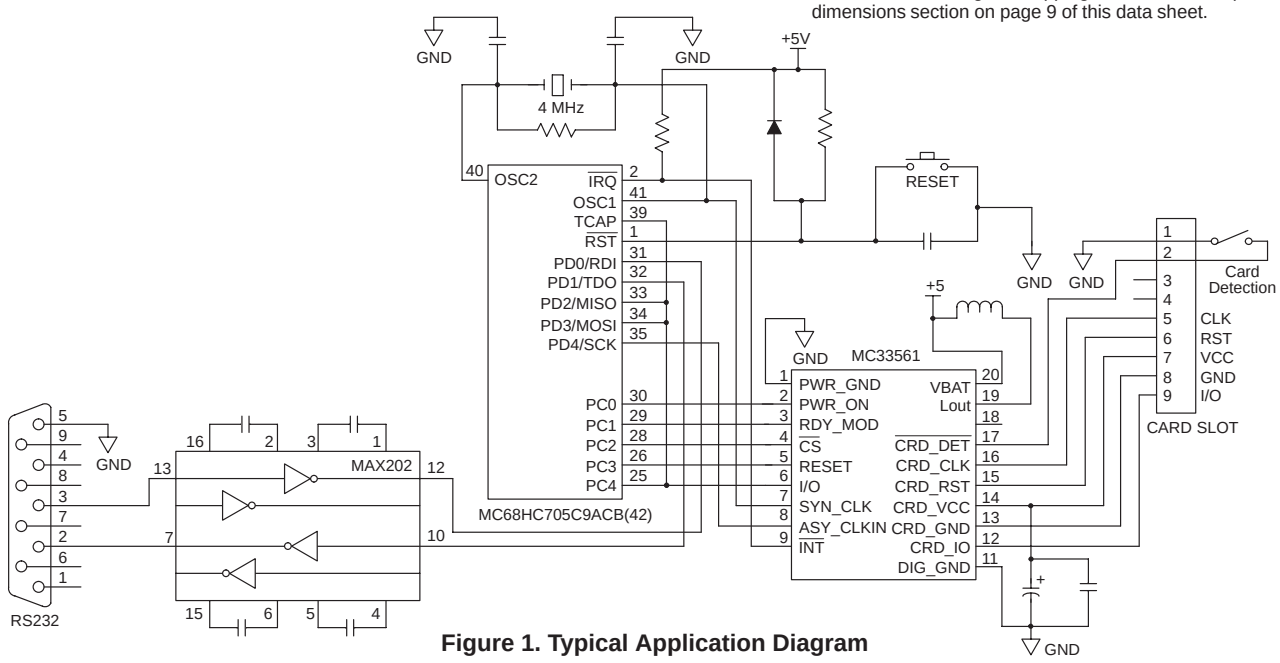


Figure 1. Typical Application Diagram

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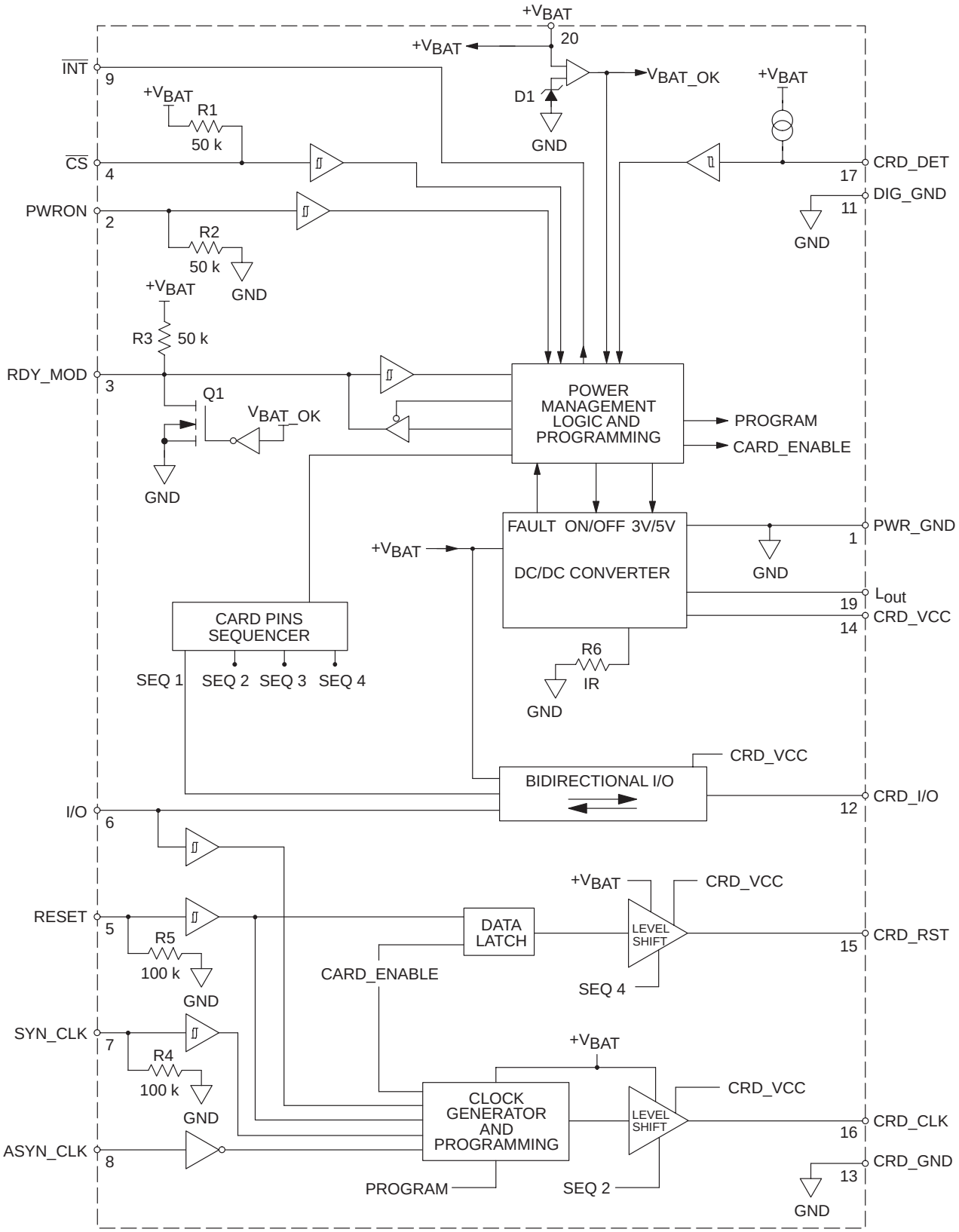


Figure 2. Detailed Block Diagram

Table 1. Pin Functions and Description

CONTROLLER INTERFACE

Pin	Symbol	Type	Name/Function
2	PWR_ON	INPUT Pull Down	This pin valid the operation of the internal DC/DC converter.
3	RDY_MOD	I/O and Pull Up	This bidirectional pin features tri–state output and schmitt trigger input. When RDY_MOD is forced to 0, the MC33xxx is set to programming mode by a negative transition on CS pin.
4	$\overline{CS}$	INPUT Pull Up	This pin provides the MC33561 chip select function. Pins x x x are disabled when CS = H. When RDY_MOD = L, the device jumps in the programming mode upon the falling edge of CS (See Figure YY).
5	RESET	INPUT Pull Down	The signal presents as this pin is translated to pin XX (card reset signal) when CS = L. The signal on this pin is latched when CS = H. This pin is also used in programming mode (See ZZZ).
6	I/O	Input/Output	This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smartcard and the microcontroller. The level translator is enabled when CS = L. The signal present on this pin is latched when CS = H. This pin is also used in programming mode (See ZZZ).
7	SYN_CLK	CLOCK INPUT Pull Down	This pin, generally connected to the controller serial interface clock, is used to set up communications with synchronous cards. The signal is fed to the internal clock selector circuit and is translated to CRD_CLK upon appropriate programming of the MC33561. When the device operates in the programming mode, the signal presents on this pin is latched when CS = H.
8	ASY_CLK_IN	CLOCK INPUT High Impedance	This pin can be connected to either the microcontroller master clock, or to any clock signal, to drive the asynchronous cards. The signal is fed to internal clock selector circuit and translated to the CRD_CLK at either the same frequency, or divided by 2 or 4, depending upon the programming mode (See AAA).
9	$\overline{INT}$	OUTPUT Pull Down	This pin is activated LOW when a card has been inserted and detected by the interface. The signal is reset to a logic 1 on the rising edge of either CS or PWR_ON. The Collector open mode makes possible the wired AND/OR external logic. When two or more interfaces share the INT function with a single micro controller, the software must polls the MC33561 to identify the origin of the interupt.

CARD INTERFACE

12	CRD_IO	I/O	This pin handles the connection to the serial I/O pin of the card connector. A bi–directional level translator adapts the serial I/O signal between the card and the micro controller.
13	CRD_GND	GROUND	This pin is connected to the external card ground. It is the ground reference for all analog and digital signals.
14	CRD_VCC	POWER	This pin provides the power to the external card. It is the logic level “1” for CRD_IO, CRD_RST and CRD_CLK signals.
15	CRD_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the RESET signal from the micro controller to the external card.
16	CRD_CLK	OUTPUT	This pin is connected to the CLK pin of the card connector. The CRD_CLK signal comes from the clock selector circuit output. The clock selection is programmed by using pins x x x with RDY_MOD forced to a logic zero.
17	$\overline{CRD\_DET}$	INPUT	The signal coming from the external card connector is used to detect the presence of the card. A built in pull up resistor makes this pin active LOW.

Pin	Symbol	Type	Name/Function
POWER SUPPLY AND GROUND			
1	PWR_GND	POWER	This pin is the current return from the external inductor L1. It is mandatory to carefully connect this pin to CRD_GND ground plane.
13	CRD_GND	POWER	This pin is the signal ground and must be connected to the ground pin of the card connector. This pin is the reference level for all analog and digital signals.
14	CRD_VCC	POWER	This pin is connected to the Vcc pin of the card connector. This pin is the logic level reference for pins xx xx xx.
19	Ext_L	POWER	This pin is connected to the external inductor used for the DC/DC converter. Please refer to the DC/DC block description.
20	Vbat	POWER	This pin is connected to the supply voltage. The MC33561 operation is inhibited when Vbat is below the minimum value.

Programming and Status Functions

The MC33561 features a programming interface and a status interface. Table 2 illustrates the programming mode.

Table 2. Programming and Status Functions Pin Out Logic

	Program CRD_VCC to 3 V/5 V	Select Vcc ON/OFF	Select Clock Input	Program ASY_CLKIN Divide Ration	Poll Card Status	Poll CRD_VCC Status
RDY_MOD (In–out)	Force to 0	READ	Force to 0	Force to 0	READ	READ
CS (in)	Rising edge	0	Rising edge	Rising edge	0	0
PWR_ON (in)	0/1	0/1	Program CRD_VCC	Program CRD_VCC	0 or Hi–Z	1
RESET (in)	Program CLK input/divide ratio	Not used	0/1	0/1	Not used	Not used
I/O (in)	Program CLK input/divide ratio	Not used	0/1	0/1	Not used	Not used

MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{bat}	Battery Supply Voltage	7.0	V
I_{bat}	Battery Supply Current	±200	mA
V_{CC}	Power Supply Voltage	6.0	V
I_{CC}	Power Supply Current	±150	mA
V_{in}	Digital Input Pins	$-0.5\ V < V_{in} < V_{bat} + 0.5\ V$, but < 7.0	V
I_{in}		±5.0	mA
V_{out}	Digital Output Pins	$-0.5\ V < V_{in} < V_{bat} + 0.5\ V$, but < 7.0	V
I_{out}		±10	mA
V_{card}	Card Interface Pins	$-0.5\ V < V_{card} < V_{cc} + 0.5\ V$,	V
I_{card}		±25	mA
I_L	Inductor Driver Pin	±200	mA
	Power Ground Pin (Pin 1)	±100	mA
V_{ESD}	ESD Capability(2)		
	Standard Pins	2	kV
	Card Interface Pins	4	kV
	SO–16WB Package		
P_D	Power Dissipation @ Tamb = +85°C	285	mW
$R_{\theta JA}$	Thermal Resistance Junction to Air	140	°C/W
T_A	Operating Ambient Temperature Range	–25 to +85	°C
T_J	Operating Junction Temperature Range	–40 to +125	°C
T_{Jmax}	Maximum Junction Temperature(3)	+150	°C
T_{sg}	Storage Temperature Range	–65 to +150	°C

(1) Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
(2) Human Body Model, R = 1500 Ω, C = 100 pF
(3) Absolute Maximum Rating beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4 V, V_{CC} = 5 V nom, PWR_ON = V_{BAT} , $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 µH, CRD_VCC capacitor = 10 µF, unless otherwise noted.)

BATTERY POWER SUPPLY SECTION

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{bat}	Supply Voltage Range	Normal Operating Range Extended Operating Range(4)	2.2 1.8	— —	6.0 6.6	V
I_{obat}	Standby Quiescent Current	PWR_ON = GND, CRDC_ON = GND ASY_CLKIN = GND, V_{bat} = 6 V, all other logic inputs and outputs open	—	—	5.0	µA
I_{batop}	DC Operating Current	$-I_{CC}$ = 10 mA, V_{cc} = 5 V, V_{bat} = 6 V	—	—	12.5	µA
	V_{bat} Under Voltage Detection Upper Voltage Lower Voltage Hysteresis		—	 1.6 1.4 0.2	—	V

(4) See Figures x and xx.

POWER SUPPLY SECTION @ V_{CC} = 5 V Nominal

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{cc}	Output Voltage	2.2 V < V_{bat} < 6 V 1 mA < $-I_{CC}$ < 25 mA 3.0 V < V_{bat} < 6 V 1 mA < $-I_{CC}$ < 60 mA	4.75 4.60	5.0 5.0	5.25 5.40	V
 V_{th} V_{tl} V_{hyss}	Card V_{cc} Under Voltage Detection Upper Threshold Lower Threshold Switching Hysteresis	RDY_MOD Output See Table 4	 4.2 120	 4.5 180	 V_{cc}–0.14 	 V V mV
$-I_{CC}Lim$	Peak Output Current	V_{CC} = 4 V, Internally Limited RDY_MOD = L	70	—	—	mA
tdy	Current Limit Time Out	V_{CC} = 4 V	—	160	—	ms
$I_{CC}st$	Start–up Current	V_{CC} = 2 V 0°C < T_A < +85°C −40°C < T_A < 0°C	 70 50	 — —	 — —	mA
V_{sat}	Low Side Power Switch Saturation	I_L = 50 mA	—	100	160	mV
V_F	Rectifier Forward Voltage	I_L = 50 mA	—	400	520	mV
F_{SW}	DC/DC Switching Frequency	T_A = +25°C	—	120	—	kHz
I_{SD}	Shut Down Current (Card Access Deactivated)	PWR_ON = GND V_{CC} = 2 V	70	—	—	mA

POWER SUPPLY SECTION @ V_{CC} = 3 V Nominal

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{cc}	Output Voltage	2.2 V < V_{bat} < 6 V 1 mA < $-I_{CC}$ < 10 mA 2.5 V < V_{bat} < 6 V 1 mA < $-I_{CC}$ < 50 mA	2.75 2.60	3.0 3.0	3.25 3.40	V
 V_{th} V_{tl} V_{hyss}	Card V_{cc} Under Voltage Detection Upper Threshold Lower Threshold Switching Hysteresis	RDY_MOD Output See Table yyy	 2.4 80	 2.7 110	V_{cc}–0.10 	 V V mV
$I_{CC}st$ I_{SD}	Start–up Current Shut Down Current	V_{CC} = 2 V 0°C < T_A < +85°C −40°C < T_A < 0°C	 50 50	 — —	 — —	mA

APPLICATION INTERFACE DC SECTION @ V_{bat} = 5 V

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Threshold Voltage (Increasing)	Pin	0.55*V_{bat}	—	0.55*V_{bat}	V
V_{IL}	Input Low Threshold Voltage (Decreasing)	Pin Pin Pin	0.3*V_{bat} 0.2*V_{bat} 0.3*V_{bat}	—	0.45*V_{bat} 0.40*V_{bat} 0.50*V_{bat}	V
V_{hyst}	Switching Hysteresis	Pin	0.06*V_{bat}	—	0.30*V_{bat}	V
	Threshold Voltage	Pin	—	—	—	V
R_{down}	Pull–down Resistance	V_{in} = V_{bat} − 1 V	50	100	200	kΩ
R_{up}	Pull–up Resistance	V_{in} = 0.5 V	50	100	200	kΩ
V_{OH}	Output High Voltage	I_{OH} = −2.5 μA, @ CS = H I_{OH} = −50 μA I_{OH} = −0.2 mA, Output Mode	V_{bat} − 1	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA I_{OL} = 0.2 mA	—	—	0.4	V
I_{leak}	Input Leakage Current	V_{in} = 2.5 V, CS = H	—	—	2.0	μA

CARD INTERFACE DC SECTION @ V_{bat} = 5 V

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −20 μA I_{OL} = 0.2 mA	V_{cc}–0.9	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA I_{OL} = 0.2 mA	—	—	0.4	V
	I/O Pull–up Resistance, Operating Mode, CS = L, PWR_ON = H	V_{OL} = 0.5 V	18	—	—	kΩ
V_{sec}	Card Pins Security Voltage (Card Access Deactivated)	PWR_ON = GND, I_{in} = 10 mA	—	—	2.0	V

DIGITAL DYNAMIC SECTION @ V_{bat} = 5 V, Normal Operating Mode(6)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
Fasyclk	Input Clock Frequency	Duty Cycle = 50%	—	—	20	MHz
Fcrdclk	Card Clock Frequency		—	—	20	MHz
Rclk	Card Clock Duty Cycle(7)	Fio = 16 MHz, 50% V_{cc}	45	—	55	%
Trclk Tfclk	Card Clock Rise/Fall Time	10 −90% V_{cc}	— —	— —	10 10	ns
Fio	I/O Data Transfer Frequency	(8)	—	1.0	—	MHz
Trio Tfio	I/O Rise and Fall Time	10%–90% V_{cc}	—	—	150 150	ns
	I/O Transfer Time	50% V_{cc}, L–<H, H–>L	—	—	—	—
Tdseq	Card Signal Sequence Interval	V_{cc} Power Up/Down	—	0.2	1.0	μs
Tdres	Internal Reset Delay	RES, V_{CC} Power Up/Down	—	20	—	μs
Tdrdy	Ready Delay Time		—	—	2.0	μs
Twon	PWR_ON Low Pulse Width	CS = L	2.0	—	—	μs

(6) Pin Load = 30 pF
(7) Since the clock buffer is optimized for low current consumption, clock signal duty cycle is guaranteed for divide by 2 and divide by 4 ratio.

DIGITAL DYNAMIC SECTION @ V_{bat} = 5 V, Programming Mode(6)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
Tsmod	Data Set–up Time RDY_MOD, PWR_ON, RESET, I/O		1.0	—	—	µs
Thmod	Data Hold Time RDY_MOD, PWR_ON, RESET, I/O		1.0	—	—	µs
Twcs	CS Low Pulse Width		2.0	—	—	µs

DETAILED OPERATING DESCRIPTION

Card Vcc and Card Clock Programming

The CRD_VCC and ASY_CLK programming options allows matching the system frequency with the card clock frequency, and to select 3 V or 5 V CRD_VCC supply. The table 3 given hereafter highlight the PWR_ON, RESET and I/O values for the possible options. The default power reset condition is state 4: synchronous clock and CRD_VCC = 5 V. All states are latched for each output variable in programming mode at the positive going slope of CS.

Table 3. Card Vcc and Card Clock Truth Table

STATE #	PWR_ON	RESET	I/O	CRD_VCC	CRD_CLK
0	L	L	L	3 V	SYN_CLK
1	L	L	H	3 V	ASY_CLKIN/4
2	L	H	H	3 V	ASY_CLKIN/2
3	L	H	L	3 V	ASY_CLKIN
4	**H**	**L**	**L**	**5 V**	**SYN_CLK**
5	H	L	H	5 V	ASY_CLKIN/4
6	H	H	H	5 V	ASY_CLKIN/2
7	H	H	L	5 V	ASY_CLKIN

NOTE: Card clock integrity is guaranteed no spikes whatever be the frequency switching. At power ON, state 4 is the default state machine.

DC/DC Converter and Card Detector Status

The MC33561 status can be polled when CS = L. Please consult Table 3 for a description of input and output signals. The status message is described in Table 4.

Table 4.

PWR_ON (Input)	RDY_MOD (Output)	Message
LOW	LOW	No Card
LOW	HIGH	Card Present
HIGH	LOW	DC/DC Converter Overloaded
HIGH	HIGH	DC/DC Converter OK

APPLICATIONS INFORMATION

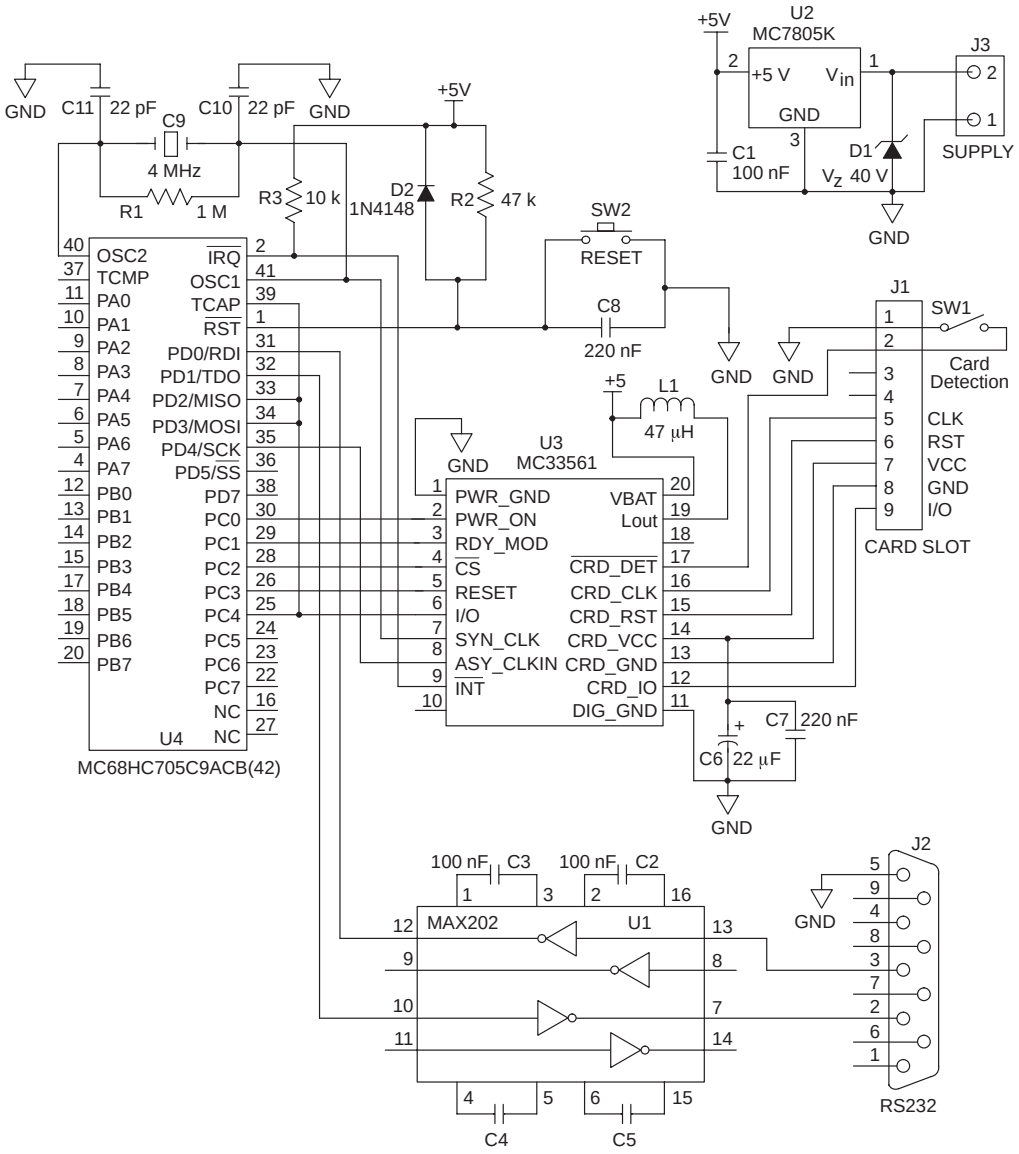


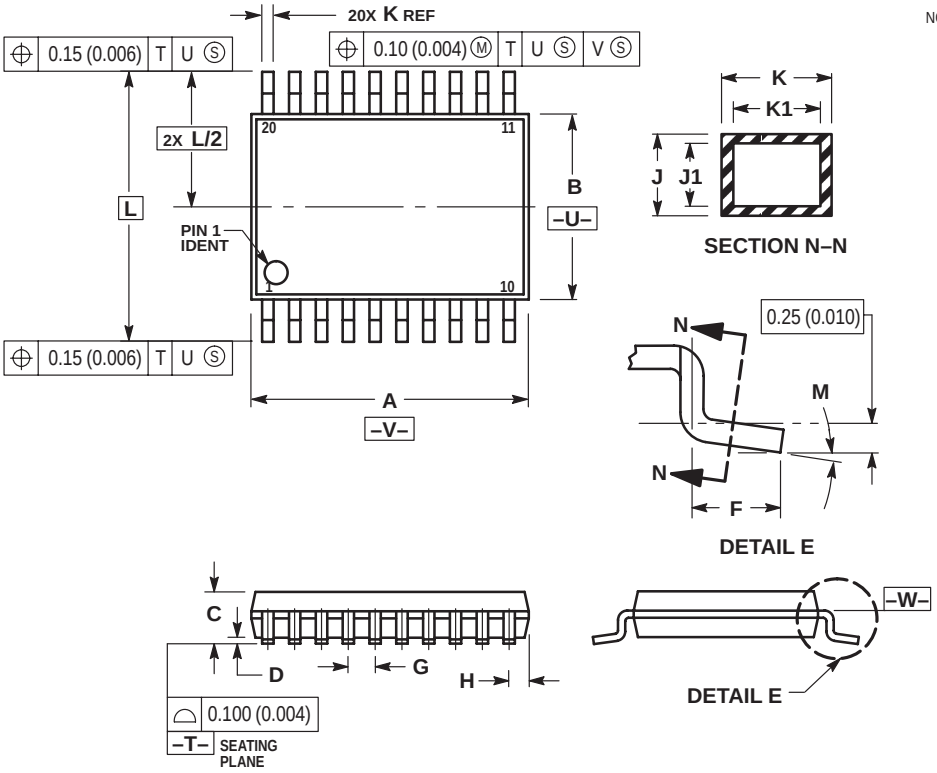
Figure 3. Typical Application Schematic Diagram

ORDERING INFORMATION

Device	Package	Shipping
MC33561DTB	TSSOP–20	75 Units / Rail
MC33561DTBR2	TSSOP–20	2500 Units / Tape & Reel

PACKAGE DIMENSIONS

TSSOP–20
DTB SUFFIX
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

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