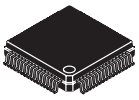
Order Number: MC100ES8223/D
Rev 0, 11/2001

Preliminary Information

Low Voltage 1:22 Differential HSTL Clock Fanout Buffer

MC100ES8223

LOW–VOLTAGE 1:22 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER



TC SUFFIX
64–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 840K

The Motorola MC100ES8223 is a bipolar monolithic differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8223 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:22 differential clock fanout buffer
- 50 ps maximum device skew[1]
- SiGe technology
- Supports DC to 800 MHz operation[1] of clock or data signals
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Standard 64 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP223

Functional Description

The MC100ES8223 is designed for low skew clock distribution systems and supports clock frequencies up to 800 MHz[1]. The device accepts two clock sources. The HCLK input can be driven by HSTL compatible signals, the PCLK input accepts PECL compatible signals. The selected input signal is distributed to 22 identical, differential HSTL outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 22 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part–to–part and output–to–output skew. The open-emitter outputs require a 50Ω DC termination to GND (0V). The output supply voltage can be either 1.5V or 1.8V, the core voltage supply is 3.3V. The output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. In the case of an asynchronous control, there is a chance of generating a 'runt' clock pulse when the device is enabled/disabled.

The MC100ES8223 is pin and function compatible to the MC100EP223.

PRELIMINARY

1. AC specifications are design targets and subject to change

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

© Motorola, Inc. 2001

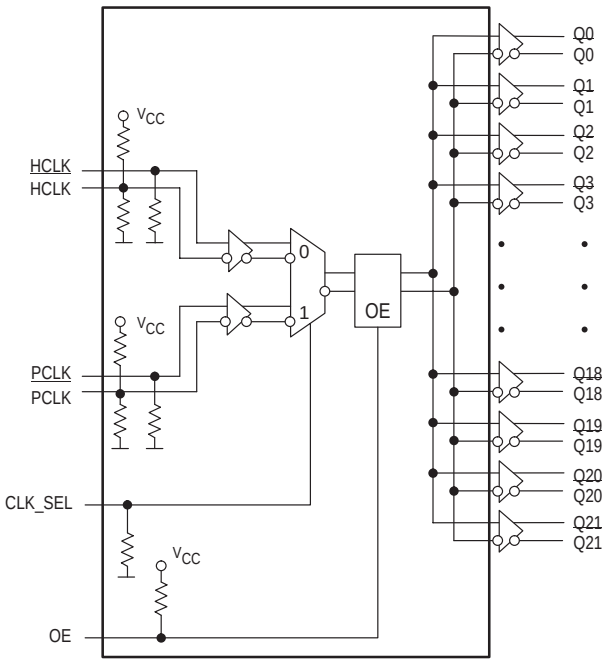


Figure 1. MC100ES8223 Logic Diagram

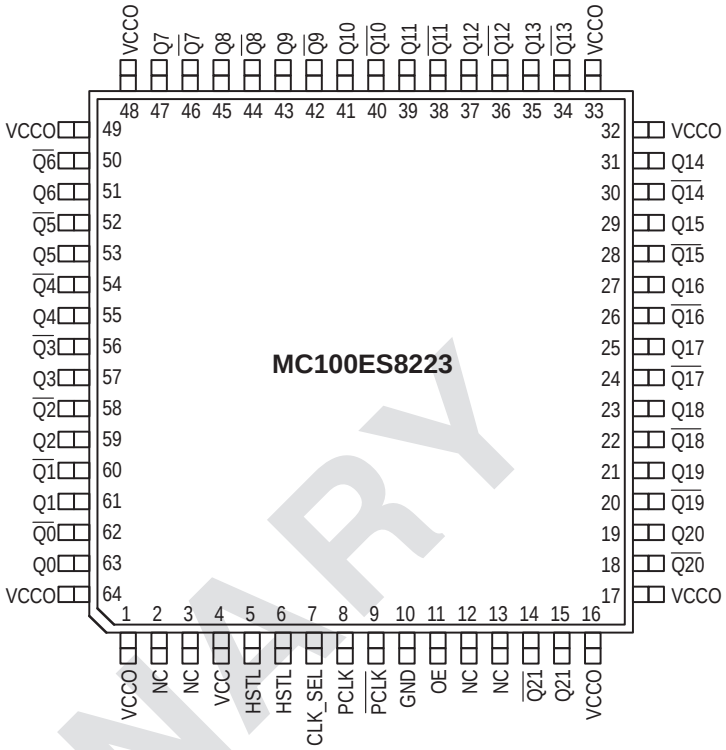


Figure 2. 64–Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
HCLK1, $\overline{\text{HCLK}}$	Input	HSTL	Differential HSTL reference clock signal input
PCLK, $\overline{\text{PCLK0}}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVCMOS	Reference clock input select
OE	Input	LVCMOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0-21], $\overline{\text{Q[0-21]}}$	Output	HSTL	Differential clock outputs
GND	Supply		Negative power supply
V_{CC}	Supply		Positive power supply of the device core (3.3V)
V_{CCO}	Supply		Positive power supply of the HSTL outputs. All V_{CCO} pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation.

Table 2. Function Table

Pin	0	1
CLK_SEL	HCLK, $\overline{\text{HCLK}}$ input pair is the reference clock. HCLK is HSTL compatible.	PCLK, $\overline{\text{PCLK}}$ input pair is the reference clock. PCLK is PECL compatible.
OE	Outputs disabled, Q[0:21]=L, $\overline{\text{Q[0:21]}}$=H	Outputs enabled

PRELIMINARY

Table 3. Absolute Maximum Ratings[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{CCO}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		0		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
$\theta_{JA}, \theta_{JB}, \theta_{JC}$	Thermal resistance (junction–to–ambient, junction–to–board, junction–to–case)	See Table 7 "Thermal Resistance" on page 6			°C/W	
T_J	Operating junction temperature[a] (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8223 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8223 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

PRELIMINARY

Table 5. DC Characteristics (V_{CC} = 3.3V±5%, V_{CCO} = 1.5V±0.1V or V_{CCO}=1.8V±0.1V, T_J = 0°C to + 110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair HCLK, $\overline{HCLK}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage[b]	0.2			V	
$V_{X, IN}$	Differential cross point voltage[c]	0.68		0.9	V	
V_{IH}	Input high voltage	V_X+0.1			V	
V_{IL}	Input low voltage			V_X-0.1	V	
I_{IN}	Input Current			±150	µA	$V_{IN} = V_X \pm 0.1V$
Clock input pair PCLK, $\overline{PCLK}$ (PECL differential signals)						
V_{PP}	Differential input voltage[d]	0.15		1.0	V	Differential operation
V_{CMR}	Differential cross point voltage[e]	1.0		V_{CC}-0.6	V	Differential operation
V_{IH}	Input voltage high	V_{CC}-1.165		V_{CC}-0.880	V	
V_{IL}	Input voltage low	V_{CC}-1.810		V_{CC}-1.475	V	
I_{IN}	Input Current[a]			±150	µA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS control inputs OE, CLK_SEL						
V_{IL}	Input voltage low			0.8	V	
V_{IH}	Input voltage high	2.0			V	
I_{IN}	Input Current			±150	µA	$V_{IN} = V_{IH}$ or V_{IN}
HSTL clock outputs (Q[0-21], $\overline{Q[0-21]}$)						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1.1			V	
V_{OL}	Output Low Voltage			0.4	V	
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)
I_{CCO}[f]	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pins (outputs)

a. DC characteristics are design targets and pending characterization.
b. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
c. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
d. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
e. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
f. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

PRELIMINARY

Table 6. AC Characteristics (V_{CC} = 3.3V±5%, V_{CCO} = 1.5V±0.1V or V_{CCO} = 1.8V±0.1V, T_J = 0°C to + 110°C)[a b]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair HCLK, $\overline{HCLK}$ (HSTL differential signals)						
V_{DIF}	Differential input voltage[c] (peak-to-peak)	0.4			V	
$V_{X, IN}$	Differential cross point voltage[d]	0.68		0.9	V	
f_{CLK}	Input Frequency		0-800	TBD	MHz	
t_{PD}	Propagation Delay HCLK0 to Q[0-21]			TBD	ps	
Clock input pair PCLK, $\overline{PCLK}$ (PECL differential signals)						
V_{PP}	Differential input voltage[e] (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential input crosspoint voltage[f]	1		V_{CC}-0.6	V	
f_{CLK}	Input Frequency		0-800		MHz	Differential
t_{PD}	Propagation Delay PCLK0 to Q[0-21]			TBD	ps	Differential
HSTL clock outputs (Q[0-21], $\overline{Q[0-21]}$)						
$V_{X, OUT}$	Output differential crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)	0.5			V	
$t_{sk(O)}$	Output-to-output skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	DC_{fref}= 50%
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%

a. DC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
d. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
e. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
f. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

PRELIMINARY

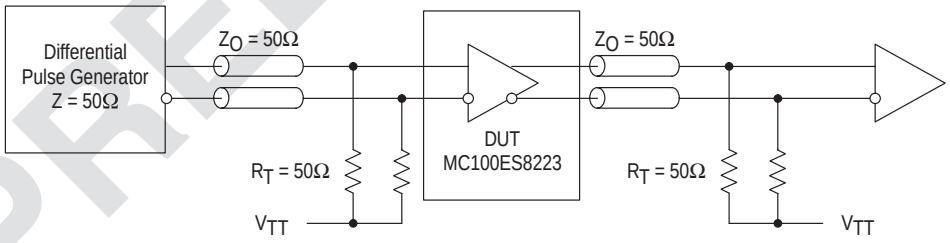


Figure 3. MC100ES8223 AC test reference

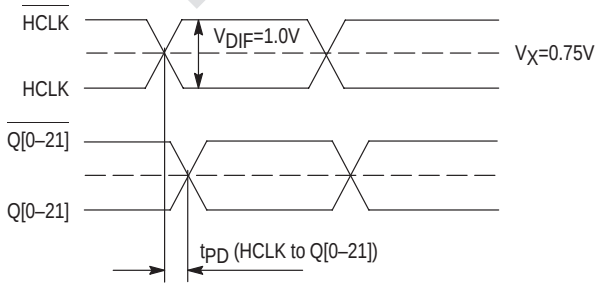


Figure 4. MC100ES8223 AC reference measurement waveform

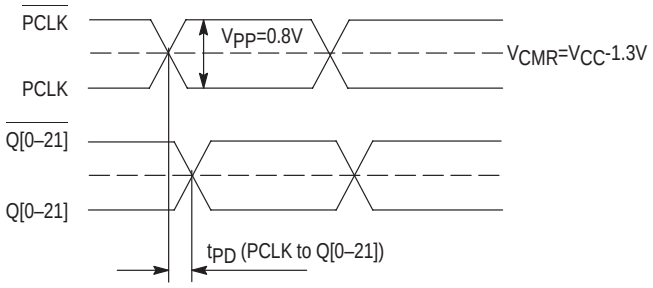


Figure 5. MC100ES8223 AC reference measurement waveform

APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100ES8223

The MC100ES8223 uses a thermally enhanced exposed pad (EP) 64 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES8223 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES8223. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100ES8223 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6. "Recommended thermal land pattern", providing an efficient heat removal path.

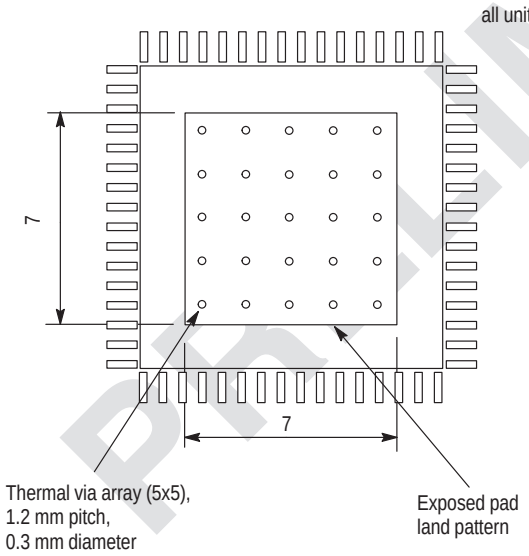


Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7. "Recommended solder mask openings" shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

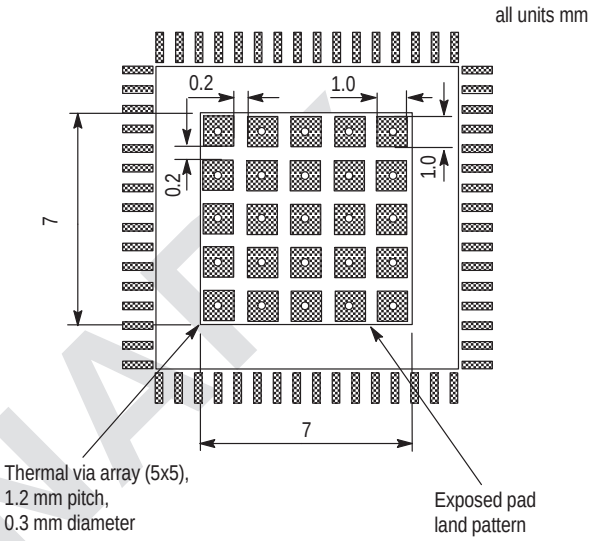


Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 7. Thermal Resistance[a]

Convection-LFPM	R_{THJA}[b] °C/W	R_{THJA}[c] °C/W	R_{THJC}[d] °C/W	R_{THJB}[e] °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

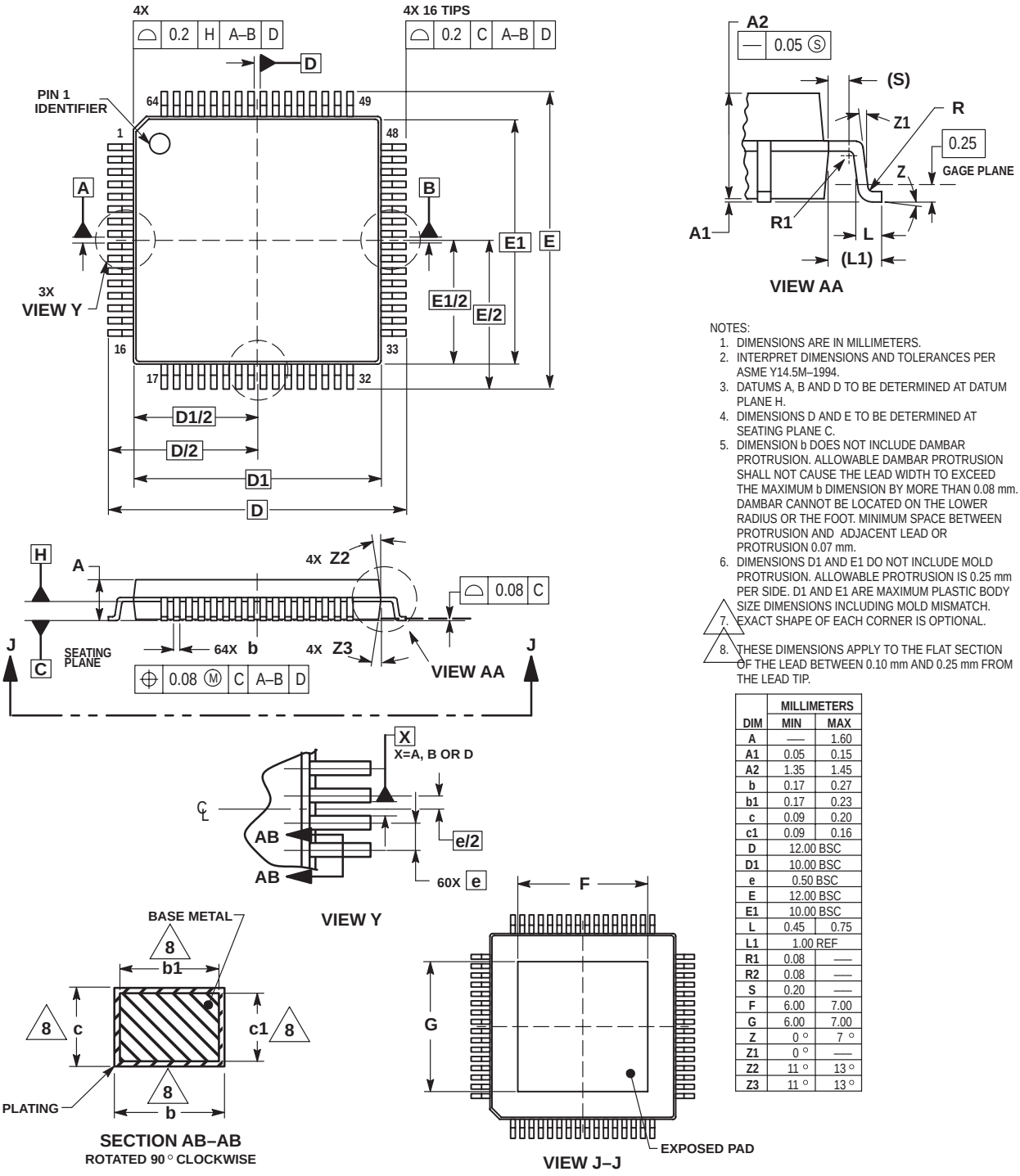
a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES8223 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

PRELIMINARY

OUTLINE DIMENSIONS

TC SUFFIX
PLASTIC LQFP PACKAGE, EXPOSED PAD
CASE 840K–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	—
R2	0.08	—
S	0.20	—
F	6.00	7.00
G	6.00	7.00
Z	0 °	7 °
Z1	0 °	—
Z2	11 °	13 °
Z3	11 °	13 °

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer. MOTOROLA and the M logo are registered in the US Patent & Trademark Office. All other product or service names are the property of their respective owners.

© Motorola, Inc. 2001.

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

HOME PAGE: http://www.motorola.com/semiconductors/