

# LOW Power, High Accuracy Quad Universal Filter Building Block

February 1998

# **FEATURES**

- Four Identical 2nd Order Filters in an SSOP Package
- Center Frequency Error: ±0.3%
- Low Noise:  $\leq$ 40µ $W_{RMS}$  per 2nd Order Section, Q  $\leq$  5
- High Dynamic Range: THD + Noise ≤ 0.01%
- Low DC Offsets: ≤10mV per 2nd Order Section
- Clock-to-Center Frequency Ratio: 50:1
- No Aliasing for Input Frequencies up to 100 × f<sub>CLITOFF</sub>
- Maximum Center Frequency up to 50kHz  $(V_S = \pm 5V)$
- Operates from ±1.57V to ±5V Power Supplies

## **APPLICATIONS**

- Low Power Linear Phase Bandpass Filters (Up to 40kHz, V<sub>S</sub> = Single 5V)
- Dual 4th Order Phase Matched Filters (Up to 40kHz, V<sub>S</sub> = Single 5V)
- Low Power Tone Detectors (High Selectivity Bandpass Filters up to 30kHz, V<sub>S</sub> = Single 5V)

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### DESCRIPTION

The LTC®1068-50 consists of four identical, low noise, high accuracy 2nd order switched-capacitor filter building blocks. Each building block, together with three to five resistors, can provide 2nd order filter functions like low-pass, bandpass, highpass and notch. High precision, high performance, quad 2nd order, dual 4th order or 8th order filters can also be designed with an LTC1068-50. The center frequency of each 2nd order section is tuned by an external clock. The clock-to-center frequency ratio is internally set to 50:1 and can be modified by external resistors.

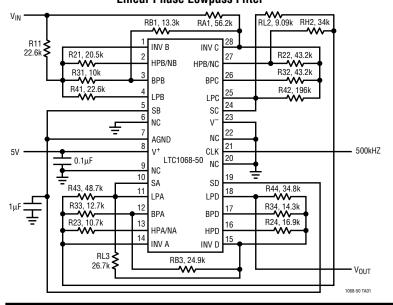
The sampling rate of the LTC1068-50 is twice the clock frequency. The maximum input frequency can approach twice the clock frequency before aliasing occurs.

A customized version of the LTC1068-50 in a 16-lead SO with internal thin film resistors can be obtained. Clock-to-center frequency ratios higher or lower than 50:1 can also be obtained. Please contact LTC Marketing for details.

The LTC1068-50 is available in a 28-pin SSOP surface mount package and is supported by FilterCAD<sup>TM</sup> 2.0 filter design software.

# TYPICAL APPLICATION

Low Power, Single 5V Supply, 10kHz, 8th Order, Linear Phase Lowpass Filter



# Frequency Response 5 0 -5 -10 -15 -20 -20 -35 -40 -45 -50 -55 -60 -65 -70 -75 1 10 100 FREQUENCY (kHz)

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# **ABSOLUTE MAXIMUM RATINGS**

Total Supply Voltage (V <sup>+</sup> to V <sup>-</sup> )	12V
Power Dissipation	500mW
Operating Temperature Range	
LTC1068CG-500	°C to 70°C
LTC1068IG-5040	°C to 85°C
Input Voltage at Any Pin $V^ 0.3V \le V_{IN} \le$	$V^{+} + 0.3V$
Storage Temperature Range65°C	C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

# PACKAGE/ORDER INFORMATION

	TOP VIEW	L	ORDER PART NUMBER
INV B		28 INV C	INUIVIDEIT
HPB/NB	2	27 HPC/NC	
ВРВ	3	26 BPC	LTC1068CG-50
LPB	4	25 LPC	LTC1068IG-50
SB	5	24 SC	
NC	6	23 V <sup>-</sup>	
AGND	7	22 NC	
V+	8	21 CLK	
NC	9	20 NC	
SA	10	19 SD	
LPA	11	18 LPD	
BPA	12	17 BPD	
HPA/NA	13	16 HPD/ND	
INV A	14	15 INV D	
ī	G PACKAGE 28-LEAD PLASTIC S <sub>JMAX</sub> = 125°C, θ <sub>JA</sub> = 9		

Consult factory for Military grade parts.

# **ELECTRICAL CHARACTERISTICS** (Internal Op Amps) $V_S = \pm 5V$ , $T_A = 25^{\circ}C$ , unless otherwise specified.

PARAMETER CONDITIONS		MIN	TYP	MAX	UNITS	
Operating Supply Voltage Range			3.14		±5.5	V
Voltage Swings	$V_S = 3.14V, R_L = 5k \text{ (Note 1)}$ $V_S = 4.75V, R_L = 5k \text{ (Note 2)}$ $V_S = \pm 5V, R_L = 5k$	•	1.2 2.6 ±3.4	1.8 3.6 ±4.1		V <sub>P-P</sub> V <sub>P-P</sub> V
Output Short-Circuit Current (Source/Sink)	$V_S = 3.14V \text{ (Note 1)}$ $V_S = \pm 5V$			17/6 20/15		mA mA
DC Open-Loop Gain	R <sub>L</sub> = 5k			85		dB
GBW Product				4		MHz
Slew Rate				10		V/µs
Analog Ground Voltage	V <sub>S</sub> = 5V, Voltage at Pin 7 (AGND) (Note 3)			2.175		V

### (Complete Filter) $T_A=25^{\circ}C,$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Center Frequency, f <sub>CLK</sub> /f <sub>0</sub> (Note 5)	$\begin{split} &V_S = 3.14 V,  f_{CLK} = 250 \text{kHz},  \text{Mode 1 (Note 1)}, \\ &f_0 = 5 \text{kHz},  Q = 5,  V_{IN} = 0.34 V_{RMS}, \\ &R1 = R3 = 49.9 \text{k},  R2 = 10 \text{k} \end{split}$	•		50 ± 0.3%	$50 \pm 0.8\% \\ 50 \pm 0.9\%$	
	$V_S = \pm 5V$ , $f_{CLK} = 500 kHz$ , Mode 1, $f_0 = 10 kHz$ , $Q = 5$ , $V_{IN} = 1V_{RMS}$ , R1 = R3 = 49.9 k, $R2 = 10 k$	•		50 ± 0.3%	$50 \pm 0.8\%$ $50 \pm 0.9\%$	
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	$V_S = 3.14V$ , $f_{CLK} = 250$ kHz, $Q = 5$ (Note 1) $V_S = \pm 5V$ , $f_{CLK} = 500$ kHz, $Q = 5$	•		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 5)	$V_S = 3.14V$ , $f_{CLK} = 250$ kHz, $Q = 5$ (Note 1) $V_S = \pm 5V$ , $f_{CLK} = 500$ kHz, $Q = 5$	•		±1 ±1	±3 ±3	% %

# **ELECTRICAL CHARACTERISTICS** (Complete Filter) $T_A = 25$ °C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f <sub>0</sub> Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	$V_S = \pm 5V$ , $f_{CLK} = 500$ kHz, $V_{OS1}$ (DC Offset of Input Inverter)	•		0	±15	mV
	$V_S = \pm 5V$ , $f_{CLK} = 500$ kHz, $V_{OS2}$ (DC Offset of First Integrator)	•		-2	±25	mV
	$V_S = \pm 5V$ , $f_{CLK} = 500$ kHz, $V_{OS3}$ (DC Offset of Second Integrator)	•		-5	±40	mV
Clock Feedthrough	$V_S = \pm 5V$ , $f_{CLK} = 500$ kHz			0.16		mV <sub>RMS</sub>
Maximum Clock Frequency	$V_S = \pm 5V, Q \le 1.6, Mode 1$			3.4		MHz
Power Supply Current	$V_S = 3.14V$ , $f_{CLK} = 250$ kHz (Note 1) $V_S = 4.75V$ , $f_{CLK} = 250$ kHz (Note 2) $V_S = \pm 5V$ , $f_{CLK} = 500$ kHz	•		3.0 4.3 6.0	5 8 11	mA mA mA

The lacktriangle denotes specifications which apply over the full operating temperature range.

**Note 1:** Production testing for single 3.14V supply is achieved by using the equivalent dual supplies of 1.7696V and -1.3704V. Note 3 is an explanation for using nonsymmetrical power supplies.

**Note 2:** Production testing for single 4.75V supply is achieved by using the equivalent dual supplies of 2.6771V and -2.0729V. Note 3 is an explanation for using nonsymmetrical power supplies.

**Note 3:** Pin 7 (AGND) is the internal analog ground of the device. For single supply applications this pin should be bypassed with a  $1\mu F$  capacitor. The biasing voltage of AGND is set with an internal resistive divider from Pin 8 to Pin 23, the value of AGND =  $0.435 \cdot V^+$ .

Note 4: See typical performance characteristics.

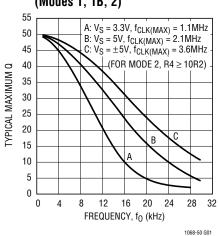
Note 5: Side D is guaranteed by design.

Table 1. Output DC Offsets One 2nd Order Section

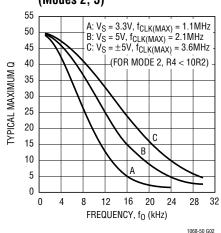
MODE	V <sub>OSN</sub>	V <sub>OSBP</sub>	V <sub>OSLP</sub>
1	$V_{0S1}[(1/Q) + 1 +   H_{0LP}  ] - V_{0S3}/Q$	V <sub>OS3</sub>	V <sub>OSN</sub> – V <sub>OS2</sub>
1B	$V_{0S1}[(1/Q) + 1 + R2/R1] - V_{0S3}/Q$	V <sub>OS3</sub>	$\sim (V_{OSN} - V_{OS2})(1 + R5/R6)$
2	[V <sub>0S1</sub> (1 + R2/R1 + R2/R3 + R2/R4) – V <sub>0S3</sub> (R2/R3)X [R4/(R2 + R4)] + V <sub>0S2</sub> [R2/(R2 + R4)]	V <sub>OS3</sub>	V <sub>OSN</sub> - V <sub>OS2</sub>
3	V <sub>0S2</sub>	V <sub>OS3</sub>	V <sub>0S1</sub> [1 + R4/R1 + R4/R2 + R4/R3] - V <sub>0S2</sub> (R4/R2) - V <sub>0S3</sub> (R4/R3)

# TYPICAL PERFORMANCE CHARACTERISTICS





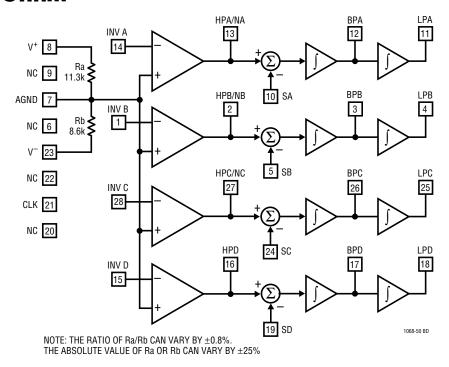
# Maximum Q vs Frequency (Modes 2, 3)





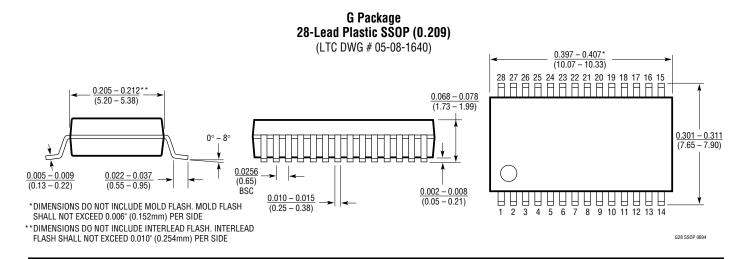


# **BLOCK DIAGRAM**



# PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.



# RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1068	Low Noise Universal Filter	100:1 Clock-to-f <sub>0</sub> Ratio, f <sub>C</sub> to 50kHz
LTC1068-25	High Speed Universal Filter	25:1 Clock-to-f <sub>0</sub> Ratio, f <sub>C</sub> to 200kHz
LTC1068-200	Universal Filter	200:1 Clock-to-f <sub>0</sub> Ratio, f <sub>C</sub> to 25kHz
LTC1064	Universal Filter	50:1 and 100:1 Clock-to- $f_0$ Ratios, $f_C$ to 100kHz, $V_S$ = Up to $\pm 7.5$ V
LTC1164	Low Power Universal Filter	50:1 and 100:1 Clock-to- $f_0$ Ratios, $f_C$ to 20kHz, $V_S$ = Up to $\pm 7.5$ V
LTC1264	High Speed Universal Filter	20:1 Clock-to- $f_0$ Ratio, $f_C$ to 200kHz, $V_S$ = Up to $\pm 7.5$ V