

16-BIT SYNCHRONOUS 2:1 MUX/DEMUX SWITCH

FEATURES:

- · Bus switches provide zero delay paths
- · Low switch on-resistance
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- · Hot insertion capability
- · Very low power dissipation
- · Available in SSOP and TSSOP packages

DESCRIPTION:

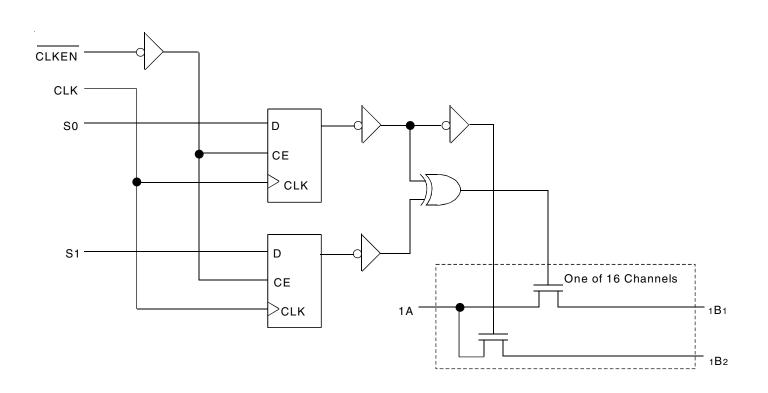
The FST163232 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163232 provides three 16-bit TTL- compatible ports that support 2:1 multiplexing. The S0,1 pins control mux select and switch enable/disable. The S0,1 inputs are synchronous and clocked on the rising edge of CLK when CLKEN is low.

Port A can be connected to port B1 or port B2 or both ports B1 and B2.

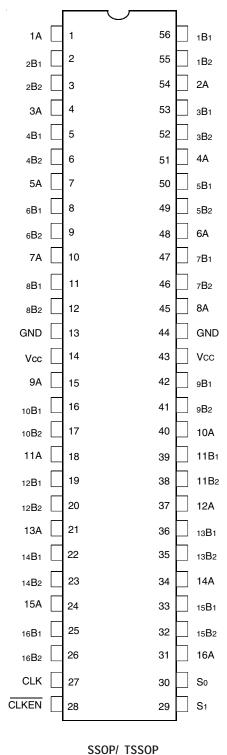
FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

PINCONFIGURATION



TOP VIEW

INDUSTRIALTEMPERATURERANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	–0.5 to +7	V
Tstg	Storage Temperature	–65 to +150	°C
Ιουτ	Maximum Continuous Channel Current	128	mA

NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Vcc, Control, and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter		Conditions ⁽²⁾	Тур.	Unit
CIN	Control Input Capacitar	ice		6	рF
CI/O	Switch Input/Output	A Port	Switch Off	17	pF
	Capacitance	B Port	Switch Off	12	

NOTES:

1. Capacitance is characterized but not tested.

2. TA = 25° C, f = 1MHz, VIN = 0V, VOUT = 0V.

PINDESCRIPTION

Pin Names	I/O	Description	
A1	I/O	Bus A1	
B1, B2	I/O	Buses B1, B2	
S0, 1	Ι	Control Pins	
CLK	I	Clock Input. Clocks So, 1 on Rising Edge.	
CLKEN	I	Clock Enable Input	

FUNCTION TABLE⁽¹⁾

S 1	S 0	CLK	CLKEN	Description
Х	Х	Х	Н	Last State
L	L	\uparrow	L	Disconnect
L	Н	\uparrow	L	A to B1 and A to B2
Н	L	\uparrow	L	A to B1 or B1 to A
Н	Н	\uparrow	L	A to B2 or B2 to A

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

Z = High-Impedance

 \uparrow = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = $5.0V \pm 10\%$

Symbol	Parameter	Test	Conditions ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Unit
Vih	Control Input HIGH Voltage	Guaranteed Logic HIGH for	Control Inputs	2	—	_	V
VIL	Control Input LOW Voltage	Guaranteed Logic LOW for	Control Inputs	_	—	0.8	V
Іін	Control Input HIGH Current	Vcc = Max.	VI = VCC	-	—	±1	μA
liL	Control Input LOW Current		VI = GND	-	—	±1	
Іоzн	Current During	Vcc = Max., Vo = 0 to 5V		-	_	±1	μA
Iozl	Bus Switch Disconnect			—	—	±1	
Vik	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		_	-0.7	-1.2	V
IOFF	Switch Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5 V		_	_	±1	μA
lcc	Quiescent Power Supply Current	Vcc = Max., VIN = GND or	· Vcc	-	0.1	3	μA

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

 $\label{eq:conditions} Following \ Conditions \ Apply \ Unless \ Otherwise \ Specified:$

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = $5.0V \pm 10\%$

Symbol	Parameter	Test Conditions	Min.	Тур. ⁽¹⁾	Max.	Unit
		Vcc = Min., $Vin = 0V$, $Ion = 64mA$	_	4	7	
Ron	Switch On Resistance ⁽²⁾	Vcc = Min., VIN = 0V, ION = 30mA	_	4	7	Ω
		Vcc = Min., $Vin = 2.4V$, $Ion = 15mA$	_	6	15	
los	Short Circuit Current, A to B ⁽³⁾	A(B) = 0V, B(A) = Vcc	100	—	_	mA

NOTES:

1. Typical values are at Vcc = 5.0V, +25°C ambient.

2. The voltage drop between the indicated ports divided by the current through the switch.

3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Condit	ions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
∆lcc	Quiescent Power Supply Current TTL Inputs HIGH	$V_{\text{IN}} = Max.$ $V_{\text{IN}} = 3.4V^{(3)}$		-	0.5	1.5	mA
ICCD	Dynamic Power Supply Current ^(4,5)	Vcc = Max. Clock Pin Toggling 50% Duty Cycle 16 Switches Toggling One Select Toggling at 50% of CLK Frequency	VIN = VCC VIN = GND				μΑ/ MHz/
ICCD	Dynamic Power Supply Current ^(4,5)	Vcc = Max. Clock Pin Toggling 50% Duty Cycle 32 Switches Toggling Two Select Pins Toggling at 50% of CLK Frequency	VIN = VCC VIN = GND				μΑ/ MHz/
lc	Total Power Supply Current ⁽⁶⁾	Vcc = Max. fcp = 10MHz (CLK) 50% Duty Cycle	VIN = VCC VIN = GND				mA
		CLKEN = LOW	VIN = VCC				
		So = HIGH or LOW	VIN = 3.4V				
		fi = 2.5MHz (S1)					
		16 Switches Toggling					-
		Vcc = Max. fcp = 10MHz (CLK) 50% Duty Cycle	VIN = VCC VIN = GND				
		CLKEN = LOW	VIN = VCC				
		S1 = HIGH	VIN = 3.4V				
		fi = 2.5MHz (So)					
		16 MUXes Exchanging					1
		Vcc = Max. fcp = 10MHz (CLK)	VIN = VCC VIN = GND				
		50% Duty Cycle					
		$\overline{\text{CLKEN}} = \text{LOW}$	VIN = VCC				1
		S1 = LOW	VIN = 3.4V				
		fi = 2.5MHz (So)					
		32 Switches Toggling					

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. TA = -40°C to +85°C

2. Typical values are at Vcc = 5.0V, +25°C ambient.

3. Per TTL driven input (VIN = 3.4V). All other inputs at Vcc or GND. Switch inputs do not contribute to △Icc.

4. This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.

Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. 5. CPD = IccD/Vcc

CPD = Power Dissipation Capacitance

6. IC = IQUIESCENT + INPUTS + IDYNAMIC

 $IC = ICC + \Delta ICC DHNT + ICCD (fiN)$

Icc = Quiescent Current

- ΔIcc = Power Supply Current for a TTL High Input (VIN = 3.4V)
- DH = Duty Cycle for TTL Inputs High
- NT = Number of TTL Inputs at DH
- IccD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
- fi = Control Input Frequency
- N = Number of Control Inputs Toggling at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40° C to $+85^{\circ}$ C, VCC = 5.0V $\pm 10\%$

			$Vcc = 5V \pm 10\%$		Vcc = 4V		
Symbol	Description ⁽¹⁾	Min.	Тур.	Max.	Min.	Max.	Unit
t PLH	Data Propagation Delay		_	0.25	_	0.25	ns
t PHL	A to B, B to A ⁽²⁾						
tрzн	Switch CONNECT Delay	1.5	-	5.8	-	6.1	ns
t PZL	CLK↑ to A-B1 or A-B2						
tрzн	Switch CONNECT Delay	1.5	-	7.9	-	8.5	ns
t PZL	CLK↑ to B1-B2						
tрнz	Switch DISCONNECT Delay	1.9	-	6.2	-	5.8	ns
t PLZ	CLK↑ to A, B						
tвх	Switch EXCHANGE Delay	1.8	-	6.2	_	6.8	ns
	CLK [↑] from A-B1(B2) to A-B2(B1)						
tsu	Clock Enable Set-Up Time	1.9	-	—	2.2	-	ns
	CLKEN to CLK [↑]						
ы	Clock Enable Hold Time	1	-	—	1.9	-	ns
	CLKEN after CLK↑						
tsu	Select Set-Up Time	1.9	-	—	2.2	-	ns
	S0, S1 to CLK↑						
tH	Select Hold Time	1	-	—	0.5	-	ns
	S0, S1 after CLK↑						
Qci	Charge Injection During Switch DISCONNECT	—	1.5	—	-	-	рС
	CLK \uparrow to A, B ⁽³⁾						
QDCI	Charge Injection During Switch Exchange	-	0.5	—	-	-	рС
	CLK \uparrow to A, B ⁽³⁾						

NOTES:

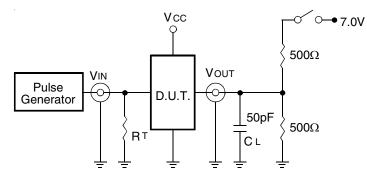
1. See test circuits and waveforms.

2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.

3. |Qci| is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers. |Qbci| is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

IDT74FST163232 16-BIT SYNCHRONOUS 2:1 MUX/DEMUX SWITCH

TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs

SWITCH POSITION

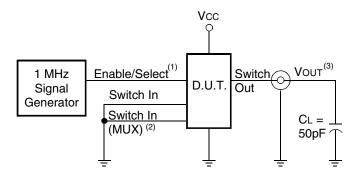
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

NOTES:

CL = Load capacitance: includes jig and probe capacitance.

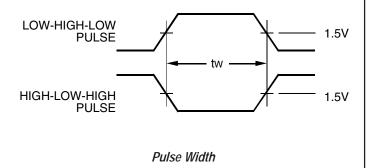
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



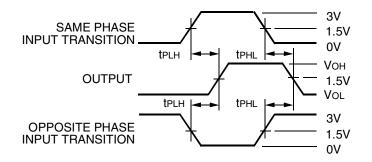
1. Select is used with multiplexers for measuring IQDCII during multiplexer select. During all other tests Enable is used.

Charge Injection

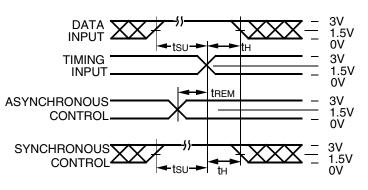
- 2. Used with multiplexers to measure IQDCII only.
- 3. Charge Injection = Δ Vout CL, with Enable toggling for IQcII or Select toggling for IQpcII. Δ Vout is the change in Vout and is measured with a 10M Ω probe.



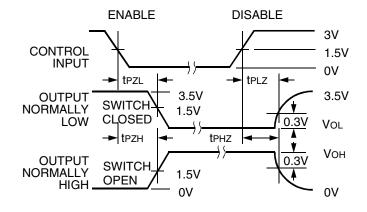
INDUSTRIAL TEMPERATURE RANGE



Propagation Delay



Set-up, Hold, and Release Times

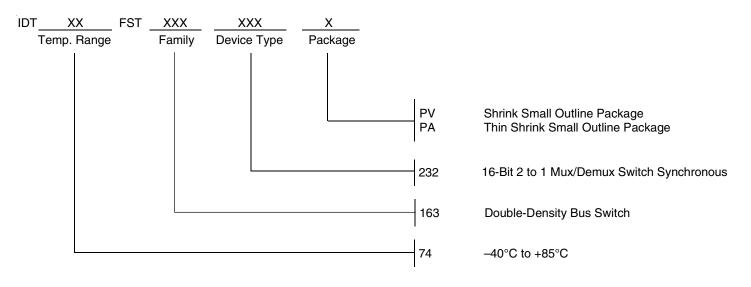


Enable and Disable Times

NOTES:

- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- 2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

5/24/2002 Removed TVSOP package



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