3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16601

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.
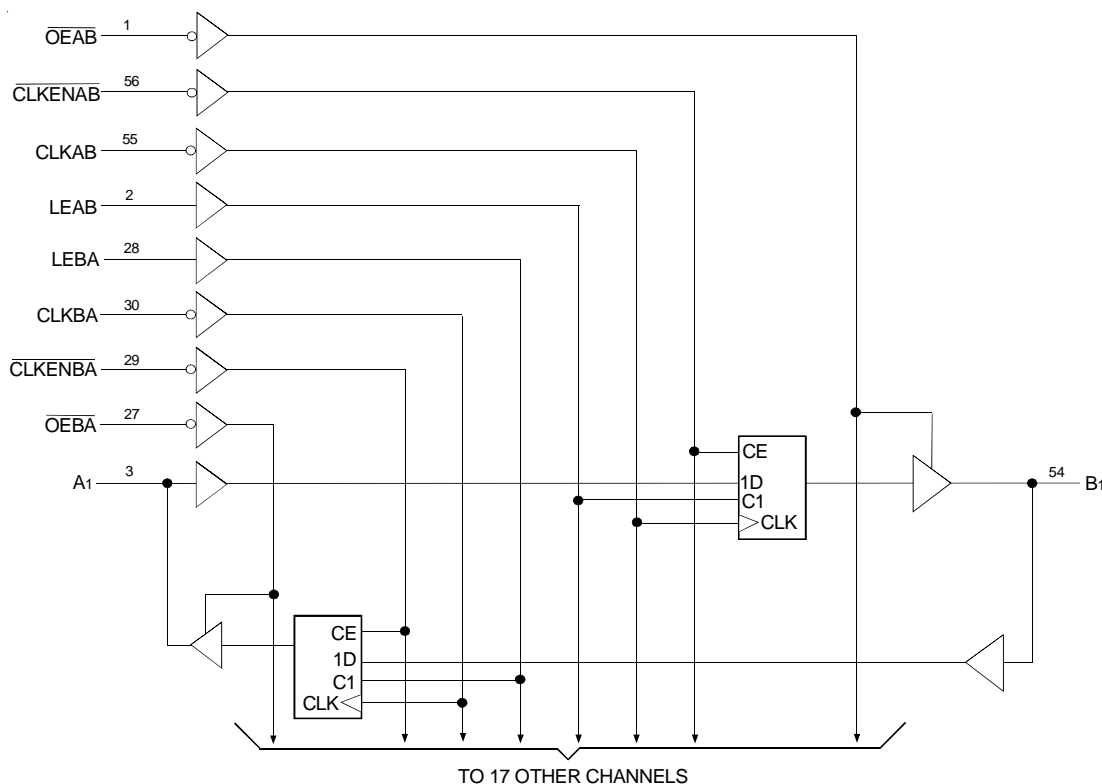
Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The ALVCH16601 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16601 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.
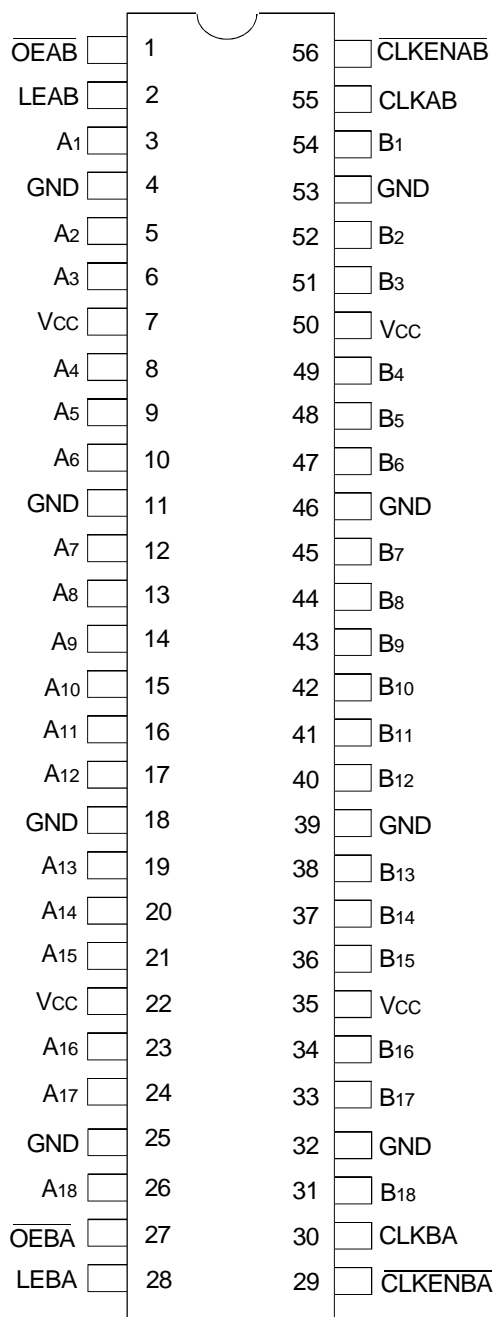
FUNCTIONAL BLOCK DIAGRAM

TO 17 OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

APRIL 1999

DSC-4732/1

PIN CONFIGURATION

$\overline{OEAB}$	1	56	CLKENAB
LEAB	2	55	CLKAB
A_1	3	54	B_1
GND	4	53	GND
A_2	5	52	B_2
A_3	6	51	B_3
V_{CC}	7	50	V_{CC}
A_4	8	49	B_4
A_5	9	48	B_5
A_6	10	47	B_6
GND	11	46	GND
A_7	12	45	B_7
A_8	13	44	B_8
A_9	14	43	B_9
A_{10}	15	42	B_{10}
A_{11}	16	41	B_{11}
A_{12}	17	40	B_{12}
GND	18	39	GND
A_{13}	19	38	B_{13}
A_{14}	20	37	B_{14}
A_{15}	21	36	B_{15}
V_{CC}	22	35	V_{CC}
A_{16}	23	34	B_{16}
A_{17}	24	33	B_{17}
GND	25	32	GND
A_{18}	26	31	B_{18}
$\overline{OEBA}$	27	30	CLKBA
LEBA	28	29	$\overline{CLKENBA}$

SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE $(T_A = +25°C, F = 1.0MHz)$

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A x	A-to-B Data Inputs or B-to-A 3-State Outputs[1]
B x	B-to-A Data Inputs or A-to-B 3-State Outputs[1]
$\overline{CLKENAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B-to-A Clock Enable Input (Active LOW)

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE[1,2]

Inputs					Output
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	Ax	Bx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B[3]
H	L	L	X	X	B[3]
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B[3]

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA, and $\overline{\text{CLKENBA}}$.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH transition
3. Level of B before the indicated steady-state inputs were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	-75	—	—	μA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	-45	—	—	μA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	μA
I_{BHLO}							

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = -0.1mA	$V_{CC} - 0.2$	—	V
		V_{CC} = 2.3V	I_{OH} = -6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = -12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = -24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40°C$ to $+85°C$.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} = 2.5V ± 0.2V Typical	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	41	52	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		6	6	

SWITCHING CHARACTERISTICS[1]

Symbol	Parameter	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	MHz
t_{PLH}	Propagation Delay	1	4	—	4.6	—	4.1	ns
t_{PHL}	Ax to Bx or Bx to Ax							
t_{PLH}	Propagation Delay	1	4.6	—	5.3	—	4.7	ns
t_{PHL}	LEAB to Bx or LEBA to Ax							
t_{PLH}	Propagation Delay	1.2	5.2	—	5.8	—	5	ns
t_{PHL}	CLKAB to Bx or CLKBA to Ax							
t_{PZH}	Output Enable Time	1.1	5.3	—	6.1	—	5.2	ns
t_{PZL}	$\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax							
t_{PHZ}	Output Disable Time	1.4	4.9	—	4.8	—	4.4	ns
t_{PLZ}	$\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax							
t_{SU}	Set-up Time, data before CLK↑	2.3	—	2.4	—	2.1	—	ns
t_{SU}	Set-up Time, data before LE↓, CLK HIGH	2	—	1.6	—	1.6	—	ns
t_{SU}	Set-up Time, data before LE↓, CLK LOW	1.3	—	1.2	—	1.1	—	ns
t_{SU}	Set-up Time, $\overline{CLKEN}$ before CLK↑	2	—	2	—	1.7	—	ns
t_H	Hold Time, data after CLK↑	0.7	—	0.7	—	0.8	—	ns
t_H	Hold Time, data after LE↓, CLK HIGH	1.3	—	1.6	—	1.4	—	ns
t_H	Hold Time, data after LE↓, CLK LOW	1.7	—	2	—	1.7	—	ns
t_H	Hold Time, $\overline{CLKEN}$ after CLK↑	0.3	—	0.5	—	0.6	—	ns
t_W	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t_W	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
$t_{SK}(o)$	Output Skew[2]	—	—	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2 Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS
TEST CONDITIONS

Symbol	Vcc[1] = 3.3V±0.3V	Vcc[1] = 2.7V	Vcc[2] = 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF
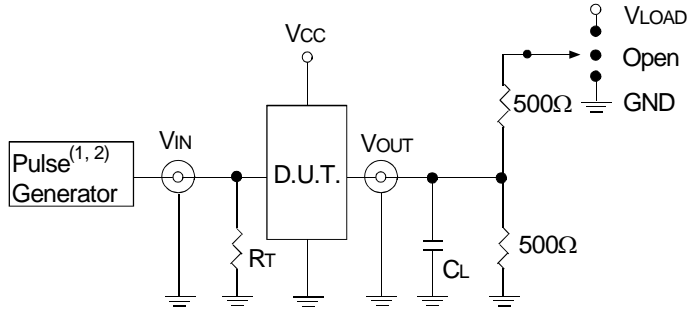
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

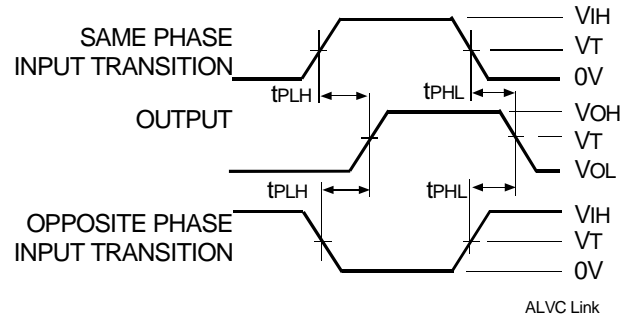| Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open
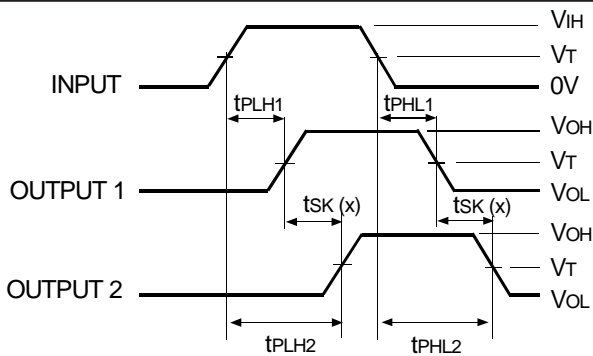
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$
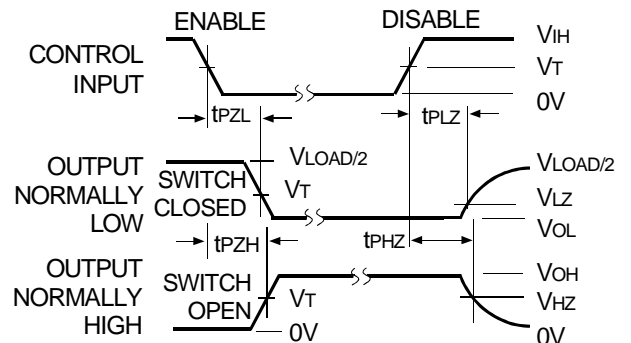
Output Skew - $t_{SK}(x)$

NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
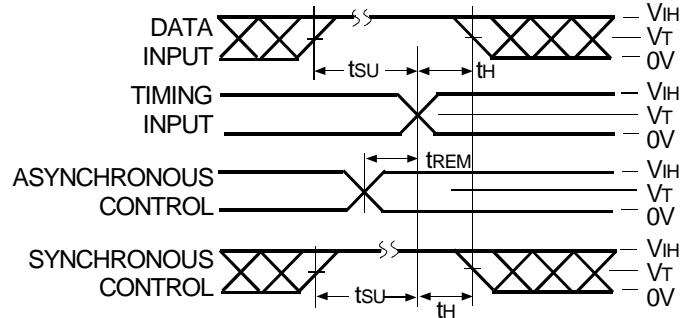2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.
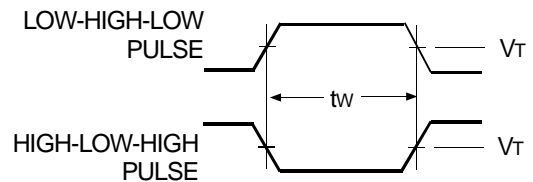

Propagation Delay

Enable and Disable Times

NOTE:
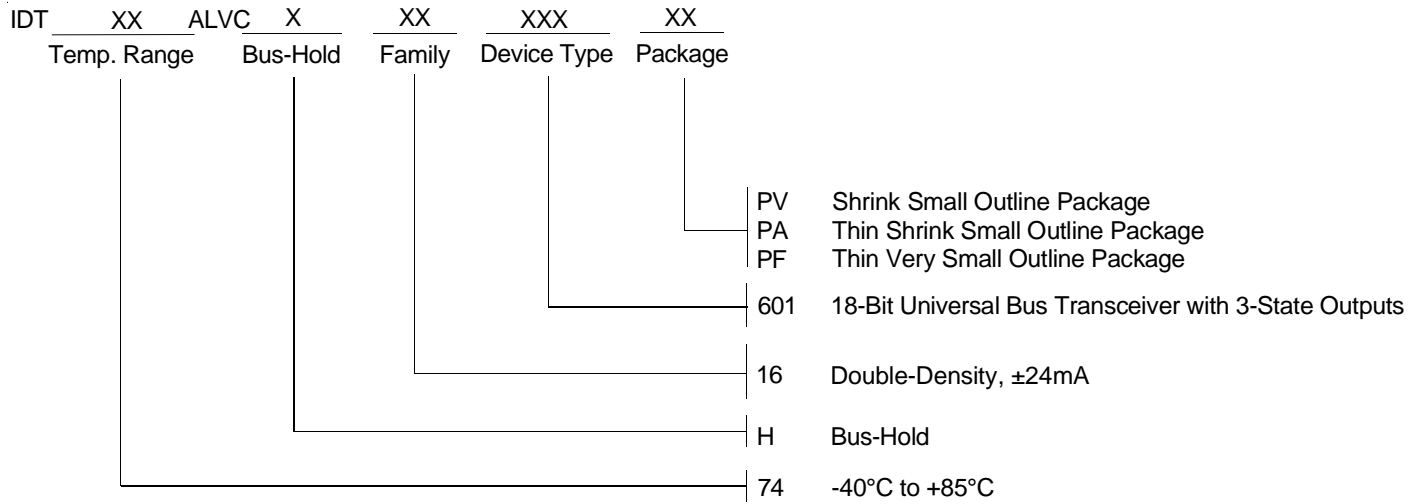1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Set-up, Hold, and Release Times

Pulse Width

ORDERING INFORMATION

IDT   XX   ALVC   X   XX   XXX   XX
     Temp. Range   Bus-Hold   Family   Device Type   Package

PV	Shrink Small Outline Package
PA	Thin Shrink Small Outline Package
PF	Thin Very Small Outline Package
601	18-Bit Universal Bus Transceiver with 3-State Outputs
16	Double-Density, ±24mA
H	Bus-Hold
74	-40°C to +85°C