PRELIMINARY

Integrated Circuit Systems, Inc.

ICS873034

LOW SKEW, ÷2, ÷4, ÷8 DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL CLOCK GENERATOR

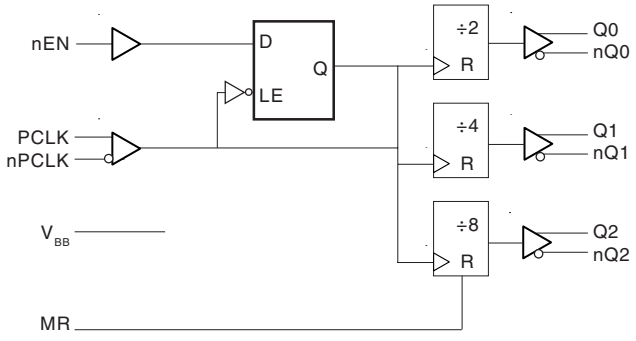
GENERAL DESCRIPTION

The ICS873034 is a low skew, high performance Differential-to-2.5V, 3.3V LVPECL/ECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS873034 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS873034 ideal for those clock distribution applications demanding well defined performance and repeatability.

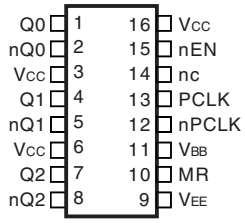
FEATURES

- 3 differential 2.5V, 3.3V LVPECL / ECL output
- 1 differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Input frequency: 3.5GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Pin compatible with MC100LVEP34

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS873034
16-Lead SOIC, 300MIL
7.5mm x 10.3mm x 2.3mm package body
M Package
Top View

ICS873034
16-Lead TSSOP
4.4mm x 3.0mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 6, 16	V_{CC}	Power		Power supply pins.
4, 5	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
7, 8	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
9	V_{EE}	Power		Negative supply pin.
10	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
11	V_{BB}	Output		Bias voltage.
12	nPCLK	Input	Pullup/ Pulldown	Clock input. Defaults to V_{CC}/2 (.66) when left open. LVPECL interface levels.
13	PCLK	Input	Pulldown	Clock input. Default LOW when left floating. LVPECL interface levels.
14	nc	Unused		No connect.
15	nEN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced LOW, nQ outputs are forced HIGH. LVTTL / LVCMOS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		KΩ
$R_{PULLDOWN}$	Input Pullup Resistor			37.5		KΩ

TABLE 3. TRUTH TABLE

Inputs			Function
PCLK	nEN	MR	
Z	L	L	Divide
ZZ	H	L	Hold Q0:Q2
X	X	H	Reset Q0:Q2

Z = LOW to HIGH transistion
ZZ = HIGH to LOW transistion

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 16 Lead SOIC	90°C/W (0 lfpm)
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 16 Lead TSSOP	89°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current			40		mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			2.275			2.295			2.33		V
V_{OL}	Output Low Voltage; NOTE 1			1.545			1.52			1.535		V
V_{IH}	Input High Voltage (Single-ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3											V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			1.475			1.495			1.53		V
V_{OL}	Output Low Voltage; NOTE 1			0.745			0.72			0.735		V
V_{IH}	Input High Voltage (Single-Ended)		1.275		1.56	1.275		1.56	1.275		1.56	V
V_{IL}	Input Low Voltage (Single-Ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2			1.2			1.2			V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1			-1.025			-1.005			-1.005		V
V_{OL}	Output Low Voltage; NOTE 1			-1.755			-1.78			-1.765		V
V_{PP}	Peak-to-Peak Input Voltage			800			800			800		V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

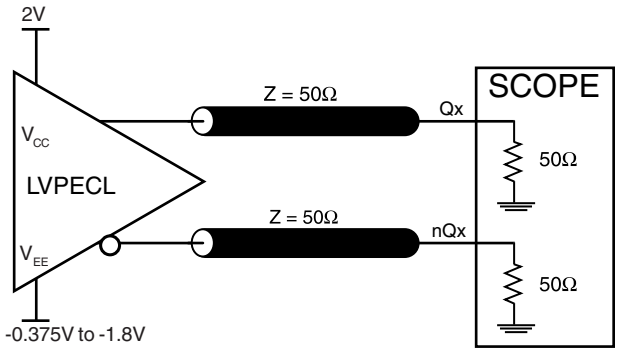
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.8V TO -2.375V OR V_{CC} = 2.375V TO 3.8V; V_{EE} = 0V

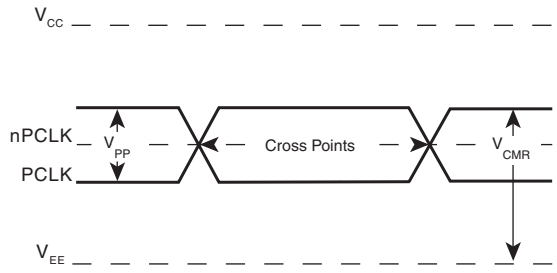
Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Input Frequency			3.5			3.5			3.5		GHz
t_{PD}	Propagation Delay; NOTE 1			530			560			610		ps
t_{RR}	Set/Reset Recovery			320			320			320		ps
t_S	Setup Time	nEN		50			50			50		ps
t_H	Hold Time	nEN		100			100			100		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%		170			180			200		ps
odc	Output Duty Cycle			50			50			50		%

All parameters are measured at f ≤ 1GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

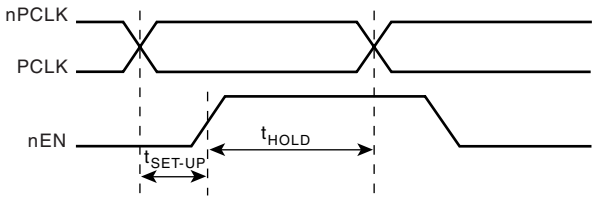
PARAMETER MEASUREMENT INFORMATION



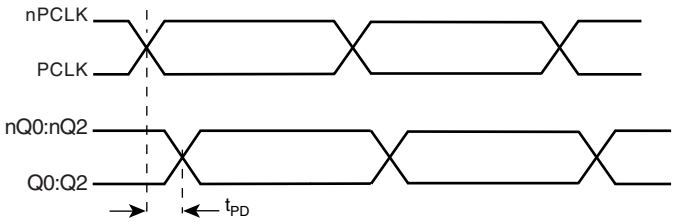
OUTPUT LOAD AC TEST CIRCUIT



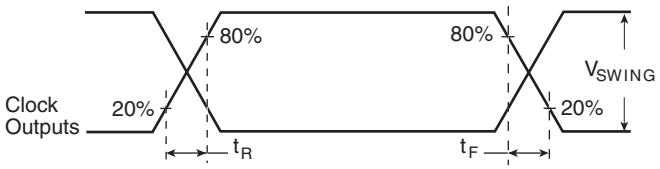
DIFFERENTIAL INPUT LEVEL



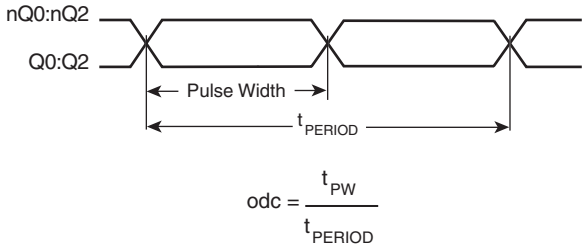
SETUP AND HOLD TIME



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS LEVELS

Figure 2A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

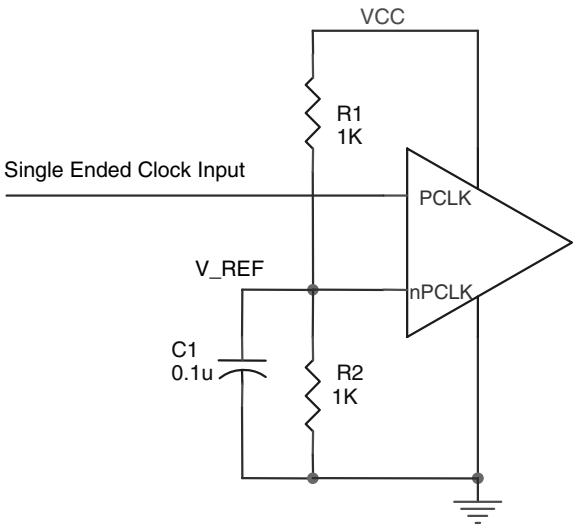


FIGURE 2A. SINGLE ENDED LVCMOS SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 2B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input.

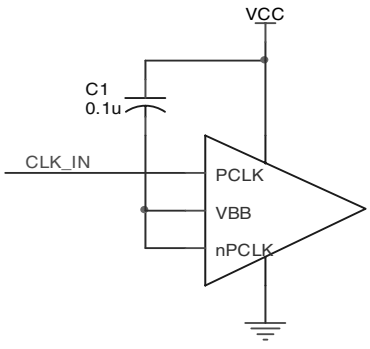


FIGURE 2B. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

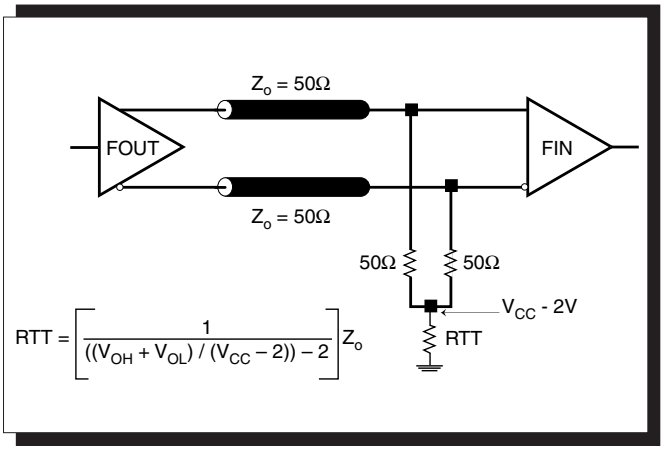


FIGURE 3A. LVPECL OUTPUT TERMINATION

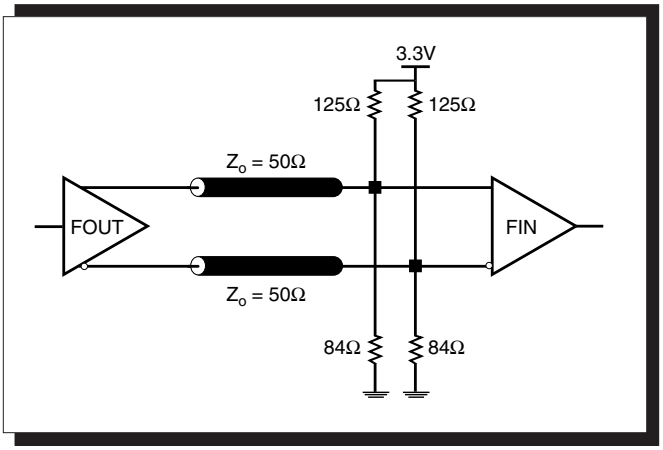


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in *Figure 4B* can be eliminated and the termination is shown in *Figure 4C.*

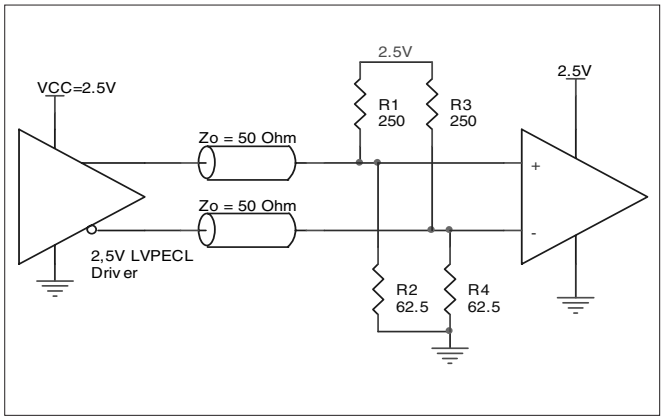


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

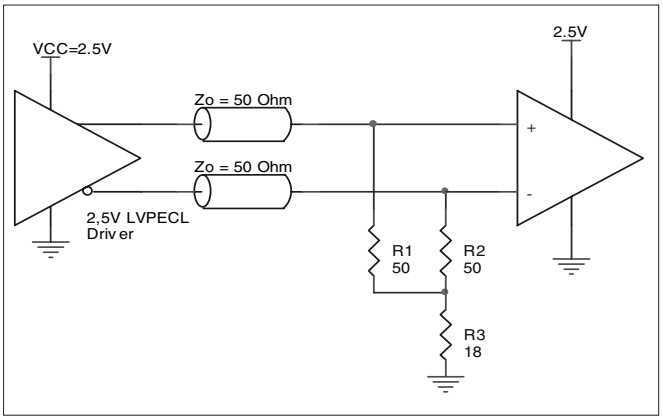


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

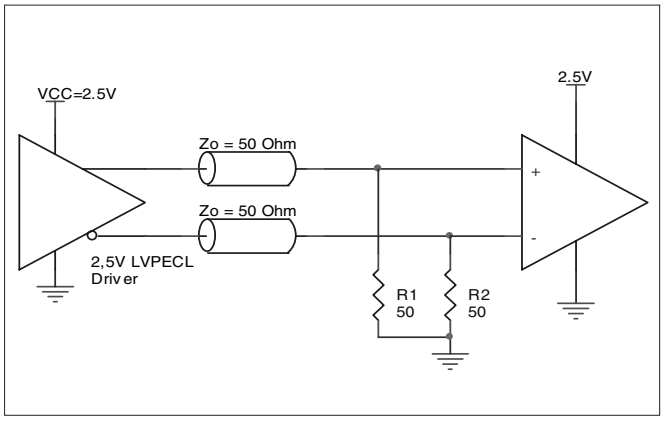


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

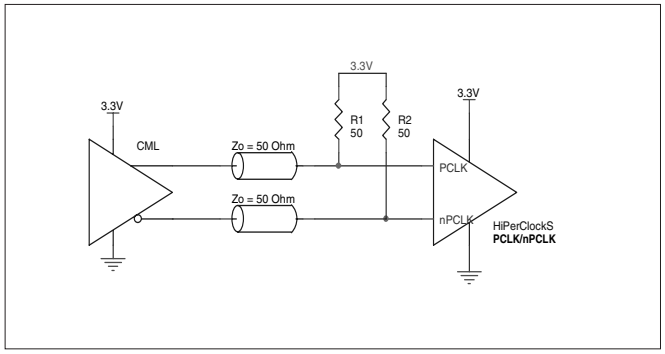


FIGURE 5A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

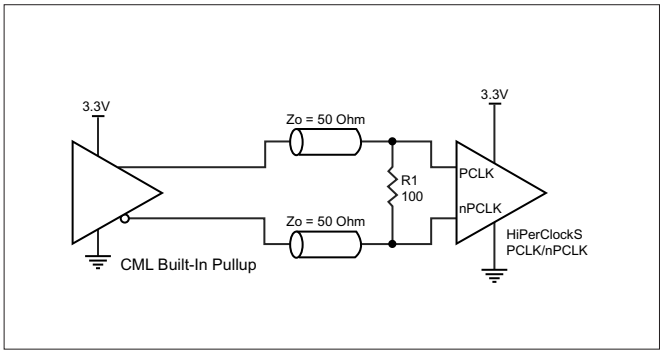


FIGURE 5B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

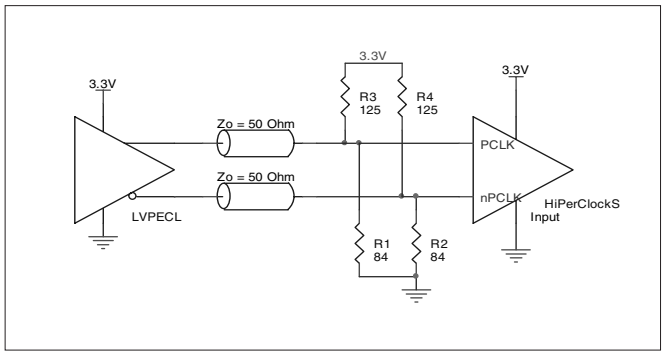


FIGURE 5C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

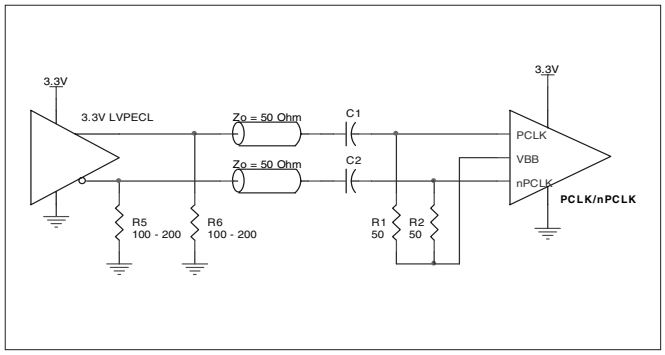


FIGURE 5D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

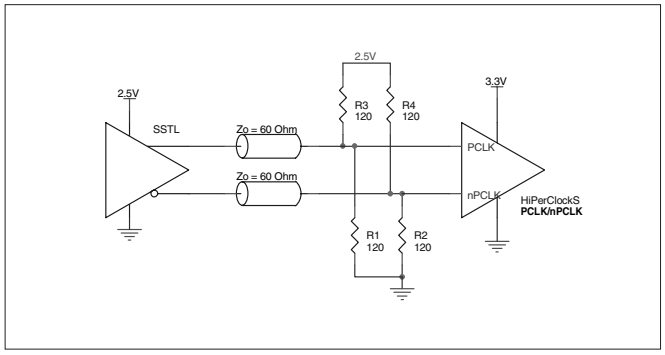


FIGURE 5E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

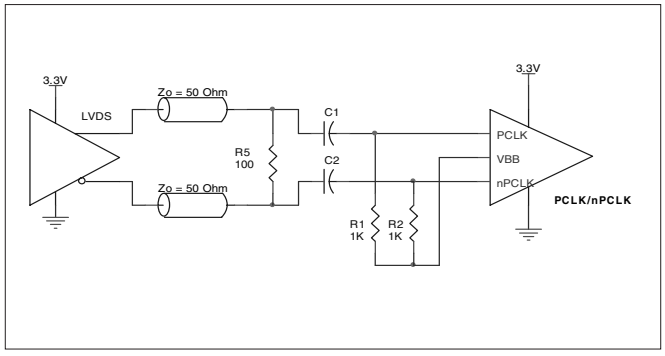


FIGURE 5F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

APPLICATION SCHEMATIC EXAMPLE

Figure 1 shows an example of ICS873034 application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. For the LVPECL output drivers, only two terminations examples are shown in this schematic. More termination approaches are shown in the LVPECL Termination Application Note.

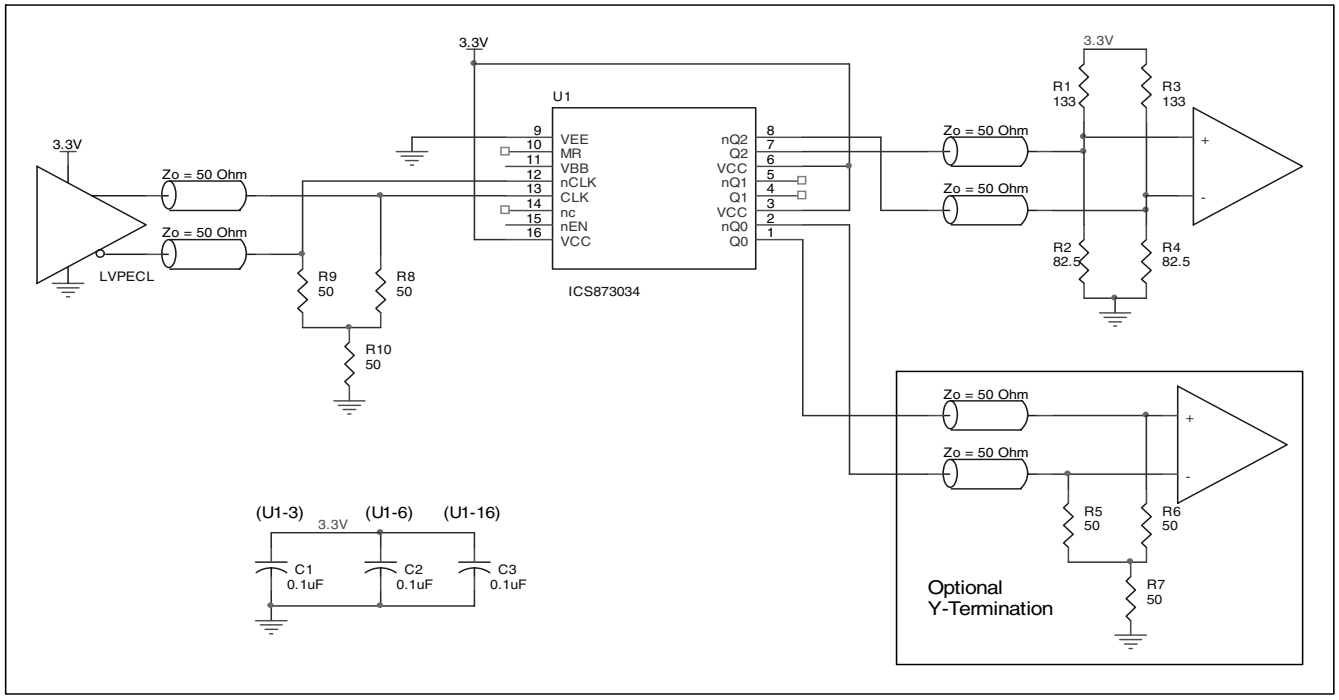


FIGURE 6. ICS873034 APPLICATION SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS873034. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS873034 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.8V * 40mA = **152mW**
- Power (outputs)$_{MAX}$ = **27.83mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 27.83mW = **83.5mW**

Total Power$_{_MAX}$ (3.8, with all outputs switching) = 152mW + 83.5mW = **235.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 82°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.236W * 82°C/W = 104.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 16-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	90°C/W	82°C/W	78°C/W

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

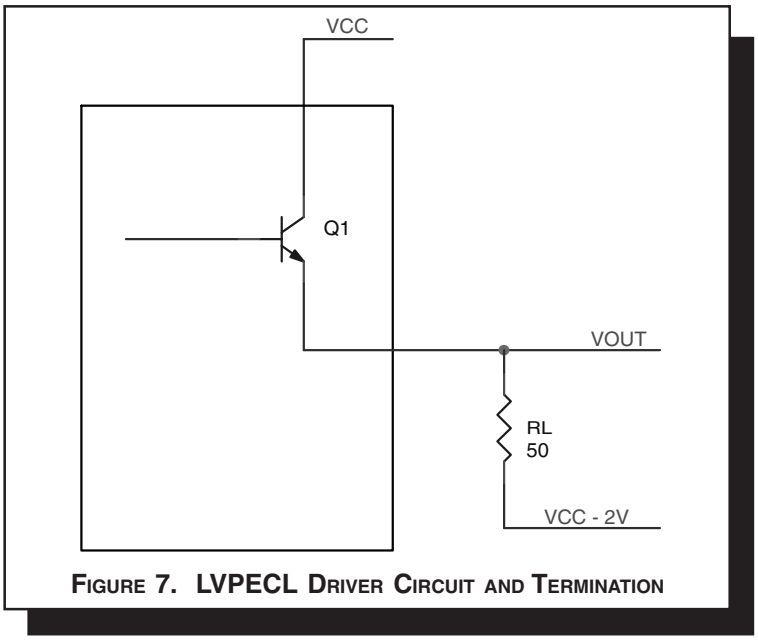


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.005V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.005}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.78V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.78V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1.005V)/50\Omega] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.78V)/50\Omega] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	90°C/W	82°C/W	78°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

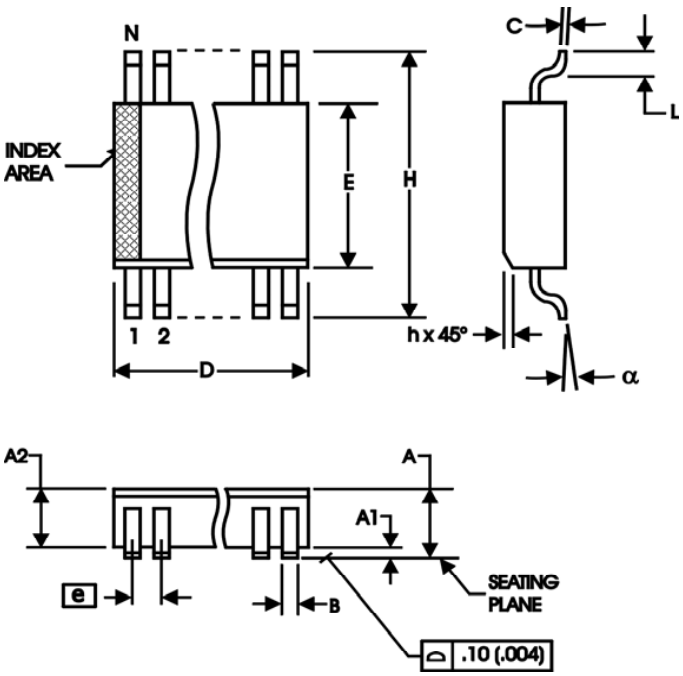
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS873034 is: 280

PACKAGE OUTLINE - M SUFFIX FOR 16 LEAD SOIC



PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

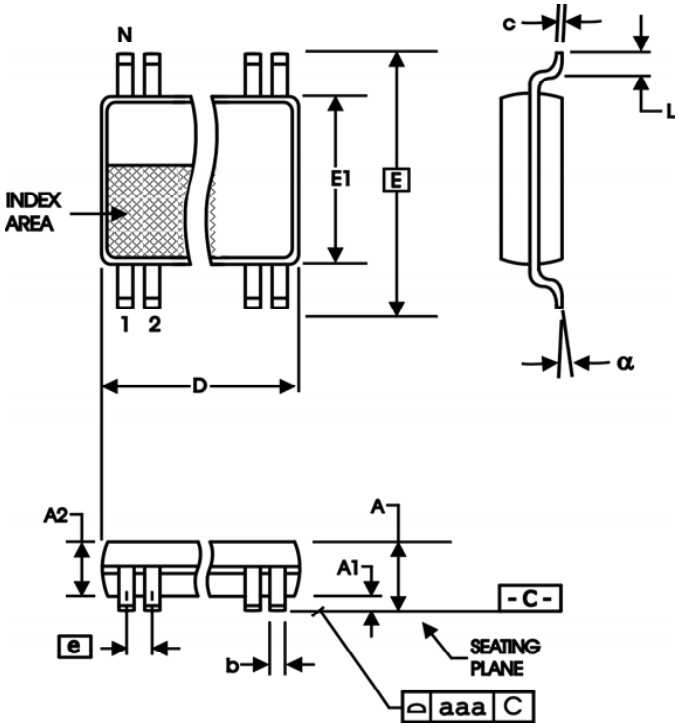


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS873034AM	ICS873034AM	16 Lead SOIC	46 per tube	0°C to 70°C
ICS873034AMT	ICS873034AM	16 Lead SOIC on Tape and Reel	1000	0°C to 70°C
ICS873034AG	ICS873034AG	16 Lead TSSOP	94 per tube	0°C to 70°C
ICS873034AGT	ICS873034AG	16 Lead TSSOP on Tape and Reel	2500	0°C to 70°C