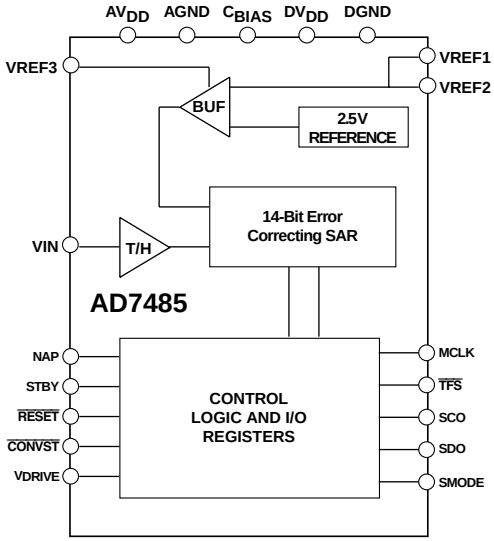
1MSPS Serial, 14-Bit SAR ADC

Preliminary Technical Data — AD7485

FEATURES

Fast Throughput Rate: 1MSPS
Wide Input Bandwidth: 10MHz
Excellent DC Accuracy Performance
Flexible Serial Interface
Low Power:
90mW (Full-Power) and 5mW (NAP Mode)
Standby Mode: 1µA max
Internal +2.5V Reference
Full-Scale Overrange Indication

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7485 is a 14-bit, high speed, low power, successive-approximation ADC. The part features a serial interface with throughput rates up to 1MSPS. The part contains a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 10MHz.

The conversion process is a proprietary algorithmic successive-approximation technique. The input signal is sampled and conversion is initiated on the falling edge of a $\overline{\text{CONVST}}$ signal. The conversion process is controlled by an external master clock. Interfacing is via standard serial signal lines making the part directly compatible with microcontrollers and DSPs.

The AD7485 provides excellent ac and dc performance specifications. Factory trimming ensures high dc accuracy resulting in very low INL, offset and gain errors.

The part uses advanced design techniques to achieve very low power dissipation at high throughput rates. Power consumption in normal mode of operation is 70mW. There are two power-saving modes: a NAP mode, which keeps reference circuitry alive for quick power up, consumes 5mW while a STANDBY mode reduces power consumption to a mere 5µW.

The AD7485 features an on-board +2.5V reference but the part can also accomodate an externally-provided +2.5V reference source. The nominal analog input range is 0 to +2.5V

The AD7485 also provides the user with overrange indication via a 15th bit. If the analog input range strays outside the 0 to +2.5V input range the 15th data bit is set to a logic high.

The AD7485 is powered from a +4.75V to +5.25V supply. The part also provides a V_{DRIVE} pin which allows the user to set the voltage levels for the digital interface lines. The range for this V_{DRIVE} pin is from +2.85V to +5.25V. The part is housed in a 48-pin LQFP package and is specified over a -40°C to +85°C temperature range.

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AD7485–SPECIFICATIONS

(T_A = 25°C, V_{DD} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, f_{SAMPLE} = 1MSPS)

Parameter	Specification	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 100kHz Sine Wave
Signal to Noise + Distortion (SINAD)[2]	78	dB min	
Signal to Noise Ratio (SNR)[2]	78	dB min	
Total Harmonic Distortion (THD)[2]	-90	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	TBD	dB max	
Intermodulation Distortion (IMD)[2]			
Second Order Terms	TBD	dB typ	
Third Order Terms	TBD	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	10	ps typ	
Full Power Bandwidth	10MHz typ	@ 3 dB	
	TBD	@0.1 dB	
DC ACCURACY			
Resolution	14	Bits	
Integral Nonlinearity[2]	TBD	LSB max	
	±1	LSB typ	
Differential Nonlinearity[2]	TBD	LSB max	Guaranteed No Missed Codes to 14 bits
	±1	LSB typ	
Offset Error[2]	±1.5	LSB max	
Gain Error[2]	±1.5	LSB max	
ANALOG INPUT			
Input Voltage	0	V min	
	+2.5	Volts max	
DC Leakage Current	TBD	µA max	
Input Capacitance	10	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	+2.5	Volts	±1% for specified performance
V_{REF} Input DC Leakage Current	±1	µA max	
V_{REF} Input Capacitance	TBD	pF max	
V_{REF} Output Voltage	+2.5	V nom	
V_{REF} Error @ 25°C	TBD	mV max	
V_{REF} Error T_{MIN} to T_{MAX}	TBD	mV max	
V_{REF} Output Impedance	TBD	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	V_{DRIVE} -1	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	TBD	µA max	
Input Capacitance, C_{IN}[2]	TBD	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	0.7 x V_{DRIVE}	V min	
Output Low Voltage, V_{OL}	0.3 x V_{DRIVE}	V max	
Floating-State Leakage Current	TBD	µA max	
Floating-State Output Capacitance[2,3]	TBD	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	TBD	ns max	
Track/Hold Acquisition Time	TBD	ns max	Sine Wave Input
	TBD	ns max	Full-Scale Step Input
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	+5	Volts	±5%
V_{DRIVE}	+2.85	V min	
	+5.25	V max	
I_{DD} Normal Mode (Static)	TBD	mA max	
Normal Mode (Operational)	14	mA max	
NAP Mode	1	mA max	
Standby Mode	1	µA max	

Parameter	Specification	Units	Test Conditions/Comments
POWER REQUIREMENTS *(continued)*			
Power Dissipation			
Normal Mode (Operational)	70	mW max	
NAP Mode	5	mW max	
Standby Mode	5	µW max	

NOTES
[1]Temperature ranges as follows: –40°C to +85°C.
[2]See Terminology
[3]Sample tested @ +25°C to ensure compliance
Specifications subject to change without notice.

TIMING CHARACTERISTICS [1,2] (V_{DD} = 5 V ±5%, AGND = DGND = 0 V, V_{REF} = Internal; All specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.85 V to 5.25 V unless otherwise noted)

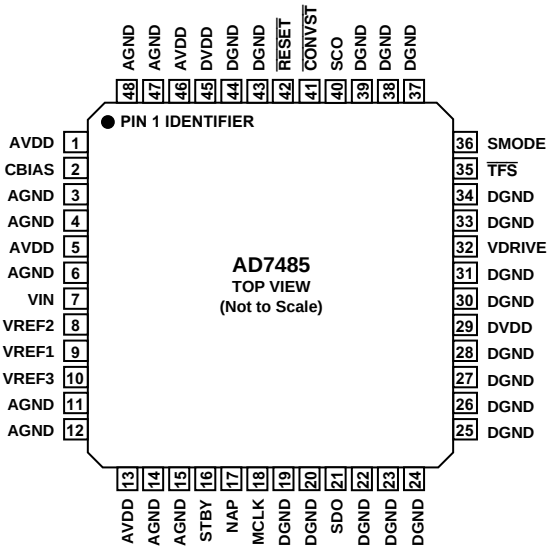
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	f_{MCLK}	TBD		TBD	MHz
MCLK Period	t_1	TBD		TBD	ns
Conversion Time	t_2	TBD		TBD	ns
$\overline{CONVST}$ Low Period	t_3	TBD		TBD	ns
$\overline{CONVST}$ High Period	t_4	TBD		TBD	ns
MCLK High Period	t_5	TBD		TBD	ns
MCLK Low Period	t_6	TBD		TBD	ns
$\overline{CONVST}$ falling edge to MCLK rising edge	t_7	TBD			ns
$\overline{CONVST}$ falling edge to MSB valid	t_8	TBD		TBD	ns
Data valid before SCO falling edge	t_9	TBD		TBD	ns
Data valid after SCO falling edge	t_{10}	TBD		TBD	ns
$\overline{CONVST}$ rising edge to SDO 3-State	t_{11}	TBD			ns
$\overline{CONVST}$ Low Period	t_{12}	TBD		TBD	ns
$\overline{CONVST}$ High Period	t_{13}	TBD		TBD	ns
$\overline{TFS}$ falling edge to MCLK rising edge	t_{14}	TBD			ns
$\overline{TFS}$ falling edge to SCO rising edge	t_{15}	TBD		TBD	ns
$\overline{TFS}$ falling edge to MSB valid	t_{16}	TBD		TBD	ns
$\overline{TFS}$ rising edge to SDO 3-State	t_{17}	TBD		TBD	ns
$\overline{TFS}$ Low Period	t_{18}	TBD		TBD	ns
$\overline{TFS}$ High Period	t_{19}	TBD		TBD	ns
MCLK Fall Time	t_{20}			TBD	ns
MCLK Rise Time	t_{21}			TBD	ns
MCLK - SCO Delay	t_{22}	TBD		TBD	ns

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... TBD
V_{DRIVE} to GND ..... TBD
Analog Input Voltage to GND ..... TBD
Digital Input Voltage to GND ..... TBD
Digital Output Voltage to GND ..... TBD
REF IN to GND ..... TBD
Input Current to Any Pin Except Supplies ..... TBD
Operating Temperature Range
Commercial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
48-Pin LQFP Package, Power Dissipation ..... TBD
θ_{JA} Thermal Impedance ..... 50°C/W
θ_{JC} Thermal Impedance ..... 10°C/W
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C
ESD ..... TBD

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Option
AD7485BST	-40°C to +85°C	Low-profile Quad Flat Pack	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
AVDD	Positive power supply for analog circuitry.
C_{BIAS}	Decoupling pin for internal bias voltage. A 100nF capacitor should be placed between this pin and AGND.
AGND	Power supply ground for analog circuitry.
VIN	Analog input. Single-ended analog input channel.
VREF1	Reference Output. VREF1 connects to the output of the internal 2.5V reference. A 1μF capacitor must be placed between this pin and AGND.
VREF2	Reference Input. A 1μF capacitor must be placed between this pin and AGND. When using an external voltage reference source, the reference voltage should be applied to this pin.
VREF3	Reference decoupling pin. When using the internal reference, a 100nF must be connected from this pin to AGND. When using an external reference source, this pin should be connected directly to AGND.
STBY	Standby logic input. When this pin is logic high, the device will be placed in Standby mode. See Power Saving Section for further details.
NAP	Nap logic input. When this pin is logic high, the device will be placed in a very low power mode. See Power Saving Section for further details.
DVDD	Positive power supply for digital circuitry.
DGND	Ground reference for digital circuitry.
V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin will determine at what voltage the interface logic of the AD7485 will operate.
$\overline{CONVST}$	Convert Start Logic Input. A conversion is initiated on the falling edge of $\overline{CONVST}$ signal. The input track/hold amplifier goes from track mode to hold mode and the conversion process commences.
$\overline{RESET}$	Reset Logic Input. A logic 0 on this pin resets the internal state machine and terminates a conversion that may be in progress. Holding this pin low keeps the part in a reset state.
MCLK	Master Clock Input. This is the input for the master clock which controls the conversion cycle. The frequency of this clock may be up to 25MHz. 24 clock cycles are required for each conversion.
SDO	Serial Data Output. The conversion data is latched out on this pin on the rising edge of SCO. It should be latched into the receiving serial port of the DSP on the falling edge of SCO. The Over-range bit is latched out first, then 14 bits of data (MSB first) followed by a trailing zero.
$\overline{TFS}$	Transmit Frame Sync input. In Serial Mode 2, this pin acts as a framing signal for the serial data being clocked out on SDO. A falling edge on $\overline{TFS}$ brings SDO out of three-state and the data starts to get clocked out on the next rising edge of SCO.
SMODE	Serial Mode Input. A logic low on this pin selects Serial Mode 1 and a logic high selects Serial Mode 2. See Serial Interface Section for further details.
SCO	Serial Clock Output. This clock is derived from MCLK and is used to latch conversion data from the device. See Serial Interface Section for further details.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 0.5 LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode).

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 14-bit converter, this is 86.04 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7485 it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7484 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7485 is a 14-bit error correcting successive approximation analog-to-digital converter based around a capacitive DAC. It provides the user with track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The analog input signal range that the AD7485 can convert is 0 to 2.5 Volts. The part requires a +2.5V reference which can be provided from the part's own internal reference or an external reference source. Figure 1 shows a very simplified schematic of the ADC. The Control Logic, SAR and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back to a balanced condition.

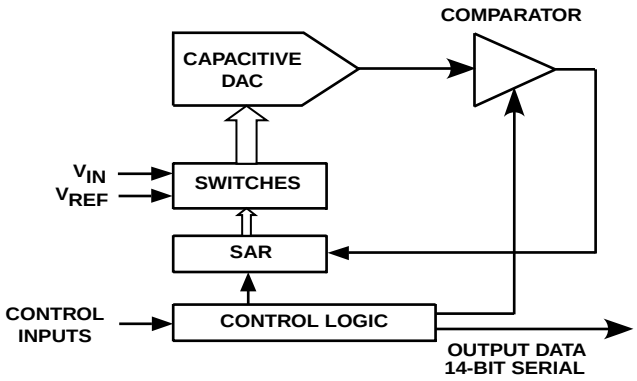


Figure 1. Simplified Block Diagram of AD7485

Conversion is initiated on the AD7485 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the track/hold goes from track to hold mode and the conversion sequence is started. Conversion time for the part is 24 MCLK periods. Figure 2 shows the ADC during conversion. When conversion starts, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

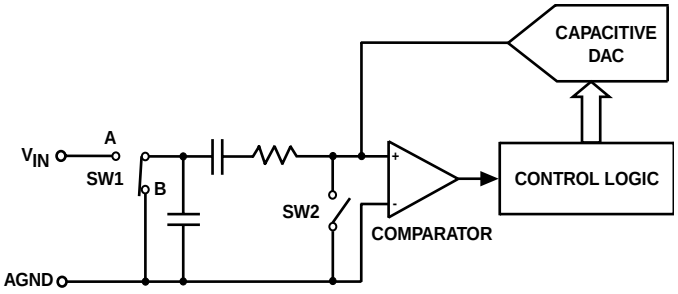


Figure 2. ADC Conversion Phase

At the end of conversion, the track/hold returns to tracking mode and the acquisition time begins. The track/hold acquisition time is TBD nS. Figure 3 shows the ADC during its acquistition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

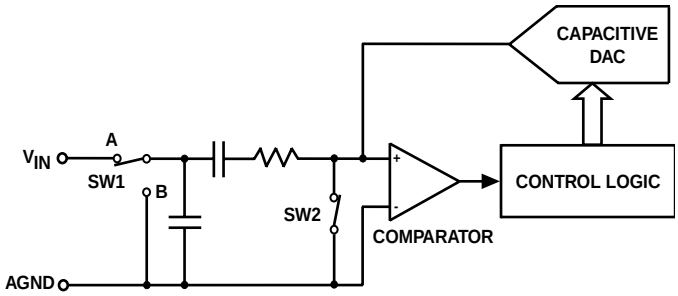


Figure 3. ADC Acquisition Phase

ADC TRANSFER FUNCTION

The output coding of the AD7485 is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The LSB size is V_{REF} / 16384. The nominal transfer characteristic for the AD7485 in shown in figure 4 below.

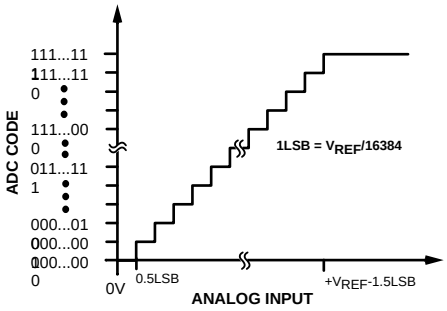


Figure 4. AD7485 Transfer Characteristic

POWER SAVING

The AD7485 uses advanced design techniques to achieve very low power dissipation at high throughput rates. In addition to this the AD7485 features two power saving modes, Nap Mode and Standby Mode. These modes are selected by bringing either the NAP or STBY pin to a logic high respectively.

When operating the AD7485 with a 25MHz MCLK in normal, fully powered mode, the current consumption is 14mA during conversion and the quiescent current is 10mA. Operating at a throughput rate of 500kSPS, the conversion time of 960nS contributes 33.6mW to the overall power dissipation.

(960nS / 2µS) x (5V x 14mA) = 33.6mW

For the remaining 1.04µS of the cycle, the AD7485 dissipates 17.5mW of power.

(1.04µS / 2µS) x (5V x 10mA) = 26mW

Thus the power dissipated during each cycle is:

33.6mW + 26mW = 59.6mW

Figure 5 below shows the AD7485 conversion sequence operating in normal mode.

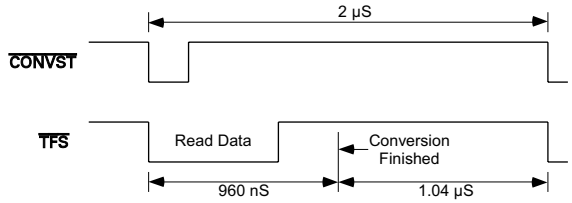


Figure 5. Normal Mode Power Dissipation

In NAP mode, all the internal circuitry except for the internal reference is powered down. In this mode, the power dissipation of the AD7485 is reduced to 5mW. When exiting NAP mode a minimum of 100nS must be waited before initiating a conversion. This is necessary to allow the internal circuitry to settle after power-up and for the track/hold to properly acquire the analog input signal.

If the AD7485 is put into NAP mode after each conversion, the average power dissipation will be reduced but the throughput rate will be limited by the power-up time. Using the AD7485 with a throughput rate of 100kSPS while placing the part in NAP mode after each conversion would result in average power dissipation as follows: The power-up and conversion phase will contribute 7.42mW to the overall power dissipation.

(1.06µS / 10µS) x (5V x 14mA) = 7.42mW

While in NAP mode for the rest of the cycle, the AD7485 dissipates only 4.47mW of power.

(8.94µS / 10µS) x (5V x 1mA) = 4.47mW

Thus the power dissipated during each cycle is:

7.42mW + 4.47mW = 11.89mW

Figure 6 shows the AD7485 conversion sequence if putting the part into NAP mode after each conversion.

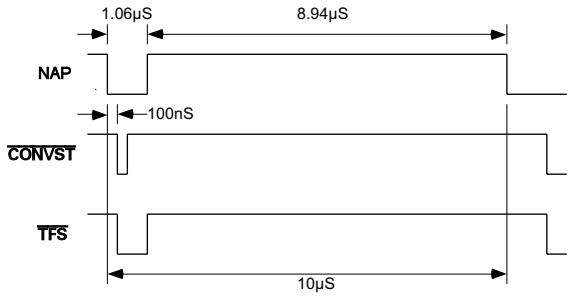


Figure 6. NAP Mode Power Dissipation

Figures 7 and 8 show a typical graphical representation of Power vs. Throughput for the AD7485 when in Normal and Nap modes respectively.

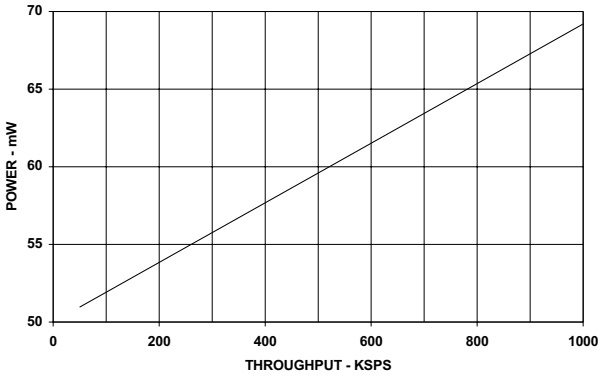


Figure 7. Normal Mode - Power vs. Throughput

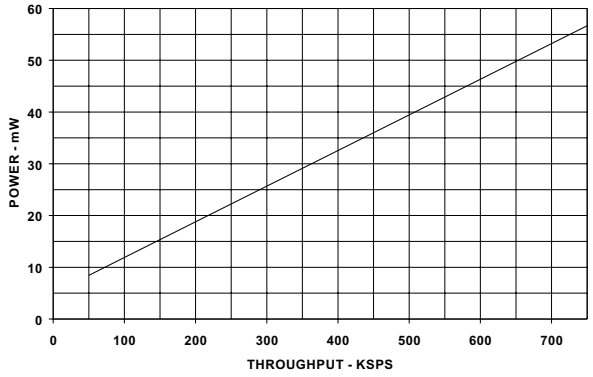


Figure 8. Nap Mode - Power vs. Throughput

In STANDBY mode, all the internal circuitry is powered down and the power consumption of the AD7485 is reduced to 5µW. Because the internal reference has been powered down, the power-up time necessary before a conversion can be initiated is longer. If using the internal reference of the AD7485, the ADC must be brought out of STANDBY mode 200µS before a conversion is initiated. Initiating a conversion before the required power-up time has elapsed will result in incorrect conversion data. If an external reference source is used and kept powered up while the AD7485 is in STANDBY mode, the power-up time required will be reduced.

SERIAL INTERFACE

The AD7485 has two serial interface modes, selected by the state of the SMODE pin. In both these modes the MCLK pin must be supplied with a clock signal of between TBD MHz and 25MHz. This MCLK signal controls the internal conversion process and is also used to derive the SCO signal. As the AD7485 uses an algorithmic successive-approximation technique, 24 MCLK cycles are required to complete a conversion. Due to the error-correcting operation of this ADC, all bit trials must be completed before the conversion result is calculated. This results in a single sample delay in the result that is clocked out.

In serial mode 1 (see Figure 10 for details), the $\overline{\text{CONVST}}$ pin is used to initiate the conversion and also frame the serial data. When $\overline{\text{CONVST}}$ is brought low, the SDO line is taken out of three-state, the over-range bit will be clocked out on the next rising edge of SCO followed by the 14 data bits (MSB first) and a trailing zero. $\overline{\text{CONVST}}$ must remain low for 16 SCO pulses to allow all the data to be clocked out. When $\overline{\text{CONVST}}$ returns to a logic high, the SDO line returns to three-state. $\overline{\text{TFS}}$ should be tied to ground in this mode.

In serial mode 2 (see Figure 11 for details), the $\overline{\text{CONVST}}$ pin is used to initiate the conversion but the $\overline{\text{TFS}}$ signal is used to frame the serial data. The duty cycle of the $\overline{\text{CONVST}}$ signal may vary as shown in the timing diagram. This allows the $\overline{\text{CONVST}}$ line to be driven by high precision, 50% duty cycle signal for extremely accurate sampling intervals. $\overline{\text{TFS}}$ must remain low for 16 SCO cycles in this mode to allow all the data to be clocked out.

Figure 9 shows a typical connection diagram for the AD7485. In this case the MCLK signal is provided by a 25MHz crystal oscillator module. It could also be provided by the second serial port of a DSP (e.g. ADSP-2189M) if such were available.

In Figure 9 the V_{DRIVE} pin is tied to DV_{DD}, which results in logic output levels being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output levels would be either 0 V or 3 V. This feature allows the AD7485 to interface to 3 V devices while still enabling the A/D to process signals at 5 V supply.

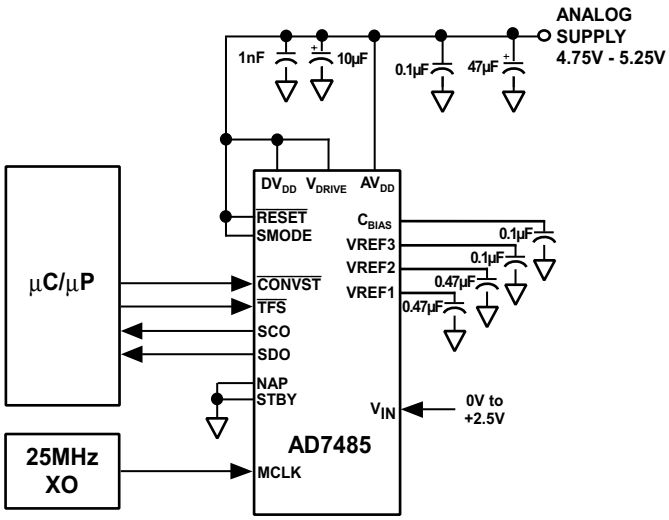


Figure 9. AD7485 Typical Connection Diagram

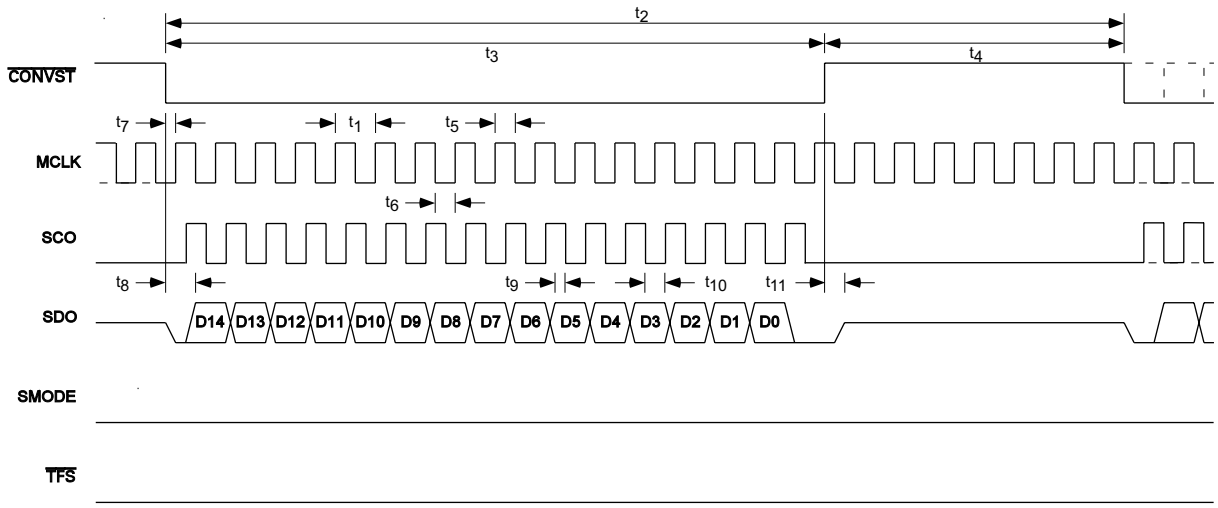


Figure 10. Serial Mode 1 (SMODE=0) Read Cycle

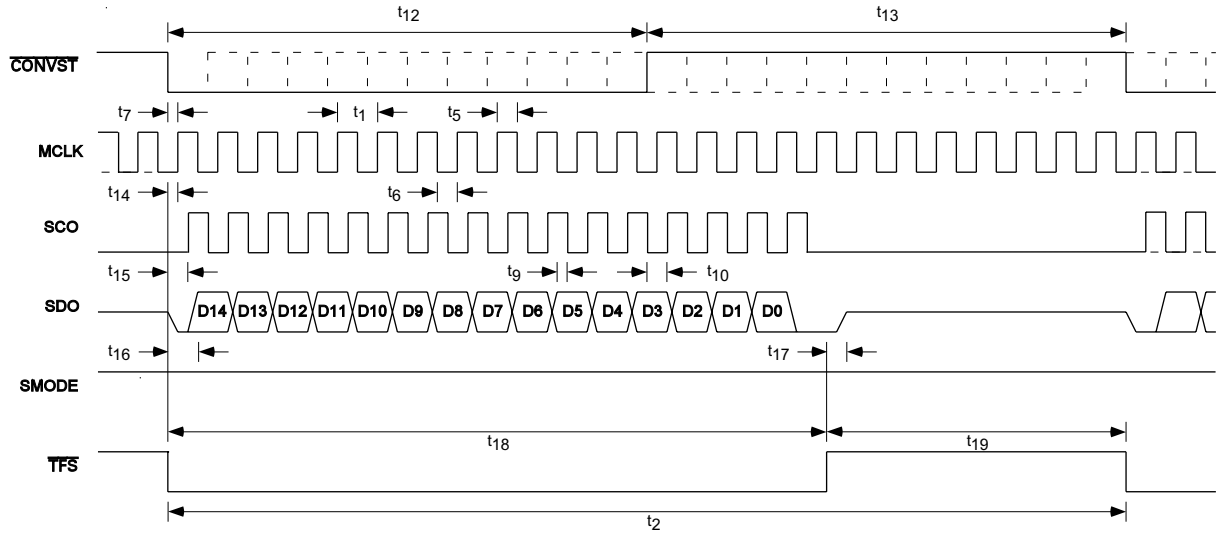


Figure 11. Serial Mode 2 (SMODE=10) Read Cycle

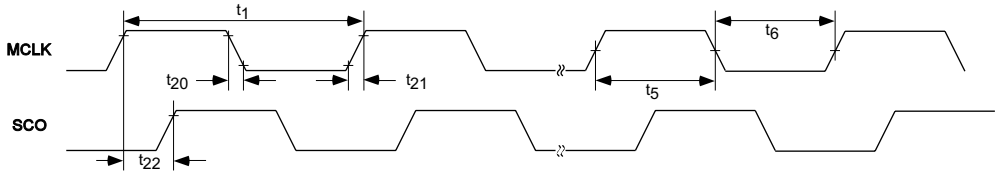


Figure 12. Serial Clock Timing

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Pin LQFP Package (ST-48)