

## 74LCX540

### Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

#### General Description

The LCX540 is an octal buffer/line driver designed to be employed as a memory and address driver, clock driver and bus oriented transmitter/receiver.

This device is similar in function to the LCX240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The LCX540 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment. The LCX540 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.5 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 10  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

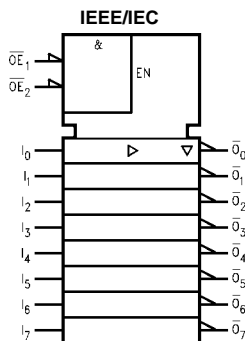
**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

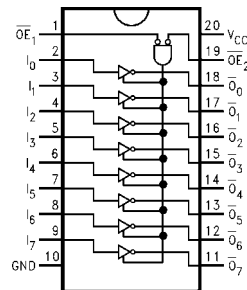
Order Number	Package Number	Package Description
74LCX540WWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX540MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



## Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

## Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	$\overline{O}_n$
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

Absolute Maximum Ratings (Note 2)					
Symbol	Parameter	Value	Conditions	Units	
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V	
$V_I$	DC Input Voltage	-0.5 to +7.0		V	
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V	
		-0.5 to $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 3)		
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA	
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA	
		+50	$V_O > V_{CC}$		
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA	
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA	
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA	
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}C$	

Recommended Operating Conditions (Note 4)					
Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V	
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V
		3-STATE	0	5.5	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		$\pm 24$	mA
		$V_{CC} = 2.7V - 3.0V$		$\pm 12$	
		$V_{CC} = 2.3V - 2.7V$		$\pm 8$	
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}C$	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V	

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Unused (inputs or I/O's) must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8 mA$	2.3		0.6	
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 3.6		$\pm 5.0$	$\mu A$
$I_{OFF}$	Power-Off Leakage Current	$V_I$ or $V_O = 5.5V$	0		10	$\mu A$

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		10	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 5)	2.3 – 3.6		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50pF		C <sub>L</sub> = 50pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t <sub>PLH</sub>		1.5	6.5	1.5	7.5	1.5	7.8	
t <sub>PZL</sub>	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t <sub>PZH</sub>		1.5	8.5	1.5	9.5	1.5	10.5	
t <sub>PLZ</sub>	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t <sub>PHZ</sub>		1.5	7.5	1.5	8.5	1.5	9.0	
t <sub>OSSL</sub>	Output to Output Skew (Note 6)		1.0					ns
t <sub>OSLH</sub>			1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
			2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V
			2.5	-0.6	

**Capacitance**

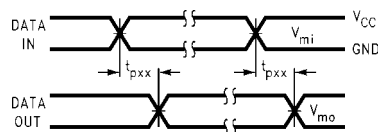
Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	25	pF

**AC LOADING and WAVEFORMS** Generic for LCX Family

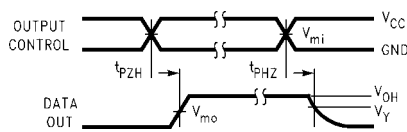


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

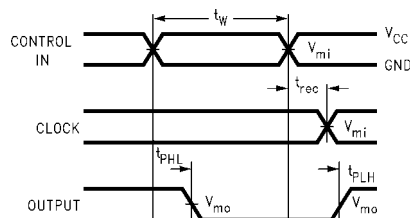
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



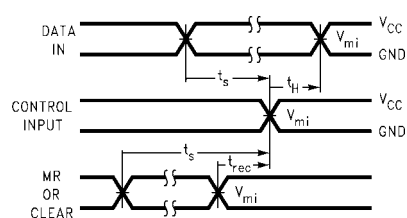
**Waveform for Inverting and Non-Inverting Functions**



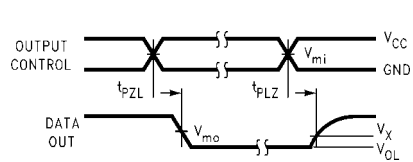
**3-STATE Output High Enable and Disable Times for Logic**



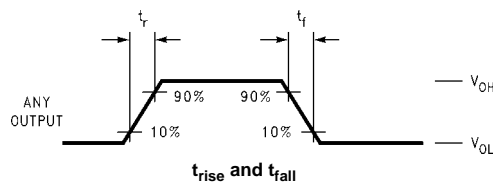
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



**3-STATE Output Low Enable and Disable Times for Logic**



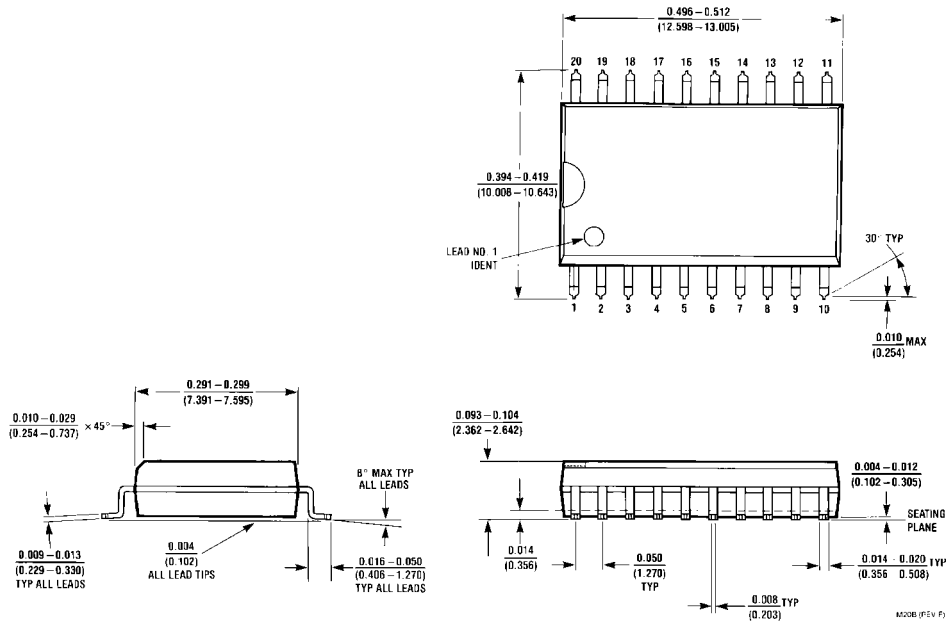
**FIGURE 2. Waveforms**  
(Input Characteristics;  $f = 1MHz, t_R = t_F = 3ns$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

**Schematic Diagram** Generic for LCX Family



**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

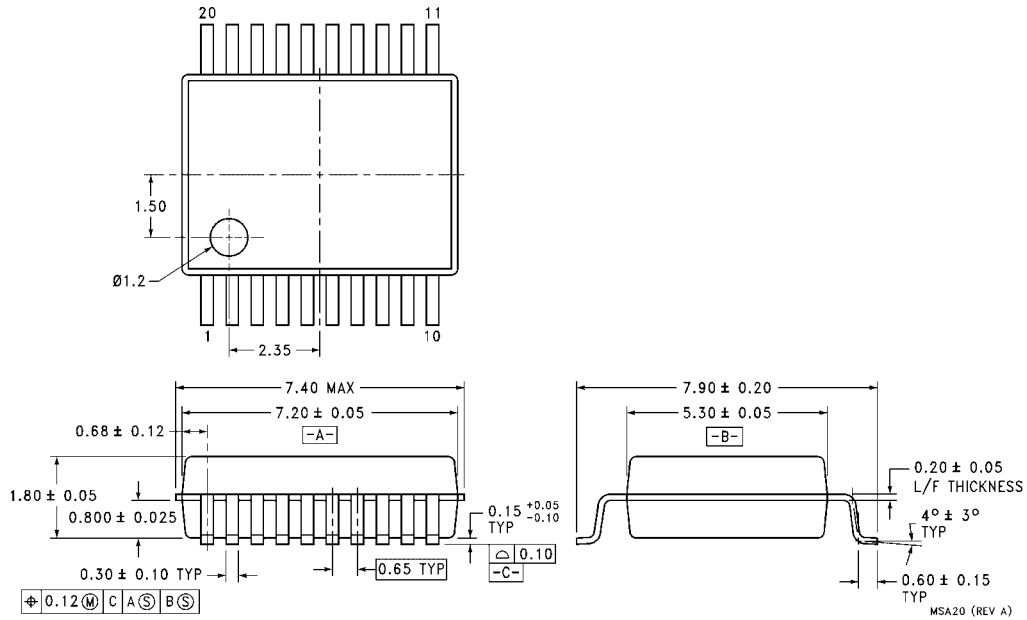
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

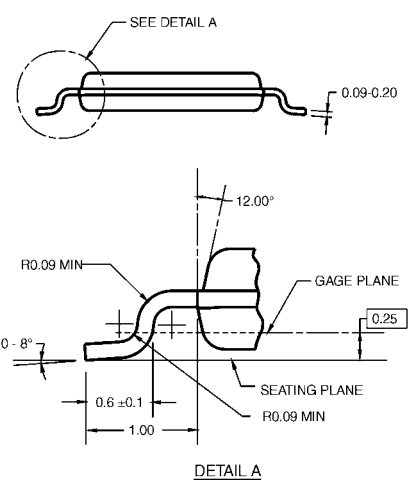
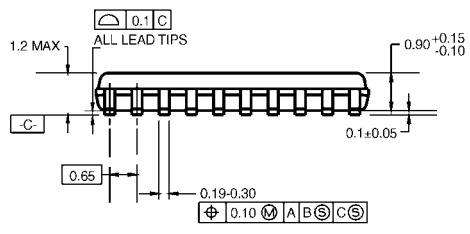
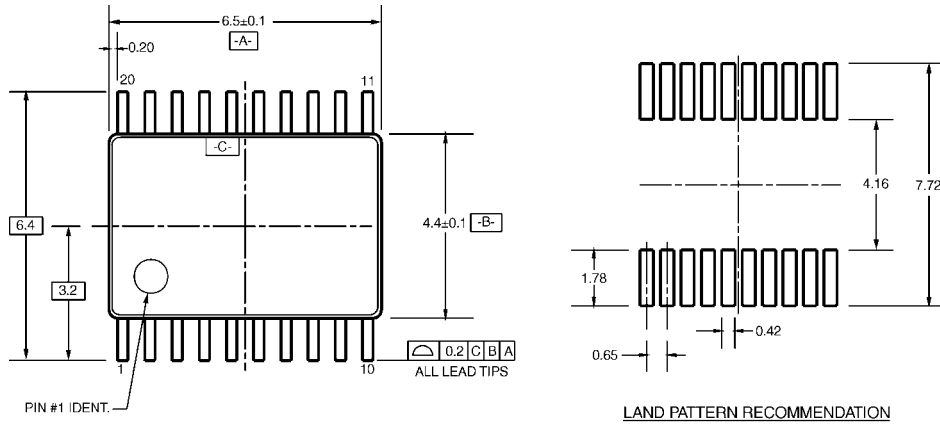


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)